Bluetooth® and Dual Mode Controller

1 FEATURES

- **Single-Chip *Bluetooth* Smart Ready Solution Integrating *Bluetooth* Basic Rate (BR)/Enhanced Data Rate (EDR)/Low Energy (LE) Features Fully Compliant With the *Bluetooth* 4.0 Specification Up to the HCI Layer**
- **BR/EDR Features Include:**
  - **Up to 7 Active Devices**
  - **Scatternet: Up to 3 Piconets Simultaneously, 1 as Master and 2 as Slaves**
  - **Up to 2 SCO Links on the Same or Different Piconets**
  - **Support for All Voice Air-Coding – Continuously Variable Slope Delta (CVSD), A-Law, μ-Law, and Transparent (Uncoded)**
- **LE Features Include:**
  - **Supports Up to 6 Simultaneous Connections**
  - **Multiple Sniff Instances that are Tightly Coupled to Achieve Minimum Power Consumption**
  - **Independent Buffering for LE Allows Large Numbers of Multiple Connections Without Affecting BR/EDR Performance.**
  - **Includes Built-In Coexistence and Prioritization Handling for BR/EDR and LE**
- **Flexibility for Easy Stack Integration and Validation into Various Microcontrollers, Such as MSP430™ and Other MCUs**
- **Highly Optimized for Low-Cost Designs:**
  - **Single-Ended 50-Ω RF Interface**
  - **Package Footprint: 76 Pins, 0.6-mm Pitch, 8.10- x 7.83-mm mrQFN**
- **Best-in-class *Bluetooth* (RF) performance (TX power, RX sensitivity, blocking)**
  - **Class 1.5" TX Power Up to +12 dBm**
  - **Internal Temperature Detection and Compensation to Ensure Minimal Variation in RF Performance Over Temperature, No External Calibration Required**
  - **Improved Adaptive Frequency Hopping (AFH) Algorithm With Minimum Adaptation Time**
  - **Provides Longer Range, Including 2x Range Over Other BLE-Only Solutions**
- **Advanced Power Management for Extended Battery Life and Ease of Design:**
  - **On-Chip Power Management, Including Direct Connection to Battery**
  - **Low Power Consumption for Active, Standby, and Scan *Bluetooth* Modes**
  - **Shutdown and Sleep Modes to Minimize Power Consumption**
- **Physical Interfaces:**
  - **Standard HCI Over H4 UART With Maximum Rate of 4 Mbps**
  - **Fully Programmable Digital PCM-I2S™ Codec Interface**
- **CC256x *Bluetooth* Hardware Evaluation Tool: PC-Based Application to Evaluate RF Performance of the Device and Configure Service Pack**

2 DESCRIPTION

The TI CC256x device is a complete *Bluetooth* BR/EDR/LE HCI solution that reduces design effort and enables fast time to market. Based on TI's seventh-generation *Bluetooth* core, the device brings a product-proven solution that supports *Bluetooth* 4.0 dual mode (BR/EDR/LE) protocols.

TI's power-management hardware and software algorithms provide significant power savings in all commonly used *Bluetooth* BR/EDR/LE modes of operation.

When coupled with an MCU device, this HCI device provides best-in-class RF performance for markets such as:

- Mobile phone accessories
- Sports and fitness applications
- Wireless audio solutions
- Remote controls
- Toys

With transmit power and receive sensitivity, this solution provides a best-in-class range of about 2x, compared to other BLE-only solutions. A royalty-free software *Bluetooth* stack available from TI is pre-integrated with TI's MSP430 and ARM® M4 MCUs. The stack is also available for MFi solutions and on other MCUs through TI's partner Stonestreet One (www.stonestreetone.com). Some of the profiles supported today include:

- Serial port profile (SPP)
- Human interface device (HID)
- Several BLE profiles (these profiles vary based on the supported MCU)

In addition to software, this solution consists of a reference design with a low BOM cost. For more information on TI's wireless platform solutions for *Bluetooth*, see TI's Wireless Connectivity Wiki (www.ti.com/connectivitywiki).

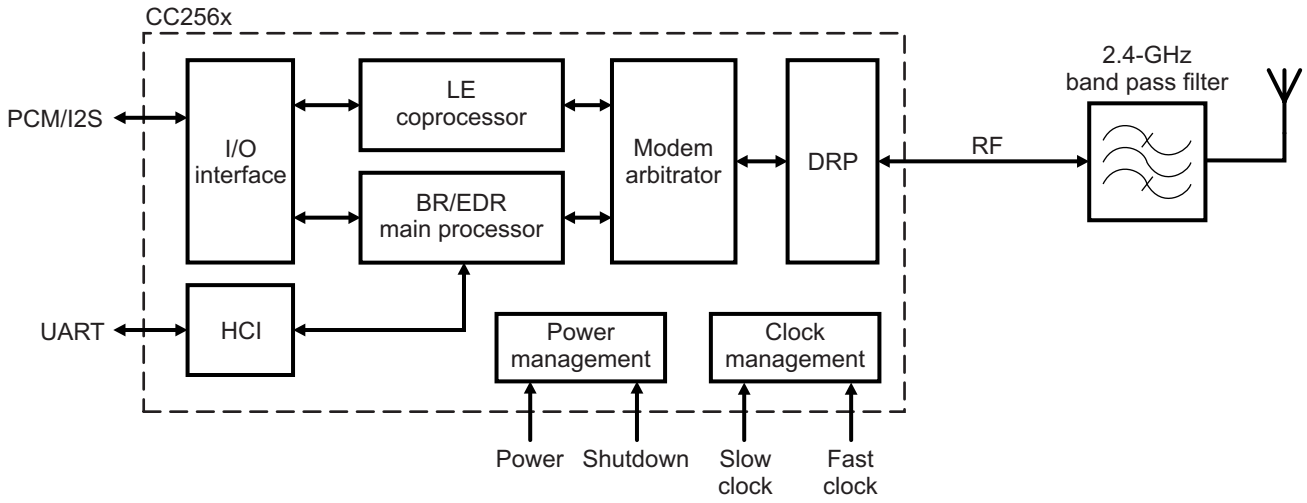
Table 2-1 shows the CC256x family members.

Table 2-1. CC256x Family Members

Device	Technology Supported			
	Description	BR/EDR	LE	ANT
CC2560A	*Bluetooth* 4.0 (with EDR)	√		
CC2564	*Bluetooth* 4.0 + BLE(1)	√	√	
	Bluetooth 4.0 + ANT(1)	√		√

(1) The CC2564 device does not support simultaneous operation of LE and ANT.

Figure 2-1 shows the device block diagram.



Note: The LE coprocessor is not enabled in the CC2560A device.

SWRS121-001

Figure 2-1. Functional Block Diagram

3 BLUETOOTH

3.1 BR/EDR Features

The CC256x device fully complies with the *Bluetooth* 4.0 specification up to the HCI level (for the family members and technology supported, see Table 2-1):

- Up to seven active devices
- Scatternet: Up to 3 piconets simultaneously, 1 as master and 2 as slaves
- Up to two synchronous connection oriented (SCO) links on the same or different piconets
- Very fast AFH algorithm for asynchronous connection-oriented link (ACL) and extended SCO (eSCO) link
- Supports typically 12-dBm TX power without an external power amplifier (PA), thus improving *Bluetooth* link robustness
- DRP single-ended 50-Ω I/O for easy RF interfacing
- Internal temperature detection and compensation to ensure minimal variation in RF performance over temperature
- Flexible pulse-code modulation (PCM) and inter-IC sound (I2S) digital codec interface:
  - Full flexibility of data format (linear, A-Law, μ-Law)
  - Data width
  - Data order
  - Sampling
  - Slot positioning
  - Master and slave modes
  - High clock rates up to 15 MHz for slave mode (or 4.096 MHz for master mode)
- Support for all voice air-coding
  - Continuously variable slope delta (CVSD)
  - A-Law
  - μ-Law
  - Transparent (uncoded)

3.2 LE Features

The device fully complies with the *Bluetooth* 4.0 specification up to the HCI level (for the family members and technology supported, see Table 2-1):

- Solution optimized for proximity and sports use cases
- Support of up to 6 simultaneous connections
- Multiple sniff instances that are tightly coupled to achieve minimum power consumption
- Independent buffering for LE, allowing large numbers of multiple connections without affecting BR/EDR performance.
- Includes built-in coexistence and prioritization handling for BR/EDR and LE

NOTE

ANT is not available when BLE is enabled.

3.3 Changes from *Bluetooth* v2.1 + EDR to v3.0 and v4.0

The *Bluetooth* core specification v3.0 and v4.0 introduces new features, including these major areas of improvement applicable to the CC256x family (*Bluetooth* HCI controller):

- v3.0 features in BR/EDR:
  - Enhanced power control (EPC)
  - *HCI Read Encryption Key Size* command
- v4.0 introduces LE, including:
  - LE physical layer and link layer
  - Enhancements to HCI for LE
  - LE direct test mode
  - Advanced Encryption Standard (AES)

No features are deprecated in v3.0 and v4.0.

For more information, see the *Bluetooth* SIG website.

3.4 Transport Layers

Figure 3-1 shows the *Bluetooth* transport layers.

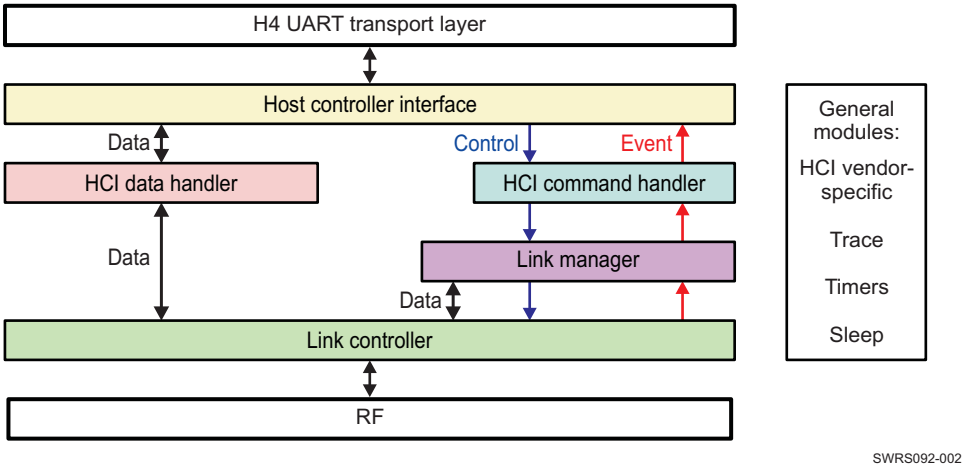
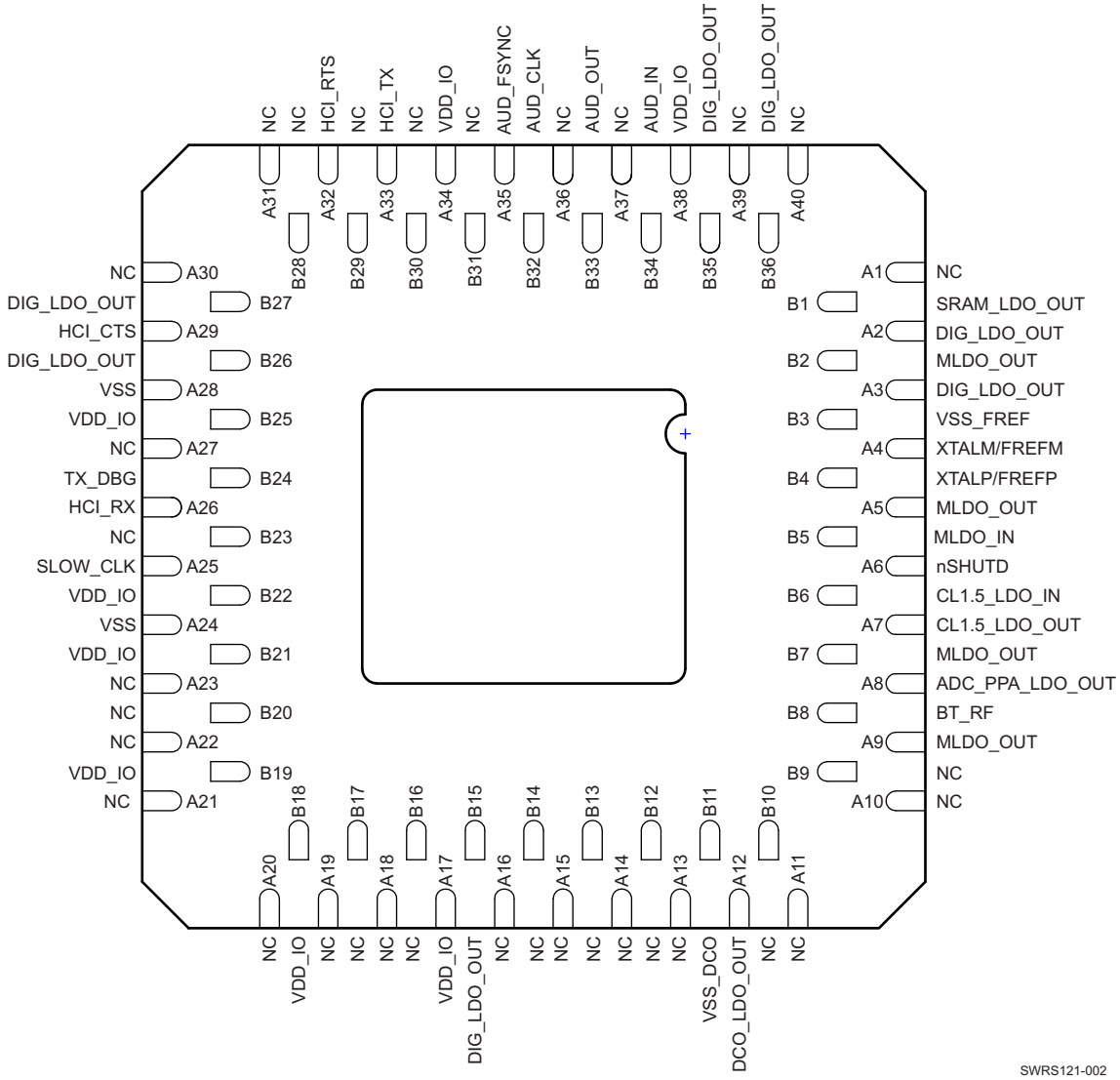


Figure 3-1. *Bluetooth* Transport Layers

4 DETAILED DESCRIPTION

4.1 Pin Designation

Figure 4-1 shows the bottom view of the pin designations.



NOTE: NC = Not connected

Figure 4-1. Pin Designation (Bottom View)

4.2 Terminal Functions

Table 4-1 describes the terminal functions.

Table 4-1. Device Pad Descriptions

Name	No.	Pull at Reset	Def. Dir.(1)	I/O Type(2)	Description
I/O Signals					
HCI_RX	A26	PU	I	8 mA	HCI universal asynchronous receiver/transmitter (UART) data receive
HCI_TX	A33	PU	O	8 mA	HCI UART data transmit
HCI_RTS	A32	PU	O	8 mA	HCI UART request-to-send The host is allowed to send data when HCI_RTS is low.
HCI_CTS	A29	PU	I	8 mA	HCI UART clear-to-send The CC256x device is allowed to send data when HCI_CTS is low.
AUD_FSYNC	A35	PD	I/O	4 mA	pulse-code modulation (PCM) frame-sync signal Fail-safe
AUD_CLK	B32	PD	I/O	HY, 4 mA	PCM clock Fail-safe
AUD_IN	B34	PD	I	4 mA	PCM data input Fail-safe
AUD_OUT	B33	PD	O	4 mA	PCM data output Fail-safe
TX_DBG	B24	PU	O	2 mA	TI internal debug messages. TI recommends leaving an internal test point.
Clock Signals					
SLOW_CLK	A25		I		32.768-kHz clock in Fail-safe
XTALP/FREFP	B4		I		Fast clock in analog (sine wave) Output terminal of fast-clock crystal Fail-safe
XTALM/FREFM	A4		I		Fast clock in digital (square wave) Input terminal of fast-clock crystal Fail-safe
Analog Signals					
BT_RF	B8		I/O		*Bluetooth* RF I/O
nSHUTD	A6	PD	I		Shutdown input (active low)
Power and Ground Signals					
VDD_IO	A17, A34, A38, B18, B19, B21, B22, B25		I		I/O power supply (1.8-V nominal)
MLDO_IN	B5		I		Main LDO input Connect directly to battery
MLDO_OUT	A5, A9, B2, B7		I/O		Main LDO output (1.8-V nominal)
CL1.5_LDO_IN	B6		I		Power amplifier (PA) LDO input Connect directly to battery
CL1.5_LDO_OUT	A7		O		PA LDO output
DIG_LDO_OUT	A2, A3, B15, B26, B27, B35, B36		O		Digital LDO output QFN pin B26 or B27 must be shorted to other DIG_LDO_OUT pins on the PCB.
SRAM_LDO_OUT	B1		O		SRAM LDO output
DCO_LDO_OUT	A12		O		DCO LDO output

(1) I = input; O = output; I/O = bidirectional
(2) I/O Type: Digital I/O cells. HY = input hysteresis, current = typical output current

Table 4-1. Device Pad Descriptions (continued)

Name	No.	Pull at Reset	Def. Dir.(1)	I/O Type(2)	Description
ADC_PPA_LDO_OUT	A8		O		ADC/PPA LDO output
VSS	A24, A28		I		Ground
VSS_DCO	B11		I		DCO ground
VSS_FREF	B3		I		Fast clock ground
No Connect					
NC	A1				Not connected
NC	A10				Not connected
NC	A11				Not connected
NC	A14				Not connected
NC	A18				Not connected
NC	A19				Not connected
NC	A20				Not connected
NC	A21				Not connected
NC	A22				Not connected
NC	A23				Not connected
NC	A27				Not connected
NC	A30				Not connected
NC	A31				Not connected
NC	A40				Not connected
NC	B9				Not connected
NC	B10				Not connected
NC	B16				Not connected
NC	B17				Not connected
NC	B20				Not connected
NC	B23				Not connected
NC	A13		O		TI internal use
NC	A15		O		TI internal use
NC	A16		I/O		TI internal use
NC	A36		I/O		TI internal use
NC	A37		I/O		TI internal use
NC	A39		I/O		TI internal use
NC	B12		I		TI internal use
NC	B13		I		TI internal use
NC	B14		O		TI internal use
NC	B29		O		TI internal use
NC	B30		I/O		TI internal use
NC	B31		I		TI internal use
NC	B28		I		TI internal use

4.3 Device Power Supply

The CC256x power-management hardware and software algorithms provide significant power savings, which is a critical parameter in a microcontroller-based system.

The power-management module is optimized for drawing very low currents.

4.3.1 Power Sources

The CC256x device requires two power sources:

- VDD_IN: Main power supply for the *Bluetooth* core
- VDD_IO: Power source for the 1.8-V I/O ring

The device includes several on-chip voltage regulators for increased noise immunity and can be connected directly to the battery.

4.3.2 Device Power-Up and Power-Down Sequencing

The device includes these power-up requirements (see also Figure 4-2):

- nSHUTD must be low. VDD_IN and VDD_IO are don't-care when nSHUTD is low. However, signals are not allowed on the I/O pins if I/O power is not supplied, because the I/Os are not fail-safe. Exceptions are SLOW_CLK_IN and AUD_xxx, which are fail-safe and can tolerate external voltages with no VDD_IO and VDD_IN.
- VDD_IO and VDD_IN must be stable before releasing nSHUTD.
- The fast clock must be stable within 20 ms of nSHUTD going high.
- The slow clock must be stable within 2 ms of nSHUTD going high.

The device indicates that the power-up sequence is complete by asserting RTS low, which occurs up to 100 ms after nSHUTD goes high. If RTS does not go low, the device is not powered-up. In this case, ensure that the sequence and requirements are met.

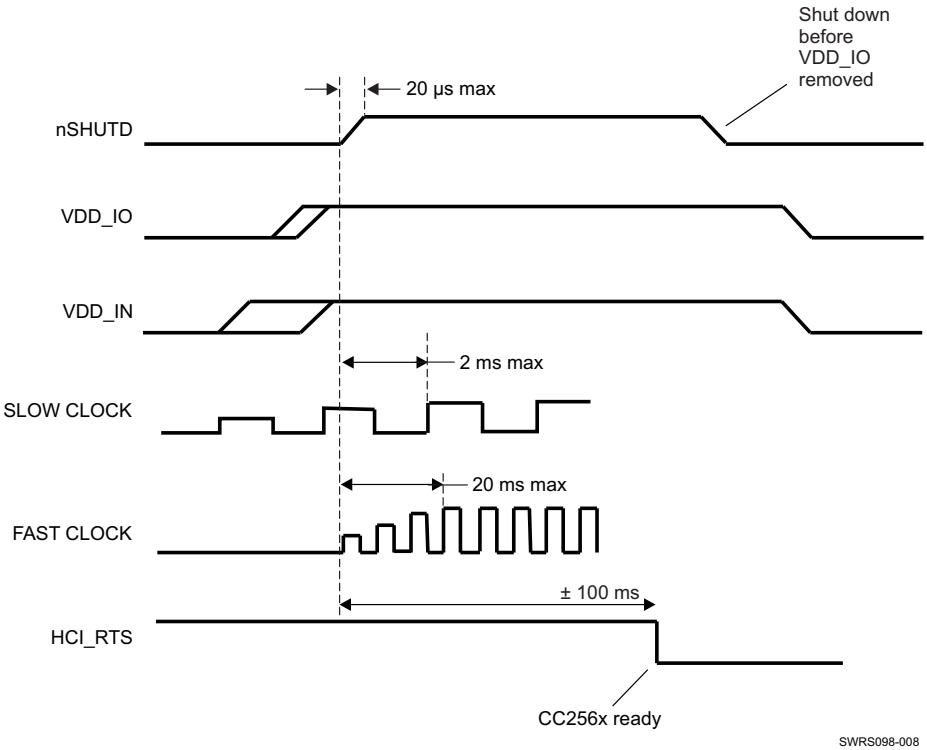


Figure 4-2. Power-Up and Power-Down Sequence

4.3.3 Power Supplies and Shutdown—Static States

The nSHUTD signal puts the device in ultra-low power mode and also performs an internal reset to the device. The rise time for nSHUTD must not exceed 20 µs, and nSHUTD must be low for a minimum of 5 ms.

To prevent conflicts with external signals, all I/O pins are set to the high-impedance state during shutdown and power up of the device. The internal pull resistors are enabled on each I/O pin, as described in Table 4-1.

Table 4-2 describes the static operation states.

Table 4-2. Power Modes

	VDD_IN(1)	VDD_IO(1)	nSHUTD(1)	PM_MODE	Comments
1	None	None	Asserted	Shut down	I/O state is undefined. No I/O voltages are allowed on non fail-safe pins.
2	None	None	Deasserted	Not allowed	I/O state is undefined. No I/O voltages are allowed on non fail-safe pins.
3	None	Present	Asserted	Shut down	I/Os are defined as 3-state with internal pullup or pulldown enabled.
4	None	Present	Deasserted	Not allowed	I/O state is undefined. No I/O voltages are allowed on nonfail-safe pins.
5	Present	None	Asserted	Shut down	I/O state is undefined. No I/O voltages are allowed on nonfail-safe pins.
6	Present	None	Deasserted	Not allowed	I/O state is undefined. No I/O voltages are allowed on nonfail-safe pins.
7	Present	Present	Asserted	Shut down	I/OS are defined as 3-state with internal pullup or pulldown enabled.
8	Present	Present	Deasserted	Active	See Section 4.3.4, *I/O States In Various Power Modes*.

(1) The terms *None* or *Asserted* can imply any of the following conditions: directly pulled to ground or driven low, pulled to ground through a pulldown resistor, or left NC or floating (high-impedance output stage).

4.3.4 I/O States In Various Power Modes

CAUTION

Some device I/Os are not fail-safe (see Table 4-1). Fail-safe means that the pins do not draw current from an external voltage applied to the pin when I/O power is not supplied to the device. External voltages are not allowed on these I/O pins when the I/O supply voltage is not supplied because of possible damage to the device.

I/O Name	Shut Down(1)		Default Active(1)		Deep Sleep(1)	
	I/O State	Pull	I/O State	Pull	I/O State	Pull
HCI_RX	Z	PU	I	PU	I	PU
HCI_TX	Z	PU	O-H	—	O	—
HCI_RTS	Z	PU	O-H	—	O	—
HCI_CTS	Z	PU	I	PU	I	PU
AUD_CLK	Z	PD	I	PD	I	PD
AUD_FSYNC	Z	PD	I	PD	I	PD
AUD_IN	Z	PD	I	PD	I	PD
AUD_OUT	Z	PD	Z	PD	Z	PD
TX_DBG	Z	PU	O	—		

(1) I = input, O = output, Z = Hi-Z, — = no pull, PU = pullup, PD = pulldown, H = high, L = low

4.4 Clock Inputs

4.4.1 Slow Clock

An external source must supply the slow clock and connect to the SLOW_CLK_IN pin. The source must be a digital signal in the range of 0 to 1.8 V.

The accuracy of the slow clock frequency must be 32.768 kHz ±250 ppm for *Bluetooth* use (as specified in the *Bluetooth* specification).

The external slow clock must be stable within 64 slow-clock cycles (2 ms) following the release of nSHUTD.

4.4.2 Fast Clock Using External Clock Source

An external clock source is fed to an internal pulse-shaping cell to provide the fast clock signal for the device. The device incorporates an internal, automatic clock-scheme detection mechanism that automatically detects the fast-clock scheme used and configures the F_{REF} cell accordingly. This mechanism ensures that the electrical characteristics (loading) of the fast-clock input remain static regardless of the scheme used and eliminates any power-consumption penalty-versus-scheme used.

This section describes the requirements for fast clock use. The frequency variation of the fast-clock source must not exceed ±20 ppm (as defined by the *Bluetooth* specification).

The external clock can be AC- or DC-coupled, sine or square wave.

4.4.2.1 External F_{REF} DC-Coupled

Figure 4-3 and Figure 4-4 show the clock configuration when using a square wave, DC-coupled external source for the fast clock input.

NOTE

A shunt capacitor with a range of 10 nF must be added on the oscillator output to reject high harmonics and shape the signal to be close to a sinusoidal waveform.

TI recommends using only a dedicated LDO to feed the oscillator. Do not use the same VIO for the oscillator and the CC256x device.

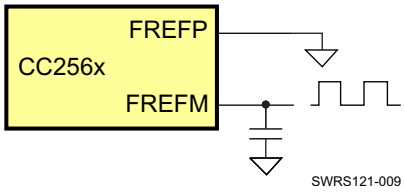


Figure 4-3. Clock Configuration (Square Wave, DC-Coupled)

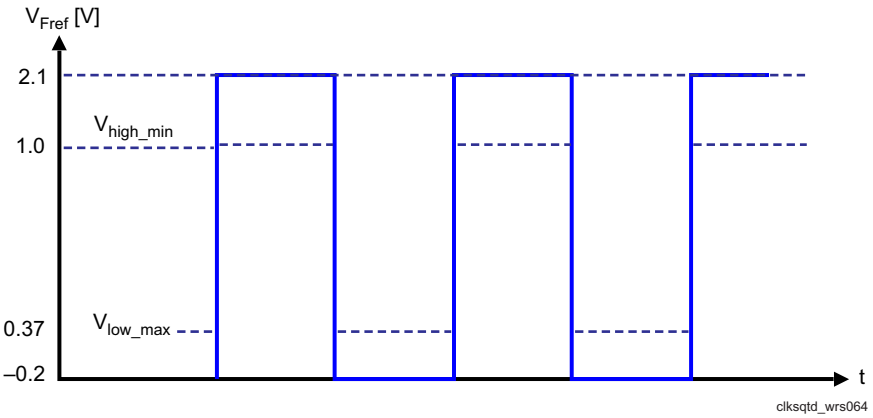


Figure 4-4. External Fast Clock (Square Wave, DC-Coupled)

Figure 4-5 and Figure 4-6 show the clock configuration when using a sine wave, DC-coupled external source for the fast clock input.

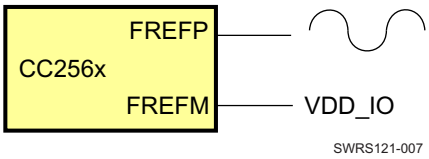


Figure 4-5. Clock Configuration (Sine Wave, DC-Coupled)

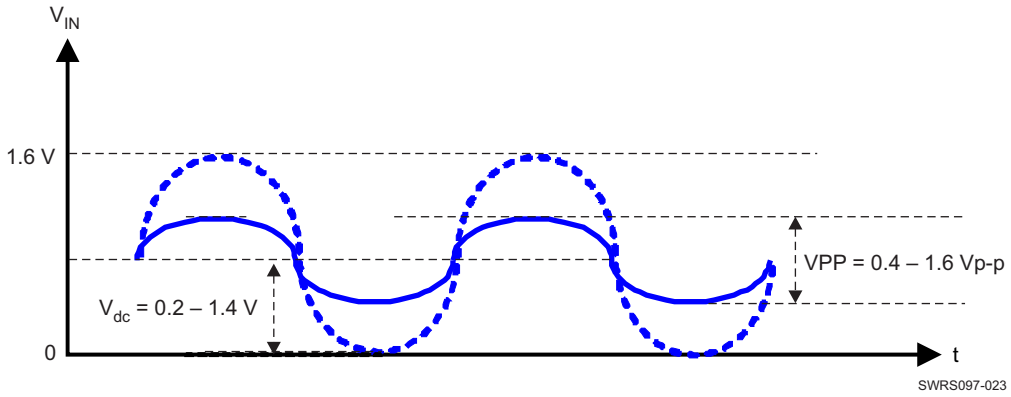


Figure 4-6. External Fast Clock (Sine Wave, DC-Coupled)

4.4.2.2 External F_{REF} Sine Wave, AC-Coupled

Figure 4-7 shows the configuration when using a sine wave, AC-coupled external source for the fast-clock input.

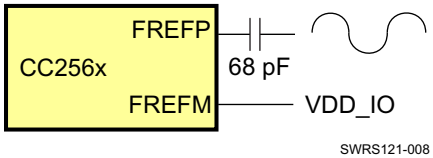


Figure 4-7. Clock Configuration (Sine Wave, AC-Coupled)

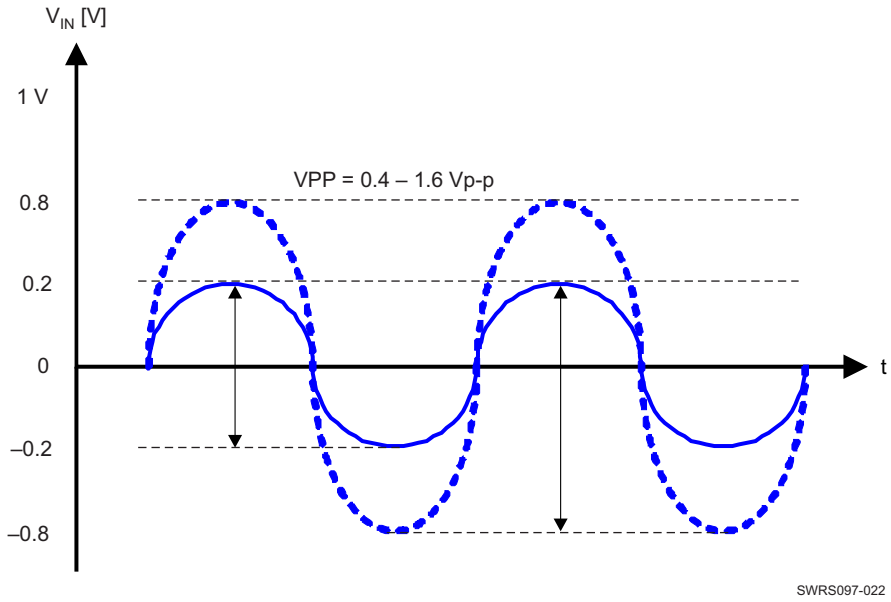


Figure 4-8. External Fast Clock (Sine Wave, AC-Coupled)

In cases where the input amplitude is greater than 1.6 Vp-p, the amplitude can be reduced to within limits. Using a small series capacitor forms a voltage divider with the internal input capacitance of approximately 2 pF to provide the required amplitude at the device input.

4.4.2.3 Fast Clock Using External Crystal

The CC256x device incorporates an internal crystal oscillator buffer to support a crystal-based fast-clock scheme. The supported crystal frequency is 26 MHz.

The frequency accuracy of the fast clock source must not exceed ±20 ppm (including the accuracy of the capacitors, as specified in the *Bluetooth* specification).

Figure 4-9 shows the recommended fast-clock circuitry.

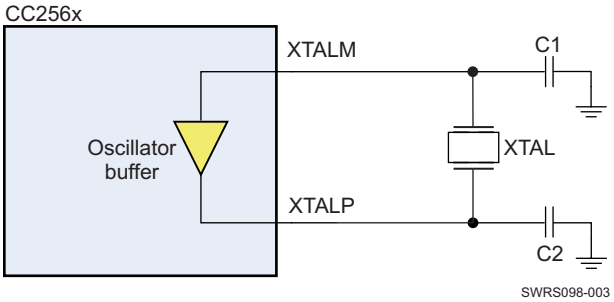


Figure 4-9. Fast-Clock Crystal Circuit

Table 4-3 lists component values for the fast-clock crystal circuit.

Table 4-3. Fast-Clock Crystal Circuit Component Values

FREQ (MHz)	C1 (pF)(1)	C2 (pF)(1)
26	12	12

(1) To achieve the required accuracy, values for C1 and C2 must be taken from the crystal manufacturer's data sheet and layout considerations.

4.5 Functional Blocks

The CC256x architecture comprises a DRP and a point-to-multipoint baseband core. The architecture is based on a single-processor ARM7TDMIE® core. The device includes several on-chip peripherals to enable easy communication with a host system and the *Bluetooth* BR/EDR/LE core.

4.5.1 DRP

The device is the third generation of TI *Bluetooth* single-chip devices using DRP architecture. Modifications and new features added to the DRP further improve radio performance.

Figure 4-10 shows the DRP block diagram.

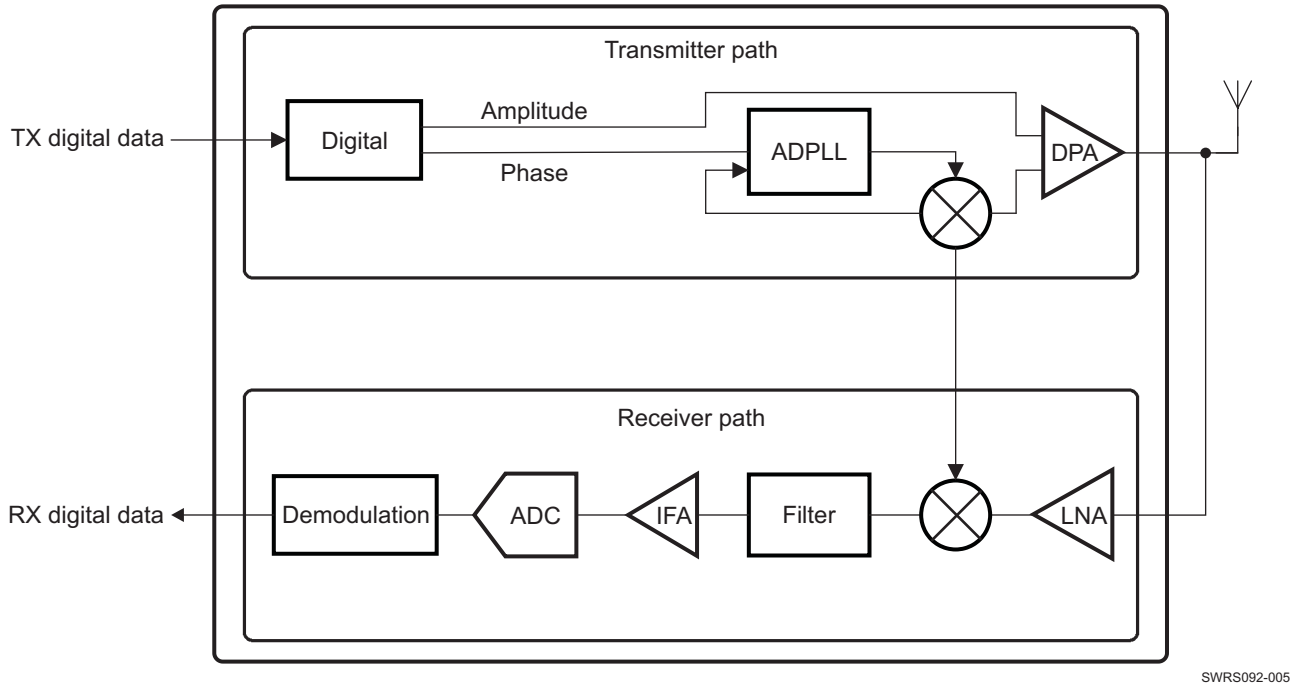


Figure 4-10. DRP Block Diagram

4.5.1.1 Receiver

The receiver uses near-zero-IF architecture to convert the RF signal to baseband data. The signal received from the external antenna is input to a single-ended LNA (low-noise amplifier) and passed to a mixer that downconverts the signal to IF, followed by a filter and amplifier. The signal is then quantized by a sigma-delta analog-to-digital converter (ADC) and further processed to reduce the interference level.

The demodulator digitally downconverts the signal to zero-IF and recovers the data stream using an adaptive-decision mechanism. The demodulator includes EDR processing with:

- State-of-the-art performance
- A maximum-likelihood sequence estimator (MLSE) to improve the performance of basic-rate GFSK sensitivity
- Adaptive equalization to enhance EDR modulation

New features include:

- LNA input range narrowed to increase blocking performance
- Active spur cancellation to increase robustness to spurs

4.5.1.2 Transmitter

The transmitter is an all-digital, sigma-delta phase-locked loop (ADPLL) based with a digitally controlled oscillator (DCO) at 2.4 GHz as the RF frequency clock. The transmitter direct modulates the digital PLL. The power amplifier is also digitally controlled. The transmitter uses the polar-modulation technique. While the phase-modulated control word is fed to the ADPLL, the amplitude-modulated controlled word is fed to the class-E amplifier to generate a *Bluetooth* standard-compliant RF signal.

New features include:

- Improved TX output power
- LMS algorithm to improve the differential error vector magnitude (DEVM)

4.5.2 Host Controller Interface

The CC256x device incorporates one UART module dedicated to the HCI transport layer. The HCI interface transports commands, events, and asynchronous connection-oriented link (ACL) between the device and the host using HCI data packets.

The UART module supports the H4 (4-wire) protocol with a maximum baud rate of 4 Mbps for all fast-clock frequencies.

After power up, the baud rate is set for 115.2 kbps, regardless of the fast-clock frequency.

The baud rate can thereafter be changed with a VS command. The device responds with a Command Complete event (still at 115.2 kbps), after which the baud rate change occurs.

HCI hardware includes the following features:

- Receiver detection of break, idle, framing, FIFO overflow, and parity error conditions
- Transmitter underflow detection
- CTS and RTS hardware flow control

Table 4-4 lists the UART module default settings.

Table 4-4. UART Default Settings

Parameter	Value
Bit rate	115.2 kbps
Data length	8 bits
Stop-bit	1
Parity	None

4.5.2.1 UART 4-Wire Interface—H4

The interface includes four signals: TX, RX, CTS, and RTS. Flow control between the host and the CC256x device is bytewise by hardware.

Figure 4-11 shows how the device obtains flow control.

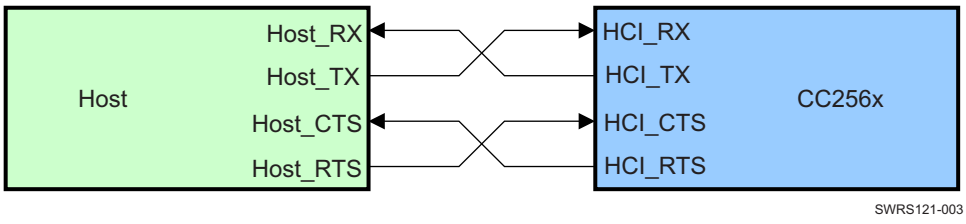


Figure 4-11. HCI UART Connection

When the UART RX buffer of the CC256x device passes the flow control threshold, it sets the UART_RTS signal high to stop transmission from the host.

When the UART_CTS signal is set high, the CC256x device stops its transmission on the interface. If HCI_CTS is set high while transmitting a byte, the CC256x device finishes transmitting the byte and stops the transmission.

4.5.2.2 eHCILL—4-Wire Power-Management Protocol

The CC256x device includes a mechanism that handles the transition between operating mode and deep-sleep low-power mode. The protocol occurs through the UART and is known as the enhanced HCI low level (eHCILL) power-management protocol.

4.5.3 Digital Codec Interface

The codec interface is a fully programmable port to support seamless interfacing with different PCM and Inter-IC Sound (I2S) codec devices. The interface includes the following features:

- Two voice channels
- Master and slave modes
- All voice coding schemes defined by the *Bluetooth* specification: linear, A-Law, and μ-Law
- Long and short frames
- Different data sizes, order, and positions
- High flexibility to support a variety of codecs
- Bus sharing: Data_Out is in Hi-Z mode when the interface is not transmitting voice data.

4.5.3.1 Hardware Interface

The interface includes four signals:

- Clock: configurable direction (input or output)
- Frame_Sync and Word_Sync: configurable direction (input or output)
- Data_In: input
- Data_Out: output or 3-state

The CC256x device can be master of the interface when generating the clock and the frame-sync signals or the slave when receiving these two signals.

For slave mode, clock input frequencies of up to 15 MHz are supported. At clock rates above 12 MHz, the maximum data burst size is 32 bits.

For master mode, the CC256x device can generate any clock frequency between 64 kHz and 4.096 MHz.

4.5.3.2 I2S

When the codec interface is configured to support the I2S protocol, these settings are recommended:

- Bidirectional, full-duplex interface
- Two time slots per frame: time slot-0 for the left channel audio data; and time slot-1 for the right channel audio data
- Each time slot is configurable up to 40 serial clock cycles long, and the frame is configurable up to 80 serial clock cycles long.

4.5.3.3 Data Format

The data format is fully configurable:

- The data length can be from 8 to 320 bits in 1-bit increments when working with 2 channels, or up to 640 bits when working with 1 channel. The data length can be set independently for each channel.
- The data position within a frame is also configurable within 1 clock (bit) resolution and can be set independently (relative to the edge of the Frame_Sync signal) for each channel.

- The Data_In and Data_Out bit order can be configured independently. For example; Data_In can start with the most-significant bit (MSB); Data_Out can start with the least-significant bit (LSB). Each channel is separately configurable. The inverse bit order (that is, LSB first) is supported only for sample sizes up to 24 bits.
- It is not necessary for Data_In and Data_Out to be the same length.
- The Data_Out line is configured to Hi-Z output between data words. Data_Out can also be set for permanent Hi-Z, regardless of data out. This allows the CC256x device to be a bus slave in a multislave PCM environment. At power up, Data_Out is configured as Hi-Z.

4.5.3.4 Frame Idle Period

The codec interface handles frame idle periods, in which the clock pauses and becomes 0 at the end of the frame, after all data are transferred.

The CC256x device supports frame idle periods both as master and slave of the codec bus.

When the CC256x device is master of the interface, the frame idle period is configurable. There are two configurable parameters:

- Clk_Idle_Start: indicates the number of clock cycles from the beginning of the frame to the beginning of the idle period. After Clk_Idle_Start clock cycles, the clock becomes 0.
- Clk_Idle_End: indicates the time from the beginning of the frame to the end of the idle period. The time is given in multiples of clock periods.

The delta between Clk_Idle_Start and Clk_Idle_End is the clock idle period.

For example, for clock rate = 1 MHz, frame sync period = 10 kHz, Clk_Idle_Start = 60, Clk_Idle_End = 90.

Between both frame-sync signals there are 70 clock cycles (instead of 100). The clock idle period starts 60 clock cycles after the beginning of the frame and lasts 90 – 60 = 30 clock cycles. This means that the idle period ends 100 – 90 = 10 clock cycles before the end of the frame. The data transmission must end before the beginning of the idle period.

Figure 4-12 shows the frame idle timing.

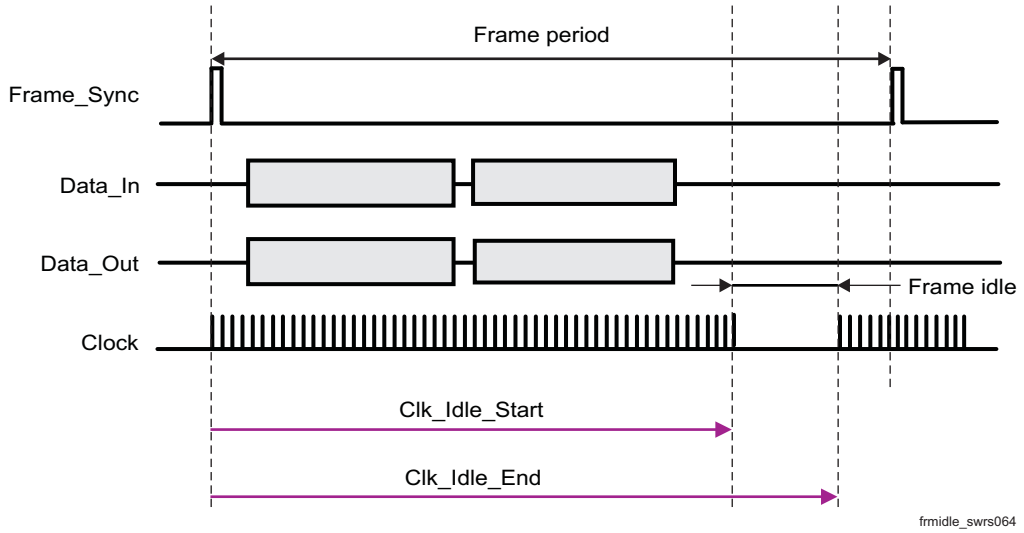


Figure 4-12. Frame Idle Period

4.5.3.5 Clock-Edge Operation

The codec interface of the CC256x device can work on the rising or the falling edge of the clock and can sample the frame-sync signal and the data at inversed polarity.

Figure 4-13 shows the operation of a falling-edge-clock type of codec. The codec is the master of the bus. The frame-sync signal is updated (by the codec) on the falling edge of the clock and is therefore sampled (by the CC256x device) on the next rising clock. The data from the codec is sampled (by the CC256x device) on the falling edge of the clock.

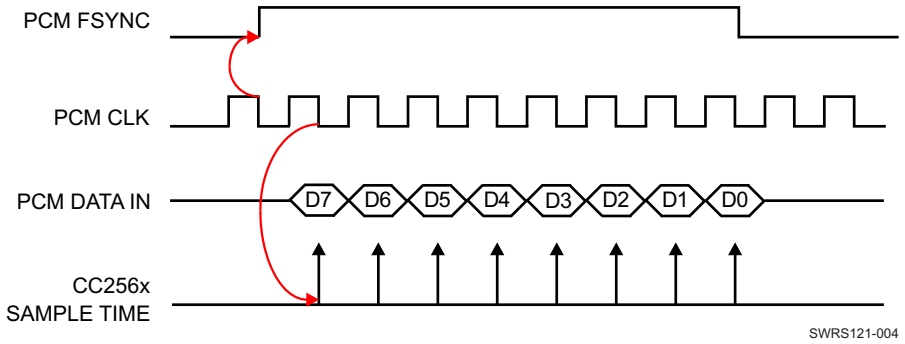


Figure 4-13. Negative Clock Edge Operation

4.5.3.6 Two-Channel Bus Example

Figure 4-14 shows a 2-channel bus in which the two channels have different word sizes and arbitrary positions in the bus frame. (FT stands for frame timer.)

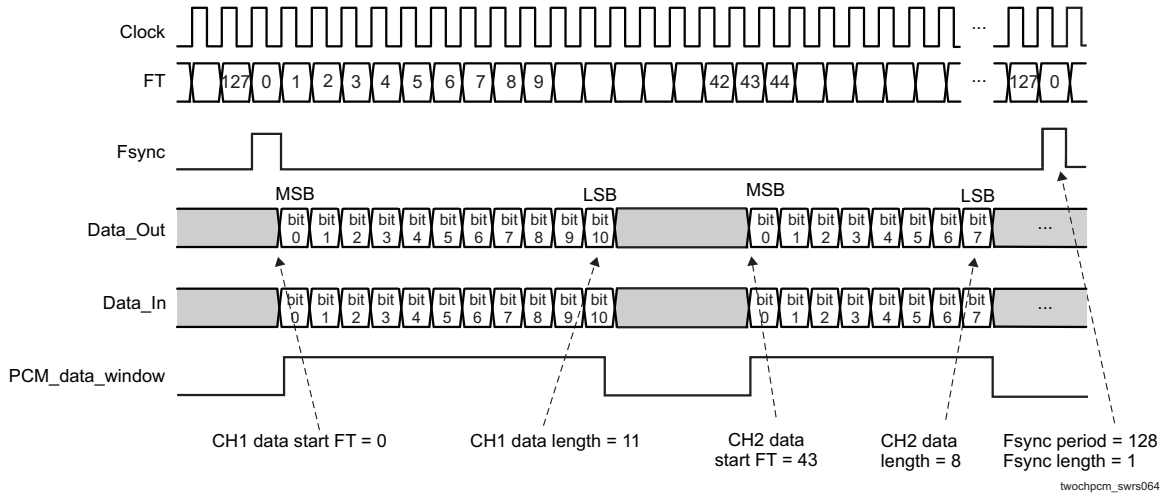


Figure 4-14. Two-Channel Bus Timing

4.5.3.7 Improved Algorithm For Lost Packets

The CC256x device features an improved algorithm to improve voice quality when received voice data packets are lost. There are two options:

- Repeat the last sample: possible only for sample sizes up to 24 bits. For sample sizes larger than 24 bits, the last byte is repeated.
- Repeat a configurable sample of 8 to 24 bits (depending on the real sample size) to simulate silence (or anything else) in the bus. The configured sample is written in a specific register for each channel.

The choice between those two options is configurable separately for each channel.

4.5.3.8 *Bluetooth* and Codec Clock Mismatch Handling

In *Bluetooth* RX, the CC256x device receives RF voice packets and writes them to the codec interface. If the CC256x device receives data faster than the codec interface output allows, an overflow occurs. In this case, the *Bluetooth* has two possible behavior modes:

- Allow overflow: if overflow is allowed, the *Bluetooth* continues receiving data and overwrites any data not yet sent to the codec.
- Do not allow overflow: if overflow is not allowed, RF voice packets received when the buffer is full are discarded.

5 DEVICE SPECIFICATIONS

Unless otherwise indicated, all measurements are taken at the device pins of the TI test evaluation board (EVB).

All specifications are over process, voltage and temperature, unless otherwise indicated.

5.1 General Device Requirements and Operation

5.1.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)

NOTE

Unless otherwise indicated, all parameters are measured as follows:

VDD_IN = 3.6 V, VDD_IO = 1.8 V

See (1)			Value	Unit
Ratings over operating free-air temperature range				
VDD_IN	Supply voltage range		–0.5 to 4.8	V(2)
VDDIO_1.8V			–0.5 to 2.145	V
	Input voltage to analog pins(3)		–0.5 to 2.1	V
	Input voltage to all other pins		–0.5 to (VDD_IO + 0.5)	V
	Operating ambient temperature range(4)		–40 to 85	°C
	Storage temperature range		–55 to 125	°C
	Bluetooth RF inputs		10	dBm
ESD stress voltage(5)	Human body model (HBM)(6)	Device	500	V
	Charged device model (CDM)(7)	Device	250	

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Maximum allowed depends on accumulated time at that voltage: VDD_IN is defined in Section 6, *Reference Design for Power and Radio Connections*.
(3) Analog pins: BT_RF, XTALP, and XTALM
(4) The reference design supports a temperature range of –20°C to 70°C because of the operating conditions of the crystal.
(5) ESD measures device sensitivity and immunity to damage caused by electrostatic discharges into the device.
(6) The level listed is the passing level per ANSI/ESDA/JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process, and manufacturing with less than 500-V HBM is possible, if necessary precautions are taken. Pins listed as 1000 V can actually have higher performance.
(7) The level listed is the passing level per EIA-JEDEC JESD22-C101E. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process, and manufacturing with less than 250-V CDM is possible, if necessary precautions are taken. Pins listed as 250 V can actually have higher performance.

5.1.2 Recommended Operating Conditions

Rating	Condition	Sym	Min	Max	Unit
Power supply voltage		VDD_IN	2.2	4.8	V
I/O power supply voltage		VDD_IO	1.62	1.92	V
High-level input voltage	Default	V_{IH}	0.65 x VDD_IO	VDD_IO	V
Low-level input voltage	Default	V_{IL}	0	0.35 x VDD_IO	V
I/O input rise and all times,10% to 90% — asynchronous mode		t_r and t_f	1	10	ns
I/O input rise and fall times, 10% to 90% — synchronous mode (PCM)			1	2.5	ns
Voltage dips on VDD_IN (V_{BAT}) duration = 577 µs to 2.31 ms, period = 4.6 ms				400	mV
Maximum ambient operating temperature(1) (2)			–40	85	°C

(1) The device can be reliably operated for 7 years at $T_{ambient}$ of 85°C, assuming 25% active mode and 75% sleep mode (15,400 cumulative active power-on hours).
(2) A crystal-based solution is limited by the temperature range required of the crystal to meet 20 ppm.

5.1.3 Current Consumption

5.1.3.1 Static Current Consumption

Operational Mode	Min	Typ	Max	Unit
Shutdown mode(1)		1	7	µA
Deep sleep mode(2)		40	105	µA
Idle mode		4		mA
Total I/O current consumption in active mode			1	mA
Continuous transmission—GFSK(3)			77	mA
Continuous transmission—EDR(4)(5)			82.5	mA

(1) $V_{BAT} + V_{IO} + V_{SHUTDOWN}$
(2) $V_{BAT} + V_{IO}$
(3) At maximum output power (12 dBm)
(4) At maximum output power (10 dBm)
(5) Both π/4 DQPSK and 8DPSK

5.1.3.2 Dynamic Current Consumption

5.1.3.2.1 Current Consumption for Different Bluetooth BR/EDR Scenarios

Conditions: VDD_IN = 3.6 V, 25°C, 26-MHz XTAL, nominal unit, 4-dBm output power

Operational Mode	Master and Slave	Average Current	Unit
Synchronous connection oriented (SCO) link HV3	Master and slave	13.7	mA
Extended SCO (eSCO) link EV3 64 kbps, no retransmission	Master and slave	13.2	mA
eSCO link 2-EV3 64 kbps, no retransmission	Master and slave	10	mA
GFSK full throughput: TX = DH1, RX = DH5	Master and slave	40.5	mA
EDR full throughput: TX = 2-DH1, RX = 2-DH5	Master and slave	41.2	mA
EDR full throughput: TX = 3-DH1, RX = 3-DH5	Master and slave	41.2	mA
Sniff, one attempt, 1.28 seconds	Master and slave	250	µA
Page or inquiry scan 1.28 seconds, 11.25 ms	Master and slave	400	µA
Page (1.28 seconds) and inquiry (2.56 seconds) scans, 11.25 ms	Master and slave	500	µA

Conditions: VDD_IN = 3.6 V, 25°C, 26-MHz fast clock, nominal unit, 4-dBm output power

Operational Mode	Master and Slave	Average Current	Unit
Synchronous connection oriented (SCO) link HV3	Master and slave	12	mA
Extended SCO (eSCO) link EV3 64 kbps, no retransmission	Master and slave	11.5	mA
eSCO link 2-EV3 64 kbps, no retransmission	Master and slave	8.3	mA
GFSK full throughput: TX = DH1, RX = DH5	Master and slave	38.5	mA
EDR full throughput: TX = 2-DH1, RX = 2-DH5	Master and slave	39.2	mA
EDR full throughput: TX = 3-DH1, RX = 3-DH5	Master and slave	39.2	mA
Sniff, one attempt, 1.28 seconds	Master and slave	76 and 100	µA
Page or inquiry scan 1.28 seconds, 11.25 ms	Master and slave	300	µA
Page (1.28 seconds) and inquiry (2.56 seconds) scans, 11.25 ms	Master and slave	430	µA

5.1.3.2.2 Current Consumption for Different LE Scenarios

Conditions: VDD_IN = 3.6 V, 25°C, 26-MHz fast clock, nominal unit, 10 dBm output power

Mode	Description	Average Current	Unit
Advertising, nonconnectable	Advertising in all three channels 1.28-seconds advertising interval 15 bytes advertise data	104	µA
Advertising, discoverable	Advertising in all three channels 1.28-seconds advertising interval 15 bytes advertise data	121	µA
Scanning	Listening to a single frequency per window 1.28-seconds scan interval 11.25-ms scan window	302	µA
Connected (master role)	500-ms connection interval 0-ms slave connection latency Empty TX and RX LL packets	169	µA

5.1.4 General Electrical Characteristics

Rating			Condition	Min	Max	Unit
High-level output voltage, V_{OH}			At 2, 4, 8 mA	0.8 x VDD_IO	VDD_IO	V
			At 0.1 mA	VDD_IO – 0.2	VDD_IO	V
Low-level output voltage, V_{OL}			At 2, 4, 8 mA	0	0.2 x VDD_IO	V
			At 0.1 mA	0	0.2	V
I/O input impedance			Resistance	1		MΩ
			Capacitance		5	pF
Output rise and fall times, 10% to 90% (digital pins)			C_L = 20 pF		10	ns
I/O pull currents	PCM-I2S bus, TX_DBG	PU	typ = 6.5	3.5	9.7	µA
		PD	typ = 27	9.5	55	
	All others	PU	typ = 100	50	300	µA
		PD	typ = 100	50	360	

5.1.5 nSHUTD Requirements

Parameter	Sym	Min	Max	Unit
Operation mode level (1)	V_{IH}	1.42	1.98	V
Shutdown mode level (1)	V_{IL}	0	0.4	V
Minimum time for nSHUT_DOWN low to reset the device		5		ms
Rise and fall times	t_r and t_f		20	µs

(1) Internal pulldown retains shut-down mode when no external signal is applied to this pin.

5.1.6 Slow Clock Requirements

Characteristics	Condition	Sym	Min	Typ	Max	Unit
Input slow clock frequency				32768		Hz
Input slow clock accuracy (Initial + temp + aging)	*Bluetooth*				±250	ppm
	Input transition time t_r and t_f (10% to 90%)		t_r and t_f		200	
Frequency input duty cycle			15%	50%	85%	
Slow clock input voltage limits	Square wave, DC-coupled	V_{IH}	0.65 × VDD_IO		VDD_IO	V peak
		V_{IL}	0		0.35 × VDD_IO	V peak
Input impedance			1			MΩ
Input capacitance					5	pF

5.1.7 External Fast Clock Crystal Requirements and Operation

Characteristics	Condition	Sym	Min	Typ	Max	Unit
Supported crystal frequencies		f_{in}		26		MHz
Frequency accuracy (Initial + temperature + aging)					±20	ppm
Crystal oscillator negative resistance	26 MHz, external capacitance = 8 pF I_{osc} = 0.5 mA		650	940		Ω
	26 MHz, external capacitance = 20 pF I_{osc} = 2.2 mA		490	710		

5.1.8 Fast Clock Source Requirements (–40°C to +85°C)

Characteristics	Condition		Sym	Min	Typ	Max	Unit
Supported frequencies			F_{REF}		26		MHz
Reference frequency accuracy	Initial + temp + aging					±20	ppm
Fast clock input voltage limits	Square wave, DC-coupled	V_{IL}		–0.2		0.37	V
		V_{IH}		1.0		2.1	V
	Sine wave, AC-coupled			0.4		1.6	V_{p-p}
	Sine wave, DC-coupled			0.4		1.6	V_{p-p}
	Sine wave input limits, DC-coupled			0		1.6	V
Fast clock input rise time (as % of clock period)	Square wave, DC-coupled					10%	
Duty cycle				35%	50%	65%	
Phase noise for 26 MHz	@ offset = 1 kHz					–123.4	dBc/Hz
	@ offset =10 kHz					–133.4	dBc/Hz
	@ offset = 100 kHz					–138.4	dBc/Hz

5.2 *Bluetooth* BR/EDR RF Performance

All parameters in this section that are fast-clock dependent are verified using a 26-MHz XTAL under a temperature range from –20°C to 70°C and an RF load of 50 Ω at the BT_RF port of the IC.

5.2.1 Bluetooth Receiver—In-Band Signals

Characteristics	Condition		Min	Typ	Max	*Bluetooth* Specification	Unit
Operation frequency range			2402		2480		MHz
Channel spacing				1			MHz
Input impedance				50			Ω
Sensitivity, dirty TX on[1]	GFSK, BER = 0.1%		–91.5	–95		–70	dBm
	Pi/4-DQPSK, BER = 0.01%		–90.5	–94.5		–70	
	8DPSK, BER = 0.01%		–81	–87.5		–70	
BER error floor at sensitivity + 10 dB, dirty TX off	Pi/4-DQPSK		1E–6	1E–7		1E–5	
	8DPSK		1E–6			1E–5	
Maximum usable input power	GFSK, BER = 0.1%		–5			–20	dBm
	Pi/4-DQPSK, BER = 0.1%		–10				
	8DPSK, BER = 0.1%		–10				
Intermodulation characteristics	Level of interferers For n = 3, 4, and 5		–36	–30		–39	dBm
C/I performance	GFSK, co-channel			8	10	11	dB
	EDR, co-channel	Pi/4-DQPSK		9.5	11	13	
Note: Numbers show desired-signal to interfering-signal ratio.		8DPSK		16.5	20	21	
	GFSK, adjacent ±1 MHz			–10	–5	0	
Smaller numbers indicate better C/I performance.	EDR, adjacent ±1 MHz, (image)	Pi/4-DQPSK		–10	–5	0	
		8DPSK		–5	–1	5	
Image = –1 MHz	GFSK, adjacent +2 MHz			–38	–35	–30	
	EDR, adjacent, +2 MHz,	Pi/4-DQPSK		–38	–35	–30	
		8DPSK		–38	–30	–25	
	GFSK, adjacent –2 MHz			–28	–20	–20	
	EDR, adjacent –2 MHz	Pi/4-DQPSK		–28	–20	–20	
		8DPSK		–22	–13	–13	
	GFSK, adjacent ≥ |±3| MHz			–45	–43	–40	
	EDR, adjacent ≥ |±3|MHz	Pi/4-DQPSK		–45	–43	–40	
		8DPSK		–44	–36	–33	
RF return loss				–10			dB
RX mode LO leakage	Frf = (received RF frequency – 0.6 MHz)			–63	–58		dBm

(1) Sensitivity degradation up to 3 dB may occur for minimum and typical values where the *Bluetooth* frequency is a harmonic of the fast clock.

5.2.2 Bluetooth Receiver—General Blocking

Characteristics	Condition	Min	Typ	Unit
Blocking performance over full range, according to *Bluetooth* specification [1]	30 to 2000 MHz		–6	dBm
	2000 to 2399 MHz		–6	
	2484 to 3000 MHz		–6	
	3 to 12.75 GHz		–6	

(1) Exceptions are taken out of the total 24 allowed in the *Bluetooth* specification.

5.2.3 Bluetooth Transmitter—GFSK

Characteristics	Min	Typ	Max	*Bluetooth* Specification	Unit
Maximum RF output power(1)	10	12			dBm
Power variation over *Bluetooth* band	–1		1		dB
Gain control range		30			dB
Power control step	2	5	8	2 to 8	
Adjacent channel power |M–N| = 2		–45	–39	≤ –20	dBm
Adjacent channel power |M–N| > 2		–50	–42	≤ –40	

(1) To modify maximum output power, use an HCI VS command.

5.2.4 Bluetooth Transmitter—EDR

Characteristics		Min	Typ	Max	*Bluetooth* Specification	Unit
Maximum RF output power(1)	Pi/4-DQPSK	6	8			dBm
	8DPSK	6	8			
Relative power		–2		1	–4 to +1	dB
Power variation over *Bluetooth* band		–1		1		
Gain control range			30			
Power control step		2	5	8	2 to 8	
Adjacent channel power |M–N| = 1			–36	–30	≤ –26	dBc
Adjacent channel power |M–N| = 2 (2)			–30	–23	≤ –20	dBm
Adjacent channel power |M–N| > 2 (2)			–42	–40	≤ –40	dBm

(1) To modify maximum output power, use an HCI VS command.
(2) Assumes 3-dB insertion loss from *Bluetooth* RF ball to antenna

5.2.5 Bluetooth Modulation—GFSK

Characteristics	Condition		Sym	Min	Typ	Max	*Bluetooth* Specification	Unit
–20 dB bandwidth	GFSK				925	995	≤ 1000	kHz
Modulation characteristics	Δf1avg	Mod data = 4 1s, 4 0s: 111100001111...	F1 avg	150	165	170	140 to 175	kHz
	Δf2max ≥ limit for at least 99.9% of all Δf2max	Mod data = 1010101...	F2 max	115	130		> 115	kHz
	Δf2avg, Δf1avg			85	88		> 80	%
Absolute carrier frequency drift	DH1			–25		25	< ±25	kHz
	DH3 and DH5			–35		35	< ±40	kHz
Drift rate						15	< 20	kHz/ 50 µs
Initial carrier frequency tolerance	f0 – fTX			–75		75	< ±75	kHz

5.2.6 Bluetooth Modulation—EDR

Characteristics	Condition	Min	Typ	Max	*Bluetooth* Specification	Unit
Carrier frequency stability			±3	±5	≤ 10	kHz
Initial carrier frequency tolerance				±75	±75	kHz
Rms DEVM (1)	Pi/4-DQPSK		6	15	20	%
	8DPSK		6	13	13	
99% DEVM(1)	Pi/4-DQPSK			30	30	
	8DPSK			20	20	
Peak DEVM (1)	Pi/4-DQPSK		14	30	35	
	8DPSK		16	25	25	

(1) Max performance refers to maximum TX power.

5.2.7 Bluetooth Transmitter—Out-of-Band and Spurious Emissions

Characteristics	Condition	Typ	Max	Unit
Second harmonic(1)	Measured at maximum output power	–14	–2	dBm
Third harmonic(1)		–10	–6	dBm
Fourth harmonics(1)		–19	–11	dBm

(1) Meets FCC and ETSI requirements with external filter shown in Figure 6-1

5.3 *Bluetooth* LE RF Performance

All parameters in this section that are fast-clock dependent are verified using a 26-MHz XTAL under a temperature range from –20°C to 70°C and an RF load of 50 Ω at the BT_RF port of the IC.

5.3.1 BLE Receiver—In Band Signals

Characteristic	Condition	Min	Typ	Max	BLE Specification	Unit
Operation frequency range		2402		2480		MHz
Channel spacing			2			MHz
Input impedance			50			Ω
Sensitivity dirty TX on(1)	PER = 30.8%; dirty TX on	–93	–96		≤ –70	dBm
Maximum usable input power	GMSK, PER = 30.8%	–5			≥ –10	dBm
Intermodulation characteristics	Level of interferers. For n = 3, 4, 5	–36	–30		≥ –50	dBm
C/I performance(2) Image = –1 MHz	GMSK, co-channel		8	12	≤ 21	dB
	GMSK, adjacent ±1 MHz		–5	0	≤ 15	
	GMSK, adjacent +2 MHz		–45	–38	≤ –17	
	GMSK, adjacent –2 MHz		–22	–15	≤ –15	
	GMSK, adjacent ≥ |±3| MHz		–47	–40	≤ –27	
RX mode LO leakage	Frf = (received freq – 0.6 MHz)		–63	–58		dBm

(1) Sensitivity degradation up to 3 dB may occur where the BLE frequency is a harmonic of the fast clock.
(2) Numbers show wanted signal-to-interfering signal ratio. Smaller numbers indicate better C/I performance.

5.3.2 BLE Receiver—General Blocking

Characteristics	Condition	Min	Typ	BLE Specification	Unit
Blocking performance over full range, according to BLE specification(1)	30–2000 MHz		–15	≥ –30	dBm
	2000–2399 MHz		–15	≥ –35	
	2484–3000 MHz		–15	≥ –35	
	3–12.75 GHz		–15	≥ –30	

(1) Exceptions are taken out of the total 10 allowed in the BLE specification.

5.3.3 BLE Transmitter

Characteristics	Min	Typ	Max	BLE Specification	Unit
Maximum RF output power(1)	10	12(2)		≤10	dBm
Power variation over BLE band	–1		1		dB
Adjacent channel power |M-N| = 2		–45	–39	≤ –20	dBm
Adjacent channel power |M-N| > 2		–50	–42	≤ –30	

(1) To modify maximum output power, use an HCI VS command.
(2) To achieve the BLE specification of 10-dBm maximum, an insertion loss of > 2 dB is assumed between the RF ball and the antenna. Otherwise, use an HCI VS command to modify the output power.

5.3.4 BLE Modulation

Characteristics	Condition		Sym	Min	Typ	Max	BLE Specification	Unit
Modulation characteristics	Δf1avg	Mod data = 4 1s, 4 0s: 1111000011110000...	Δf1 avg	240	250	260	225 to 275	kHz
	Δf2max ≥ limit for at least 99.9% of all Δf2max	Mod data = 1010101...	Δf2 max	185	210		≥ 185	kHz
	Δf2avg, Δf1avg			0.85	0.9		≥ 0.8	
Absolute carrier frequency drift				–25		25	≤ ±50	kHz
Drift rate						15	≤ 20	kHz/50 ms
Initial carrier frequency tolerance				–75		75	≤ ±100	kHz

5.3.5 BLE Transceiver, Out-Of-Band and Spurious Emissions

See Section 5.2.7, *Bluetooth Transmitter, Out-of-Band and Spurious Emissions*.

5.4 Interface Specifications

5.4.1 UART

Figure 5-1 shows the UART timing diagram. Table 5-1 lists the UART timing characteristics.

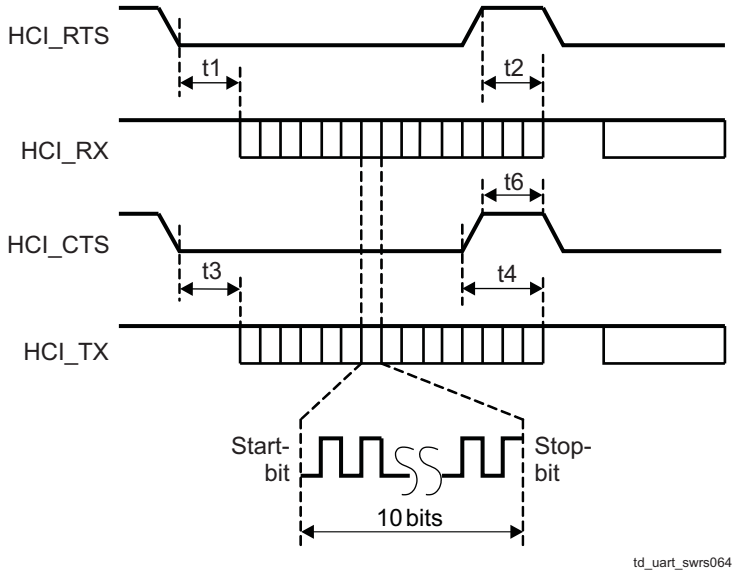


Figure 5-1. UART Timing

Table 5-1. UART Timing Characteristics

Symbol	Characteristics	Condition	Min	Typ	Max	Unit
	Baud rate		37.5		4000	kbps
	Baud rate accuracy per byte	Receive and transmit	–2.5		1.5	%
	Baud rate accuracy per bit	Receive and transmit	–12.5		12.5	%
t3	CTS low to TX_DATA on		0	2		µs
t4	CTS high to TX_DATA off	Hardware flow control			1	byte
t6	CTS-high pulse width		1			bit
t1	RTS low to RX_DATA on		0	2		µs
t2	RTS high to RX_DATA off	Interrupt set to 1/4 FIFO			16	byte

Figure 5-2 shows the UART data frame. Table 5-2 describes the symbols used in Figure 5-2.

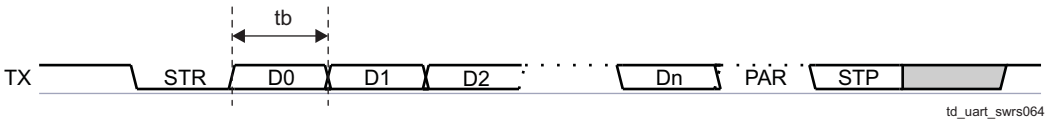


Figure 5-2. Data Frame

Table 5-2. Data Frame Key

Symbol	Description
STR	Start-bit
D0...Dn	Data bits (LSB first)
PAR	Parity bit (optional)
STP	Stop-bit

5.4.2 PCM

Figure 5-3 shows the interface timing for the PCM. Table 5-3 and Table 5-4 list the associated master and slave parameters.

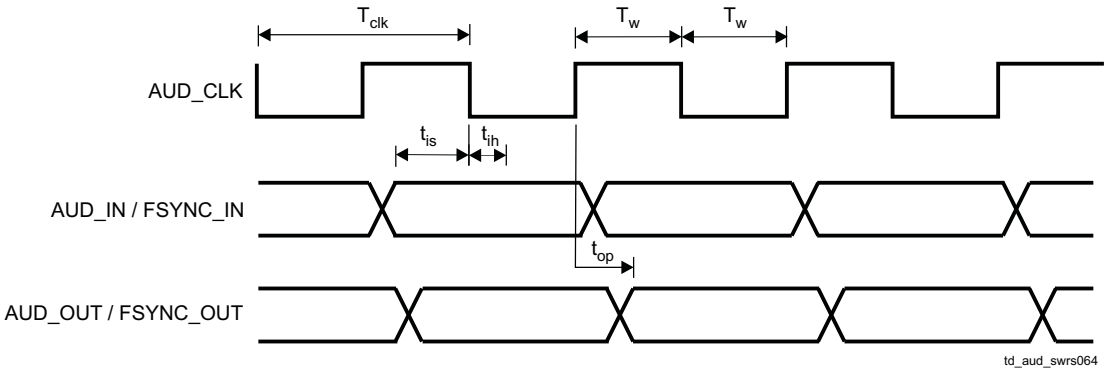


Figure 5-3. PCM Interface Timing

Table 5-3. PCM Master

Symbol	Parameter	Condition	Min	Max	Unit
T_{clk}	Cycle time		244.14 (4.096 MHz)	15625 (64 kHz)	ns
T_w	High or low pulse width		50% of T_{clk} min		
t_{is}	AUD_IN setup time		25		
t_{ih}	AUD_IN hold time		0		
t_{op}	AUD_OUT propagation time	40-pF load	0	10	
t_{op}	FSYNC_OUT propagation time	40-pF load	0	10	

Table 5-4. PCM Slave

Symbol	Parameter	Condition	Min	Max	Unit
T_{clk}	Cycle time		66.67 (15 MHz)		ns
T_w	High or low pulse width		40% of T_{clk}		
T_{is}	AUD_IN setup time		8		
T_{ih}	AUD_IN hold time		0		
t_{is}	AUD_FSYNC setup time		8		
t_{ih}	AUD_FSYNC hold time		0		
t_{op}	AUD_OUT propagation time	40-pF load	0	21	

6 REFERENCE DESIGN AND BOM FOR POWER AND RADIO CONNECTIONS

Figure 6-1 shows the reference schematics for the CC256x device.

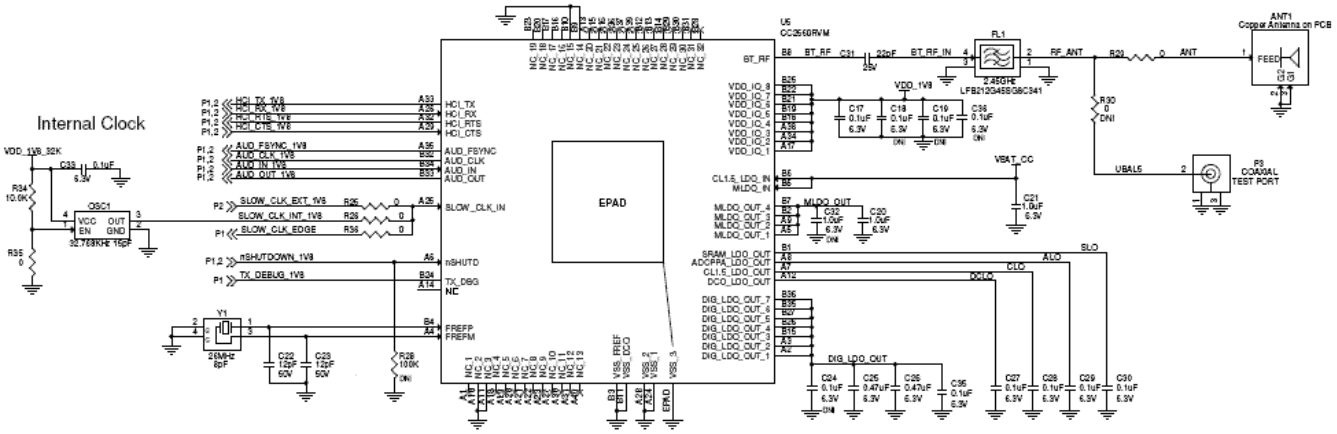


Figure 6-1. Reference Schematics

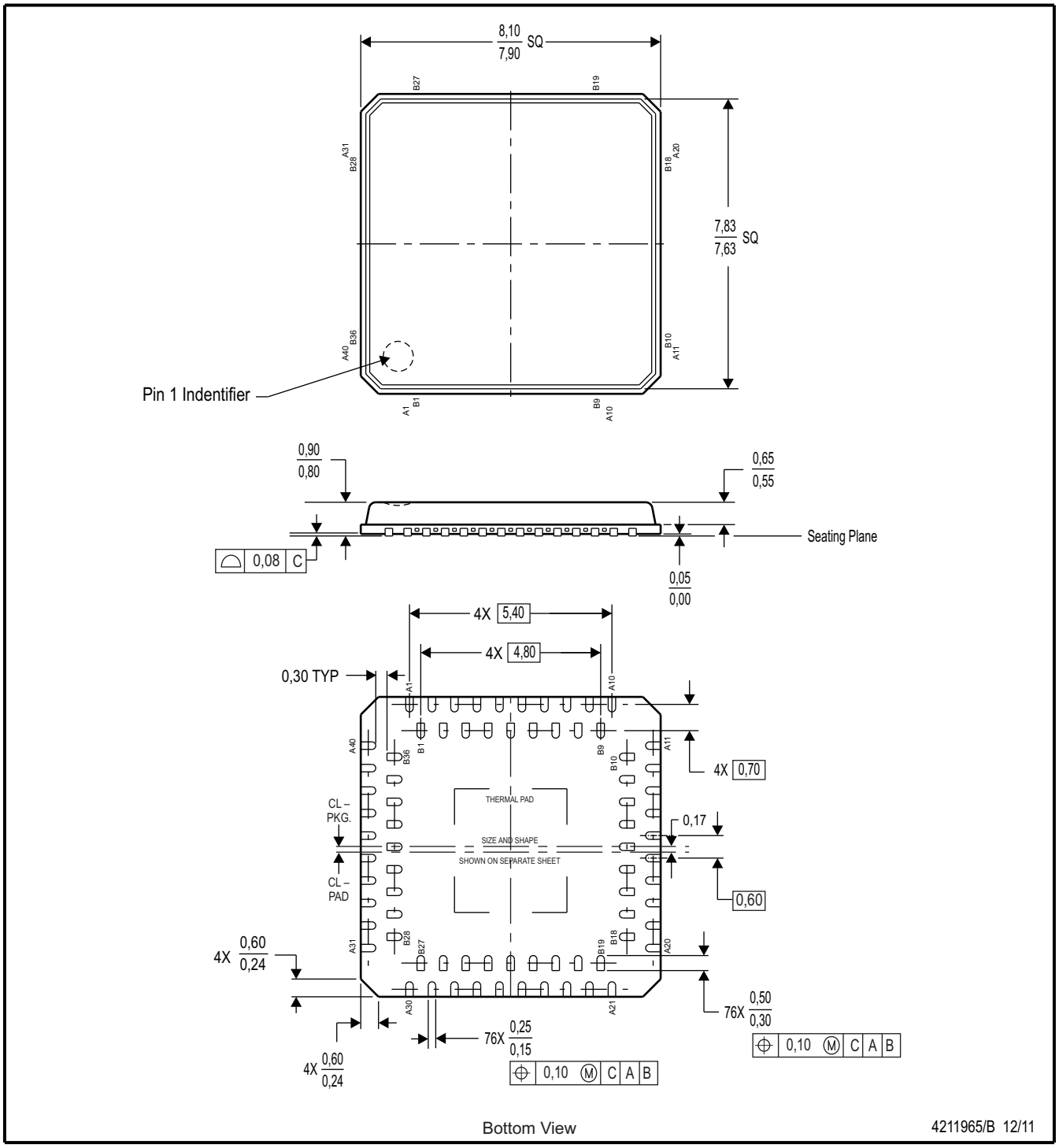
Table 6-1 lists the BOM for the CC256x device.

Table 6-1. Bill of Materials

Qty	Reference Des.	Value	Description	Manufacturer	Manufacturer Part Number	Alternate Part	Note
1	ANT1	NA	ANT_IIFA_CC2420_32mil_MIR	NA	IIFA_CC2420	Chip antenna	Copper antenna on PCB
6	Capacitor	0.1 µF	CAP CER 1.0UF 6.3 V X5R 10% 0402	Kemet	C0402C104K9RACTU		
2	Capacitor	1.0 µF	CAP CER 10-pF 50 V 5% NP0 0402	Taiyo Yuden	JMK105BJ105KV-F		
2	Capacitor	12 pF (TBD)	CAP CER 12 pF 6.3 V X5R 10% 0402	Murata Electronics	GRM1555C1H120JZ01D		
2	Capacitor	0.47 µF	CAP CER .47UF 6.3V X5R ±10% 0402	Taiyo Yuden	JMK105BJ474KV-F		
1	FL1	2.45 GHz	FILTER CER BAND PASS 2.45 GHZ SMD	Murata Electronics	LFB212G45SG8C341		Place brown marking up
1	OSC1	32,768 kHz 15 pF	OSC 32.768 KHZ 15 pF 1.5 V 3.3 V SMD	Abracon Corporation	ASH7K-32.768KHZ-T		Optional
1	U5	CC2560RVM or CC2564RVM	Bluetooth BR/EDR/LE or ANT Single-Chip Solution	Texas Instruments	CC256xRVM		
1	Y1	26 MHz	Crystal, 26 MHz	NDK	NX2016SA	TZ1325D (Tai-Saw TST)	
1	C31	22 pF	CAP CER 22PF 25V 5% NP0 0201	Murata Electronics North America	GRM0335C1E220JD01D		

7 mrQFN MECHANICAL DATA

RVM (S-PVQFN-N76) PLASTIC QUAD FLATPACK NO-LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5-1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No-Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

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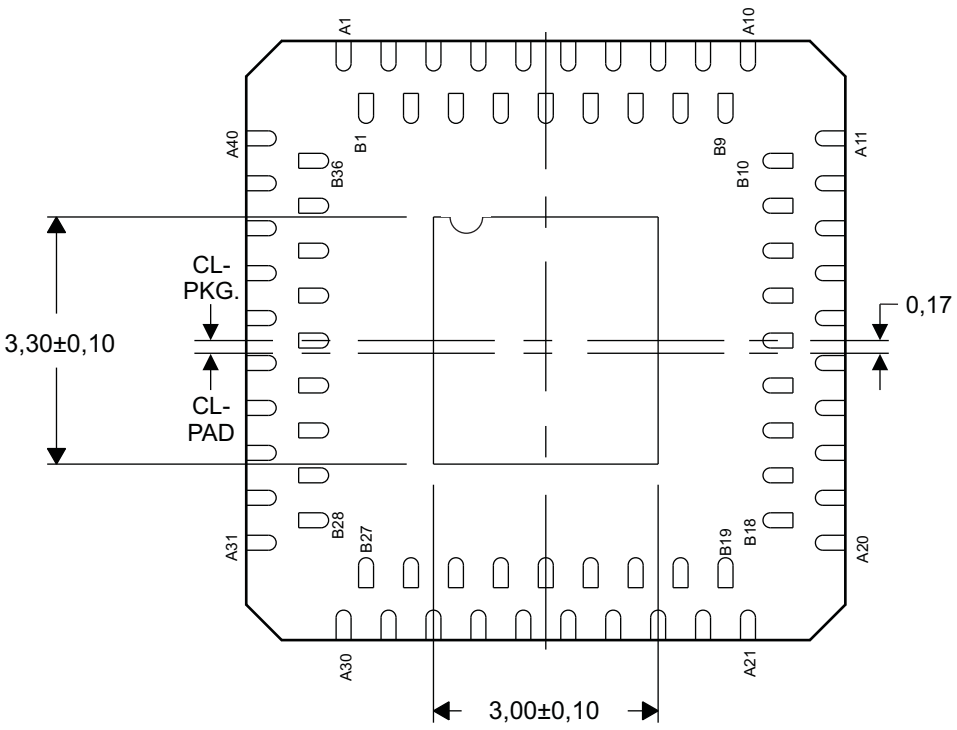
RVM (S-PVQFN-N76) PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4212066/B 12/11

NOTE: All linear dimensions are in millimeters

SWRS115-018

8 CHIP PACKAGING AND ORDERING

8.1 Package and Ordering Information

The mrQFN packaging is 76 pins and a 0.6-mm pitch.

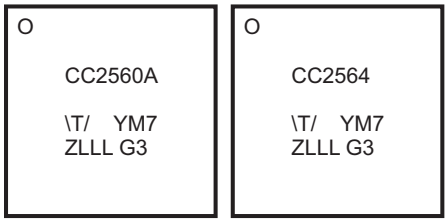
For detailed information, see Section 7, *mrQFN Mechanical Data*.

Table 8-1 lists the package and order information for the device family members.

Table 8-1. Package and Order Information

Device	Package Suffix	Pieces/Reel
CC2560ARVMT	RVM	250
CC2560ARVMR	RVM	2500
CC2564RVMT	RVM	250
CC2564RVMR	RVM	2500

Figure 8-1 shows the chip markings for the CC256x family.



\T/ = TI logo
Y = Last digit of the year
M = Month in hex number, 1-C for Jan-Dec
7 = Primary site code for ANM
Z = Secondary site code for ANM
LLL = Assembly lot code
O = Pin 1 indicator

SWRS121-010

Figure 8-1. Chip Markings

8.1.1 Device Support Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers. These prefixes represent evolutionary stages of product development from engineering prototypes through fully qualified production devices.

X Experimental, preproduction, sample or prototype device. Device may not meet all product qualification conditions and may not fully comply with TI specifications. Experimental/Prototype devices are shipped against the following disclaimer: “This product is still in development and is intended for internal evaluation purposes.” Notwithstanding any provision to the contrary, TI makes no warranty expressed, implied, or statutory, including any implied warranty of merchantability of fitness for a specific purpose, of this device.

null Device is qualified and released to production. TI’s standard warranty applies to production devices.

8.2 Empty Tape Portion

Figure 8-2 shows the empty portion of the carrier tape.

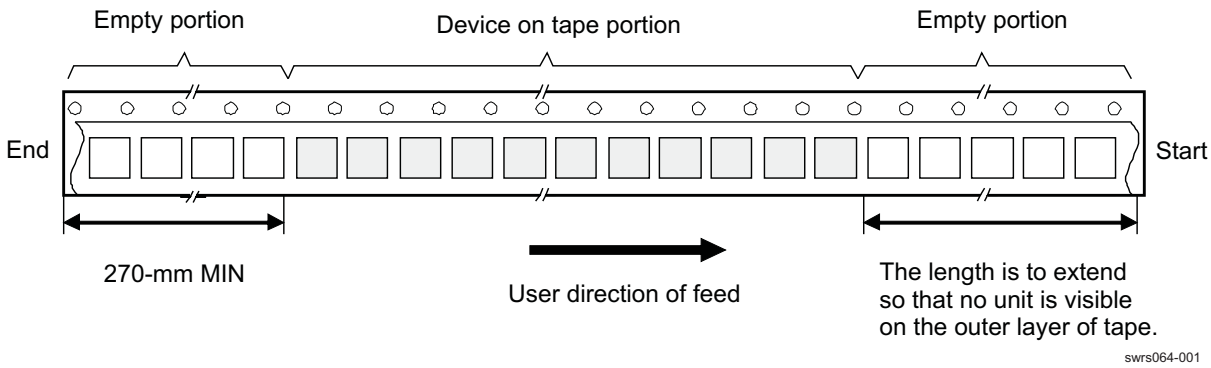


Figure 8-2. Carrier Tape and Pockets

8.3 Device Quantity and Direction

When pulling out the tape, the A1 corner is on the left side (see Figure 8-3).

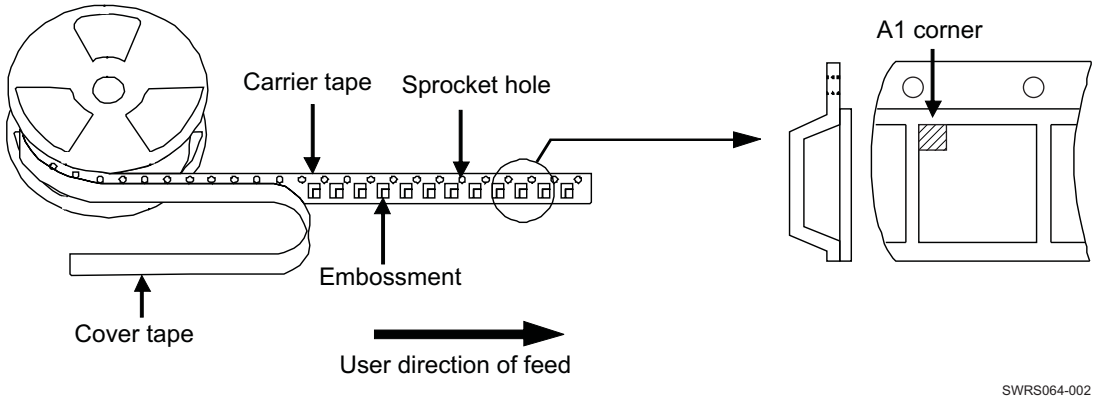


Figure 8-3. Direction of Device

8.4 Insertion of Device

Figure 8-4 shows the insertion of the device.

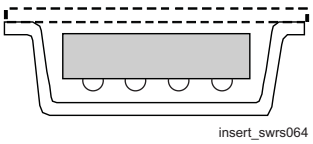


Figure 8-4. Insertion of Device

8.5 Tape Specification

The dimensions of the tape are:

- Tape width: 16 mm
- Cover tape: The cover tape does not cover the index hole and does not shift to outside from the carrier tape.
- Tape structure: The carrier tape is made of plastic. The device is put in the embossed area of the carrier tape and covered by the cover tape, which is made of plastic.
- ESD countermeasure: The plastic material used in the carrier tape and the cover tape is static dissipative.

8.6 Reel Specification

Figure 8-5 shows the reel specifications:

- 330-mm reel, 16-mm width tape
- Reel material: Polystyrene (static dissipative/antistatic)

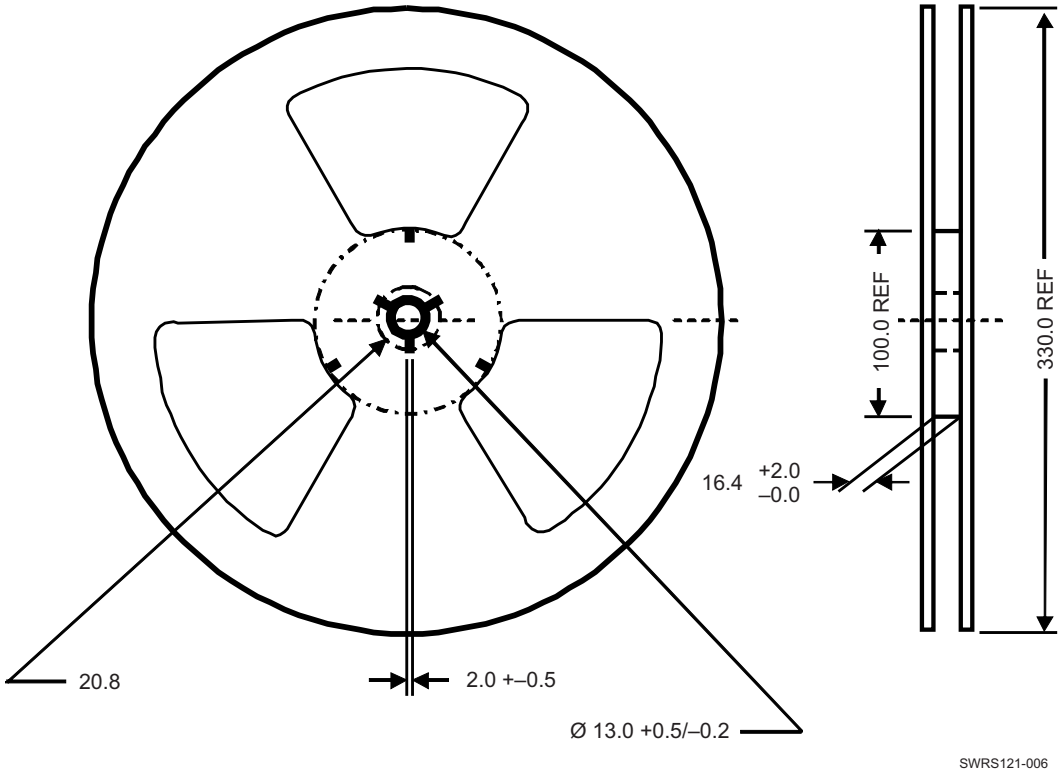


Figure 8-5. Reel Dimensions (mm)

8.7 Packing Method

The end of the leader tape is secured by drafting tape. The reel is packed in a moisture barrier bag fastened by heat-sealing (see Figure 8-6).

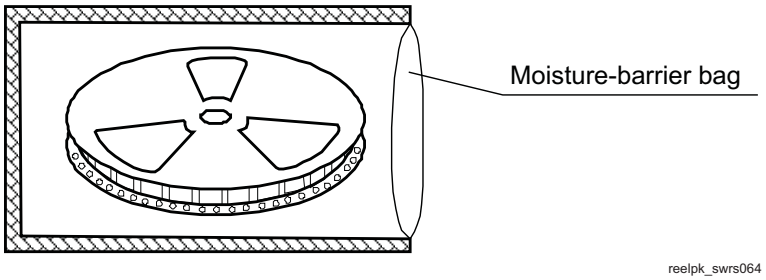


Figure 8-6. Reel Packing Method

CAUTION

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause devices not to meet their published specifications.

8.8 Packing Specification

8.8.1 Reel Box

Each moisture-barrier bag is packed into a reel box, as shown in Figure 8-7.

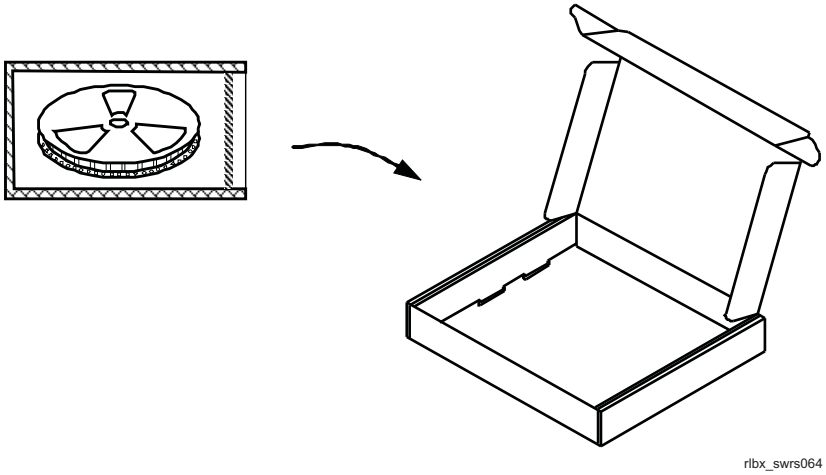


Figure 8-7. Reel Box (Carton)

8.8.2 Reel Box Material

The reel box is made from corrugated fiberboard.

8.8.3 Shipping Box

If the shipping box has excess space, filler (such as cushion) is added.

Figure 8-8 shows a typical shipping box.

NOTE

The size of the shipping box may vary depending on the number of reel boxes packed.

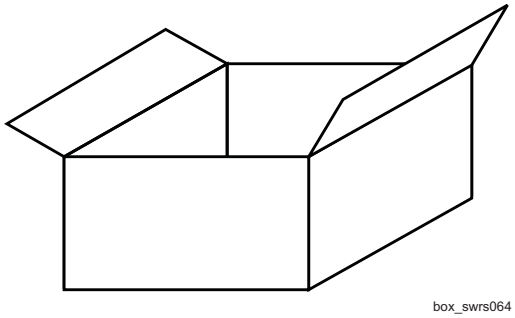


Figure 8-8. Shipping Box (Carton)

8.8.4 Shipping Box Material

The shipping box is made from corrugated fiberboard.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CC2560ARVMR	ACTIVE	VQFN	RVM	76	2500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 85	CC256 0A	Samples
CC2560ARVMT	ACTIVE	VQFN	RVM	76	250	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 85	CC256 0A	Samples
CC2564NSRVMR	ACTIVE	VQFN	RVM	76	2500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 85	CC256 4	Samples
CC2564NSRVMT	ACTIVE	VQFN	RVM	76	250	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 85	CC256 4	Samples
CC2564NSYFVR	ACTIVE	DSBGA	YFV	54	5000	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM		CC2564	Samples
CC2564NSYFVT	ACTIVE	DSBGA	YFV	54	250	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM		CC2564	Samples
CC2564NYFVR	ACTIVE	DSBGA	YFV	54	5000	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM		CC2564	Samples
CC2564NYFVT	ACTIVE	DSBGA	YFV	54	250	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM		CC2564	Samples
CC2564RVMR	ACTIVE	VQFN	RVM	76	2500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 85	CC256 4	Samples
CC2564RVMT	ACTIVE	VQFN	RVM	76	250	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 85	CC256 4	Samples
CC2564YFVR	ACTIVE	DSBGA	YFV	54	5000	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM		CC2564	Samples
CC2564YFVT	ACTIVE	DSBGA	YFV	54	250	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM		CC2564	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265