DRV8829 5-A 45-V Single H-Bridge Motor Driver

1 Features

- Single H-Bridge PWM Motor Driver
  - Single Brushed-DC Motor Driver
  - 1/2 Bipolar Stepper Motor Driver
- 5-A peak or 3.5-A rms Output Current
- 6.5- to 45-V Operating Supply Voltage Range
- Simple PH/EN Control Interface
- Multiple Decay Modes
  - Mixed Decay
  - Slow Decay
  - Fast Decay
- Low-Current Sleep Mode (10 µA)
- Small Package and Footprint
  - 28 HTSSOP (PowerPAD)

- **Protection Features**
  - VM Undervoltage Lockout (UVLO)
  - Overcurrent Protection (OCP)
  - Thermal Shutdown (TSD)
  - Fault Condition Indication Pin (nFAULT)

2 Applications

- Automatic Teller and Money Handling Machines
- Video Security Cameras
- Multi-Function Printers and Scanners
- Office Automation Machines
- Gaming Machines
- Factory Automation and Robotics
- Stage Lighting Equipment

3 Description

The DRV8829 is a brushed-DC motor or 1/2 bipolar stepper driver for industrial applications. The device output stage consists of an N-channel power MOSFET H-bridge driver. The DRV8829 is capable of driving up to 5-A peak current or 3.5-A rms current (with proper printed-circuit-board ground plane for thermal dissipation and at 24 V and T_A = 25°C).

The PH/EN pins provide a simple control interface. An internal sense amplifier allows for adjustable current control. A low-power sleep mode is provided for very low quiescent current standby using a dedicated nSLEEP pin. Current regulation decay mode can be set to slow, fast, or mixed decay.

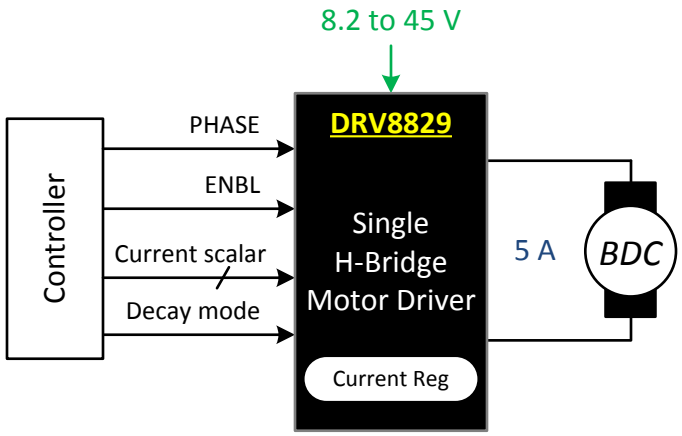
Internal protection functions are provided for undervoltage, overcurrent, short-circuits, and overtemperature. Fault conditions are indicated by a nFAULT pin.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DRV8829	HTSS0P (28)	9.70 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (June 2015) to Revision E — **Page**

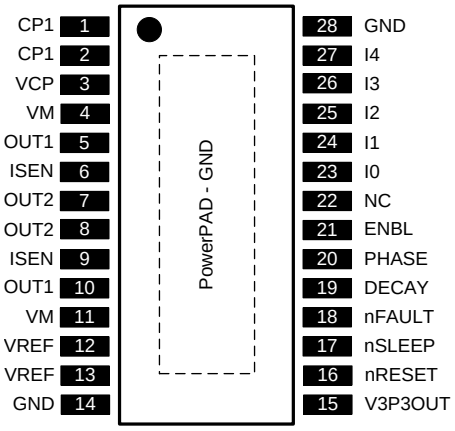
- Increased the power supply voltage maximum to 50 ... 5

Changes from Revision C (August 2013) to Revision D — **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 5

5 Pin Configuration and Functions

PWP Package
28-Pin HTSSOP
Top View



Pin Functions

PIN		I/O(1)	DESCRIPTION	EXTERNAL COMPONENTS OR CONNECTIONS
NAME	NO.			
POWER AND GROUND				
GND	14, 28	—	Device ground	
VM	4, 11	—	Bridge power supply	Connect to motor supply (8.2 V to 45 V). Both pins must be connected to same supply.
V3P3OUT	15	O	3.3-V regulator output	Bypass to GND with a 0.47-µF to 6.3-V ceramic capacitor. Can be used to supply VREF.
CP1	1	IO	Charge pump flying capacitor	Connect a 0.01-µF to 50-V capacitor between CP1 and CP2.
CP2	2	IO	Charge pump flying capacitor	
VCP	3	IO	High-side gate drive voltage	Connect a 0.1-µF to 16-V ceramic capacitor and 1-MΩ resistor to VM.
CONTROL				
ENBL	21	I	Bridge enable	Logic high to enable H-bridge. Internal pulldown.
PHASE	20	I	Bridge phase (direction)	Logic high sets OUT1 high, OUT2 low. Internal pulldown.
I0	23	I	Current set inputs	Sets winding current as a percentage of full-scale. Internal pulldown.
I1	24	I		
I2	25	I		
I3	26	I		
I4	27	I		
DECAY	19	I	Decay mode	Low = slow decay, open = mixed decay, high = fast decay Internal pulldown and pullup.
nRESET	16	I	Reset input	Active-low reset input initializes internal logic and disables the H-bridge outputs. Internal pulldown.
nSLEEP	17	I	Sleep mode input	Logic high to enable device, logic low to enter low-power sleep mode. Internal pulldown.
VREF	12, 13	I	Current set reference input	Reference voltage for winding current set. Both pins must be connected together on the PCB.
STATUS				
nFAULT	18	OD	Fault	Logic low when in fault condition (overtemperature, overcurrent)

(1) Directions: I = input, O = output, OZ = tri-state output, OD = open-drain output, IO = input/output

Pin Functions (continued)

PIN		I/O[1]	DESCRIPTION	EXTERNAL COMPONENTS OR CONNECTIONS
NAME	NO.			
OUTPUT				
ISEN	6, 9	IO	Bridge ground / Isense	Connect to current sense resistor. Both pins must be connected together on the PCB.
OUT1	5, 10	O	Bridge output 1	Connect to motor winding. Both pins must be connected together on the PCB.
OUT2	7, 8	O	Bridge output 2	

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1) (2)

		MIN	MAX	UNIT
VM	Power supply voltage	–0.3	50	V
	Digital pin voltage	–0.5	7	V
VREF	Input voltage	–0.3	4	V
	ISENSE pin voltage	–0.3	0.8	V
	Peak motor drive output current, t < 1 µs	Internally limited		A
	Continuous motor drive output current(3)		5	A
	Continuous total power dissipation	See *Thermal Information*		
T_J	Operating virtual junction temperature	–40	150	°C
T_A	Operating ambient temperature	–40	85	°C
T_{stg}	Storage temperature	–60	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) Power dissipation and thermal limits must be observed.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_M	Motor power supply voltage range(1)	8.2		45	V
V_{REF}	VREF input voltage(2)	1		3.5	V
I_{V3P3}	V3P3OUT load current	0		1	mA
f_{PWM}	Externally applied PWM frequency	0		100	kHz

(1) All V_M pins must be connected to the same supply voltage.
(2) Operational at VREF from 0 V to 1 V, but accuracy is degraded.

6.4 Thermal Information

THERMAL METRIC(1)		DRV8829 PWP (HTSSOP) 28 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	31.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	15.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	5.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	5.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES						
I_{VM}	VM operating supply current	V_M = 24 V, f_{PWM} < 50 kHz		5	8	mA
I_{VMQ}	VM sleep mode supply current	V_M = 24 V		10	20	µA
V_{UVLO}	VM undervoltage lockout voltage	V_M rising		7.8	8.2	V
V3P3OUT REGULATOR						
V_{3P3}	V3P3OUT voltage	IOUT = 0 to 1 mA	3.2	3.3	3.4	V
LOGIC-LEVEL INPUTS						
V_{IL}	Input low voltage			0.6	0.7	V
V_{IH}	Input high voltage		2.2		5.25	V
V_{HYS}	Input hysteresis		0.3	0.45	0.6	V
I_{IL}	Input low current	VIN = 0	–20		20	µA
I_{IH}	Input high current	VIN = 3.3 V			100	µA
R_{PD}	Internal pulldown resistance			100		kΩ
nFAULT OUTPUT (OPEN-DRAIN OUTPUT)						
V_{OL}	Output low voltage	I_O = 5 mA			0.5	V
I_{OH}	Output high leakage current	V_O = 3.3 V			1	µA
DECAY INPUT						
V_{IL}	Input low threshold voltage	For slow decay mode			0.8	V
V_{IH}	Input high threshold voltage	For fast decay mode	2			V
I_{IN}	Input current				±40	µA
R_{PU}	Internal pullup resistance			130		kΩ
R_{PD}	Internal pulldown resistance			80		kΩ
H-BRIDGE FETS						
$R_{DS(ON)}$	HS FET on resistance	V_M = 24 V, I_O = 1 A, T_J = 25°C		0.1		Ω
		V_M = 24 V, I_O = 1 A, T_J = 85°C		0.13	0.16	
$R_{DS(ON)}$	LS FET on resistance	V_M = 24 V, I_O = 1 A, T_J = 25°C		0.1		Ω
		V_M = 24 V, I_O = 1 A, T_J = 85°C		0.13	0.16	
I_{OFF}	Off-state leakage current		–40		40	µA
MOTOR DRIVER						
f_{PWM}	Internal current control PWM frequency			50		kHz
t_{BLANK}	Current sense blanking time			3.75		µs
t_R	Rise time		30		200	ns
t_F	Fall time		30		200	ns
PROTECTION CIRCUITS						
I_{OCP}	Overcurrent protection trip level		6		6	A
t_{TSD}	Thermal shutdown temperature	Die temperature	150	160	180	°C
CURRENT CONTROL						
I_{REF}	VREF input current	VREF = 3.3 V	–3		3	µA
V_{TRIP}	ISENSE trip voltage	VREF = 3.3 V, 100% current setting	635	660	685	mV
ΔI_{TRIP}	Current trip accuracy (relative to programmed value)	VREF = 3.3V , 5% - 34% current setting	–15%		15%	
		VREF = 3.3 V, 38% - 67% current setting	–10%		10%	
		VREF = 3.3 V, 71% - 100% current setting	–5%		5%	
A_{ISENSE}	Current sense amplifier gain	Reference only		5		V/V

6.6 Typical Characteristics

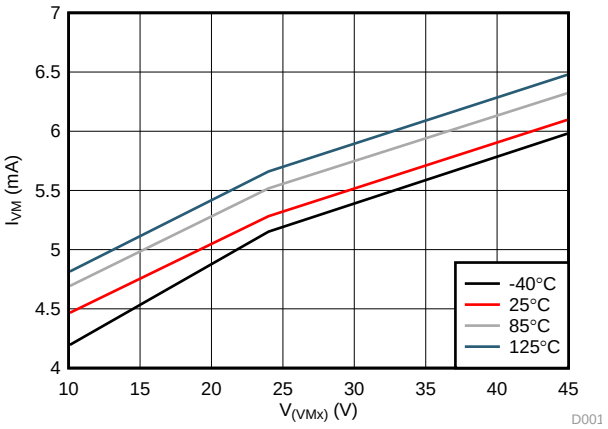


Figure 1. Active Supply Current Over Supply Voltage and Temperature

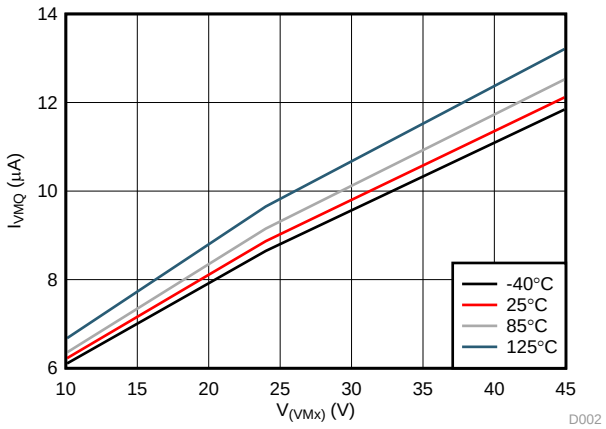


Figure 2. Sleep Current Over Supply Voltage and Temperature

7 Detailed Description

7.1 Overview

The DRV8829 is an integrated motor driver solution for bipolar stepper motors or single/dual brushed-DC motors. The device integrates an NMOS H-bridge and current regulation circuitry. The DRV8829 can be powered with a supply voltage from 8.2 to 45 V, and is capable of providing an output current up to 5-A peak or 3.5-A rms. Actual operable rms current will depend on ambient temperature, supply voltage, and PCP ground plane size.

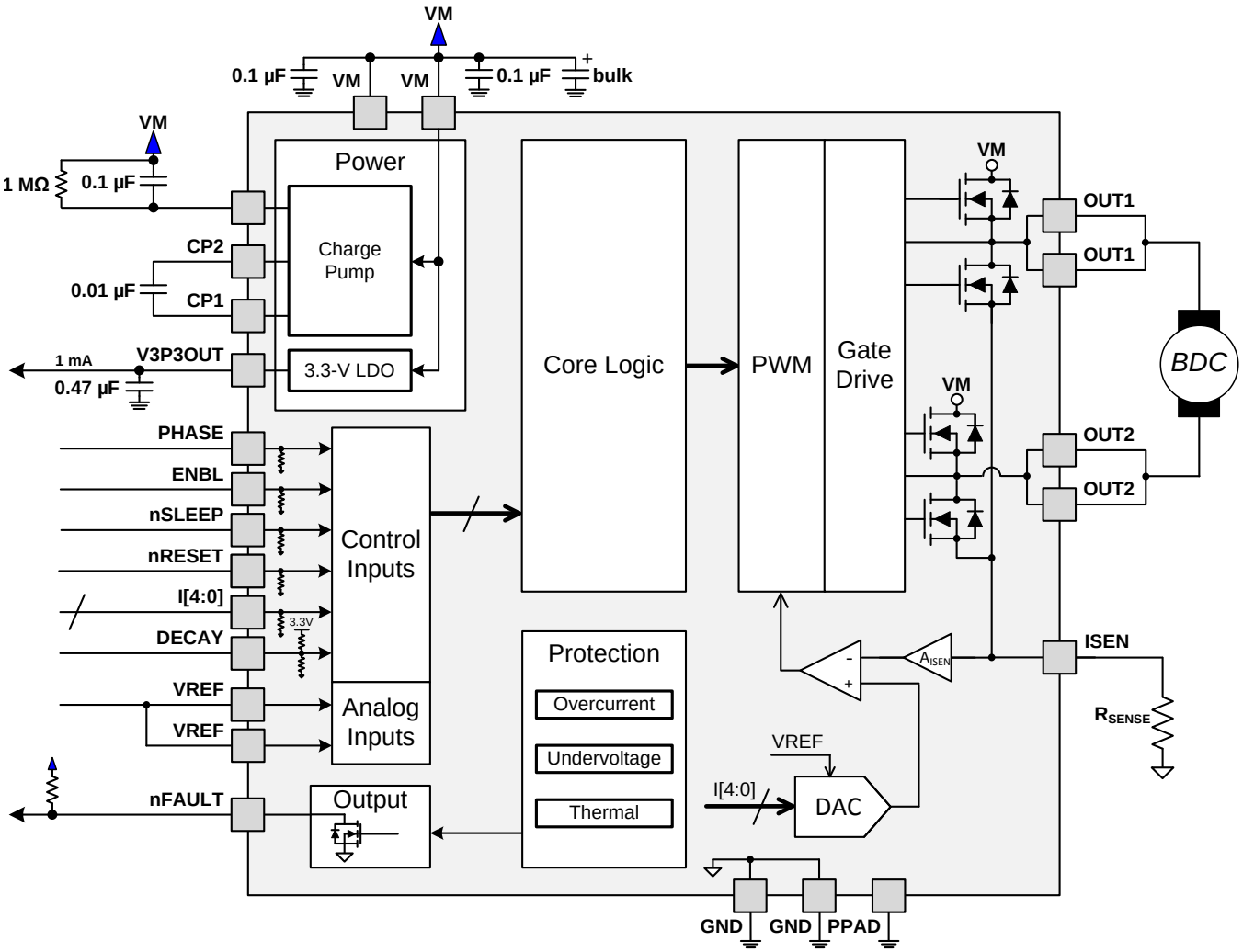
A simple PH/EN interface allows easy interfacing to the controller circuit.

The current regulation is highly configurable, with several decay modes of operation. The decay mode can be selected as a fixed slow, mixed, or fast decay.

A current scalar feature allows the controller to scale the output current without needing to scale the analog reference voltage input VREF. The DAC is accessed using digital input pins. This allows the controller to save power by decreasing the current consumption when not required.

A low-power sleep mode is included which allows the system to save power when not driving the motor.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 PWM Motor Drivers

The DRV8829 contains one H-bridge motor driver with current-control PWM circuitry. Figure 3 shows a block diagram of the motor control circuitry. A bipolar stepper motor is shown, but the driver can also drive a DC motor.

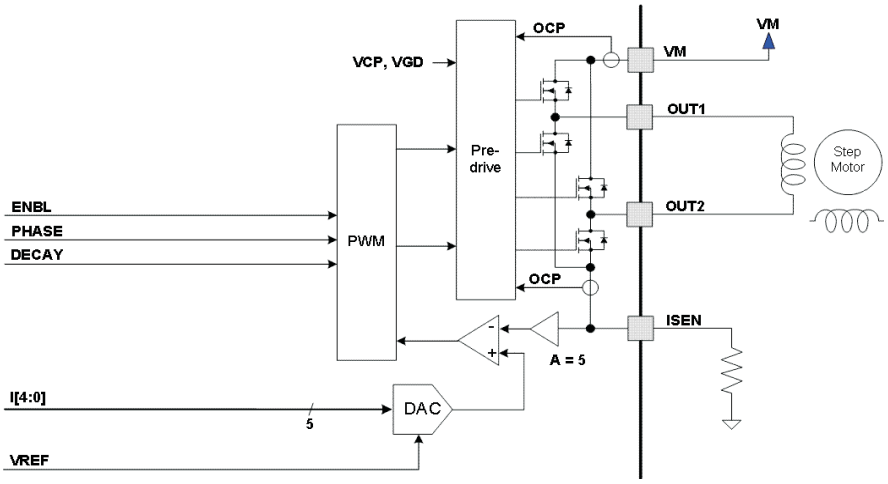


Figure 3. Motor Control Circuitry

There are multiple VM, ISEN, OUT, and VREF pins. All like-named pins must be connected together on the PCB.

7.3.2 Blanking Time

After the current is enabled in the H-bridge, the voltage on the ISEN pin is ignored for a fixed period of time before enabling the current sense circuitry. This blanking time is fixed at 3.75 µs. The blanking time also sets the minimum on time of the PWM.

7.3.3 nRESET and nSLEEP Operation

The nRESET pin, when driven active low, resets the internal logic. It also disables the H-bridge drivers. All inputs are ignored while nRESET is active.

Driving nSLEEP low will put the device into a low-power sleep state. In this state, the H-bridge is disabled, the gate drive charge pump is stopped, the V3P3OUT regulator is disabled, and all internal clocks are stopped. In this state all inputs are ignored until nSLEEP returns inactive high. When returning from sleep mode, some time (approximately 1 ms) needs to pass before the motor driver becomes fully operational. The nRESET and nSLEEP have internal pulldown resistors of approximately 100 kΩ. These signals need to be driven to logic high for device operation.

7.3.4 Protection Circuits

The DRV8829 is fully protected against undervoltage, overcurrent and overtemperature events.

7.3.4.1 Overcurrent Protection (OCP)

An analog current limit circuit on each FET limits the current through the FET by removing the gate drive. If this analog current limit persists for longer than the OCP time, all FETs in the H-bridge will be disabled and the nFAULT pin will be driven low. The device will remain disabled until either nRESET pin is applied, or VM is removed and re-applied.

Overcurrent conditions on both high and low side devices; that is, a short to ground, supply, or across the motor winding will all result in an overcurrent shutdown. The overcurrent protection does not use the current sense circuitry used for PWM current control, and is independent of the I_{SENSE} resistor value or VREF voltage.

Feature Description (continued)

7.3.4.2 Thermal Shutdown (TSD)

If the die temperature exceeds safe limits, all FETs in the H-bridge will be disabled and the nFAULT pin will be driven low. Once the die temperature has fallen to a safe level operation will automatically resume.

7.3.4.3 Undervoltage Lockout (UVLO)

If at any time the voltage on the VM pins falls below the undervoltage lockout threshold voltage, all circuitry in the device will be disabled and internal logic will be reset. Operation will resume when V_M rises above the UVLO threshold.

7.3.5 Current Regulation

The current through the motor winding is regulated by a fixed-frequency PWM current regulation, or current chopping. When the H-bridge is enabled, current rises through the winding at a rate dependent on the DC voltage and inductance of the winding. Once the current hits the current chopping threshold, the bridge disables the current until the beginning of the next PWM cycle.

For stepping motors, current regulation is normally used at all times, and can changing the current can be used to microstep the motor. For DC motors, current regulation is used to limit the start-up and stall current of the motor.

If the current regulation feature is not needed, it can be disabled by connecting the ISENSE pins directly to ground and the VREF pins to V3P3.

The PWM chopping current in each bridge is set by a comparator which compares the voltage across a current sense resistor connected to the ISEN pin, multiplied by a factor of 5, with a reference voltage. The reference voltage is input from the xVREF pins, and is scaled by a 5-bit DAC that allows current settings of zero to 100% in an approximately sinusoidal sequence.

The full-scale (100%) chopping current is calculated in Equation 1.

$$I_{CHOP} = \frac{V_{REFX}}{5 \bullet R_{ISENSE}} \quad (1)$$

Example:

If a 0.25-Ω sense resistor is used and the VREFx pin is 2.5 V, the full-scale (100%) chopping current will be 2.5 V / (5 × 0.25 Ω) = 2 A.

Five input pins (I0 - I4) are used to scale the current in the bridge as a percentage of the full-scale current set by the VREF input pin and sense resistance. The I0 - I4 pins have internal pulldown resistors of approximately 100 kΩ. The function of the pins is shown in Table 1.

Table 1. Current Scalar Logic

I[4..0]	RELATIVE CURRENT (% FULL-SCALE CHOPPING CURRENT)
0x00h	0% (Bridge disabled)
0x01h	5%
0x02h	10%
0x03h	15%
0x04h	20%
0x05h	24%
0x06h	29%
0x07h	34%
0x08h	38%
0x09h	43%
0x0Ah	47%
0x0Bh	51%
0x0Ch	56%

Table 1. Current Scalar Logic (continued)

I[4..0]	RELATIVE CURRENT (% FULL-SCALE CHOPPING CURRENT)
0x0Dh	60%
0x0Eh	63%
0x0Fh	67%
0x10h	71%
0x11h	74%
0x12h	77%
0x13h	80%
0x14h	83%
0x15h	86%
0x16h	88%
0x17h	90%
0x18h	92%
0x19h	94%
0x1Ah	96%
0x1Bh	97%
0x1Ch	98%
0x1Dh	99%
0x1Eh	100%
0x1Fh	100%

7.4 Device Functional Modes

7.4.1 Bridge Control

The PHASE input pin controls the direction of current flow through the H-bridge. The ENBL input pin enables the H-bridge outputs when active high. Table 2 shows the logic.

Table 2. H-Bridge Logic

ENBL	PHASE	OUT1	OUT2
0	X	Z	Z
1	1	H	L
1	0	L	H

The control inputs have internal pulldown resistors of approximately 100 kΩ.

7.4.2 Decay Mode

During PWM current chopping, the H-bridge is enabled to drive current through the motor winding until the PWM current chopping threshold is reached. This is shown in Figure 4 as case 1. The current flow direction shown indicates the state when the PHASE pin is high.

Once the chopping current threshold is reached, the H-bridge can operate in two different states, fast decay or slow decay.

In fast decay mode, once the PWM chopping current level has been reached, the H-bridge reverses state to allow winding current to flow in a reverse direction. As the winding current approaches zero, the bridge is disabled to prevent any reverse current flow. Fast decay mode is shown in Figure 4 as case 2.

In slow decay mode, winding current is recirculated by enabling both of the low-side FETs in the bridge. This is shown in Figure 4 as case 3.

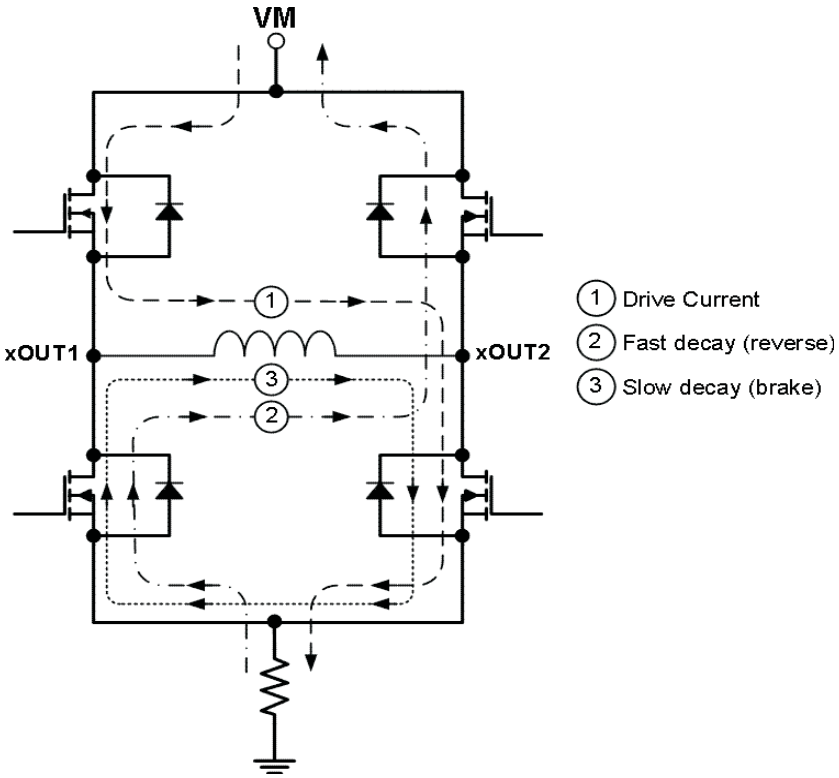


Figure 4. Decay Modes

The DRV8829 supports fast decay, slow decay and a mixed decay mode. Slow, fast, or mixed decay mode is selected by the state of the DECAY pin - logic low selects slow decay, open selects mixed decay operation, and logic high sets fast decay mode. The DECAY pin has both an internal pullup resistor of approximately 130 kΩ and an internal pulldown resistor of approximately 80 kΩ. This sets the mixed decay mode if the pin is left open or undriven.

Mixed decay mode begins as fast decay, but at a fixed period of time (75% of the PWM cycle) switches to slow decay mode for the remainder of the fixed PWM period.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DRV8829 is used in brushed motor or stepper control.

8.2 Typical Application

In this application, the DRV8829 will be used to drive a brushed-DC motor. The following design procedure can be used to configure the DRV8829.

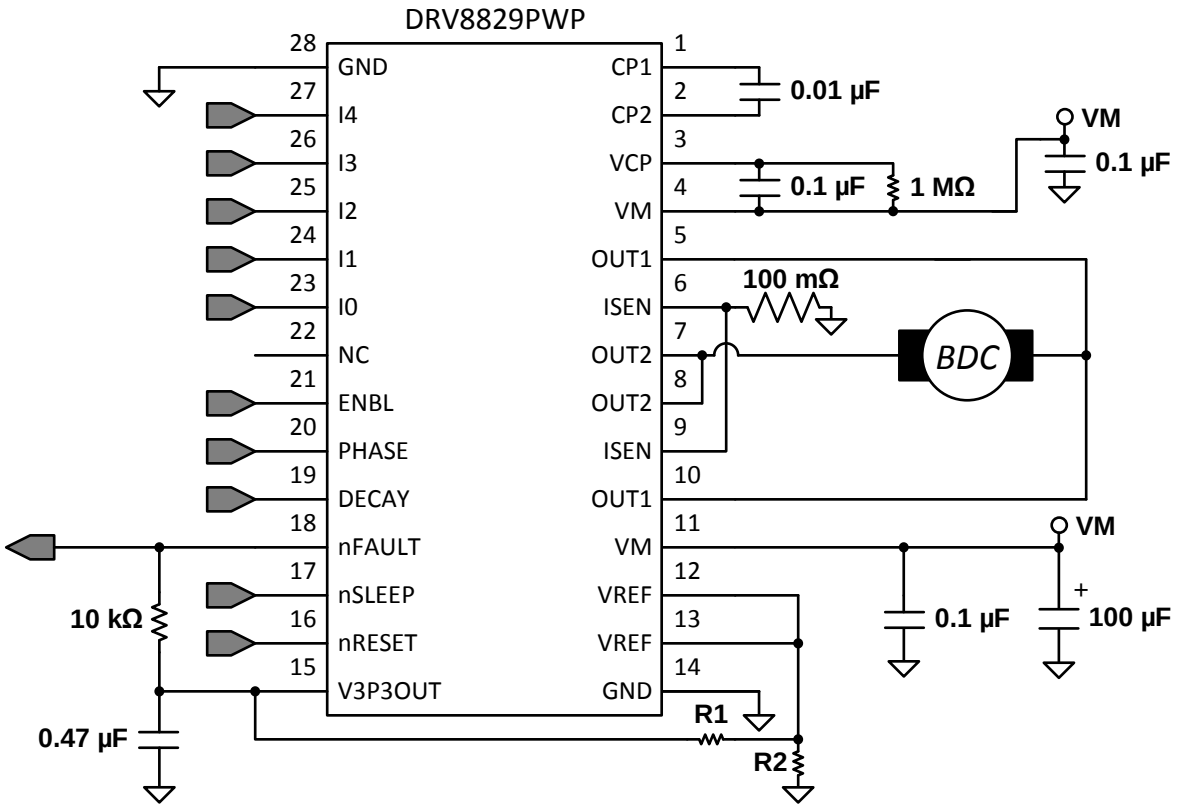


Figure 5. Typical Application Schematic

8.2.1 Design Requirements

Table 3 gives design input parameters for system design.

Table 3. Design Parameters

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Supply voltage	VM	24 V
Motor winding resistance	R_L	0.83 Ω
Motor winding inductance	L_L	232.5 µH
Target chopping current	I_{TRIP}	3.5 A

8.2.2 Detailed Design Procedure

The maximum current (I_{TRIP}) is set by the Ix pins, the VREF analog voltage, and the sense resistor value (R_{SENSE}). When starting a brushed-DC motor, a large inrush current may occur because there is no back-EMF. Current regulation will act to limit this inrush current and prevent high current on start-up.

$$I_{CHOP} = \frac{V_{REFX}}{5 \bullet R_{ISENSE}} \quad (2)$$

Example: If the desired chopping current is 3.5 A

Set R_{SENSE} = 100 mΩ

VREF would have to be 1.75 V.

Create a resistor divider from V3P3OUT (3.3 V) to set VREF ≈ 1.75 V.

Set R2 = 18 kΩ, set R1 = 16 kΩ

8.2.2.1 Sense Resistor

For optimal performance, it is important for the sense resistor to be:

- Surface-mount
- Low inductance
- Rated for high enough power
- Placed closely to the motor driver

The power dissipated by the sense resistor equals Irms² x R. For example, if the rms motor current is 2-A and a 100-mΩ sense resistor is used, the resistor will dissipate 2 A² × 0.1 Ω = 0.4 W. The power quickly increases with greater current levels.

Resistors typically have a rated power within some ambient temperature range, along with a de-rated power curve for high ambient temperatures. When a PCB is shared with other components generating heat, margin should be added. It is always best to measure the actual sense resistor temperature in a final system, along with the power MOSFETs, as those are often the hottest components.

Because power resistors are larger and more expensive than standard resistors, it is common practice to use multiple standard resistors in parallel, between the sense node and ground. This distributes the current and heat dissipation.

8.2.3 Application Curves

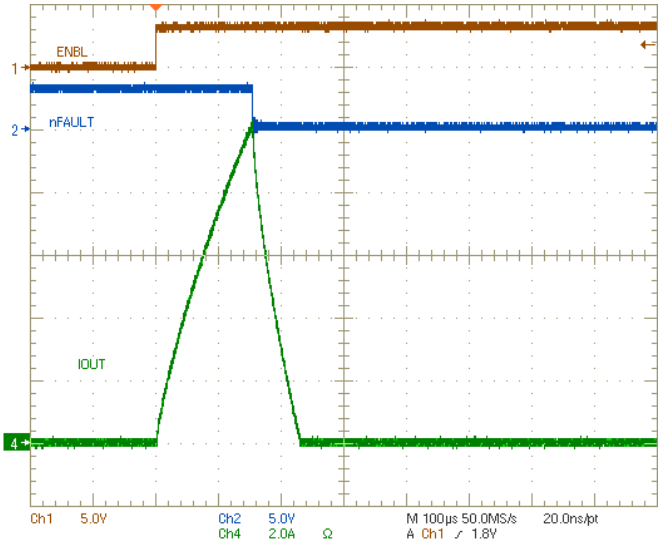


Figure 6. Motor Start-up without Current Regulation, Overcurrent Trips

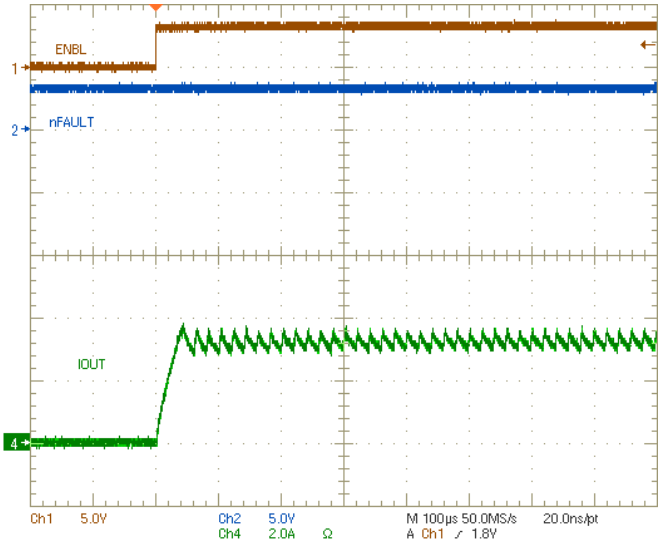


Figure 7. Motor Start-up With Current Regulation

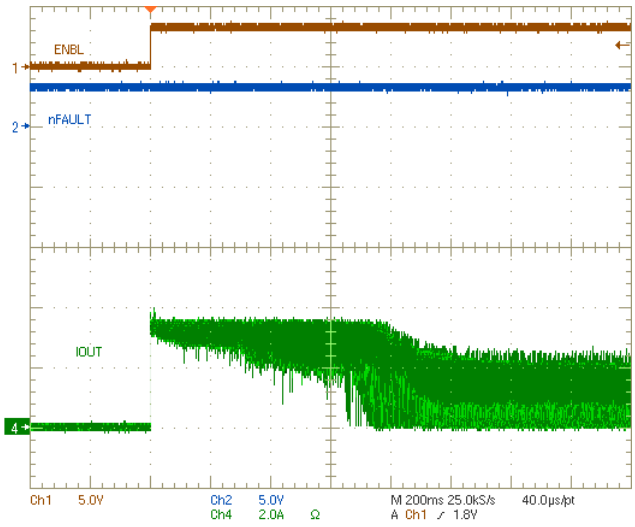


Figure 8. Motor Start-up With Current Regulation, Motor Reaches Steady State

9 Power Supply Recommendations

The DRV8829 is designed to operate from an input voltage supply (VM) range from 8.2 V to 45 V. The device has an absolute maximum rating of 47 V. A 0.1-µF ceramic capacitor rated for VM must be placed at each VM pin as close to the DRV8829 as possible. In addition, a bulk capacitor must be included on VM.

9.1 Bulk Capacitance Sizing

Having appropriate local bulk capacitance is an important factor in motor drive system design. It is generally beneficial to have more bulk capacitance, while the disadvantages are increased cost and physical size.

The amount of local capacitance needed depends on a variety of factors, including:

- The highest current required by the motor system.
- The power supply's capacitance and ability to source current.
- The amount of parasitic inductance between the power supply and motor system.
- The acceptable voltage ripple.
- The type of motor used (Brushed DC, Brushless DC, Stepper).
- The motor braking method.

The inductance between the power supply and motor drive system will limit the rate current can change from the power supply. If the local bulk capacitance is too small, the system will respond to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.

The data sheet generally provides a recommended value, but system-level testing is required to determine the appropriate sized bulk capacitor.

The voltage rating for bulk capacitors should be greater than the operating voltage, to provide margin for cases when the motor transfers energy to the supply.

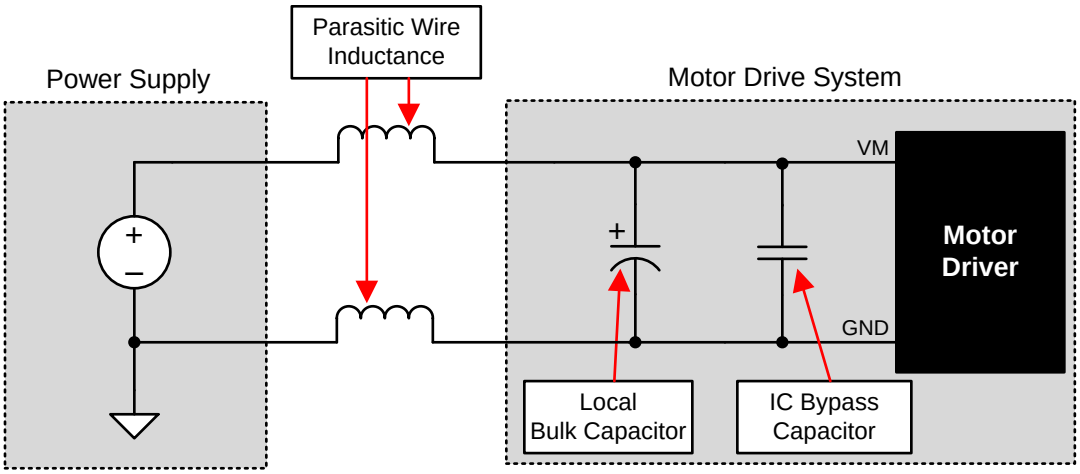


Figure 9. Setup of Motor Drive System With External Power Supply

10 Layout

10.1 Layout Guidelines

Each VM terminal must be bypassed to GND using a low-ESR ceramic bypass capacitors with recommended values of 0.1 µF rated for VM. These capacitors should be placed as close to the VM pins as possible with a thick trace or ground plane connection to the device GND pin.

The VM pin must be bypassed to ground using a bulk capacitor rated for VM. This component may be an electrolytic.

A low-ESR ceramic capacitor must be placed in between the CP1 and CP2 pins. TI recommends a value of 0.1 µF rated for VM . Place this component as close to the pins as possible.

A low-ESR ceramic capacitor must be placed in between the VM and VCP pins. TI recommends a value of 0.47 µF rated for 16 V. Place this component as close to the pins as possible. In addition, place a 1 MΩ between VM and VCP.

Bypass V3P3OUT to ground with a ceramic capacitor rated 6.3 V. Place this bypassing capacitor as close to the pin as possible.

The current sense resistor should be placed as close as possible to the device pins to minimize trace inductance between the pin and resistor.

10.2 Layout Example

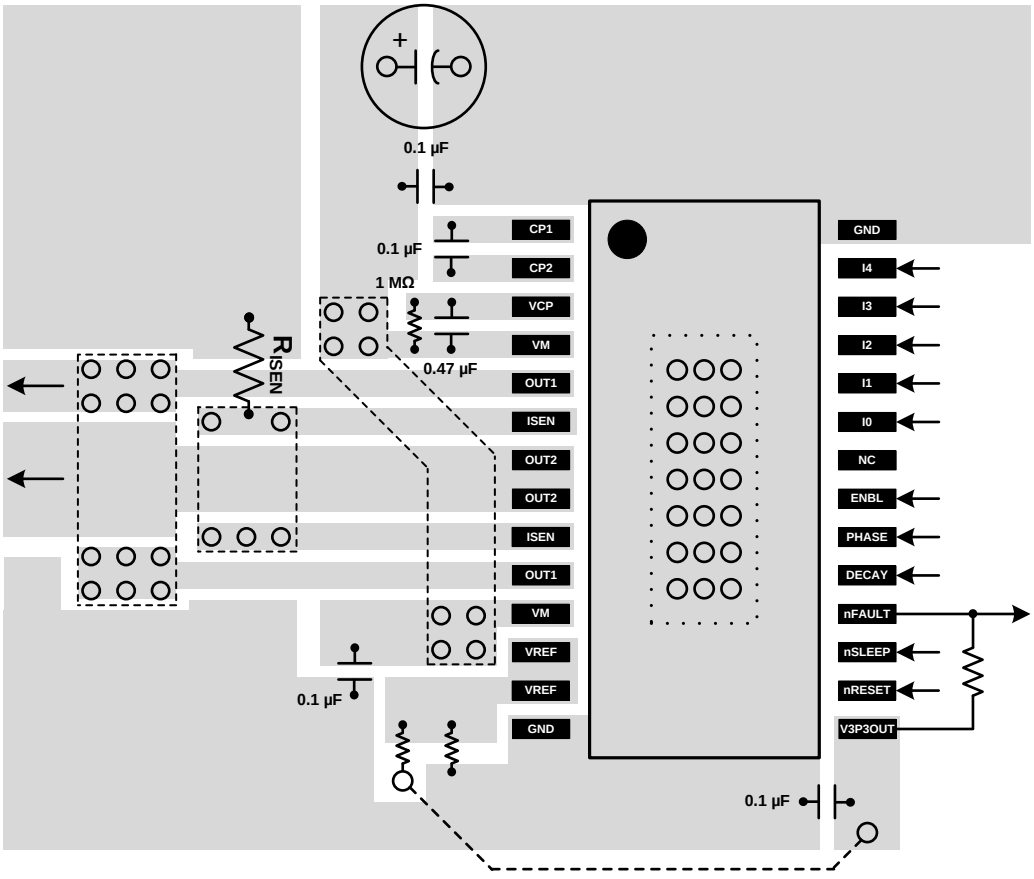


Figure 10. Example Layout

10.3 Thermal Considerations

The DRV8829 has thermal shutdown (TSD) as described above. If the die temperature exceeds approximately 150°C, the device will be disabled until the temperature drops to a safe level.

Any tendency of the device to enter TSD is an indication of either excessive power dissipation, insufficient heatsinking, or too high an ambient temperature.

10.4 Power Dissipation

Power dissipation in the DRV8829 is dominated by the power dissipated in the output FET resistance, or $R_{DS(ON)}$. Average power dissipation when running a stepper motor can be roughly estimated by Equation 3.

$$P_{TOT}\,(W) = \left[R_{DS(ON),HS}\,(\Omega) + R_{DS(ON),LS}\,(\Omega)\right] \times \left[I_{OUT(RMS)}\,(A)\right]^2 \quad (3)$$

where

- P_{TOT} is the total power dissipation
- $R_{DS(ON)}$ is the resistance of each FET (high-side and low-side)
- $I_{OUT(RMS)}$ is the RMS output current being applied to each winding

$I_{OUT(RMS)}$ is equal to the approximately 0.7x the full-scale output current setting.

The maximum amount of power that can be dissipated in the device is dependent on ambient temperature and heatsinking.

$R_{DS(ON)}$ increases with temperature, so as the device heats, the power dissipation increases. This must be taken into consideration when sizing the heatsink.

10.4.1 Heatsinking

The PowerPAD™ package uses an exposed pad to remove heat from the device. For proper operation, this pad must be thermally connected to copper on the PCB to dissipate heat. On a multi-layer PCB with a ground plane, this can be accomplished by adding a number of vias to connect the thermal pad to the ground plane. On PCBs without internal planes, copper area can be added on either side of the PCB to dissipate heat. If the copper area is on the opposite side of the PCB from the device, thermal vias are used to transfer the heat between top and bottom layers.

For details about how to design the PCB, refer to TI application report SLMA002, "PowerPAD™ Thermally Enhanced Package" and TI application brief SLMA004, "PowerPAD™ Made Easy", available at www.ti.com.

In general, the more copper area that can be provided, the more power can be dissipated.

11 Device and Documentation Support

11.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.2 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV8829PWP	ACTIVE	HTSSOP	PWP	28	50	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	DRV8829	Samples
DRV8829PWPR	ACTIVE	HTSSOP	PWP	28	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	DRV8829	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

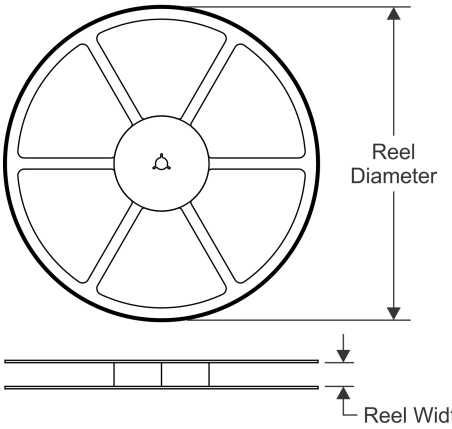
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

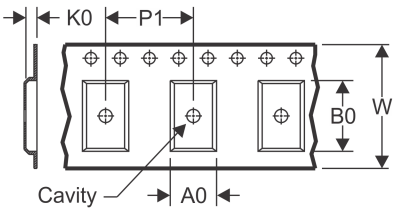
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

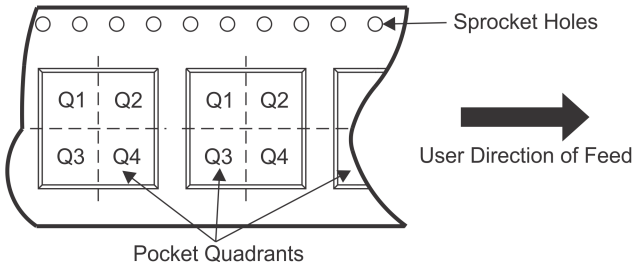


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

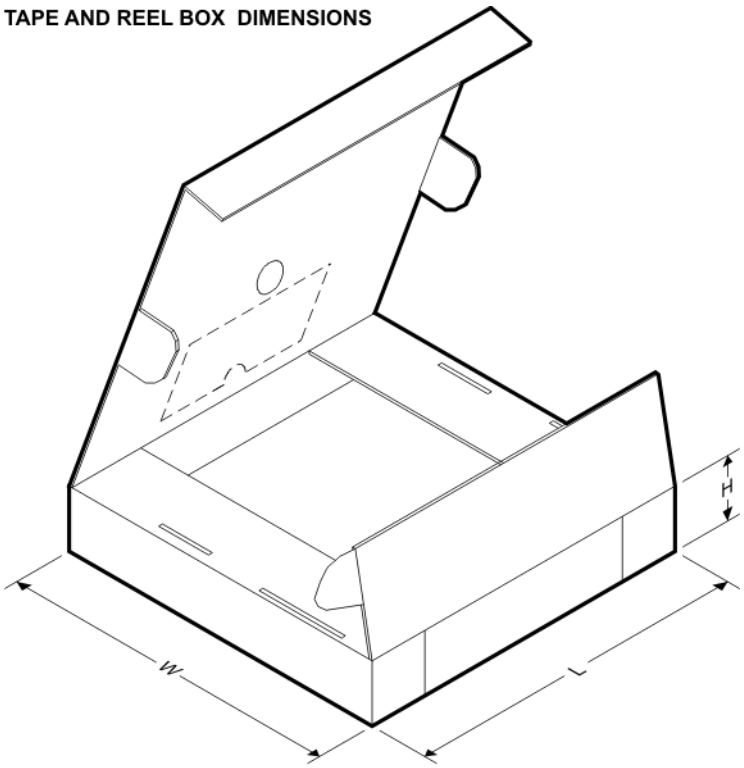
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8829PWPR	HTSSOP	PWP	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8829PWPR	HTSSOP	PWP	28	2000	350.0	350.0	43.0

GENERIC PACKAGE VIEW

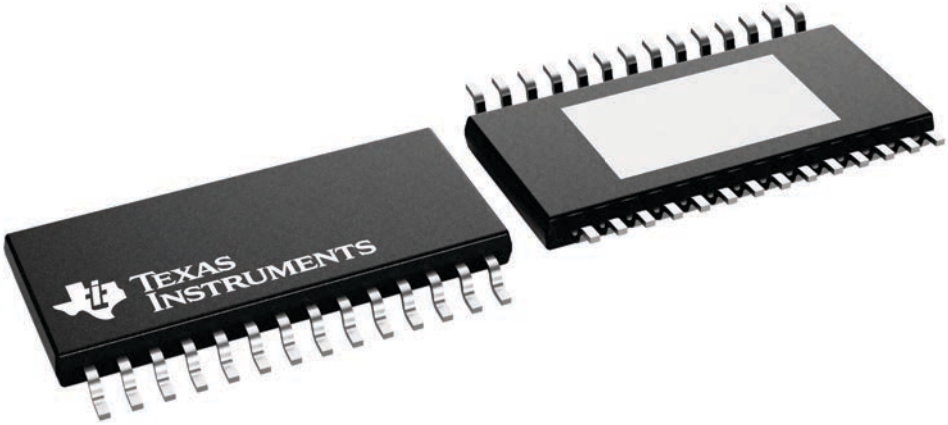
PWP 28

PowerPAD™ TSSOP - 1.2 mm max height

4.4 x 9.7, 0.65 mm pitch

SMALL OUTLINE PACKAGE

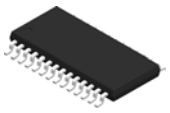
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224765/B

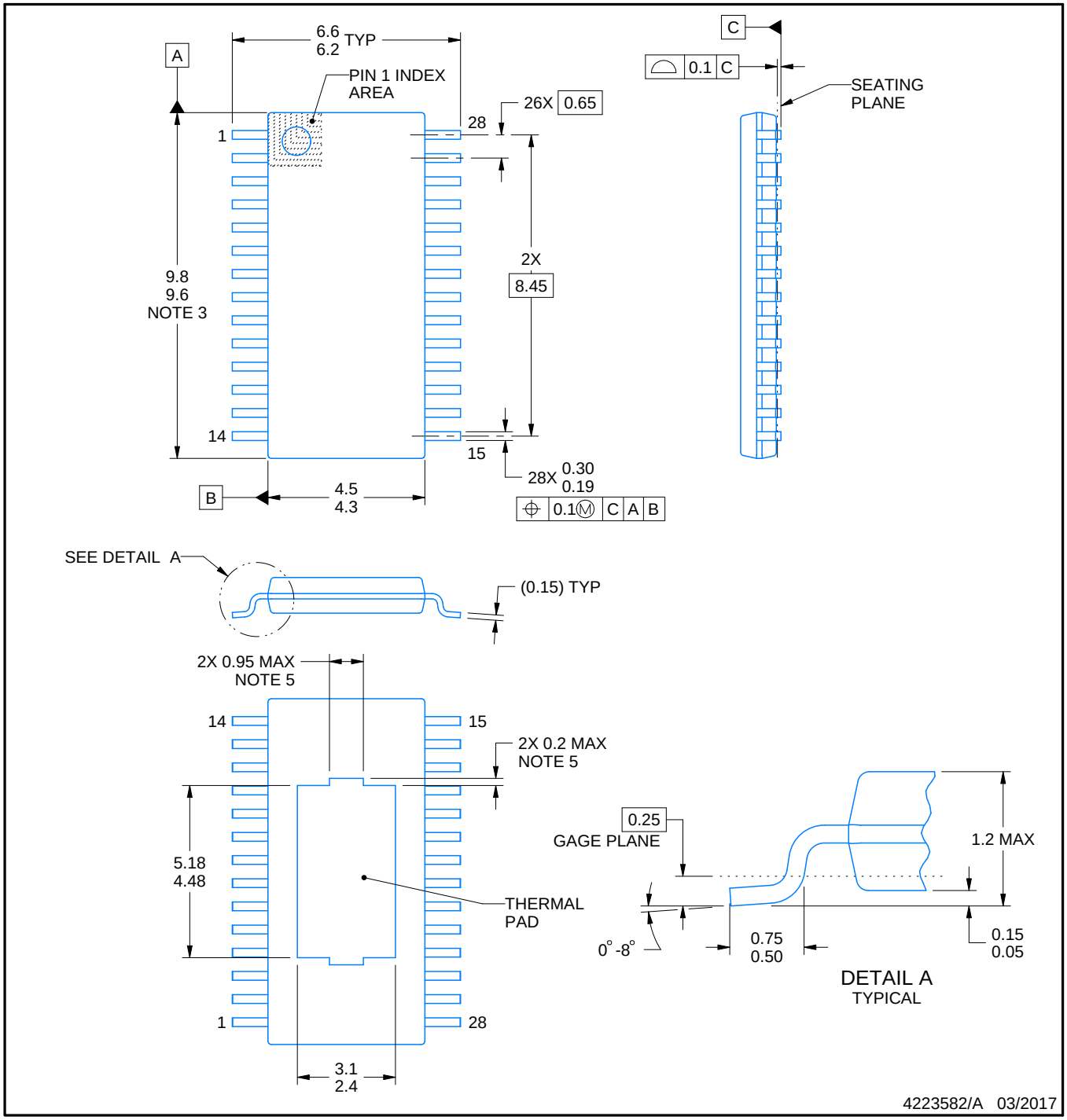
PACKAGE OUTLINE

PWP0028C



PowerPAD™ TSSOP - 1.2 mm max height

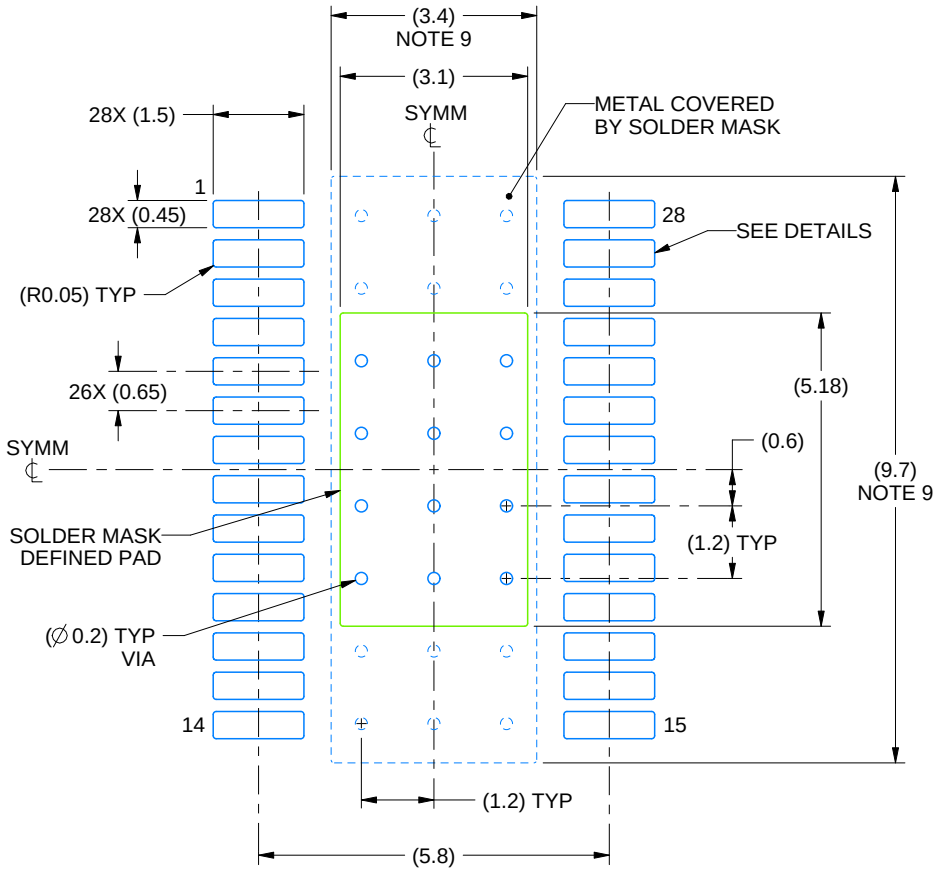
SMALL OUTLINE PACKAGE



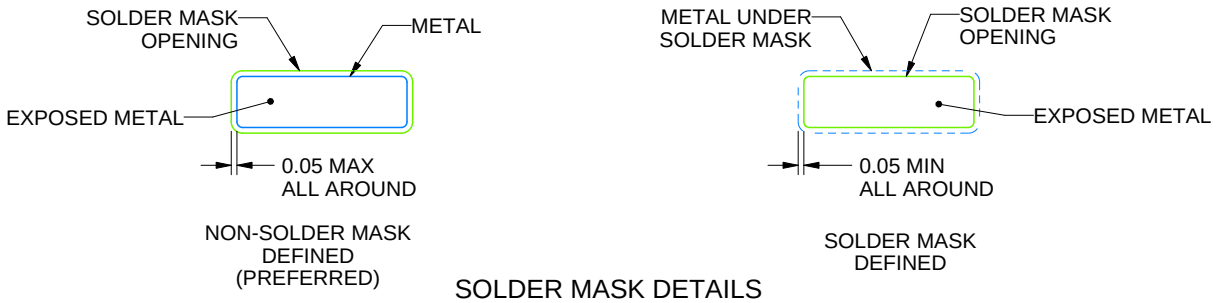
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 8X



SOLDER MASK DETAILS

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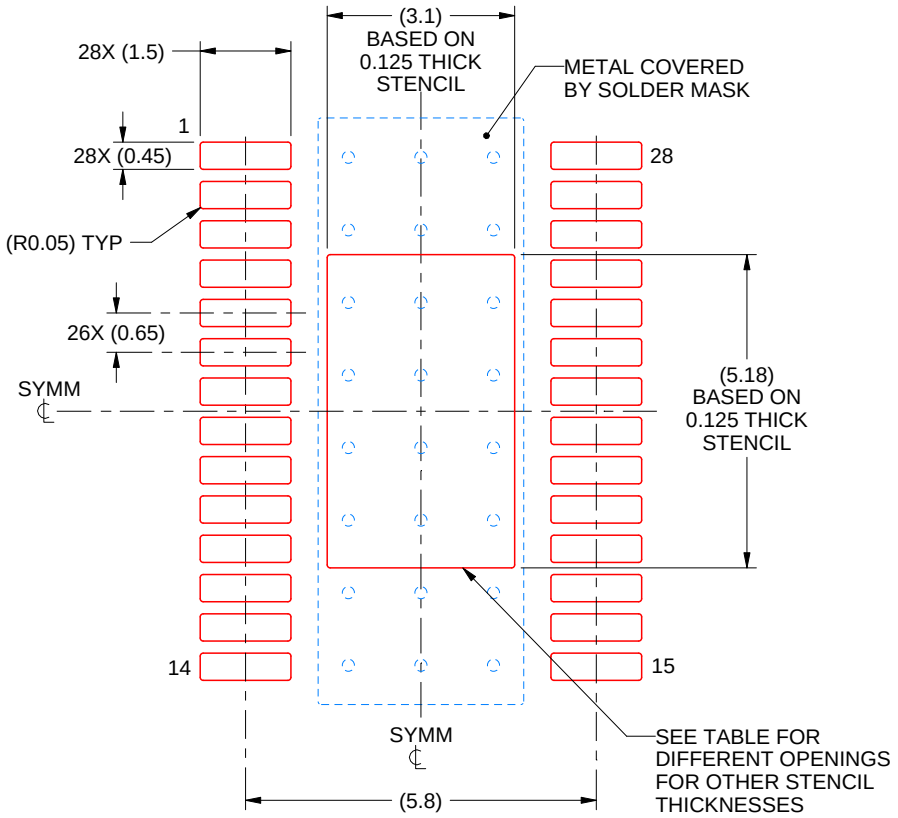
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.47 X 5.79
0.125	3.10 X 5.18 (SHOWN)
0.15	2.83 X 4.73
0.175	2.62 X 4.38

4223582/A 03/2017

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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