DS26LS32AC/DS26LS32C/DS26LS32M/DS26LS33M Quad Differential Line Receivers

Check for Samples: DS26LS32AC, DS26LS32C, DS26LS32M, DS26LS33M

FEATURES

- **High Differential or Common-Mode Input Voltage Ranges of ±7V on the DS26LS32 and DS26LS32A and ±15V on the DS26LS33**
- **±0.2V Sensitivity Over the Input Voltage Range on the DS26LS32 and DS26LS32A, ±0.5V Sensitivity on the DS26LS33**
- **DS26LS32 and DS26LS32A Meet All Requirements of RS-422 and RS-423**
- **6k Minimum Input Impedance**
- **100 mV Input Hysteresis on the DS26LS32 and DS26LS32A, 200 mV on the DS26LS33**
- **Operation From a Single 5V Supply**
- **TRI-STATE Outputs, with Choice of Complementary Output Enables for Receiving Directly onto a Data Bus**

DESCRIPTION

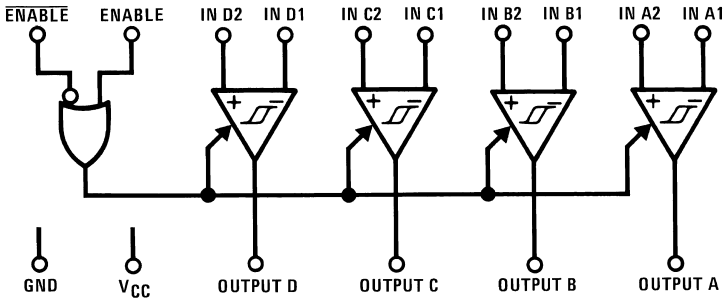
The DS26LS32 and DS26LS32A are quad differential line receivers designed to meet the RS-422, RS-423 and Federal Standards 1020 and 1030 for balanced and unbalanced digital data transmission.

The DS26LS32 and DS26LS32A have an input sensitivity of 200 mV over the input voltage range of ±7V and the DS26LS33 has an input sensitivity of 500 mV over the input voltage range of ±15V.

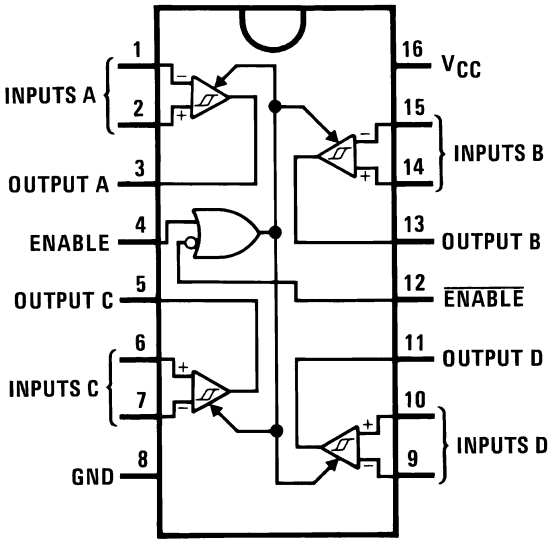
The DS26LS32A differs in function from the popular DS26LS32 and DS26LS33 in that input pull-up and pull-down resistors are included which prevent output oscillation on unused channels.

Each version provides an enable and disable function common to all four receivers and features TRI-STATE outputs with 8 mA sink capability. Constructed using low power Schottky processing, these devices are available over the full military and commercial operating temperature ranges.

Logic Diagram



Connection Diagram



For Complete Military Product Specifications, refer to the appropriate SMD or MDS.

Figure 1. Dual-In-Line Package (Top View)
D Package or NFG0016E Package

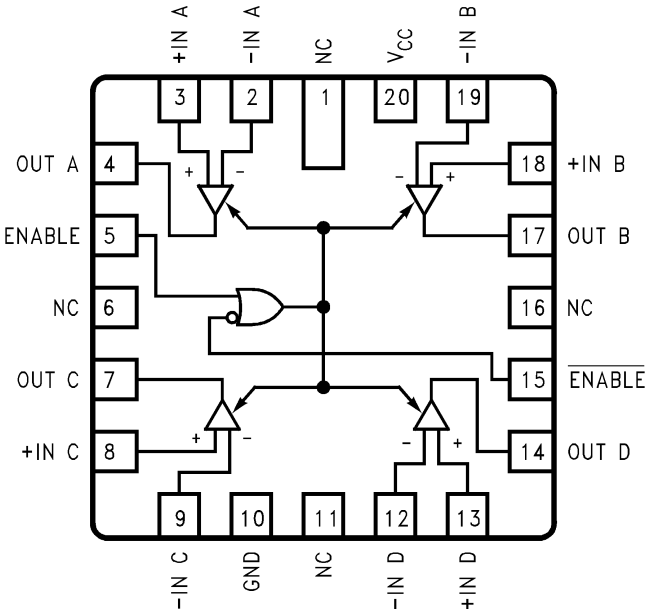


Figure 2. 20-Lead Ceramic Leadless Chip Carrier

Truth Table (1)

ENABLE	$\overline{\text{ENABLE}}$	Input	Output
0	1	X	Hi-Z
See note below.(2)		$V_{ID} \geq V_{TH}$ (Max)	1
		$V_{ID} \leq V_{TH}$ (Min)	0

(1) Hi-Z = TRI-STATE
(2) Note: Input conditions may be any combination not defined for ENABLE and $\overline{\text{ENABLE}}$.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1) (2)

Supply Voltage	7V
Common-Mode Range	±25V
Differential Input Voltage	±25V
Enable Voltage	7V
Output Sink Current	50 mA
Maximum Power Dissipation (3) at 25°C	
Cavity Package	1433 mW
Molded DIP Package	1362 mW
SOIC Package (4) DS26LS32	1002 mW
DS26LS32A	1051 mW
Storage Temperature Range	−65°C to +165°C
Lead Temperature (Soldering, 4 seconds)	260°C

(1) "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.
(3) Derate cavity package 9.6 mW/°C above 25°C; derate molded DIP package 10.9 mW/°C above 25°C.
(4) Derate SOIC Package 8.01 mW/°C for DS26LS32 8.41 mW/°C for DS26LS32A

Operating Conditions

	Min	Max	Units
Supply Voltage, (V_{CC})			
DS26LS32M, DS26LS33M (MIL)	4.5	5.5	V
DS26LS32C, DS26LS32AC (COML)	4.75	5.25	V
Temperature, (T_A)			
DS26LS32M, DS26LS33M (MIL)	−55	+125	°C
DS26LS32C, DS26LS32AC (COML)	0	+70	°C

Electrical Characteristics (1) (2) (3)

over the operating temperature range unless otherwise specified

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{TH}	Differential Input Voltage	$V_{OUT} = V_{OH}$ or V_{OL}	DS26LS32, DS26LS32A, −7V ≤ V_{CM} ≤ +7V	−0.2	±0.07	0.2	V
			DS26LS33, DS26LS33A, −15V ≤ V_{CM} +15V	−0.5	±0.14	0.5	V
R_{IN}	Input Resistance	−15V ≤ V_{CM} ≤ +15V (One Input AC GND)		6.0	8.5		kΩ
I_{IN}	Input Current (Under Test)	V_{IN} = 15V, Other Input −15V ≤ V_{IN} ≤ +15V				2.3	mA
		V_{IN} = −15V, Other Input −15V ≤ V_{IN} ≤ +15V				−2.8	mA
V_{OH}	Output High Voltage	V_{CC} = MIN, ΔV_{IN} = 1V,	Commercial	2.7	4.2		V
		$V_{\overline{ENABLE}}$ = 0.8V, I_{OH} = −440 µA	Military	2.5	4.2		V
V_{OL}	Output Low Voltage	V_{CC} = Min, ΔV_{IN} = −1V,	I_{OL} = 4 mA			0.4	V
		$V_{\overline{ENABLE}}$ = 0.8V	I_{OL} = 8 mA			0.45	V
V_{IL}	Enable Low Voltage					0.8	V
V_{IH}	Enable High Voltage			2.0			V
V_I	Enable Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA				−1.5	V

(1) All currents into device pins are shown as positive, all currents out of device pins are shown as negative, all voltages are referenced to ground, unless otherwise specified. All values shown as max or min are so classified on absolute value basis.
(2) All typical values are V_{CC} = 5V, T_A = 25°C.
(3) Only one output at a time should be shorted.

Electrical Characteristics (1) (2) (3) (continued)

over the operating temperature range unless otherwise specified

Symbol	Parameter	Conditions		Min	Typ	Max	Units
I_O	OFF-State (High Impedance) Output Current	V_{CC} = Max	V_O = 2.4V			20	µA
			V_O = 0.4V			−20	µA
I_{IL}	Enable Low Current	V_{IN} = 0.4V				−0.36	mA
I_{IH}	Enable High Current	V_{IN} = 2.7V				20	µA
I_{SC}	Output Short-Circuit Current	V_O = 0V, V_{CC} = Max, ΔV_{IN} = 1V		−15		−85	mA
I_{CC}	Power Supply Current	V_{CC} = Max, All V_{IN} = GND,	DS26LS32, DS26LS32A		52	70	mA
		Outputs Disabled	DS26LS33, DS26LS33A		57	80	mA
I_I	Input High Current	V_{IN} = 5.5V				100	µA
V_{HYST}	Input Hysteresis	T_A = 25°C, V_{CC} = 5V,	DS26LS32, DS26S32A		100		mV
		V_{CM} = 0V	DS26LS33, DS26LS33A		200		mV

Switching Characteristics

V_{CC} = 5V, T_A = 25°C

Symbol	Parameter	Conditions	DS26LS32/DS26LS33			DS26LS32A/DS26LS33A			Units
			Min	Typ	Max	Min	Typ	Max	
t_{PLH}	Input to Output	C_L = 15 pF		17	25		23	35	ns
t_{PHL}				17	25		23	35	ns
t_{LZ}	ENABLE to Output	C_L = 5 pF		20	30		15	30	ns
t_{HZ}				15	22		20	25	ns
t_{ZL}	ENABLE to Output	C_L = 15 pF		15	22		14	22	ns
t_{ZH}				15	22		15	22	ns

AC TEST CIRCUIT AND SWITCHING TIME WAVEFORMS

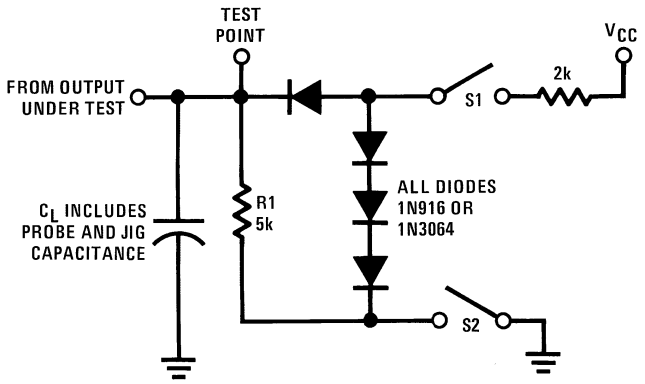


Figure 3. Load Test Circuit for TRI-STATE Outputs

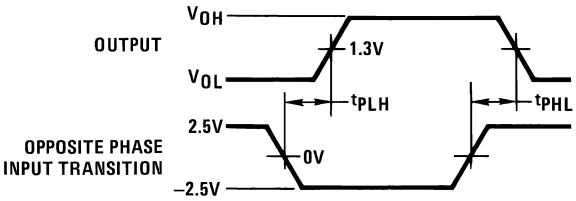
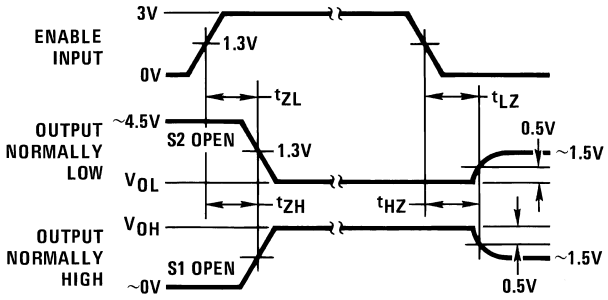


Diagram shown for $\overline{\text{ENABLE}}$ low.

Pulse generator for all pulses: Rate = 1.0 MHz; Z_O = 50Ω; $t_r \leq 6$ ns; $t_f \leq 6.0$ ns.

Figure 4. Propagation Delay



S1 and S2 of load circuit are closed except where shown.

Pulse generator for all pulses: Rate = 1.0 MHz; Z_O = 50Ω; $t_r \leq 6$ ns; $t_f \leq 6.0$ ns.

Figure 5. Enable and Disable Times

TYPICAL APPLICATIONS

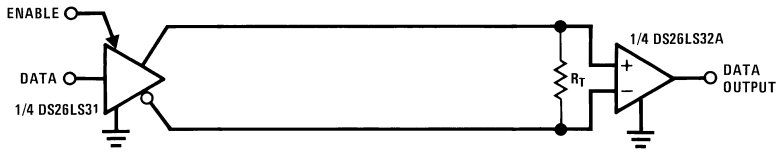


Figure 6. Two-Wire Balanced Interface—RS-422

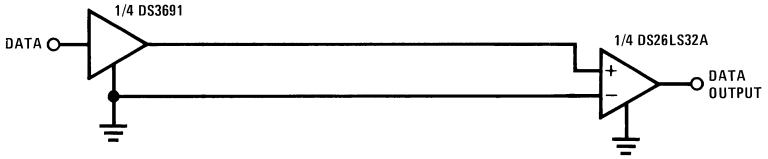


Figure 7. Single Wire with Driver Ground Reference—RS-423

REVISION HISTORY

Changes from Revision B (February 2013) to Revision C	Page
• Changed layout of National Data Sheet to TI format	5

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS26LS32ACM/NOPB	ACTIVE	SOIC	D	16	48	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	DS26LS32 ACM	Samples
DS26LS32ACMX/NOPB	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	DS26LS32 ACM	Samples
DS26LS32CM/NOPB	ACTIVE	SOIC	D	16	48	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	DS26LS32CM	Samples
DS26LS32CMX/NOPB	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	DS26LS32CM	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

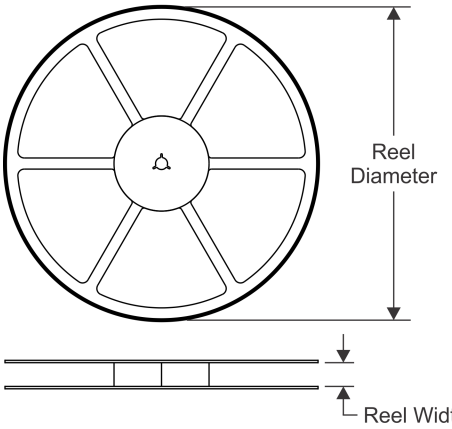
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

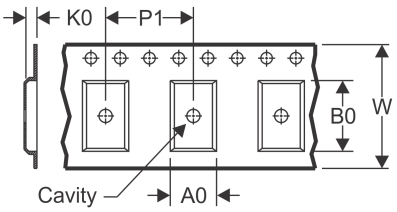
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

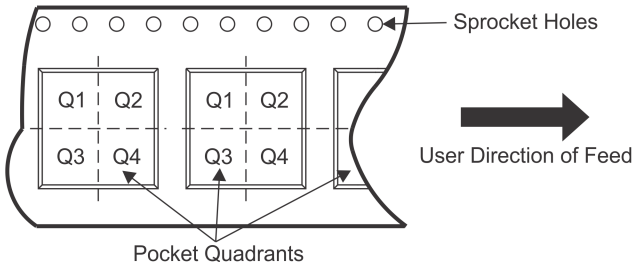


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

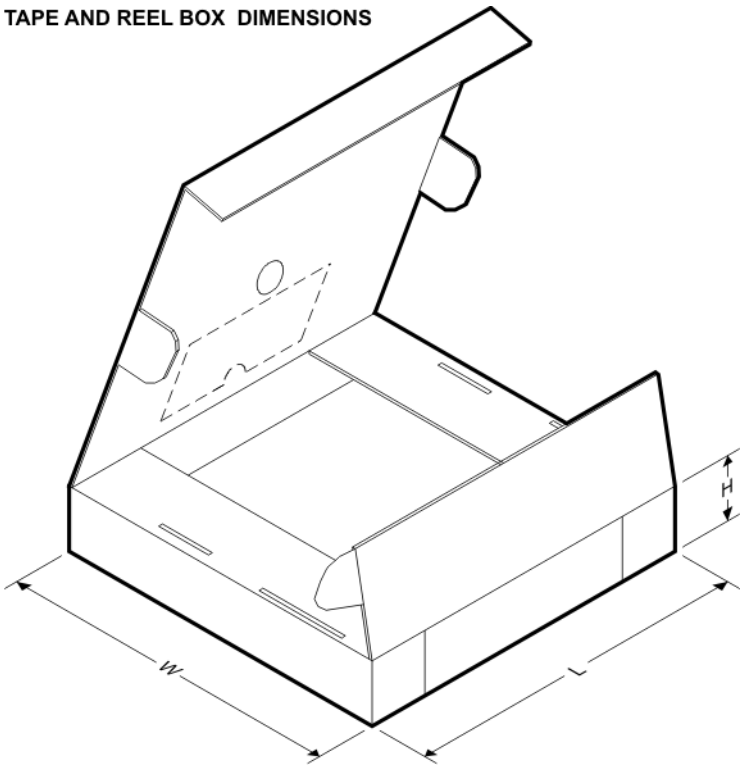
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS26LS32ACMX/NOPB	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.3	8.0	16.0	Q1
DS26LS32CMX/NOPB	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.3	8.0	16.0	Q1

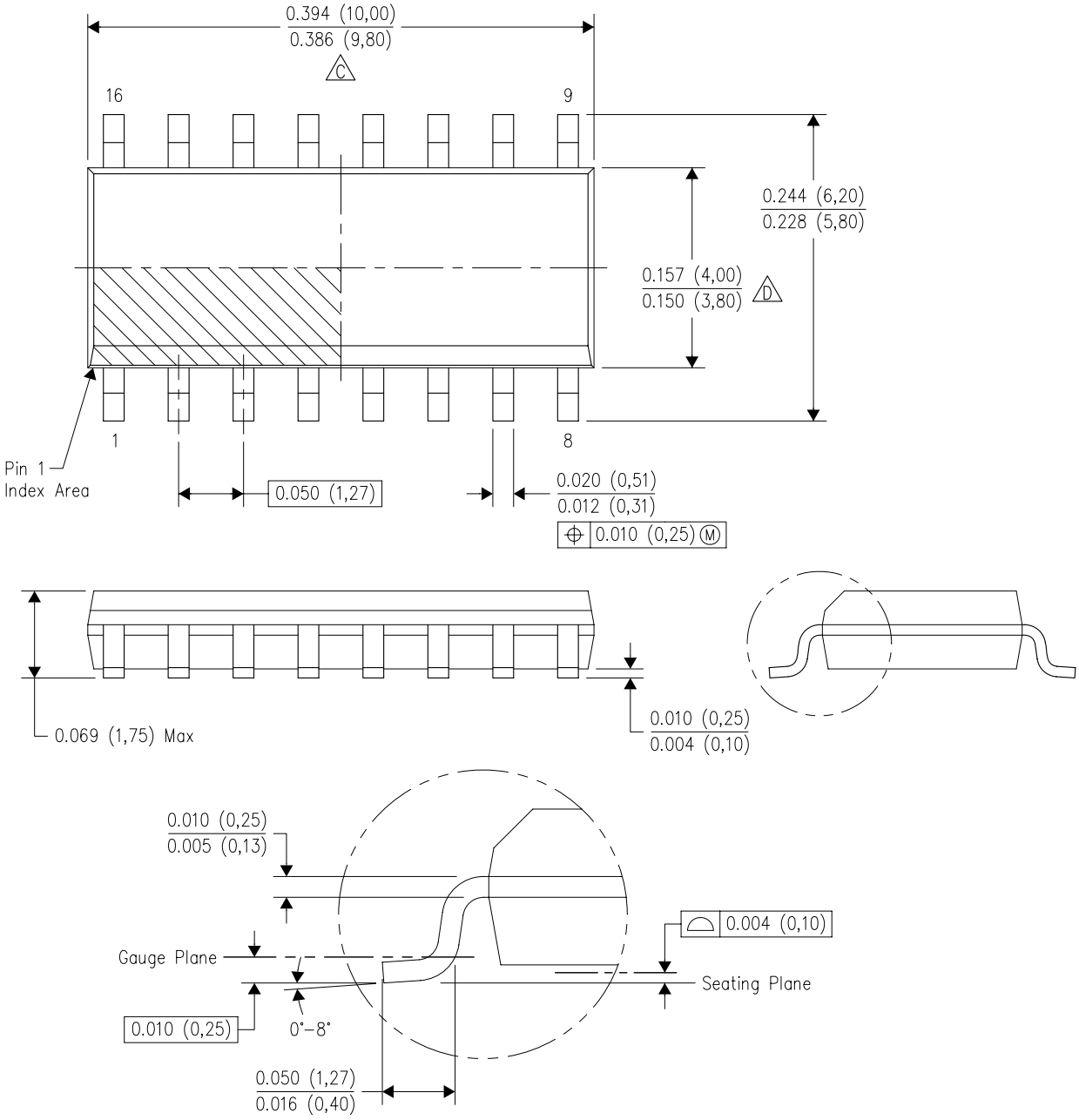
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS26LS32ACMX/NOPB	SOIC	D	16	2500	367.0	367.0	35.0
DS26LS32CMX/NOPB	SOIC	D	16	2500	367.0	367.0	35.0

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.