

DS280DF810 28 Gbps Multi-Rate 8-Channel Retimer

1 Features

- Octal-Channel Multi-Rate Retimer with Integrated Signal Conditioning
- All Channels Lock Independently from 20.2 to 28.4 Gbps (Including Sub-Rates Like 10.1376 Gbps, 10.3125 Gbps, 12.5 Gbps, and More)
- Ultra-Low Latency: <500 ps typical for 28.4 Gbps data rate
- Single Power Supply, No Low-Jitter Reference Clock Required, and Integrated AC Coupling Capacitors to Reduce Board Routing Complexity and BOM Cost
- Integrated 2x2 Cross Point
- Adaptive Continuous Time Linear Equalizer (CTLE)
- Adaptive Decision Feedback Equalizer (DFE)
- Low-Jitter Transmitter with 3-Tap FIR Filter
- Combined Equalization Supporting 35+ dB Channel Loss at 12.9 GHz; 30+ dB Channel Loss at 14 GHz
- Adjustable Transmit Amplitude: 205 mVppd to 1225 mVppd (typical)
- On-Chip Eye Opening Monitor (EOM), PRBS Pattern Checker/Generator
- Small 8 mm x 13 mm BGA Package with Easy Flow-Through Routing

- Unique Pinout Allows Routing High-Speed Signals Underneath the Package
- Pin-Compatible Repeater Available
- Extended Temperature Range: -40 °C to 85 °C

2 Applications

- Backplane/Mid-plane Reach Extension
- Jitter Cleaning for Front-Port Optical
- IEEE802.3bj 100GbE, Infiniband EDR, and OIF-CEI-25G-LR/MR/SR/VSR Electrical Interfaces
- SFP28, QSFP28, CFP2/CFP4, CDFP

3 Description

The DS280DF810 is an eight-channel multi-rate Retimer with integrated signal conditioning. It is used to extend the reach and robustness of long, lossy, crosstalk-impaired high-speed serial links while achieving a bit error rate (BER) of 10^{-15} or less.

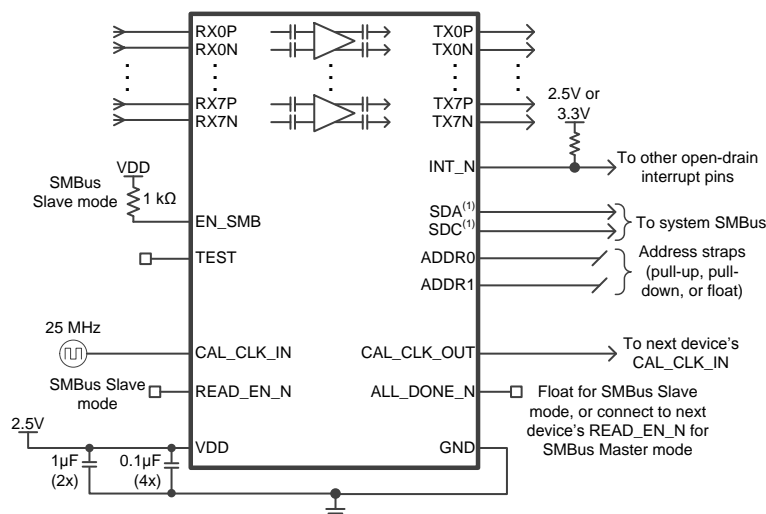
Each channel of the DS280DF810 independently locks to serial data rates in a continuous range from 20.2 Gbps to 28.4 Gbps or to any supported sub-rate ($\div 2$ and $\div 4$), including key data rates such as 10.1376 Gbps, 10.3125 Gbps, and 12.5 Gbps, which allows the DS280DF810 to support individual lane Forward Error Correction (FEC) pass-through.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DS280DF810	135-pin fcBGA (135)	8.0 mm x 13.0 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

4 Simplified Schematic



(1) SMBus signals need to be pulled up elsewhere in the system.



5 Description (Continued)

Integrated physical AC coupling capacitors (TX and RX) eliminate the need for external capacitors on the PCB. The DS280DF810 has a single power supply and minimal need for external components. These features reduce PCB routing complexity and BOM cost.

The advanced equalization features of the DS280DF810 include a low-jitter 3-tap transmit finite impulse response (FIR) filter, an adaptive continuous-time linear equalizer (CTLE), and an adaptive decision feedback equalizer (DFE). This enables reach extension for lossy interconnect and backplanes with multiple connectors and crosstalk. The integrated CDR function is ideal for front-port optical module applications to reset the jitter budget and retime the high-speed serial data. The DS280DF810 implements 2x2 cross-point on each channel pair, providing the host with both lane crossing and fanout options.

The DS280DF810 can be configured either via the SMBus or through an external EEPROM. Up to 16 devices can share a single EEPROM. A non-disruptive on-chip eye monitor and a PRBS generator/checker allow for in-system diagnostics.

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6 Revision History

DATE	REVISION	NOTES
June 2016	*	Initial release.

7 Device and Documentation Support

7.1 Documentation Support

7.1.1 Related Documentation

For related documentation see the following:

- [SNLU182 25G/28G Retimer Programmer's Guide](#)

7.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

7.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

7.4 Trademarks

E2E is a trademark of Texas Instruments.

7.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

8 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS280DF810ABVR	PREVIEW	FCBGA	ABV	135	1000	TBD	Call TI	Call TI	-40 to 85	DS280DF8	
DS280DF810ABVT	PREVIEW	FCBGA	ABV	135	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 85	DS280DF8	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

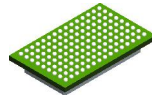
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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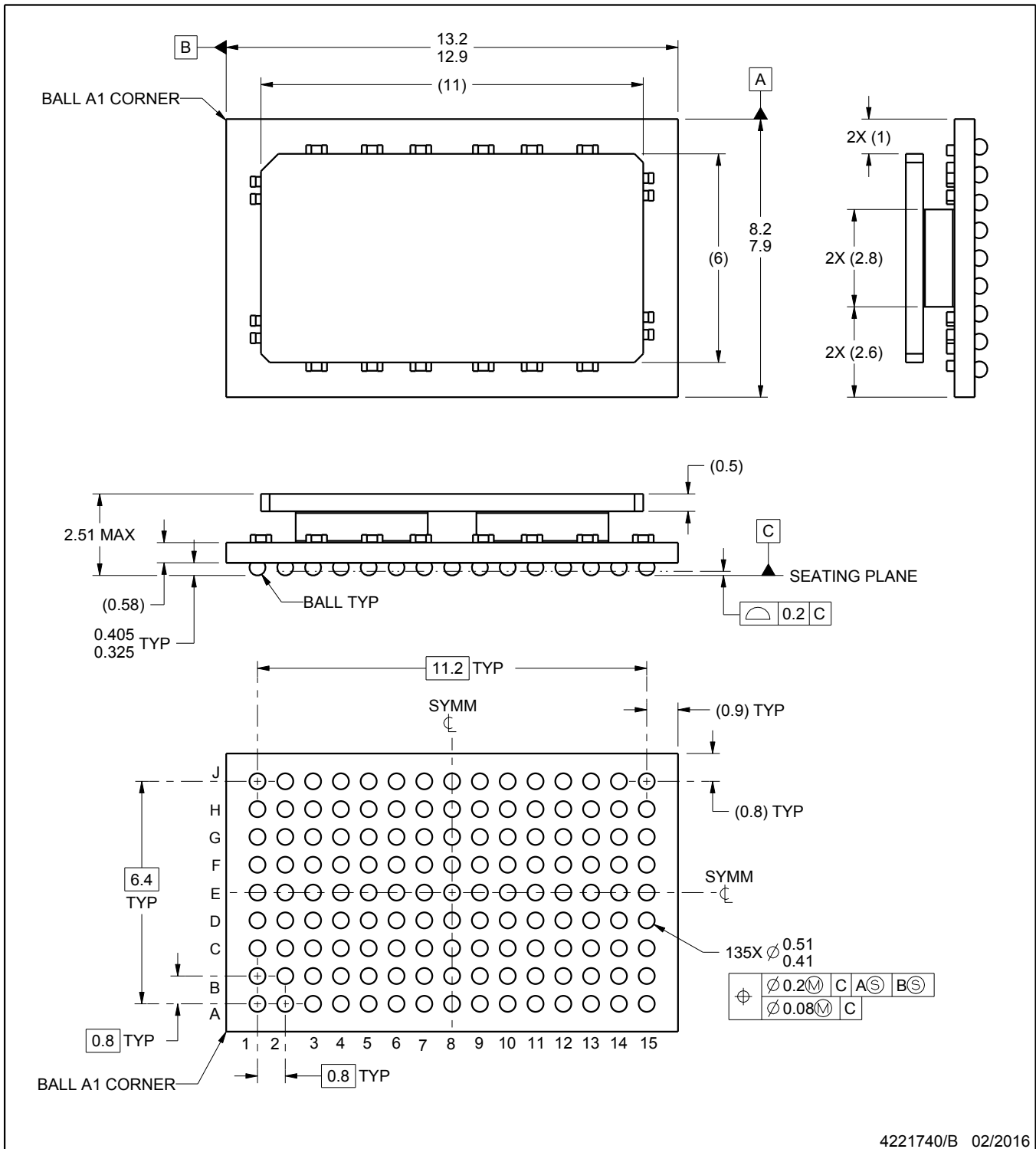
ABV0135A



PACKAGE OUTLINE

FCBGA - 2.51 mm max height

BALL GRID ARRAY



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NOTES:

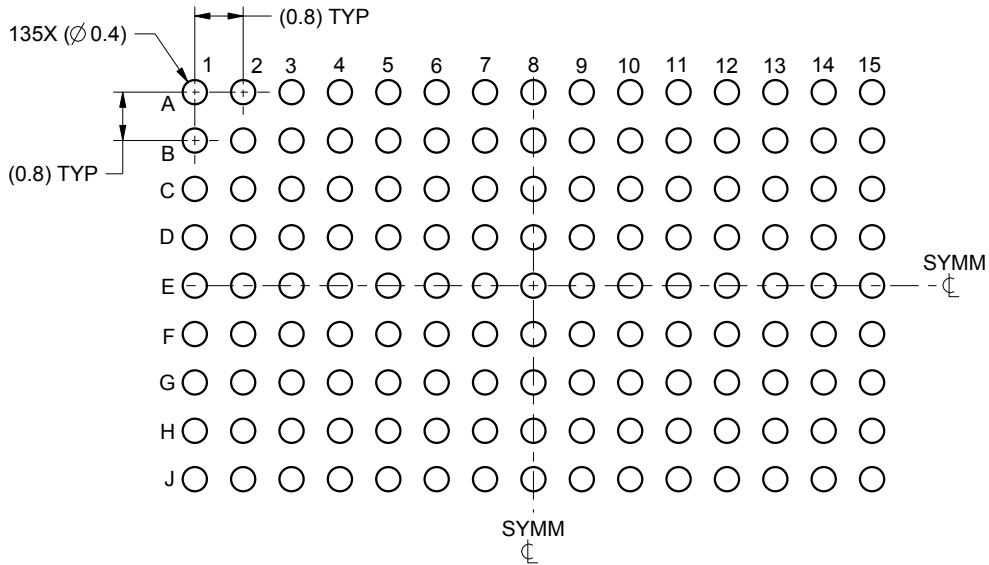
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

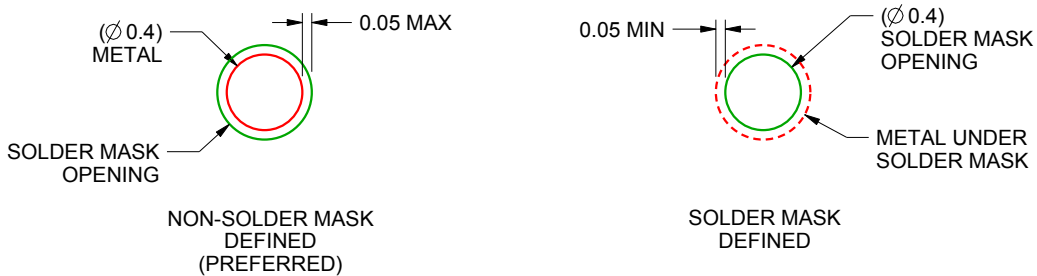
ABV0135A

FCBGA - 2.51 mm max height

BALL GRID ARRAY



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS
NOT TO SCALE

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NOTES: (continued)

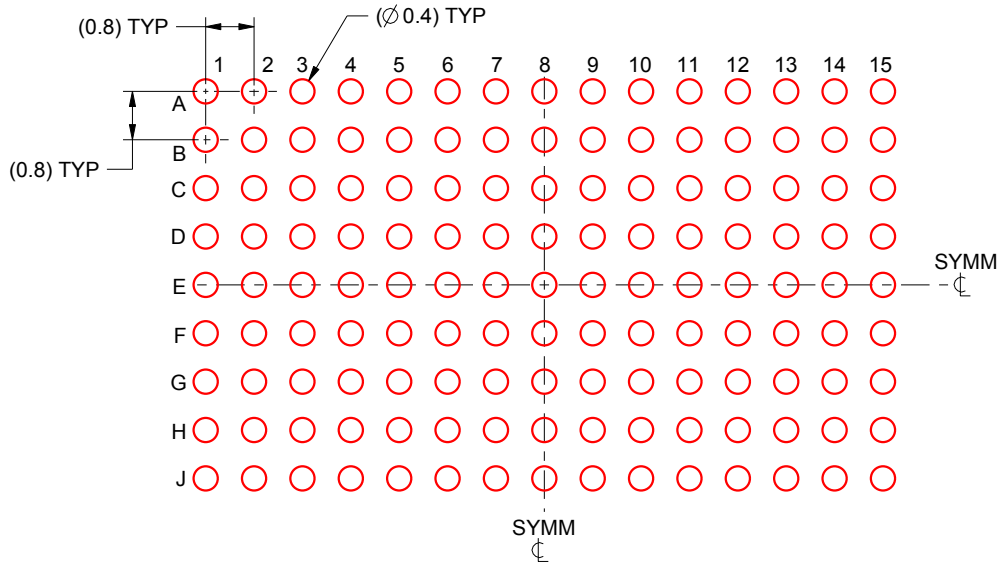
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For information, see Texas Instruments literature number SPRU811 (www.ti.com/lit/spru811).

EXAMPLE STENCIL DESIGN

ABV0135A

FCBGA - 2.51 mm max height

BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.15 mm THICK STENCIL
SCALE:8X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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