

DS3695A/DS3695AT/DS3696A Multipoint RS485/RS422 Transceivers

Check for Samples: [DS3695A](#), [DS3695AT](#), [DS3696A](#)

FEATURES

- Meets EIA Standard RS485 for Multipoint Bus Transmission and is Compatible with RS-422
- 10 Ns Driver Propagation Delays (Typical)
- Single +5V Supply
- -7V to +12V Bus Common Mode Range Permits $\pm 7V$ Ground Difference between Devices on the Bus
- Thermal Shutdown Protection
- High Impedance to Bus with Driver in TRI-STATE or with Power Off, over the Entire Common Mode Range Allows the Unused Devices on the Bus to be Powered Down
- Combined Impedance of a Driver Output and Receiver Input is less than One RS485 Unit Load, Allowing up to 32 Transceivers on the Bus
- 70 mV Typical Receiver Hysteresis
- Available in SOIC Packaging

DESCRIPTION

The DS3695A and DS3696A are high speed differential TRI-STATE bus/line transceivers designed to meet the requirements of EIA standard RS485 with extended common mode range (+12V to -7V), for multipoint data transmission. In addition they are compatible with requirements of RS-422.

The driver and receiver outputs feature TRI-STATE capability. The driver outputs remain in over the entire common mode range of +12V to -7V. Bus faults that cause excessive power dissipation within the device trigger a thermal shutdown circuit, which forces the driver outputs into the high impedance state. The DS3696A provides an output pin (TS) which reports the thermal shutdown of the device. TS is an "open collector" pin with an internal 10 k Ω pull-up resistor. This allows the TS outputs of several devices to be wire OR-ed.

Both AC and DC specifications are guaranteed over the 0°C to 70°C temperature and 4.75V to 5.25V supply voltage range.

Connection and Logic Diagrams

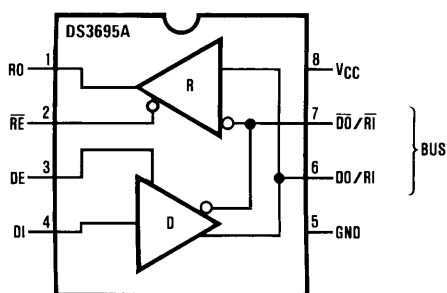


Figure 1. Molded Package, Small Outline (D0008A)
Top View

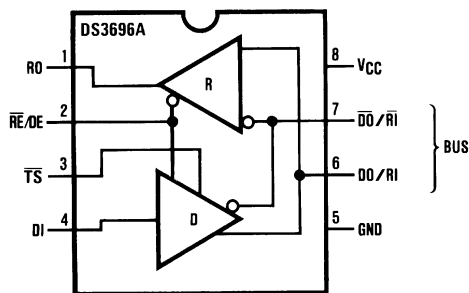


Figure 2. Top View
(See Package Number D0008A)

\overline{TS} was \overline{LF} (Line Fault) on previous datasheets, \overline{TS} goes low upon thermal shutdown.



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings ⁽¹⁾⁽²⁾

Supply Voltage, V_{CC}	7V
Control Input Voltages	7V
Driver Input Voltage	7V
Driver Output Voltages	+15V/–10V
Receiver Input Voltages	+15V/–10V
Receiver Output Voltage	5.5V
Continuous Power Dissipation @ 25°C	
D0008A Package	630 mW ⁽³⁾
Storage Temp. Range	–65°C to +150°C
Lead Temp. (Soldering 4 seconds)	260°C

- (1) “Absolute maximum ratings” are those beyond which the safety of the device cannot be verified. They are not meant to imply that the device should be operated at these limits. The tables of “Electrical Characteristics” provide conditions for actual device operation.
- (2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
- (3) Derate linearly at 6.5 mW/°C to 337 mW at 70°C.

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}	4.75	5.25	V
Bus Voltage	–7	+12	V
Operating Free Air Temperature (T_A)			
Commercial (DS3695AM)	0	+70	°C
Industrial (DS3695ATM)	–40	+85	°C
Commercial (DS3696AM)	0	+70	°C

Electrical Characteristics ^{(1) (2)}

0°C ≤ T_A ≤ 70°C, 4.75V < V_{CC} < 5.25V unless otherwise specified

Parameter		Test Conditions	Min	Typ	Max	Units	
V_{OD1}	Differential Driver Output Voltage (Unloaded)	$I_O = 0$			5	V	
V_{OD2}	Differential Driver Output Voltage (with Load)	$R = 50\Omega$; (RS-422) ⁽³⁾	2			V	
		$R = 27\Omega$; (RS-485)	1.5			V	
ΔV_{OD}	Complementary Output States Differential Output Voltage For Change in Magnitude of Driver	$R = 27\Omega$			0.2	V	
V_{OC}	Driver Common Mode Output Voltage				3.0	V	
$\Delta V_{OC} $	Change in Magnitude of Driver Common Mode Output Voltage For Complementary Output States				0.2	V	
V_{IH}	Input High Voltage	$DI, DE, \overline{RE},$ RE/DE	2			V	
V_{IL}	Input Low Voltage				0.8	V	
V_{CL}	Input Clamp Voltage		$I_{IN} = -18 \text{ mA}$			–1.5	V
I_{IL}	Input Low Current		$V_{IL} = 0.4V$			–200	μA
I_{IH}	Input High Current		$V_{IH} = 2.4V$			20	μA

- (1) All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified.
- (2) All typicals are given for $V_{CC} = 5V$ and $T_A = 25^\circ\text{C}$.
- (3) All limits for which this note is applied must be derated by 10% for DS3695AT. Other parameters remain the same for this extended temperature range device (–40°C ≤ T_A ≤ +85°C).

Electrical Characteristics ⁽¹⁾ ⁽²⁾ (continued)
 $0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$, $4.75\text{V} < V_{CC} < 5.25\text{V}$ unless otherwise specified

Parameter			Test Conditions	Min	Typ	Max	Units	
I_{IN}	Input Current	\overline{RI} , \overline{RI} , DO/RI, DO/RI	$V_{CC} = 0\text{V}$ or 5.25V , DE or $\overline{RE}/\overline{DE} = 0\text{V}$	$V_{IN} = 12\text{V}$		+1.0	mA	
				$V_{IN} = -7\text{V}$		-0.8	mA	
V_{TH}	Differential Input Threshold Voltage for Receiver		$-7\text{V} \leq V_{CM} \leq +12\text{V}$	-0.2		+0.2	V	
ΔV_{TH}	Receiver Input Hysteresis		$V_{CM} = 0\text{V}$		70		mV	
V_{OH}	Receiver Output High Voltage		$I_{OH} = -400\ \mu\text{A}$	2.4			V	
V_{OL}	Output Low Voltage	RO	$I_{OL} = 16\ \text{mA}$ ⁽³⁾			0.5	V	
		\overline{TS}	$I_{OL} = 8\ \text{mA}$			0.45	V	
I_{OZR}	Output Current at Receiver OFF-State (High Impedance)		$0.4\text{V} \leq V_O \leq 2.4\text{V}$, $V_{CC} = \text{Max}$,			± 20	μA	
R_{IN}	Receiver Input Resistance		$-7\text{V} \leq V_{CM} \leq +12\text{V}$	12			k Ω	
I_{CC}	Supply Current		No Load ⁽³⁾	Driver Outputs Enabled		42	60	mA
				Driver Outputs Disabled		27	40	mA
I_{OSD}	Output Current Driver Short-Circuit		$V_O = -7\text{V}$ ⁽³⁾			-250	mA	
			$V_O = +12\text{V}$ ⁽³⁾			+250	mA	
I_{OSR}	Output Current Receiver Short-Circuit		$V_O = 0\text{V}$	-15		-85	mA	

Receiver Switching Characteristics
 $0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$, $4.75\text{V} < V_{CC} < 5.25\text{V}$ unless otherwise specified ⁽⁴⁾

Symbol	Test Conditions	Min	Typ	Max	Units
t_{PLH}	$C_L = 15\ \text{pF}$	15	28	42	ns
t_{PHL}	S1 and S2	15	28	42	ns
$ t_{PLH} - t_{PHL} $	Closed	0	3		ns
t_{PLZ}	$C_L = 15\ \text{pF}$, S2 Open	5	29	35	ns
t_{PHZ}	$C_L = 15\ \text{pF}$, S1 Open	5	12	16	ns
t_{PZL}	$C_L = 15\ \text{pF}$, S2 Open	7	15	28	ns
t_{PZH}	$C_L = 15\ \text{pF}$, S1 Open	7	15	20	ns

⁽⁴⁾ All typicals are given for $V_{CC} = 5\text{V}$ and $T_A = 25^{\circ}\text{C}$.

Driver Switching Characteristics
 $0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$, $4.75\text{V} < V_{CC} < 5.25\text{V}$ unless otherwise specified ⁽¹⁾

Symbol	Test Conditions	Min	Typ	Max	Units
SINGLE ENDED CHARACTERISTICS (Figure 7, Figure 8, and Figure 10)					
t_{PLH}	$R_{L\text{DIFF}} = 60\ \Omega$	9	15	22	ns
t_{PHL}	$C_{L1} = C_{L2} = 100\ \text{pF}$	9	15	22	ns
$t_{\text{SKEW}} t_{PLH} - t_{PHL} $		0	2	8	ns
t_{PLZ}	$C_L = 15\ \text{pF}$, S2 Open	7	15	30	ns
t_{PHZ}	$C_L = 15\ \text{pF}$, S1 Open	7	15	30	ns
t_{PZL}	$C_L = 100\ \text{pF}$, S2 Open	30	35	50	ns
t_{PZH}	$C_L = 100\ \text{pF}$, S1 Open	30	35	50	ns
DIFFERENTIAL SWITCHING CHARACTERISTICS (Figure 10)					
t_r, t_f	$R_{L\text{DIFF}} = 60\ \Omega$ $C_{L1} = C_{L2} = 100\ \text{pF}$	6	10	18	ns

⁽¹⁾ All typicals are given for $V_{CC} = 5\text{V}$ and $T_A = 25^{\circ}\text{C}$.

AC TEST CIRCUITS AND SWITCHING WAVEFORMS

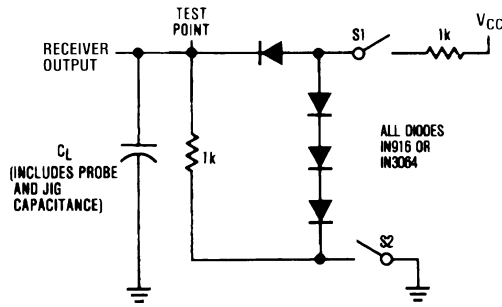
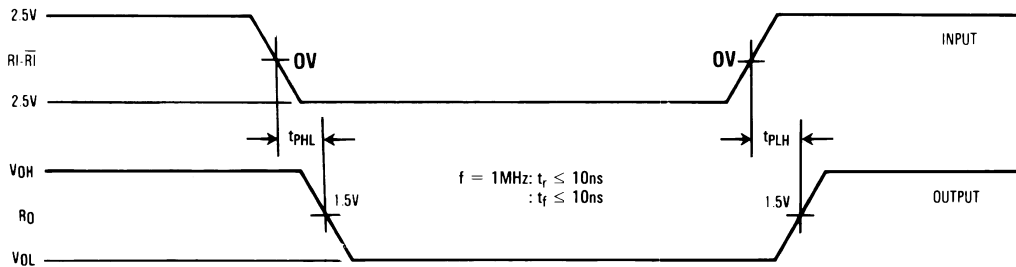


Figure 3. Receiver Propagation Delay Test Circuit



Differential input voltage may be realized by grounding $\bar{R}\bar{I}$ and pulsing $R\bar{I}$ between +2.5V and -2.5V

Figure 4. Receiver Input-to-Output Propagation Delay Timing

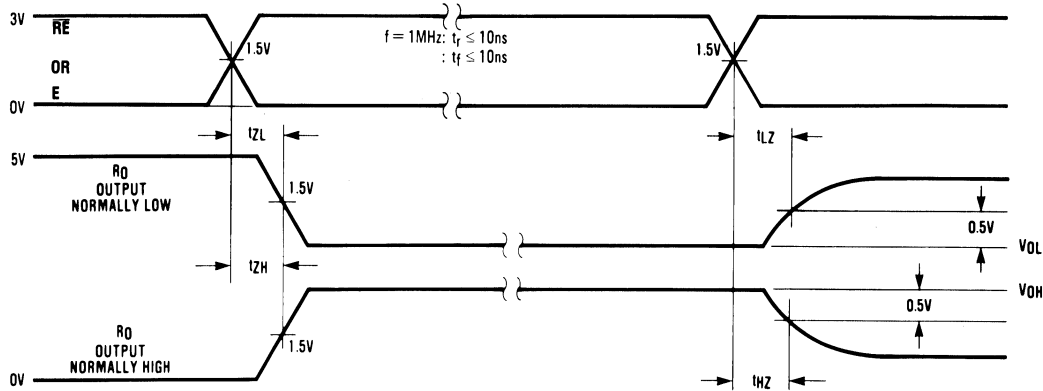


Figure 5. Receiver Enable/Disable Propagation Delay Timing

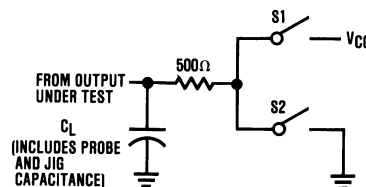


Figure 6. Unless Otherwise Specified the Switches are Closed

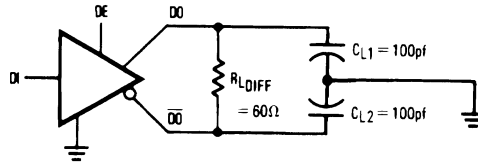
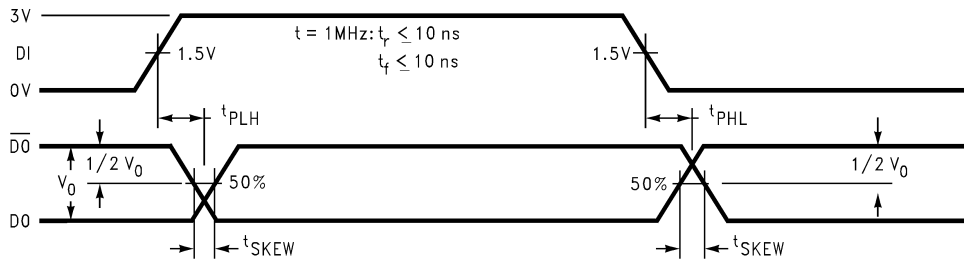


Figure 7. Driver Propagation Delay Test Circuits



t_{PLH} and t_{PHL} are measured to the respective 50% points. t_{SKEW} is the difference between propagation delays of the complementary outputs.

Figure 8. Driver Input-to-Output Propagation Delay Timing (Single-Ended)

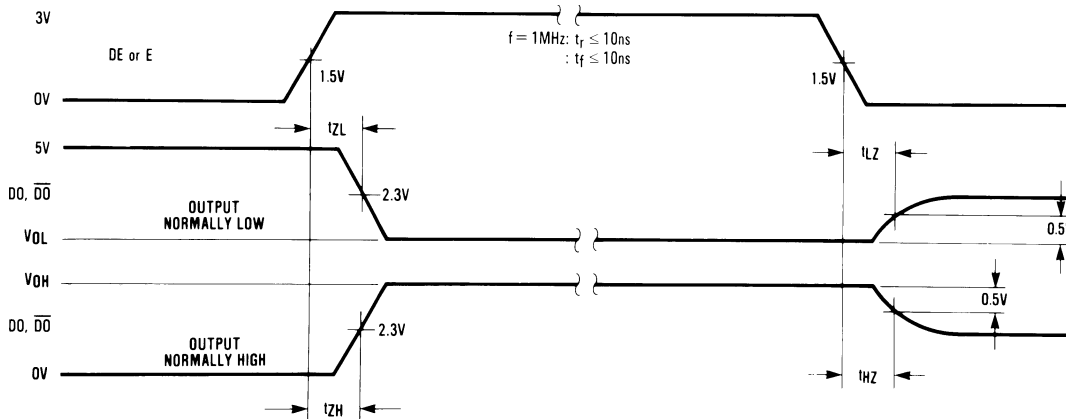


Figure 9. Driver Enable/Disable Propagation Delay Timing

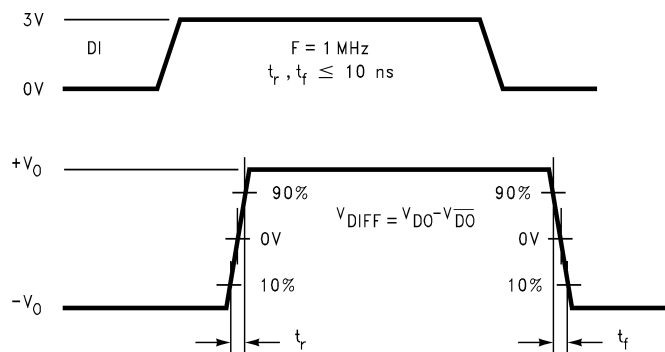


Figure 10. Driver Differential Transition Timing

Table 1. Function Tables DS3695A/DS3696A Transmitting⁽¹⁾

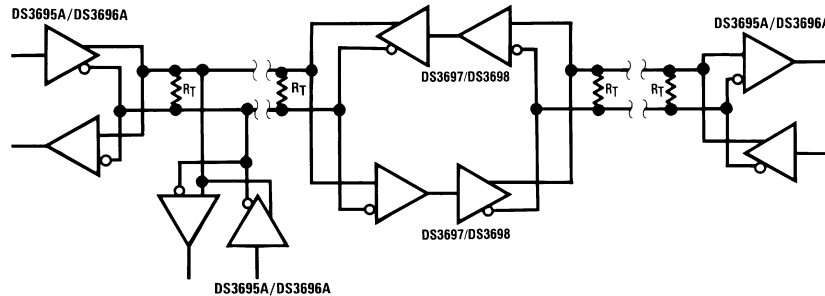
Inputs			Line	Outputs		
\overline{RE}	DE	DI	Condition	\overline{DO}	DO	\overline{TS}^* (DS3696A Only)
X	1	1	No Fault	0	1	H
X	1	0	No Fault	1	0	H
X	0	X	X	Z	Z	H
X	1	X	Fault	Z	Z	L

Table 2. Function Tables DS3695A/DS3696A Receiving⁽¹⁾

Inputs			Line	RO	\overline{TS}^* (DS3696A Only)
\overline{RE}	DE	$RI-\overline{RI}$			
0	0	$\geq +0.2V$		1	H
0	0	$\leq -0.2V$		0	H
0	0	Inputs Open**		1	H
1	0	X		Z	H

- (1) X — Don't care condition
 Z — High impedance state
 Fault — Improper line conditions causing excessive power dissipation in the driver, such as shorts or bus contention situations
 * \overline{TS} is an "open collector" output with an on-chip 10 k Ω pull-up resistor.
**** This is a fail safe condition**
- (1) X — Don't care condition
 Z — High impedance state
 Fault — Improper line conditions causing excessive power dissipation in the driver, such as shorts or bus contention situations
 * \overline{TS} is an "open collector" output with an on-chip 10 k Ω pull-up resistor.
**** This is a fail safe condition**

Typical Application



Repeater control logic not shown.

Figure 11.

REVISION HISTORY

Changes from Revision B (April 2013) to Revision C	Page
<hr/> <ul style="list-style-type: none">• Changed layout of National Data Sheet to TI format	<hr/> 6

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS3695AM	NRND	SOIC	D	8	95	TBD	Call TI	Call TI	0 to 70	DS36 95AM	
DS3695AM/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	DS36 95AM	Samples
DS3695AMX	NRND	SOIC	D	8	2500	TBD	Call TI	Call TI	0 to 70	DS36 95AM	
DS3695AMX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	DS36 95AM	Samples
DS3695ATM	NRND	SOIC	D	8	95	TBD	Call TI	Call TI	-40 to 85	DS369 5ATM	
DS3695ATM/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	DS369 5ATM	Samples
DS3695ATMX	NRND	SOIC	D	8	2500	TBD	Call TI	Call TI	-40 to 85	DS369 5ATM	
DS3695ATMX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	DS369 5ATM	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS3695AMX	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
DS3695AMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
DS3695ATMX	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
DS3695ATMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

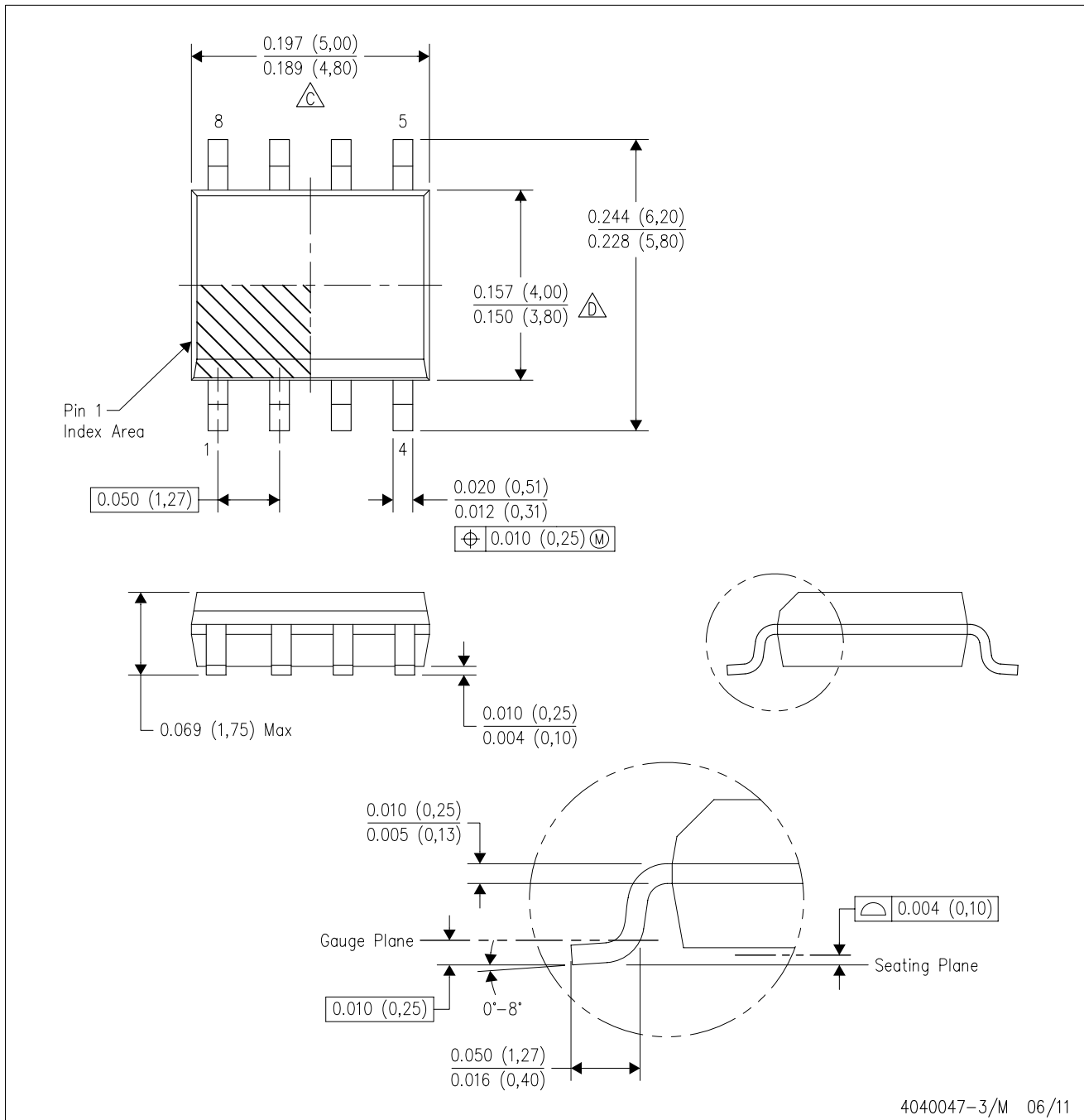


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS3695AMX	SOIC	D	8	2500	367.0	367.0	35.0
DS3695AMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
DS3695ATMX	SOIC	D	8	2500	367.0	367.0	35.0
DS3695ATMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AA.

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