DS90UB914A-Q1 25-MHz to 100-MHz 10/12-Bit FPD-Link III Deserializer

1 Features

- Qualified for Automotive Applications AEC-Q100
  - Device Temperature Grade 2: –40°C to +105°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level ±8kV
  - Device CDM ESD Classification Level C6
- 25-MHz to 100-MHz Input Pixel Clock Support
- Programmable Data Payload:
  - 10-bit Payload up to 100 MHz
  - 12-bit Payload up to 75 MHz
- Continuous Low Latency Bidirectional Control Interface Channel with I2C Support at 400 kHz
- 2:1 Multiplexer to choose between two input images
- Capable of Receiving over 15m Coaxial or 20m Shielded Twisted-pair Cables
- Robust Power-Over-Coaxial (PoC) Operation
- Receive Equalizer Automatically Adapts for Changes in Cable Loss
- LOCK Output Reporting Pin and @SPEED BIST Diagnosis Feature to Validate Link Integrity
- Single Power Supply at 1.8 V
- ISO 10605 and IEC 61000-4-2 ESD Compliant
- EMI/EMC Mitigation with Programmable Spread Spectrum (SSCG) and Receiver Staggered Outputs

2 Applications

- Automotive
  - Surround View Systems (SVS)
  - Rear and Front View Cameras
  - Driver Monitor Cameras (DMS)
  - Remote Satellite RADAR Sensors
- Security and Surveillance
- Industrial Machine Vision

3 Description

The DS90UB914A-Q1 device offers an FPD-Link III interface with a high-speed forward channel and a bidirectional control channel for data transmission over a single coaxial cable or differential pair. The DS90UB914A-Q1 device incorporates differential signaling on both the high-speed forward channel and bidirectional control channel data paths. The deserializer is targeted for connections between imagers and video processors in an ECU (Electronic Control Unit). This device is ideally suited for driving video data requiring up to 12-bit pixel depth plus two synchronization signals along with bidirectional control channel bus.

The deserializer features a multiplexer to allow selection between two input imagers, one active at a time. The primary video transport converts 10-bit or 12-bit data to a single high-speed serial stream, along with a separate low latency bidirectional control channel transport that accepts control information from an I2C port and is independent of video blanking period.

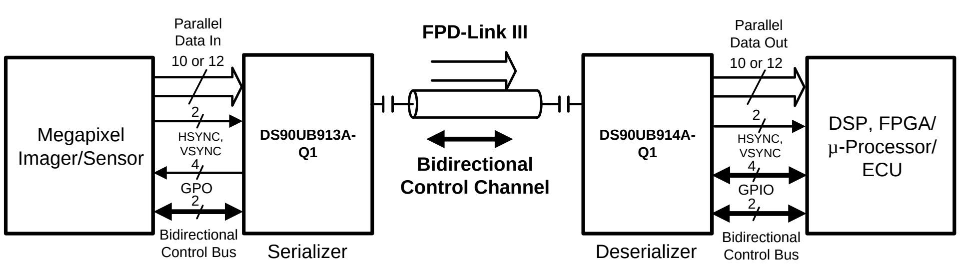
Using TI's embedded clock technology allows transparent full-duplex communication over a single differential pair, carrying asymmetrical-bidirectional control channel information. This single serial stream simplifies transferring a wide data bus over PCB traces and cable by eliminating the skew problems between parallel data and clock paths. This significantly saves system cost by narrowing data paths that in turn reduce PCB layers, cable width, and connector size and pins. In addition, the Deserializer inputs provide adaptive equalization to compensate for loss from the media over longer distances. Internal DC-balanced encoding/decoding is used to support AC-coupled interconnects.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DS90UB914A-Q1	WQFN (48)	7.00 mm x 7.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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4 Revision History

Changes from Revision A (June 2016) to Revision B — **Page**

- Added Back Channel Line Rate specification; also added footnote for clarification between MHz and Mbps distinction. 9
- Revised back channel VOD specification from 175mV to 182 mV. 9
- Removed 'ns' unit from specifications referencing period in units of T. 16
- Revise Deserializer Delay specification due to the swapped information. 16
- Revised jitter tolerance curve to be for typical system IJT configuration with DS90UB913A linked to DS90UB914A. 17
- Added device functional mode table for external oscillator operation with example XCLKIN = 48MHz. 23
- Fixed typo and changed "deserializer" to "serializer". 35
- Added register 0x05 for Forward Channel Low Frequency Gain. 35
- Added registers 0x27, 0x47 for Forward Channel Tuning/Impedance Control. 43
- Revised rise time and delay conditions to include 10% to 90% parameters instead of VIH and VIL. 46
- Changed max rise time for V_{DDIO} and V_{DD_N} to be 5ms instead of 1.5ms during power-up. 46
- Revised power-up timing paragraph for clarity and correctness. 46
- Changed VIL and VIH specs to 10% and 90% respectively for rising/falling edges. 46

Changes from Original (April 2016) to Revision A — **Page**

- Split document into two separate documents for parts DS90UB913A-Q1 SNLS443 and DS90UB914A-Q1 SNLS499. 1
- Combined revision history showing changes when this document was part of the DS90UB913A-Q1 SNLS443 datasheet 1
- Added Automotive Features 1
- Updated pin description for ROUT to include active/inactive outputs corresponding to MODE setting. 4
- Added pin description to GPIO pins to leave open if unused. 5
- Updated frequency requirements for 10-bit and 12-bit HF modes. 10-bit mode – 50 MHz to 100 MHz; 12-bit HF mode – 37.5 MHz to 75 MHz; 12-bit LF mode (no change) – 25 MHz to 50 MHz. 5
- Added pin description to RIN pins to leave open if unused. 6

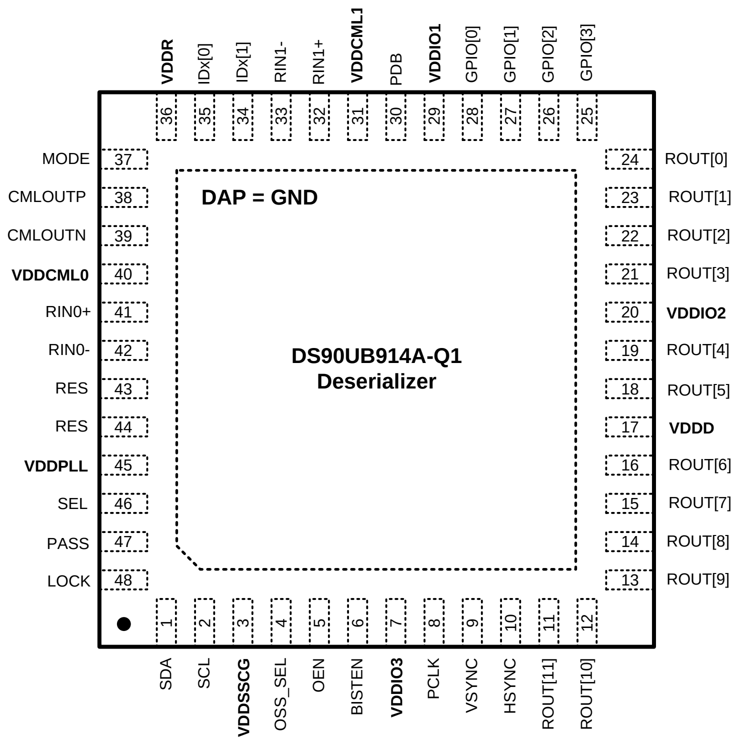
- Changed Air Discharge ESD Rating (IEC61000-4-2: RD = 330 Ω, CS = 150 pF) to minimum ±25000 V. 7
- Added additional thermal characteristics. 8
- Added GPIO[3:0] typical pin capacitances. 8
- Changed Differential Input Voltage minimum specification. 9
- Changed Single-Ended Input Voltage minimum specification. 9
- Added Back Channel Differential Output Voltage minimum specification. 9
- Added Back Channel Single-Ended Output Voltage minimum specification. 9
- Added footnote that states the following: "UI – Unit Interval is equivalent to one serialized data bit width. The UI scales with PCLK frequency." Also added below calculations to footnote. 12-bit LF mode 1 UI = 1 / (PCLK_Freq. x 28) 12-bit HF mode 1 UI = 1 / (PCLK_Freq. x 2/3 x 28) 10-bit mode 1 UI = 1 / (PCLK_Freq. /2 x 28) 9
- Updated I_{DDIOR} for V_{DDIO}=1.89V, C_L=8pF, Worst-Case Pattern with f=50 MHz, 12-bit low freq mode to typical value of 16 mA; value is currently 21 mA. 10
- Updated I_{DDIOR} for V_{DDIO}=1.89V, C_L=8pF, Random Pattern with f=50 MHz, 12-bit low freq mode to typical value of 10 mA; value is currently 14 mA. 10
- Updated I_{DDR} for V_{DD_n}=1.89V, C_L=4pF, Random Pattern with f=100 MHz, 10-bit mode to typical value of 69 mA; value is currently 57 mA. 10
- Updated I_{DDR} for V_{DD_n}=1.89V, C_L=4pF, Random Pattern with f=75 MHz, 12-bit high freq mode to typical value of 71 mA; value is currently 60 mA. 10
- Updated I_{DDR} for V_{DD_n}=1.89V, C_L=4pF, Random Pattern with f=50 MHz, 12-bit low freq mode to typical value of 67 mA; value is currently 56 mA. 10
- Updated V_{OL} Output Low Level row with revised I_{OL} currents and max V_{OL} voltages, dependent upon V_{DDIO} voltage. 13
- Updated Figure 2 title to state '"Worst-Case" Test Pattern for Power Consumption' 13
- Updated Figure 3 "Deserializer Vswing Diagram" with correct notation. 13
- Changed Figure 3 to clarify difference between STP and Coax 13
- Updated frequency ranges for MODE settings and also revised with correct maximum clock periods. Added footnote and nominal clock period to be in terms of 'T'. 15
- Changed typo on footnote to reflect 't_{DPJ}'. 16
- Table 2, row 5 with "static" input LOCK output status changed to "L". 26
- Table 5 heading updated to state "DS90UB914A-Q1 DESERIALIZER. 32
- Changed description of deserializer reg 0x00 bit[0]=0 from "set using address coming from CAD" to "set from ID[x]" 34
- Added row to register 0x01[2] for Back Channel Enable – 0: Disable 1: Enable. 34
- Changed SSCG Units for fmod (register 0x02[3:0]) to Reflect Hz instead of KHz. 34
- Changed parity error reset bit to be NOT self-clearing. 35
- Changed EQ gain values (dB) @ maximum line rate (1.4Gbps). 35
- Changed description of deserializer reg 0x04 to have correct register setting for each equalization gain level. 35
- Added registers 0x26, 0x46 for Bidirectional Control Channel (BCC)Tuning. 43
- Added deserializer 0x4C SEL register. 44
- Updated EQ Register Bits 0x4E[3:0] to be Reserved. Also changed EQ gain values (dB) @ maximum line rate (1.4Gbps). 44
- Added reference to Power over Coax Application report 45
- Updated power up sequencing information and timing diagram. 45
- Added power up sequencing information and timing diagram. 45
- Added 914A PDB Reset timing constraints and diagram. 46
- Removed Figure 21 and Figure 43 regarding adaptive equalizer graphs for loss compensation (Coax/STP). 47
- Renamed C1 and C2 to C22 and C23 for RIN0+ and RIN0- respectively on Typical Application Diagrams (Coax & STP). 49
- Added description specifying that the voltage applied on V_{DDIO} (1.8 V, 3.3 V) or V_{DD_n} (1.8 V) should be at the input pin – any board level DC drop should be compensated. 52
- Added 914A EVM layout example image. 55

5 Device Comparison Table

PART NUMBER	FPD-III FUNCTION	PACKAGE	TRANSMISSION MEDIA	PCLK FREQUENCY
DS90UB914Q-Q1	Deserializer	WQFN RHS (48)	STP	10 to 100 MHz
DS90UB914A-Q1	Deserializer	WQFN RHS (48)	Coax or STP	25 to 100 MHz

6 Pin Configuration and Functions

48-Pin WQFN
Package RHS
Top View



Pin Functions: DS90UB914A-Q1 Deserializer

PIN		I/O	DESCRIPTION
NAME	NO.		
LVCMOS PARALLEL INTERFACE			
ROUT[11:0]	11,12,13,14, 15,16,18,19, 21,22,23,24	Outputs, LVCMOS	Parallel Data Outputs For 10-bit MODE, parallel outputs ROUT[9:0] are active. ROUT[11:10] are inactive and should not be used. Any unused outputs (including ROUT[11:10]) should be No Connect. For 12-bit MODE (HF or LF), parallel outputs ROUT[11:0] are active. Any unused outputs should be No Connect.
HSYNC	10	Output, LVCMOS	Horizontal SYNC Output. Note: HS transition restrictions: 1. 12-bit Low-Frequency mode: No HS restrictions (raw) 2. 12-bit High-Frequency mode: No HS restrictions (raw) 3. 10-bit mode: HS restricted to no more than one transition per 10 PCLK cycles. Leave open if unused.
VSYNC	9	Output, LVCMOS	Vertical SYNC Output. Note: VS transition restrictions: 1. 12-bit Low-Frequency mode: No VS restrictions (raw) 2. 12-bit High-Frequency mode: No VS restrictions (raw) 3. 10-bit mode: VS restricted to no more than one transition per 10 PCLK cycles. Leave open if unused.
PCLK	8	Output, LVCMOS	Pixel Clock Output Pin Strobe edge set by RRFB control register.

Pin Functions: DS90UB914A-Q1 Deserializer (continued)

PIN NAME	PIN NO.	I/O	DESCRIPTION
GENERAL PURPOSE INPUT/OUTPUT (GPIO)			
GPI0[1:0]	27,28	Digital Input/Output, LVCMOS	General-purpose input/output pins can be used to control and respond to various commands. They may be configured to be the input signals for the corresponding GPOs on the serializer or they may be configured to be outputs to follow local register settings. Leave open if unused.
GPIO[3:2]	25,26	Digital Input/Output LVCMOS	General purpose input/output pins GPO[3:2] can be configured to be input signals for GPOs on the Serializer. In addition they can also be configured to be outputs to follow the local register settings. When the SerDes chipsets are working with an external oscillator, these pins can be configured only to be outputs to follow the local register settings. Leave open if unused.
BIDIRECTIONAL CONTROL BUS - I2C COMPATIBLE			
SCL	2	Input/Output, Open Drain	Clock line for the bidirectional control bus communication SCL requires an external pullup resistor to V_{DDIO}.
SDA	1	Input/Output, Open Drain	Data line for bidirectional control bus communication SDA requires an external pullup resistor to V_{DDIO}.
MODE	37	Input, analog	Device Mode Select Resistor to Ground and 10-kΩ pullup to 1.8 V rail. The MODE pin on the Deserializer can be used to configure the Serializer and Deserializer to work in different input PCLK range. See details in Table 2. **12– bit low frequency mode – (25 – 50 MHz operation):** In this mode, the Serializer and Deserializer can accept up to 12-bits DATA+2 SYNC. Input PCLK range is from 25 MHz to 50 MHz. Note: No HS/VS restrictions. **12– bit high frequency mode – (37.5 – 75 MHz operation):** In this mode, the Serializer and Deserializer can accept up to 12-bits DATA + 2 SYNC. Input PCLK range is from 37.5 MHz to 75 MHz. Note: No HS/VS restrictions. **10–bit mode– (50 – 100 MHz operation):** In this mode, the Serializer and Deserializer can accept up to 10-bits DATA + 2 SYNC. Input PCLK frequency can range from 50 MHz to 100 MHz. Note: HS/VS restricted to no more than one transition per 10 PCLK cycles. Please refer to Table 2 on how to configure the MODE pin on the Deserializer.
IDx[0:1]	35,34	Input, analog	Device ID Address Select The IDx[0] and IDx[1] pins on the Deserializer are used to assign the I2C slave device address. Resistor to Ground and 10-kΩ pullup to 1.8 V rail. See Table 6
CONTROL AND CONFIGURATION			
PDB	30	Input, LVCMOS w/ pulldown	Power Down Mode Pin PDB = H, Deserializer is enabled and is ON. PDB = L, Deserializer is in power down mode. When the Deserializer is in power down mode, programmed control register data are NOT retained and reset to default values.
LOCK	48	Output, LVCMOS	LOCK Status Output Pin LOCK = H, PLL is Locked, outputs are active. LOCK = L, PLL is unlocked, ROUT and PCLK output states are controlled by OSS_SEL control register. May be used as Link Status.
BISTEN	6	Input LVCMOS w/ pulldown	BIST Enable Pin BISTEN=H, BIST Mode is enabled. BISTEN=L, BIST Mode is disabled. See *Built In Self Test* for more information.
PASS	47	Output, LVCMOS	PASS Output Pin PASS = H, ERROR FREE Transmission. PASS = L, one or more errors were detected in the received payload. See *Built In Self Test* for more information. Leave Open if unused. Route to test point (pad) recommended.
OEN	5	Input LVCMOS w/ pulldown	Output Enable Input Refer to Table 3.
OSS_SEL	4	Input LVCMOS w/ pulldown	Output Sleep State Select Pin Refer to Table 3.
SEL	46	Input LVCMOS w/ pulldown	MUX Select Line SEL = L, RIN0+/- input. This selects input A as the active channel on the Deserializer. SEL = H, RIN1+/- input. This selects input B as the active channel on the Deserializer.

Pin Functions: DS90UB914A-Q1 Deserializer (continued)

PIN NAME	PIN NO.	I/O	DESCRIPTION
FPD–Link III INTERFACE			
RIN0+	41	Input/Output, CML	Non-Inverting Differential input, bidirectional control channel. The IO must be AC coupled with a 0.1-µF capacitor. Leave open if unused.
RIN0-	42	Input/Output, CML	Inverting Differential input, bidirectional control channel. The IO must be AC coupled with a 0.1-µF capacitor. For applications using single-ended coaxial interconnect, a 0.047-µF AC coupling capacitor should be placed in series with a 50Ω resistor before terminating to GND. Leave open if unused.
RIN1+	32	Input/Output, CML	Non-Inverting Differential input, bidirectional control channel. The IO must be AC coupled with a 0.1-µF capacitor. Leave open if unused.
RIN1-	33	Input/Output, CML	Inverting Differential input, bidirectional control channel. The IO must be AC coupled with a 0.1-µF capacitor. For applications using single-ended coaxial interconnect, a 0.047-µF AC coupling capacitor should be placed in series with a 50Ω resistor before terminating to GND. Leave open if unused.
RES	43,44	—	Reserved. **This pin must always be tied low**.
CMLOUTP/N	38,39	Output, CML	Route to test point or leave open if unused.
POWER AND GROUND (1)			
VDDIO1/2/3	29, 20, 7	Power, Digital	LVCMOS I/O Buffer Power, The single-ended outputs and control input are powered from V_{DDIO}. V_{DDIO} can be connected to a 1.8 V ±5% or 3.3 V ±10%.
VDDD	17	Power, Digital	Digital Core Power, 1.8 V ±5%.
VDDSSCG	3	Power, Analog	SSCG PLL Power, 1.8 V ±5%.
VDDR	36	Power, Analog	Rx Analog Power, 1.8 V ±5%.
VDDCML0/1	40,31	Power, Analog	CML and Bidirectional control channel Drive Power, 1.8 V ±5%.
VDDPLL	45	Power, Analog	PLL Power, 1.8 V ±5%.
VSS	DAP	Ground, DAP	DAP must be grounded. DAP is the large metal contact at the bottom side, located at the center of the WQFN package. Connected to the ground plane (GND) with at least 16 vias.

(1) See *Power-Up Requirements and PDB Pin*.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)]

	MIN	MAX	UNIT
Supply Voltage – V_{DD_n} (1.8 V)	−0.3	2.5	V
Supply Voltage – V_{DDIO}	−0.3	4.0	V
LVCMOS Input Voltage	−0.3	V_{DDIO} + 0.3	V
CML Receiver I/O Voltage (V_{DD})	-0.3	V_{DD} + 0.3	V
Junction Temperature		150	°C
Storage temperature range, T_{stg}	-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002[(1)]		±8000	V
		Charged device model (CDM), per AEC Q100-011	Corner pins (1, 12, 13, 24, 25, 36, 37, 48)	±1000	
			Other pins		
ESD Rating (IEC 61000-4-2) R_D = 330 Ω, C_s = 150pF		Air Discharge (DOUT+, DOUT-, RIN+, RIN-)		±25000	V
		Contact Discharge (DOUT+, DOUT-, RIN+, RIN-)		±7000	
ESD Rating (ISO10605) R_D = 330 Ω, C_s = 150/330 pF R_D = 2 KΩ, C_s = 150/330 pF		Air Discharge (DOUT+, DOUT-, RIN+, RIN-)		±15000	
		Contact Discharge (DOUT+, DOUT-, RIN+, RIN-)		±8000	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Supply Voltage (V_{DD_n})		1.71	1.8	1.89	V
LVCMOS Supply Voltage (V_{DDIO}= 1.8 V) OR		1.71	1.8	1.89	V
LVCMOS Supply Voltage (V_{DDIO}= 3.3 V)		3.0	3.3	3.6	
Supply Noise[(1)]	V_{DD_n} (1.8 V)			25	mVp-p
	V_{DDIO} (1.8 V)			25	
	V_{DDIO} (3.3 V)			50	
Operating Free Air Temperature (T_A)		–40	25	105	°C
PCLK Clock Frequency		25		100	MHz

(1) Supply noise testing was done with minimum capacitors (as shown on *Pin Configuration and Functions* and Figure 33 on the PCB. A sinusoidal signal is AC coupled to the V_{DD_n} (1.8 V) supply with amplitude = 25 mVp-p measured at the device V_{DD_n} pins. Bit error rate testing of input to the Ser and output of the Des with 10-meter cable shows no error when the noise frequency on the Ser is less than 1 MHz. The Des on the other hand shows no error when the noise frequency is less than 750 kHz.

7.4 Thermal Information

THERMAL METRIC[(1)]		DS90UB914A-Q1 RHS (WQFN) 48 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	29.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	10.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	6.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	6.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics[(1)(2)(3)]

Over recommended operating supply and temperature ranges unless otherwise specified.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
LVCMOS DC SPECIFICATIONS 3.3 V I/O (DES OUTPUTS, GPIO, CONTROL INPUTS AND OUTPUTS)							
V_{IH}	High Level Input Voltage	V_{IN} = 3 V to 3.6 V		2		V_{IN}	V
V_{IL}	Low Level Input Voltage	V_{IN} = 3 V to 3.6 V		GND		0.8	V
I_{IN}	Input Current	V_{IN} = 0 V or 3.6 V, V_{IN} = 3 V to 3.6 V		–20	±1	20	µA
V_{OH}	High Level Output Voltage	V_{DDIO} = 3 V to 3.6 V, I_{OH} = −4 mA		2.4		V_{DDIO}	V
V_{OL}	Low Level Output Voltage	V_{DDIO} = 3 V to 3.6 V, I_{OL} = 4 mA		GND		0.4	V
I_{OS}	Output Short Circuit Current	V_{OUT} = 0 V	Deserializer GPO Outputs		–15		mA
			LVCMOS Outputs		–35		mA
I_{OZ}	TRI-STATE Output Current	PDB = 0 V, V_{OUT} = 0 V or V_{DD}	LVCMOS Outputs, GPO Outputs	–20		20	µA
C_{GPIO}	Pin Capacitance	GPIO [3:0]			1.5		pF
LVCMOS DC SPECIFICATIONS 1.8 V I/O (DES OUTPUTS, GPIO, CONTROL INPUTS AND OUTPUTS)							
V_{IH}	High Level Input Voltage	V_{IN} = 1.71 V to 1.89 V		0.65 V_{IN}		V_{IN}	V
V_{IL}	Low Level Input Voltage	V_{IN} = 1.71 V to 1.89 V		GND		0.35 V_{IN}	V
I_{IN}	Input Current	V_{IN} = 0 V or 1.89 V, V_{IN} = 1.71 V to 1.89 V		–20	±1	20	µA
V_{OH}	High Level Output Voltage	V_{DDIO} = 1.71 V to 1.89 V, I_{OH} = −4 mA		V_{DDIO} - 0.45		V_{DDIO}	V
V_{OL}	Low Level Output Voltage	V_{DDIO} = 1.71 V to 1.89 V I_{OL} = 4 mA		GND		0.45	V
I_{OS}	Output Short Circuit Current	V_{OUT} = 0 V	Deserializer GPO Outputs		–11		mA
			LVCMOS Outputs		–17		mA
I_{OZ}	TRI-STATE Output Current	PDB = 0 V, V_{OUT} = 0 V or V_{DD}	LVCMOS Outputs, GPO Outputs	-20		20	µA
C_{GPIO}	Pin Capacitance	GPIO [3:0]			1.5		pF

(1) The Electrical Characteristics tables list verified specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not verified.
(2) Current into device pins is defined as positive. Current out of a device pin is defined as negative. Voltages are referenced to ground except VOD, ΔVOD, VTH and VTL which are differential voltages.
(3) Typical values represent most likely parametric norms at 1.8 V or 3.3 V, T_A = 25°C, and at the Recommended Operation Conditions at the time of product characterization and are not verified.

Electrical Characteristics[1][2][3] (continued)

Over recommended operating supply and temperature ranges unless otherwise specified.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CML RECEIVER DC SPECIFICATIONS (RIN0+,RIN0–,RIN1+,RIN1–)						
I_{IN}	Input Current	$V_{IN} = V_{DD}$ or 0 V, V_{DD} = 1.89 V,	–20	1	20	µA
R_T	Differential Internal Termination Resistance	Differential across RIN+ and RIN–	80	100	120	Ω
	Single-ended Termination Resistance	RIN+ or RIN–	40	50	60	
V_{ID}	Differential Input Voltage	Back Channel Disabled, (Figure 3)	210			mV
V_{IN}	Single-Ended Input Voltage	Back Channel Disabled, (Figure 3)	105			mV
f_{BC}	Back Channel Frequency[4]		3.3		4.2	MHz
$V_{OD\text{-}BC}$	Back Channel Differential Output Voltage		350		540	mV
$V_{OUT\text{-}BC}$	Back Channel Single-Ended Output Voltage		182		270	mV
CML MONITOR OUTPUT DRIVER SPECIFICATIONS(CMLOUTP, CMLOUTN)						
E_W	Differential Output Eye Opening[5]	R_L = 100 Ω Jitter Frequency > f/15 (Figure 8)		0.45		UI
E_H	Differential Output Eye Height			200		mV

(4) The back channel frequency (MHz) listed is the frequency of the internal clock used to generate the encoded back channel data stream. The data rate (Mbps) of the encoded back channel stream is the back channel frequency divided by 2.
(5) UI – Unit Interval is equivalent to one ideal serialized data bit width. The UI scales with PCLK frequency.
10-bit mode: 1 UI = 1 / (PCLK_Freq. /2 x 28)
12-bit HF mode: 1 UI = 1 / (PCLK_Freq. x 2/3 x 28)
12-bit LF mode: 1 UI = 1 / (PCLK_Freq. x 28)

Electrical Characteristics[1][2][3] (continued)

Over recommended operating supply and temperature ranges unless otherwise specified.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DESERIALIZER SUPPLY CURRENT							
I_{DDIOR}	Deserializer (Rx) Total Supply Current (includes load current)	V_{DDIO}=1.89 V C_L=8 pF Worst Case Pattern	f = 100 MHz, 10–bit mode		22	42	mA
			f = 75 MHz, 12–bit high freq mode		19	39	
			f = 50 MHz, 12–bit low freq mode		16	32	
		V_{DDIO}=1.89 V C_L=8 pF Random Pattern	f = 100 MHz, 10–bit mode		15		mA
			f = 75 MHz, 12–bit high freq mode		12		
			f = 50 MHz, 12–bit low freq mode		10		
		V_{DDIO}=3.6 V C_L=8 pF Worst Case Pattern	f = 100 MHz, 10–bit mode		42	55	mA
			f = 75 MHz, 12–bit high freq mode		37	50	
			f = 50 MHz, 12–bit low freq mode		25	38	
		V_{DDIO}= 3.6 V C_L= 8 pF Random Pattern	f = 100 MHz, 10–bit mode		35		mA
			f = 75 MHz, 12–bit high freq mode		30		
			f = 50 MHz, 12–bit low freq mode		18		
		V_{DDIO}= 1.89 V C_L= 4 pF Worst Case Pattern	f = 100 MHz, 10–bit mode		15		mA
			f = 75 MHz, 12–bit high freq mode		11		
			f = 50 MHz, 12–bit low freq mode		16		
		V_{DDIO}= 1.89 V C_L= 4 pF Random Pattern	f = 100 MHz, 10–bit mode		8		mA
			f = 75 MHz, 12–bit high freq mode		4		
			f = 50 MHz, 12–bit low freq mode		9		
		V_{DDIO}= 3.6 V C_L= 4 pF Worst Case Pattern	f = 100 MHz, 10–bit mode		36		mA
			f = 75 MHz, 12–bit high freq mode		29		
			f = 50 MHz, 12–bit low freq mode		20		
		V_{DDIO}= 3.6 V C_L= 4 pF Random Pattern	f = 100 MHz, 10–bit mode		29		mA
			f = 75 MHz, 12–bit high freq mode		22		
			f = 50 MHz, 12–bit low freq mode		13		

Electrical Characteristics[1][2][3] (continued)

Over recommended operating supply and temperature ranges unless otherwise specified.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{DDR}	Deserializer (Rx) V_{DD_n} Supply Current (includes load current)	V_{DD_n} = 1.89 V C_L = 4 pF Worst Case Pattern	f = 100 MHz, 10–bit mode		64	110	mA
			f = 75 MHz, 12–bit high freq mode		67	114	
			f = 50 MHz, 12–bit low freq mode		63	96	
		V_{DD_n} = 1.89 V C_L = 4 pF Random Pattern	f = 100 MHz, 10–bit mode		69		
			f = 75 MHz, 12–bit high freq mode		71		
			f = 50 MHz, 12–bit low freq mode		67		
I_{DDRZ}	Deserializer (Rx) Supply Current Power Down	PDB = 0 V, All other LVCMOS Inputs=0 V	V_{DDIO} = 1.89 V Default Registers		42	900	µA
		PDB = 0 V, All other LVCMOS Inputs = 0 V	V_{DDIO}=3.6 V Default Registers		42	900	
I_{DDIORZ}	Deserializer (Rx) V_{DDIO} Supply Current Power Down	PDB = 0 V, All other LVCMOS Inputs = 0 V	V_{DDIO} = 1.89 V		8	40	µA
			V_{DDIO} = 3.6 V		360	800	

7.6 AC Timing Specifications (SCL, SDA) - I2C-Compatible

Over recommended supply and temperature ranges unless otherwise specified. (Figure 1)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
RECOMMENDED INPUT TIMING REQUIREMENTS						
f_{SCL}	SCL Clock Frequency	Standard Mode			100	kHz
		Fast Mode			400	kHz
t_{LOW}	SCL Low Period	Standard Mode	4.7			µs
		Fast Mode	1.3			µs
t_{HIGH}	SCL High Period	Standard Mode	4.0			µs
		Fast Mode	0.6			µs
$t_{HD:STA}$	Hold time for a start or a repeated start condition	Standard Mode	4.0			µs
		Fast Mode	0.6			µs
$t_{SU:STA}$	Set Up time for a start or a repeated start condition	Standard Mode	4.7			µs
		Fast Mode	0.6			µs
$t_{HD:DAT}$	Data Hold Time	Standard Mode	0		3.45	µs
		Fast Mode	0		900	ns
$t_{SU:DAT}$	Data Set Up Time	Standard Mode	250			ns
		Fast Mode	100			ns
$t_{SU:STO}$	Set Up Time for STOP Condition	Standard Mode	4.0			µs
		Fast Mode	0.6			µs
t_{BUF}	Bus Free time between Stop and Start	Standard Mode	4.7			µs
		Fast Mode	1.3			µs
t_r	SCL & SDA Rise Time	Standard Mode			1000	ns
		Fast Mode			300	ns
t_f	SCL & SDA Fall Time	Standard Mode			300	ns
		Fast Mode			300	ns

7.7 Bidirectional Control Bus DC Timing Specifications (SCL, SDA) - I2C-Compatible(1)

Over recommended supply and temperature ranges unless otherwise specified

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
RECOMMENDED INPUT TIMING REQUIREMENTS						
V_{IH}	Input High Level	SDA and SCL	0.7*V_{DDIO}		V_{DDIO}	V
V_{IL}	Input Low Level	SDA and SCL	GND		0.3*V_{DDIO}	V
V_{HY}	Input Hysteresis			>50		mV
V_{OL}	Output Low Level(2)	SDA, V_{DDIO} = 1.8 V, I_{OL}= 0.9 mA	0		0.36	V
		SDA, V_{DDIO} = 3.3 V, I_{OL}= 1.6 mA	0		0.4	
I_{IN}	Input Current	SDA or SCL, V_{IN}= V_{DDIO} OR GND	−10		10	µA
t_R	SDA Rise Time-READ	SDA, RPU = 10 kΩ, Cb ≤ 400 pF (Figure 1)		430		ns
t_F	SDA Fall Time-READ			20		ns
t_{SP}				50		ns
C_{IN}		SDA or SCL		<5		pF

(1) Specification is verified by design.
(2) FPD-Link device was designed primarily for point-to-point operation and a small number of attached slave devices. As such the Minimum I_{OL} pullup current is targeted to lower value than the minimum I_{OL} in the I2C specification.

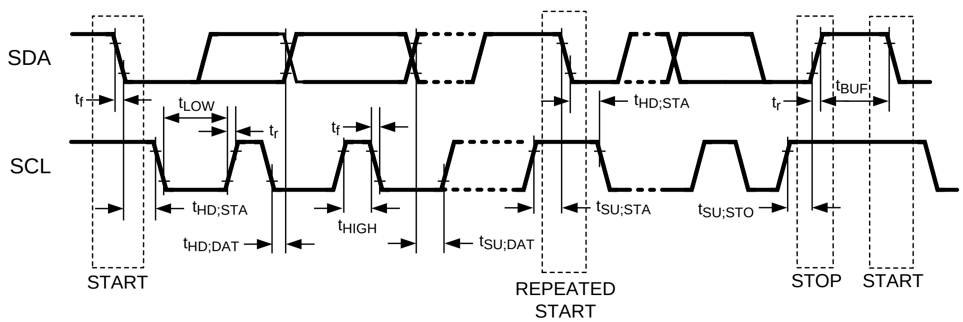


Figure 1. Bi-directional Control Bus Timing

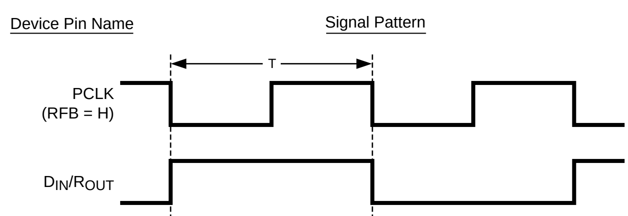


Figure 2. “Worst Case” Test Pattern for Power Consumption

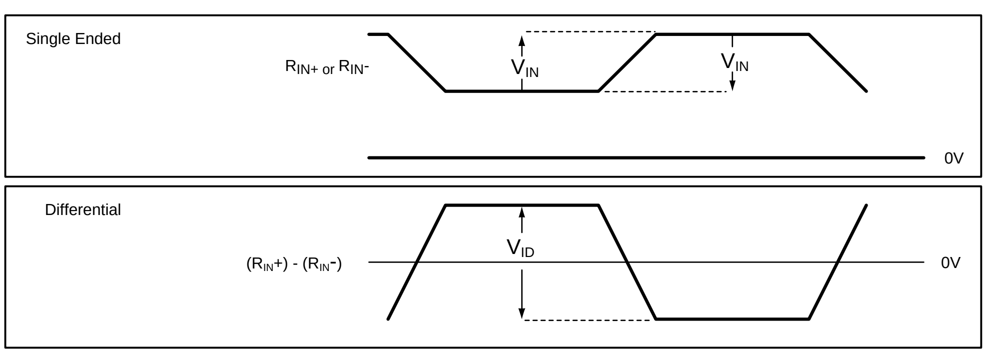


Figure 3. Deserializer VID Diagram

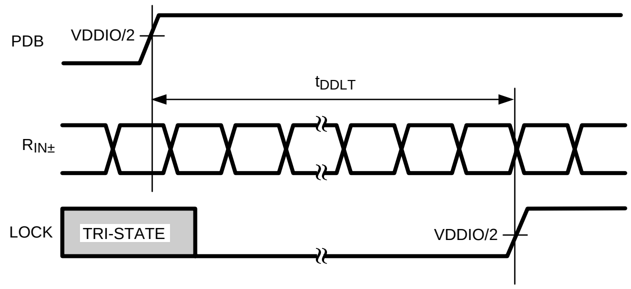


Figure 4. Deserializer Data Lock Time

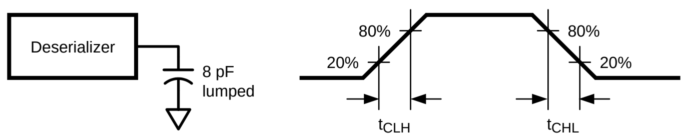


Figure 5. Deserializer LVCMOS Output Load and Transition Times

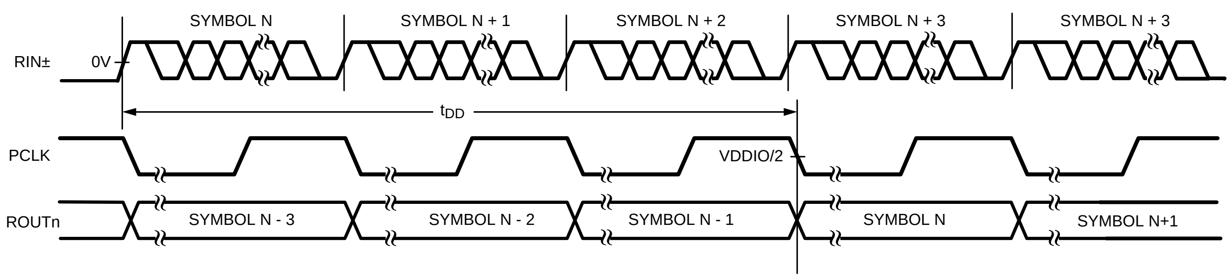


Figure 6. Deserializer Delay

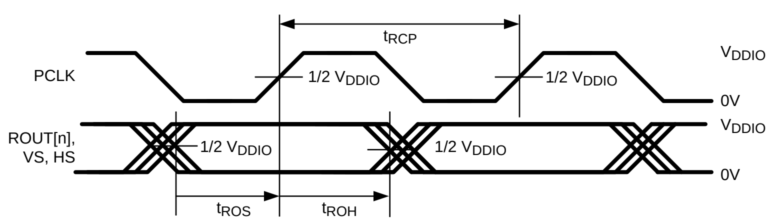


Figure 7. Deserializer Output Setup/Hold Times

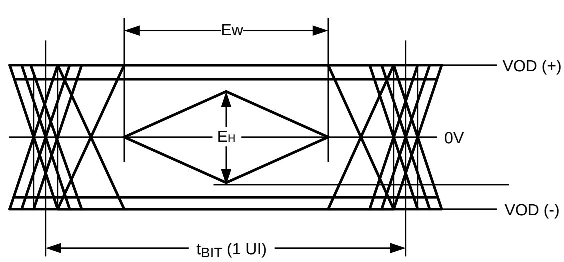


Figure 8. CML Output Driver

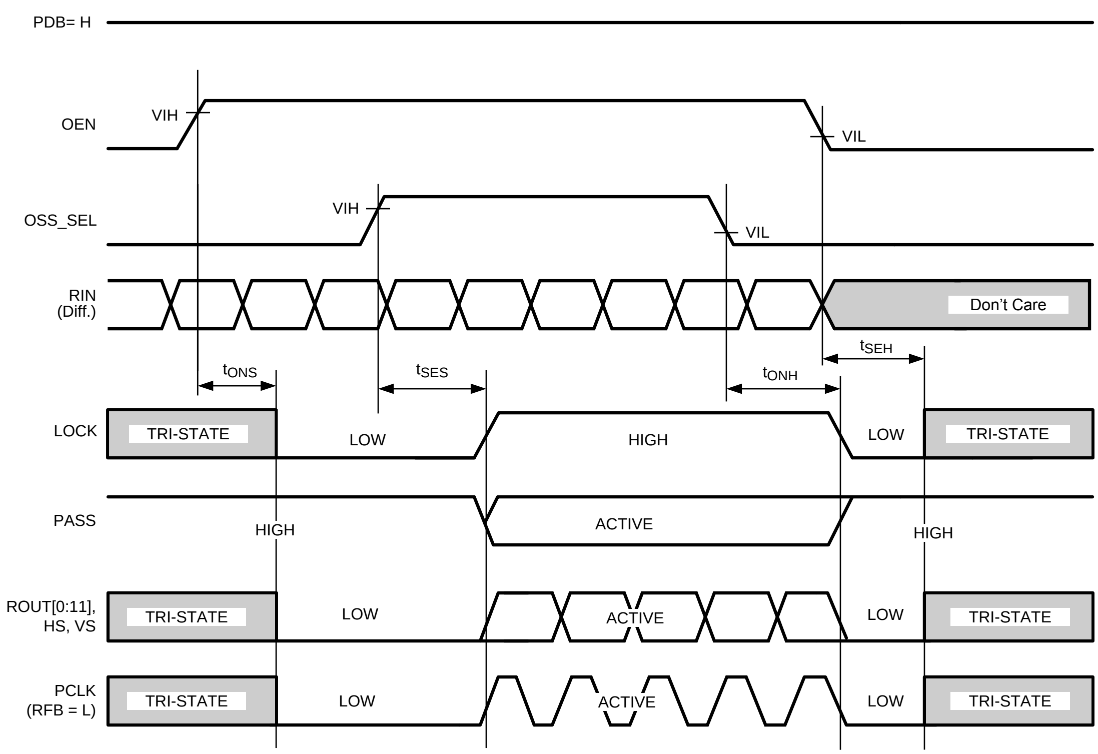


Figure 9. Output State (Setup and Hold) Times

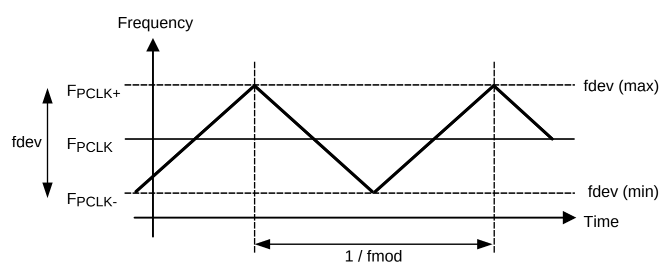


Figure 10. Spread Spectrum Clock Output Profile

7.8 Deserializer Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

PARAMETER		TEST CONDITIONS	PIN / FREQ	MIN	NOM	MAX	UNIT
t_{RCP}	Receiver Output Clock Period(1)	10-bit mode 50 MHz – 100 MHz	PCLK (Figure 7)	10	T	20	ns
		12-bit high frequency mode 37.5 MHz - 75MHz		13.33	T	26.67	
		12-bit low frequency mode 25 MHz - 50MHz		20	T	40	
t_{PDC}	PCLK Duty Cycle	10-bit mode 50 MHz – 100 MHz	PCLK	45%	50%	55%	
		12-bit high frequency mode 37.5 MHz - 75MHz		40%	50%	60%	
		12-bit low frequency mode 25 MHz - 50MHz		40%	50%	60%	

(1) T is the period of the PCLK.

Deserializer Switching Characteristics (continued)

Over recommended operating supply and temperature ranges unless otherwise specified.

PARAMETER		TEST CONDITIONS	PIN / FREQ	MIN	NOM	MAX	UNIT
t_{CLH}	LVCMOS Low-to-High Transition Time	V_{DDIO}: 1.71 V to 1.89 V or 3 V to 3.6 V, C_L = 8 pF (lumped load) Default Registers (Figure 5)(2)	PCLK	1.3	2	2.8	ns
t_{CHL}	LVCMOS High-to-Low Transition Time			1.3	2	2.8	
t_{CLH}	LVCMOS Low-to-High Transition Time	V_{DDIO}: 1.71 V to 1.89 V or 3 V to 3.6 V, C_L = 8 pF (lumped load) Default Registers (Figure 5)(2)	ROUT[11:0], HS, VS	1	2.5	4	ns
t_{CHL}	LVCMOS High-to-Low Transition Time			1	2.5	4	
t_{ROS}	ROUT Setup Data to PCLK (1)	V_{DDIO}: 1.71 V to 1.89 V or 3 V to 3.6 V, C_L = 8 pF (lumped load), Default Registers (Figure 7)	ROUT[11:0], HS, VS	0.38T	0.5T		
t_{ROH}	ROUT Hold Data to PCLK (1)			0.38T	0.5T		
t_{DD}	Deserializer Delay(1)	Default Registers Register 0x03h b[0] (RRFB = 1) (Figure 6)(2)	10–bit mode 50 - 100 MHz	154T		158T	
			12–bit low frequency mode 25 - 50 MHz	73T		75T	
			12–bit high frequency mode 37.5 - 75 MHz	109T		112T	
t_{DDLT}	Deserializer Data Lock Time	With Adaptive Equalization (Figure 4)	10–bit mode 50 - 100 MHz		15	22	ms
			12–bit low frequency mode 25 - 50 MHz		15	22	
			12–bit high frequency mode 37.5 - 75 MHz		15	22	
t_{RCJ}	Receiver Clock Jitter	PCLK SSCG[3:0] = OFF(2)	10–bit mode PCLK = 100 MHz		20	30	ps
			12–bit low frequency mode, PCLK = 50 MHz		22	35	
			12–bit high frequency mode, PCLK = 75 MHz		45	90	
t_{DPJ}	Deserializer Period Jitter	PCLK SSCG[3:0] = OFF(2) (3)	10–bit mode PCLK = 100 MHz		170	815	ps
			12–bit low frequency mode, PCLK = 50 MHz		180	330	
			12–bit high frequency mode, PCLK = 75 MHz		300	515	
t_{DCCJ}	Deserializer Cycle-to-Cycle Clock Jitter	PCLK SSCG[3:0] = OFF(2) (4)	10–bit mode PCLK = 100 MHz		440	1760	ps
			12–bit low frequency mode, PCLK = 50 MHz		460	730	
			12–bit high frequency mode, PCLK = 75 MHz		565	985	
f_{dev}	Spread Spectrum Clocking Deviation Frequency	LVCMOS Output Bus SSC[3:0] = ON (Figure 10)(2)	25 MHz – 100 MHz		±0.5% to ±1.5%		
f_{mod}	Spread Spectrum Clocking Modulation Frequency		25 MHz – 100 MHz		5 to 50		kHz

(2) Specification is verified by characterization and is not tested in production.
(3) t_{DPJ} is the maximum amount of jitter measured over 30,000 samples based on Time Interval Error (TIE).
(4) t_{DCCJ} is the maximum amount of jitter between adjacent clock cycles measured over 30,000 samples.

7.9 Typical Characteristics

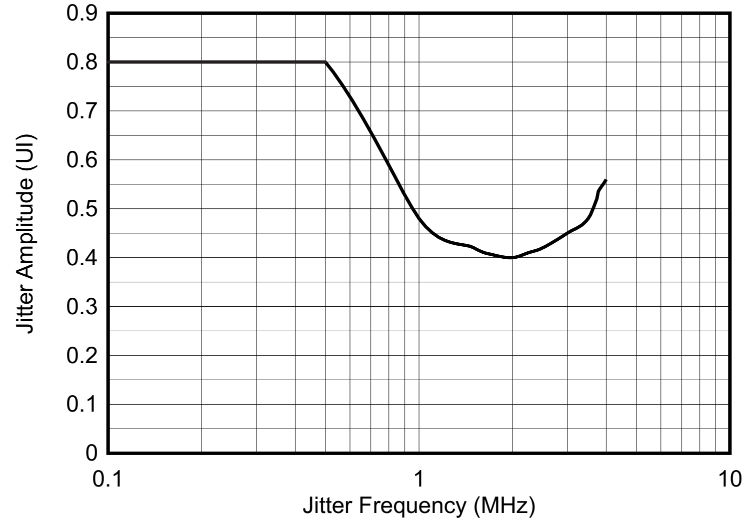


Figure 11. Typical System Input Jitter Tolerance Curve - DS90UB913A Linked to DS90UB914A

8 Detailed Description

8.1 Overview

The DS90UB913A-Q1 is optimized to interface with the DS90UB914A-Q1 using a 50-Ω coax interface. The DS90UB913A-Q1 will also work with the DS90UB914A-Q1 using an STP interface.

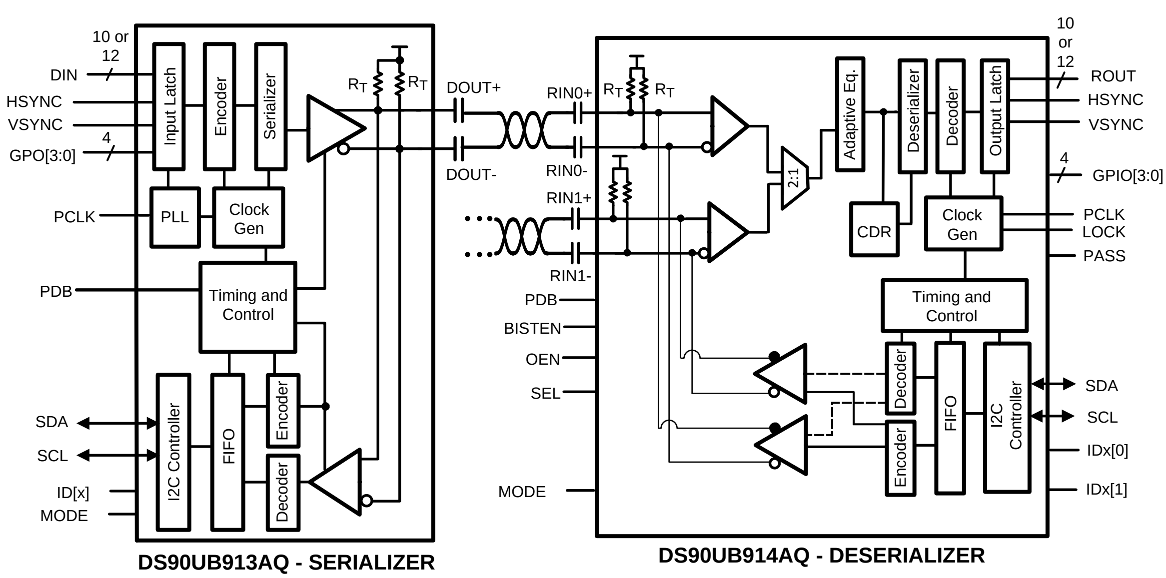
The DS90UB913A/914A FPD- Link III chipsets are intended to link mega-pixel camera imagers and video processors in ECUs. The Serializer/Deserializer chipset can operate from 25 MHz to 100 MHz pixel clock frequency. The DS90UB913A-Q1 device transforms a 10/12-bit wide parallel LVCMOS data bus along with a bidirectional control channel control bus into a single high-speed differential pair. The high speed serial bit stream contains an embedded clock and DC-balanced information which enhances signal quality to support AC coupling. The DS90UB914A-Q1 device receives the single serial data stream and converts it back into a 10/12-bit wide parallel data bus together with the control channel data bus. The DS90UB913A/914A chipsets can accept up to:

- 12-bits of DATA + 2 bits SYNC for an input PCLK range of 25 MHz to 50 MHz in the 12-bit low frequency mode. Note: No HS/VS restrictions (raw).
- 12-bits of DATA + 2 SYNC bits for an input PCLK range of 37.5 MHz to 75 MHz in the 12-bit high frequency mode. Note: No HS/VS restrictions (raw).
- 10-bits of DATA + 2 SYNC bits for an input PCLK range of 50 MHz to 100 MHz in the 10-bit mode. Note: HS/VS restricted to no more than one transition per 10 PCLK cycles.

The DS90UB914A-Q1 device has a 2:1 multiplexer which allows customers to select between two Serializer inputs. The control channel function of the DS90UB913A/DS90UB914A-Q1 chipset provides bidirectional communication between the image sensor and ECUs. The integrated bidirectional control channel transfers data bidirectionally over the same differential pair used for video data interface. This interface offers advantages over other chipsets by eliminating the need for additional wires for programming and control. The bidirectional control channel bus is controlled via an I2C port. The bidirectional control channel offers asymmetrical communication and is not dependent on video blanking intervals.

The DS90UB913A/914A chipset offer customers the choice to work with different clocking schemes. The DS90UB913A/914A chipsets can use an external oscillator as the reference clock source for the PLL (see section *DS90UB913A/914A Operation with External Oscillator as Reference Clock*) or PCLK from the imager as primary reference clock to the PLL (see section *DS90UB913A/914A Operation with Pixel Clock from Imager as Reference Clock*).

8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 Serial Frame Format

The High Speed Forward Channel is composed of 28 bits of data containing video data, sync signals, I2C and parity bits. This data payload is optimized for signal transmission over an AC-coupled link. Data is randomized, balanced and scrambled. The 28-bit frame structure changes in the 12-bit low frequency mode, 12-bit high frequency mode and the 10-bit mode internally and is seamless to the customer. The bidirectional control channel data is transferred over the single serial link along with the high-speed forward data. This architecture provides a full duplex low speed forward and backward path across the serial link together with a high speed forward channel without the dependence on the video blanking phase.

8.3.2 Line Rate Calculations for the DS90UB913A/914A

The DS90UB913A-Q1 device divides the clock internally by divide-by-1 in the 12-bit low frequency mode, by divide-by-2 in the 10-bit mode and by divide-by-1.5 in the 12-bit high frequency mode. Conversely, the DS90UB914A-Q1 multiplies the recovered serial clock to generate the proper pixel clock output frequency. Thus the maximum line rate in the three different modes remains 1.4 Gbps. The following are the formulae used to calculate the maximum line rate in the different modes:

- For the 12-bit low frequency mode, Line rate = f_{PCLK}*28; for example, f_{PCLK} = 50 MHz, line rate = 50*28 = 1.4 Gbps
- For the 12-bit high frequency mode, Line rate = f_{PCLK}*(2/3)*28; for example, f_{PCLK} = 75 MHz, line rate = (75)*(2/3)*28 = 1.4 Gbps
- For the 10-bit mode, Line rate = f_{PCLK}/2*28; for example, f_{PCLK} = 100 MHz, line rate = (100/2)*28 = 1.4 Gbps

8.3.3 Deserializer Multiplexer Input

The DS90UB914A-Q1 offers a 2:1 multiplexer that can be used to select which camera is used as the input. Figure 12 shows the operation of the 2:1 multiplexer in the Deserializer. The selection of the camera can be pin controlled as well as register controlled. Both the Deserializer inputs cannot be enabled at the same time. If the Serializer A is selected as the active Serializer, the back-channel for Deserializer A turns ON and vice versa. To switch between the two cameras, first the Serializer B has to be selected using the SEL pin/register on the Deserializer. After that the back channel driver for Deserializer B has to be enabled using the register in the Deserializer.

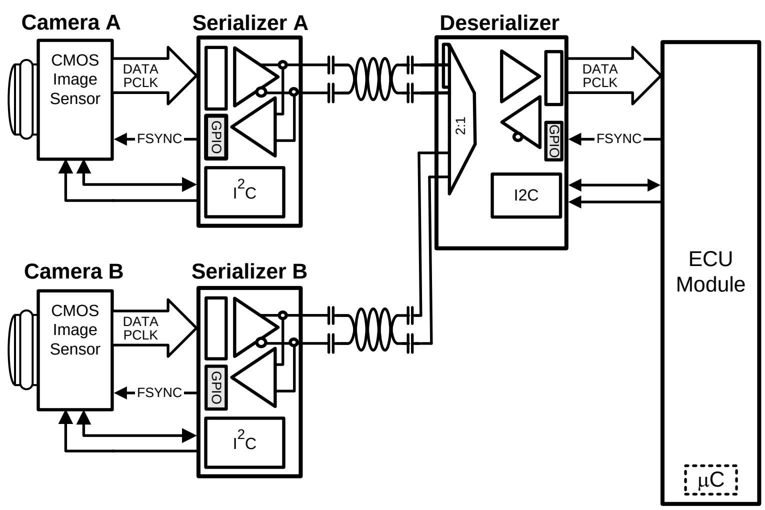

Figure 12. Using the Multiplexer on the Deserializer to Enable a Two-Camera System

Feature Description (continued)

8.3.4 Error Detection

The chipset provides error detection operations for validating data integrity in long distance transmission and reception. The data error detection function offers users flexibility and usability of performing bit-by-bit data transmission error checking. The error detection operating modes support data validation of the following signals:

- Bidirectional control channel data across the serial link
- Parallel video/sync data across the serial link

The chipset provides 1 parity bit on the forward channel and 4 cyclic redundancy check (CRC) bits on the back channel for error detection purposes. The DS90UB913A/914A chipset checks the forward and back channel serial links for errors and stores the number of detected errors in two 8-bit registers in the Serializer and the Deserializer respectively.

To check parity errors on the forward channel, monitor registers 0x1A and 0x1B on the Deserializer. If there is a loss of LOCK, then the counters on registers 0x1A and 0x1B are reset. ***Whenever there is a parity error on the forward channel, the PASS pin will go low.***

To check CRC errors on the back-channel, monitor registers 0x0A and 0x0B on the Serializer.

8.3.5 Synchronizing Multiple Cameras

For applications requiring multiple cameras for frame-synchronization, it is recommended to utilize the General Purpose Input/Output (GPIO) pins to transmit control signals to synchronize multiple cameras together. To synchronize the cameras properly, the system controller needs to provide a field sync output (such as a vertical or frame sync signal) and the cameras must be set to accept an auxiliary sync input. The vertical synchronize signal corresponds to the start and end of a frame and the start and end of a field. Note this form of synchronization timing relationship has a non-deterministic latency. After the control data is reconstructed from the bidirectional control channel, there will be a time variation of the GPIO signals arriving at the different target devices (between the parallel links). The maximum latency delta (t1) of the GPIO data transmitted across multiple links is 25 µs.

NOTE

The user must verify that the timing variations between the different links are within their system and timing specifications.

See Figure 13 for an example of this function.

The maximum time (t1) between the rising edge of GPIO (that is, sync signal) to the time the signal arrives at Camera A and Camera B is 25 µs.

Feature Description (continued)

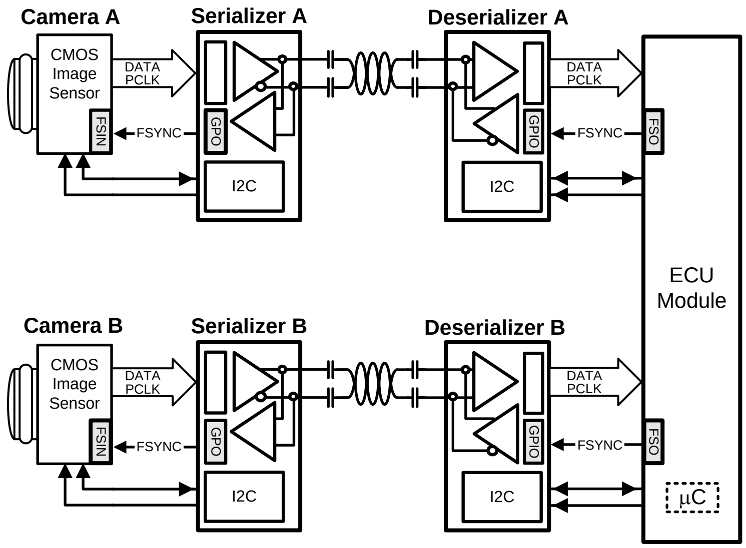

Figure 13. Synchronizing Multiple Cameras

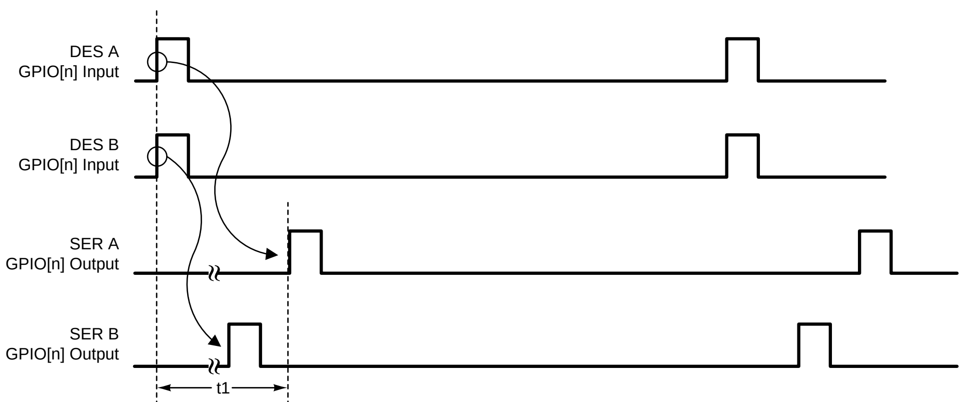

Figure 14. GPIO Delta Latency

8.3.6 General Purpose I/O (GPIO) Descriptions

There are 4 GPOs on the Serializer and 4 GPIOs on the Deserializer when the DS90UB913A/914A chipsets are run off the pixel clock from the imager as the reference clock source. The GPOs on the Serializer can be configured as outputs for the input signals that are fed into the Deserializer GPIOs. In addition, the GPOs on the Serializer can behave as outputs of the local register on the Serializer. The GPIOs on the Deserializer can be configured to be the input signals feeding the GPOs (configured as outputs) on the Serializer. In addition the GPIOs on the Deserializer can be configured to behave as outputs of the local register on the Deserializer. The DS90UB913A Serializer GPOs cannot be configured as inputs for remote communication with Deserializer. If the DS90UB913A/914A chipsets are run off the external oscillator source as the reference clock, then GPO3 on the Serializer is automatically configured to be the input for the external clock and GPO2 is configured to be the output of the divide-by-2 clock which is fed into the imager as its reference clock. In this case, the GPIO2 and GPIO3 on the Deserializer can only behave as outputs of the local register on the Deserializer. The GPIO maximum switching rate is up to 66 kHz when configured for communication between Deserializer GPIO to Serializer GPO.

Feature Description (continued)

8.3.7 LVCMOS V_{DDIO} Option

1.8 V/3.3 V Deserializer outputs are user configurable to provide compatibility with 1.8 V and 3.3 V system interfaces.

8.3.8 EMI Reduction

8.3.8.1 Deserializer Staggered Output

The receiver staggers output switching to provide a random distribution of transitions within a defined window. Outputs transitions are distributed randomly. This minimizes the number of outputs switching simultaneously and helps to reduce supply noise. In addition it spreads the noise spectrum out reducing overall EMI.

8.3.8.2 Spread Spectrum Clock Generation (SSCG) on the Deserializer

The DS90UB914A-Q1 parallel data and clock outputs have programmable SSCG ranges from 25 MHz to 100 MHz. The modulation rate and modulation frequency variation of output spread is controlled through the SSCG control registers on the DS90UB914A-Q1 device. SSCG profiles can be generated using bits [3:0] in register 0x02 on the Deserializer.

8.3.9 Pixel Clock Edge Select (TRFB / RRFB)

The TRFB/RRFB selects which edge of the Pixel Clock is used. For the SER, this register determines the edge that the data is latched on. If TRFB register is 1, data is latched on the Rising edge of the PCLK. If TRFB register is 0, data is latched on the Falling edge of the PCLK. For the DES, this register determines the edge that the data is strobed on. If RRFB register is 1, data is strobed on the Rising edge of the PCLK. If RRFB register is 0, data is strobed on the falling edge of the PCLK.

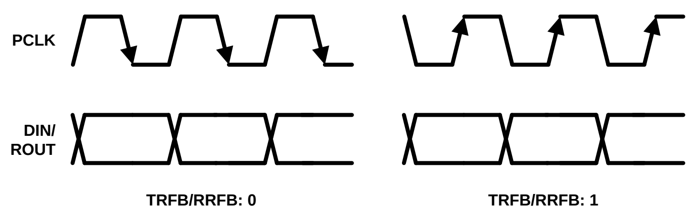

Figure 15. Programmable PCLK Strobe Select

8.3.10 Power Down

The DES has a PDB input pin to ENABLE or power down the device. Enabling PDB on the DES will disable the link to save power. If PDB = HIGH, the DES locks to the input stream and assert the LOCK pin (HIGH) and output valid data. When PDB = LOW, all outputs are in TRI-STATE. Please refer to *Power-Up Requirements and PDB Pin* for power-up requirements.

8.4 Device Functional Modes

8.4.1 DS90UB913A/914A Operation with External Oscillator as Reference Clock

In some applications, the pixel clock that comes from the imager can have jitter which exceeds the tolerance of the DS90UB913A/914A chipsets. In this case, the DS90UB913A-Q1 device should be operated by using an external clock source as the reference clock for the DS90UB913A/914A chipsets. **This is the recommended operating mode.** The external oscillator clock output goes through a divide-by-2 circuit in the DS90UB913A-Q1 Serializer and this divided clock output is used as the reference clock for the imager. The output data and pixel clock from the imager are then fed into the DS90UB913A-Q1 device. Figure 16 shows the operation of the DS90UB13A/914A chipsets while using an external automotive grade oscillator.

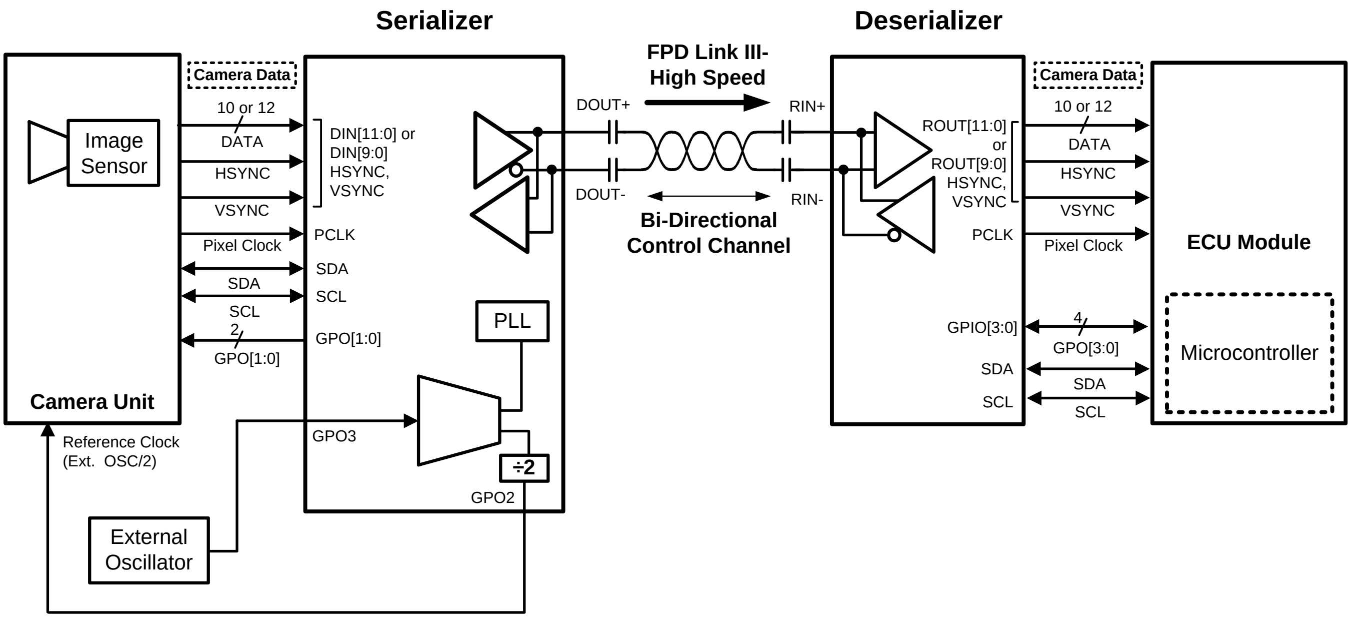

Figure 16. DS90UB913A-Q1/914A-Q1 Operation in the External Oscillator Mode

When the DS90UB913A-Q1 device is operated using an external oscillator, the GPO3 pin on the DS90UB913A-Q1 is the input pin for the external oscillator. In applications where the DS90UB913A-Q1 device is operated from an external oscillator, the divide-by-2 circuit in the DS90UB913A-Q1 device feeds back the divided clock output to the imager device through GPO2 pin. The pixel clock to external oscillator ratios needs to be fixed for the 12–bit high frequency mode and the 10–bit mode. **In the 10-bit mode, the pixel clock frequency divided by the external oscillator frequency must be 2. In the 12-bit high frequency mode, the pixel clock frequency divided by the external oscillator frequency must be 1.5.** For example, if the external oscillator frequency is 48 MHz in the 10–bit mode, the pixel clock frequency of the imager needs to be twice of the external oscillator frequency, that is, 96 MHz. If the external oscillator frequency is 48MHz in the 12-bit high frequency mode, the pixel clock frequency of the imager needs to be 1.5 times of the external oscillator frequency, that is, 72 MHz. In external oscillator mode, GPO2 and GPO3 on the Serializer cannot act as the output of the input signal coming from GPIO2 or GPIO3 on the Deserializer.

Table 1. Device Functional Mode w/ Example XCLKIN = 48 MHz

MODE	GPIO3 XCLKIN	GPIO2 XCLKOUT = XCLKIN / 2	Ratio	Input PCLK Frequency = XLCKIN * Ratio
10-bit	48 MHz	24 MHz	2	96 MHz
12-bit High Frequency (HF)	48 MHz	24 MHz	1.5	72 MHz
12-bit Low Frequency (LF)	48 MHz	24 MHz	1	48 MHz

8.4.2 DS90UB913A/914A Operation with Pixel Clock from Imager as Reference Clock

The DS90UB913A/914A chipsets can be operated by using the pixel clock from the imager as the reference clock. Figure 17 shows the operation of the DS90UB913A/914A chipsets using the pixel clock from the imager. If the DS90UB913A-Q1 device is operated using the pixel clock from the imager as the reference clock, then the imager uses an external oscillator as its reference clock. There are 4 GPIOs available in this mode (PCLK from imager mode).

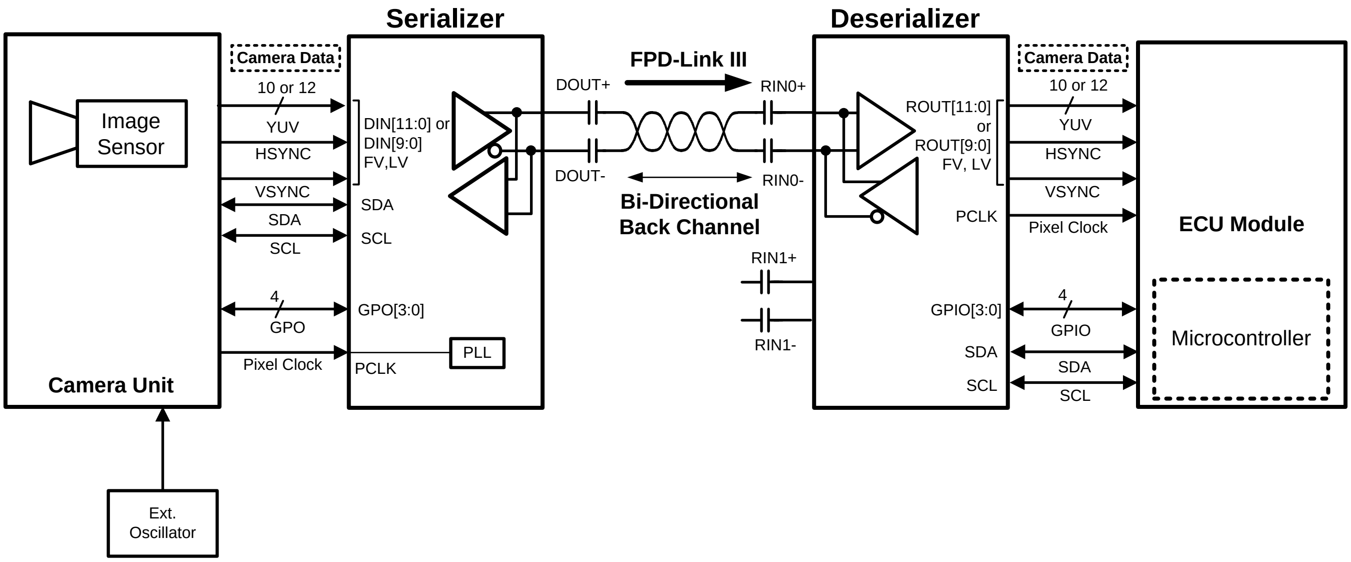

Figure 17. DS90UB913A-Q1/914A-Q1 Operation in PCLK mode

8.4.3 MODE Pin on Deserializer

The MODE pin on the Deserializer can be used to configure the device to work in the 12-bit low-frequency mode, 12-bit high-frequency mode, or the 10-bit mode of operation. Internally, the DS90UB913A/914A chipset operates in a divide-by-1 mode in the 12-bit low-frequency mode, divide-by-2 mode in the 10-bit mode and a divide-by-1.5 mode in the 12-bit high frequency mode. The pin must be pulled to V_{DD} (1.8 V, not V_{DDIO}) with a 10-kΩ resistor and a pull-down resistor R_{MODE} of the recommended value to set the different modes in the Deserializer as mentioned in Table 2. The Deserializer automatically configures the Serializer to correct mode via the back-channel. The recommended maximum resistor tolerance is 1%.

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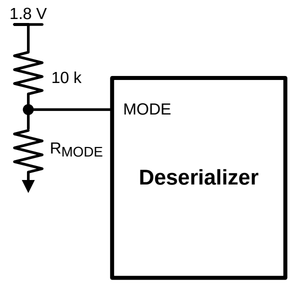


Figure 18. Mode Pin Configuration on DS90UB914A-Q1 Deserializer

Table 2. DS90UB914A-Q1 Deserializer MODE Resistor Value

DS90UB914A-Q1 DESERIALIZER MODE RESISTOR VALUE	
MODE SELECT	**R_{MODE} RESISTOR VALUE (kΩ)**
12-bit low frequency mode 25-50 MHz PCLK, 10/12-bits DATA+ 2 SYNC. Note: No HS/VS restrictions (raw).	0
12-bit high frequency mode 37.5-75 MHz PCLK, 10/12-bits DATA+ 2 SYNC. Note: No HS/VS restrictions (raw).	3
10-bit mode 50–100 MHz PCLK, 10-bits DATA+ 2 SYNC. Note: HS/VS restricted to no more than one transition per 10 PCLK cycles.	11

8.4.4 Clock-Data Recovery Status Flag (LOCK), Output Enable (OEN) and Output State Select (OSS_SEL)

When PDB is driven HIGH, the Deserializer's CDR PLL begins locking to the serial input and LOCK is TRI-STATE or LOW (depending on the value of the OEN setting). After the DS90UB914A-Q1 completes its lock sequence to the input serial data, the LOCK output is driven HIGH, indicating valid data and clock recovered from the serial input is available on the parallel bus and PCLK outputs. The states of the outputs are based on the OEN and OSS_SEL setting (Table 3). See Figure 9.

Table 3. Output States

INPUTS				OUTPUTS			
SERIAL INPUTS	PDB	OEN	OSS_SEL	LOCK	PASS	DATA, GPIO	CLK
X	0	X	X	Z	Z	Z	Z
X	1	0	0	L or H	L	L	L
X	1	0	1	L or H	Z	Z	Z
Static	1	1	0	L	L	L	L/Osc (Register Bit Enable)
Static	1	1	1	L	Previous State	L	L
Active	1	1	0	H	L	L	L
Active	1	1	1	H	Valid	Valid	Valid

8.4.5 Built In Self Test

An optional At-Speed Built In Self Test (BIST) feature supports the testing of the high-speed serial link and low-speed back channel. This is useful in the prototype stage, equipment production, and in-system test and also for system diagnostics.

8.4.6 BIST Configuration and Status

The chipset can be programmed into BIST mode using either pins or registers on the DES only. By default, BIST configuration is controlled through pins. BIST can be configured via registers using BIST Control register (0x24). Pin-based configuration is defined as follows:

- BISTEN = HIGH: Enable the BIST mode, BISTEN = LOW: Disable the BIST mode.
- Deserializer GPIO0 and GPIO1: Defines the BIST clock source (PCLK vs. various frequencies of internal OSC)

Table 4. BIST Pin Configuration

DESERIALIZER GPIO[0:1]	OSCILLATOR SOURCE	BIST FREQUENCY
00	External PCLK	PCLK or External Oscillator
01	Internal	~50 MHz
10	Internal	~25 MHz

Table 5. BIST Register Configuration

DS90UB914A-Q1 Reg 0x24 [2:1]	10–BIT MODE	12–BIT HIGH-FREQUENCY MODE	12–BIT LOW-FREQUENCY MODE
00	PCLK	PCLK	PCLK
01	100 MHz	75 MHz	50 MHz
10	50 MHz	37.5 MHz	25 MHz
11	Reserved	Reserved	Reserved

BIST mode provides various options for the PCLK source. Either external pins (GPIO0 and GPIO1) or registers can be used to program the BIST to use external PCLK or various OSC frequencies. Refer to Table 4 for pin settings and refer to Table 7 for register settings. The BIST status can be monitored real-time on the PASS pin. For every frame with error(s), the PASS pin toggles low for one-half PCLK period. If two consecutive frames have errors, PASS will toggle twice to allow counting of frames with errors. Once the BIST is done, the PASS pin reflects the pass/fail status of the last BIST run only for one PCLK cycle. The status can also be read through I2C for the number of frames in errors. BIST status register retains results until it is reset by a new BIST session or a device reset. To evaluate BIST in external oscillator mode, both the external oscillator and PCLK need to be present. For all practical purposes, the BIST status can be monitored from the BIST Error Count register 0x25 on the DS90UB914A Deserializer.

8.4.7 Sample BIST Sequence

Step 1. For the DS90UB913A/914A FPD-Link III chipset, BIST Mode is enabled via the BISTEN pin of DS90UB914A-Q1 FPD-Link III deserializer. The desired clock source is selected through the deserializer GPIO0 and GPIO1 pins as shown in Table 4.

Step 2. The DS90UB913A-Q1 Serializer BIST pattern is enabled through the back channel. The BIST pattern is sent through the FPD-Link III to the deserializer. Once the serializer and deserializer are in the BIST mode and the deserializer acquires Lock, the PASS pin of the deserializer goes high and BIST starts checking FPD-Link III serial stream. If an error in the payload is detected, the PASS pin will switch low for one half of the clock period. During the BIST test, the PASS output can be monitored and counted to determine the payload error rate.

Step 3. To stop the BIST mode, the deserializer BISTEN pin is set LOW. The deserializer stops checking the data. The final test result is not maintained on the PASS pin. To monitor the BIST status, check the BIST Error Count register, 0x25 on the Deserializer.

Step 4. The link returns to normal operation after the deserializer BISTEN pin is low. Figure 20 shows the waveform diagram of a typical BIST test for two cases. Case 1 is error free, and Case 2 shows one with multiple errors. In most cases, it is difficult to generate errors due to the robustness of the link (differential data transmission etc.), thus they may be introduced by greatly extending the cable length, faulting the interconnect, or by reducing signal condition enhancements (Rx equalization).

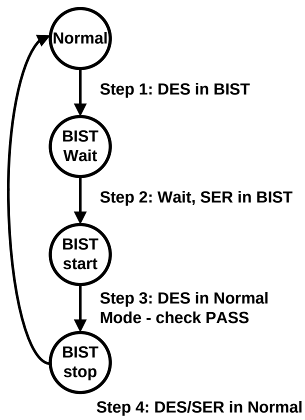


Figure 19. AT-Speed BIST System Flow Diagram

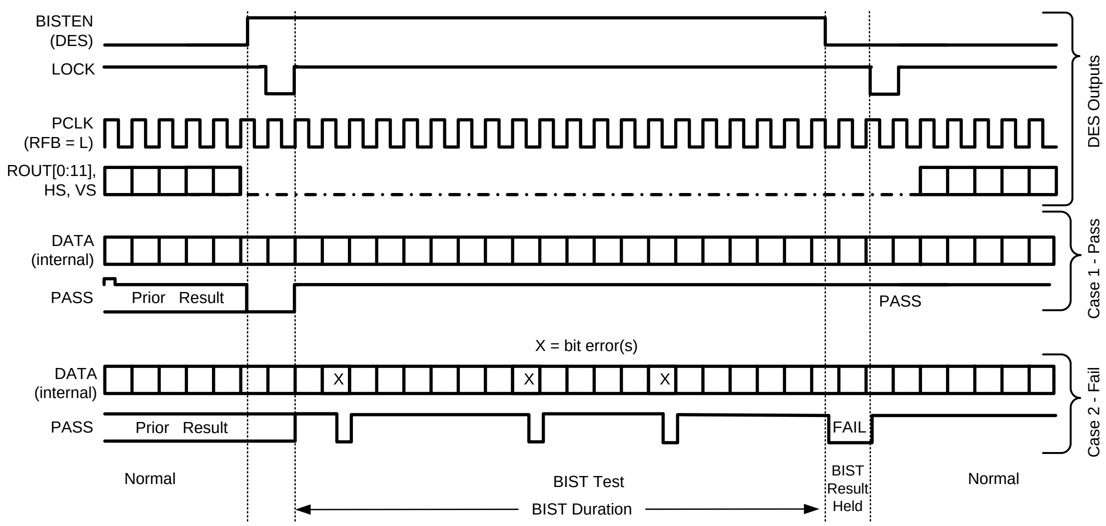


Figure 20. BIST Timing Diagram

8.5 Programming

8.5.1 Programmable Controller

An integrated I2C slave controller is embedded in the DS90UB914A-Q1 Deserializer. It must be used to configure the extra features embedded within the programmable registers or it can be used to control the set of programmable GPIOs.

8.5.2 Description of Bidirectional Control Bus and I2C Modes

The I2C-compatible interface allows programming of the DS90UB913A-Q1, DS90UB914A-Q1, or an external remote device (such as image sensor) through the bidirectional control channel. Register programming transactions to/from the DS90UB913A-Q1/914A-Q1 chipset are employed through the clock (SCL) and data (SDA) lines. These two signals have open drain I/Os and both lines must be pulled-up to V_{DDIO} by an external resistor. Pullup resistors or current sources are required on the SCL and SDA busses to pull them high when they are not being driven low. A logic LOW is transmitted by driving the output low. Logic HIGH is transmitted by releasing the output and allowing it to be pulled-up externally. The appropriate pullup resistor values will depend upon the total bus capacitance and operating speed. The DS90UB913A/914A I2C bus data rate supports up to 400 kbps according to I2C fast mode specifications.

For further description of general I2C communication, please refer to application note *Understanding the I2C Bus* (SLVA704). For more information on choosing appropriate pullup resistor values, please refer to application note *I2C Bus Pullup Resistor Calculation* (SLVA689).

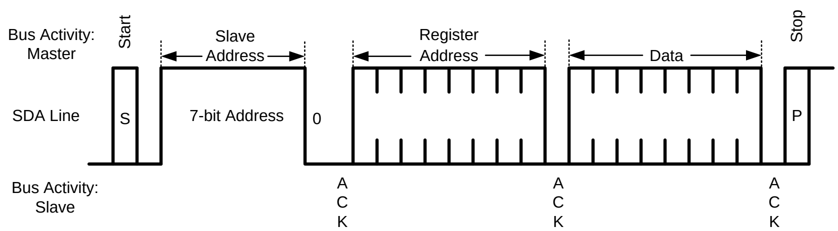


Figure 21. Write Byte

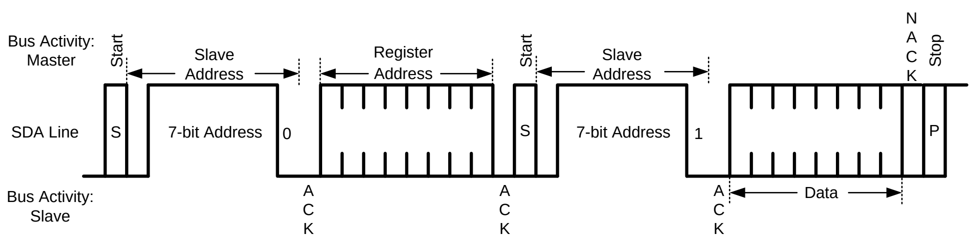


Figure 22. Read Byte

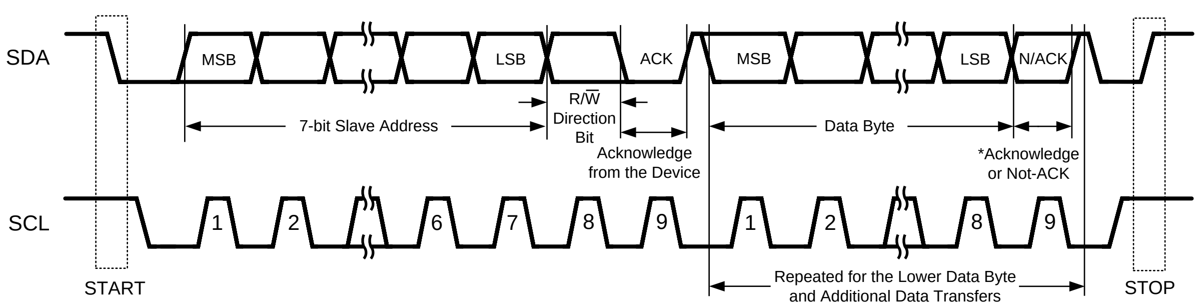


Figure 23. Basic Operation

Programming (continued)

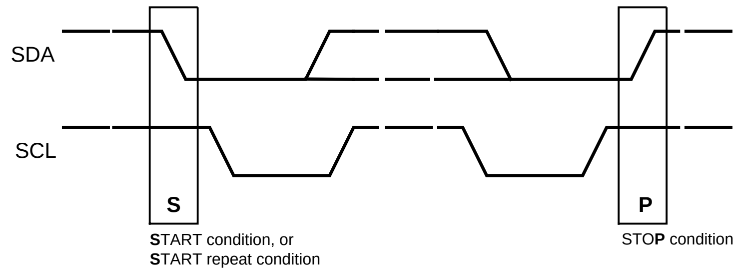


Figure 24. Start and Stop Conditions

8.5.3 I2C Pass-Through

I2C pass-through provides a way to access remote devices at the other end of the FPD-Link III interface. This option is used to determine if an I2C instruction is transferred over to the remote I2C bus. For example, when the I2C master is connected to the deserializer and I2C pass-through is enabled on the deserializer, any I2C traffic targeted for the remote serializer or remote slave will be allowed to pass through the deserializer to reach those respective devices.

See Figure 25 for an example of this function and refer to application note: *I2C over DS90UB913/4 FPD-Link III with Bidirectional Control Channel* (SNLA222).

If master controller transmits I2C transaction for address 0xA0, the DES A with I2C pass-through enabled will transfer I2C commands to remote Camera A. The DES B with I2C pass-through disabled, any I2C commands will NOT be passed on the I2C bus to Camera B.

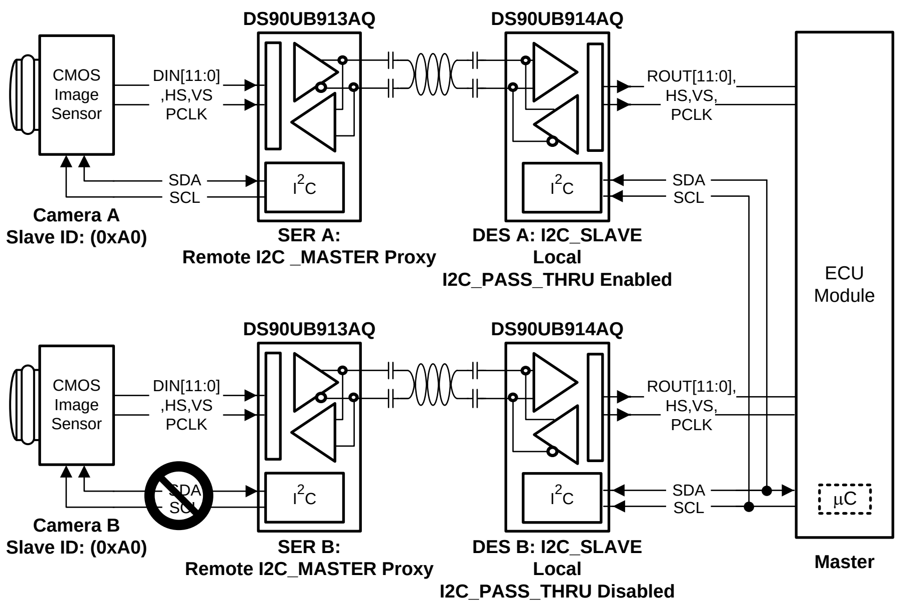


Figure 25. I2C Pass-Through

Programming (continued)

8.5.4 Slave Clock Stretching

The I2C-compatible interface allows programming of the DS90UB913A-Q1, DS90UB914A-Q1, or an external remote device (such as image sensor) through the bidirectional control. To communicate and synchronize with remote devices on the I2C bus through the bidirectional control channel/MCU, **the chipset utilizes bus clock stretching (holding the SCL line low) during data transmission**; where the I2C slave pulls the SCL line low on the 9th clock of every I2C transfer (before the ACK signal). The slave device will not control the clock and only stretches it until the remote peripheral has responded. The I2C master must support clock stretching to operate with the DS90UB913A/914A chipset.

8.5.5 ID[x] Address Decoder on the Deserializer

The IDx[0] and IDx[1] pins on the Deserializer are used to decode and set the physical slave address of the Deserializer (I2C only) to allow up to 16 devices on the bus using only two pins. The pins set one of 16 possible addresses for each Deserializer device. As there will be more Deserializer devices connected on the same board than Serializers, more I2C device addresses have been defined for the DS90UB914A-Q1 Deserializer than the DSDS90UB913A-Q1 Serializer. The pins must be pulled to V_{DD} (1.8 V, not V_{DDIO}) with a 10-kΩ resistor and two pulldown resistors (R_{ID0} and R_{ID1}) of the recommended value to set the physical device address. The recommended maximum resistor tolerance is 1%.

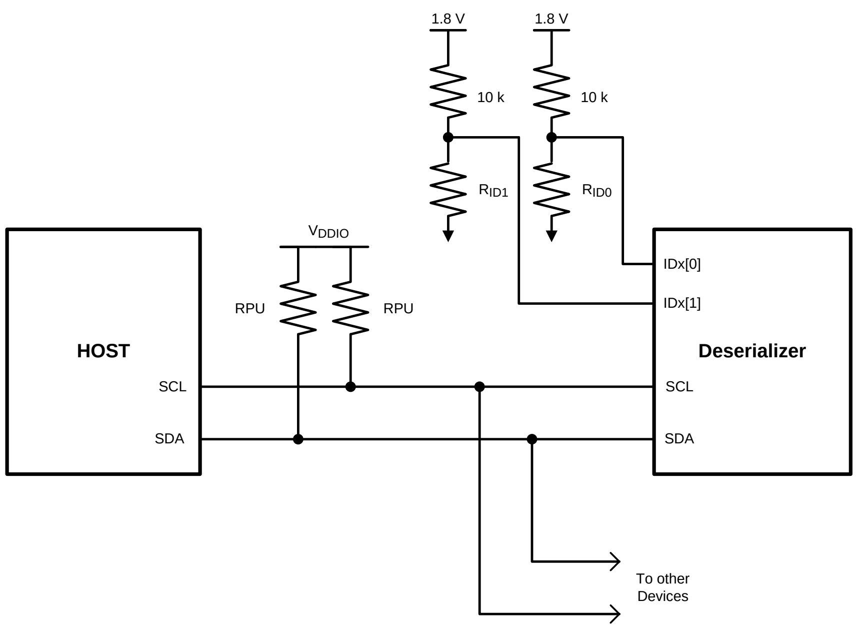


Figure 26. ID[x[Address Decoder on the Deserializer

Table 6. Resistor Values for IDx[0] and IDx[1] on DS90UB914A-Q1 Deserializer

ID[x] RESISTOR VALUE — DS90UB914A-Q1 DESERIALIZER			
Resistor R_{ID1} (kΩ) (1%Tolerance)	Resistor R_{ID0} (kΩ) (1%Tolerance)	Address 7'b	Address 8'b 0 appended (WRITE)
0	0	0x60	0xC0
0	3	0x61	0xC2
0	11	0x62	0xC4
0	100	0x63	0xC6
3	0	0x64	0xC8
3	3	0x65	0xCA
3	11	0x66	0XCC
3	100	0x67	0XCE
11	0	0x68	0XD0
11	3	0x69	0XD2
11	11	0x6A	0XD4
11	100	0x6B	0XD6
100	0	0x6C	0XD8
100	3	0x6D	0XDA
100	11	0x6E	0XDC
100	100	0x6F	0XDE

8.5.6 Multiple Device Addressing

Some applications require multiple camera devices with the same fixed address to be accessed on the same I2C bus. The DS90UB914A provides slave ID matching/aliasing to generate different target slave addresses when connecting more than two identical devices together on the same bus. This allows the slave devices to be independently addressed. Each device connected to the bus is addressable through a unique ID by programming of the Slave alias register on Deserializer. This will remap the Slave alias address to the target SLAVE_ID address; up to 1 ID Alias is supported when slaves are attached to the DS90UB914A deserializer The ECU Controller must keep track of the list of I2C peripherals in order to properly address the target device.

See Figure 27 for an example of this function.

- ECU is the I2C master and has an I2C master interface
- The I2C interfaces in DES A and DES B are both slave interfaces
- The I2C protocol is bridged from DES A to SER A and from DES B to SER B
- The I2C interfaces in SER A and SER B are both master interfaces

If master controller transmits I2C slave 0xA0, DES A (address 0xC0), with pass through enabled, will forward the transaction to remote Camera A. If the controller transmits slave address 0xA4, the DES B 0xC2 will recognize that 0xA4 is mapped to 0xA0 and will be transmitted to the remote Camera B. If controller sends command to address 0xA6, the DES B (address 0xC2), with pass through enabled, will forward the transaction to slave device 0xA2.

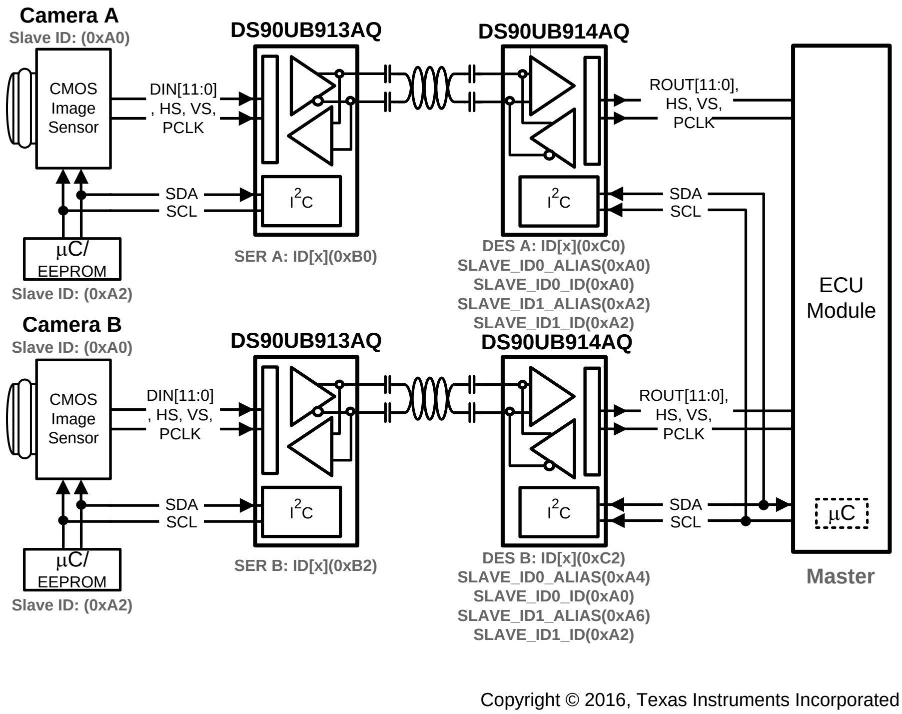


Figure 27. Multiple Device Addressing

8.6 Register Maps

Table 7. DS90UB914A-Q1 Control Registers(1)

ADDR (HEX)	NAME	BITS	FIELD	R/W	DEFAULT	DESCRIPTION
0x00	I2C Device ID	7:1	DEVICE ID	RW	0xC0'h (1100_0000'b)	7-bit address of Deserializer; 0x60'h. (110_0000'b) default
		0	Deserializer ID Select	RW		0: Deserializer Device ID is set from ID[x]. 1: Register I2C Device ID overrides ID[x].
0x01	Reset	7:6	RSVD			Reserved.
		5	ANAPWDN	RW	0	This register can be set only through local I2C access. 1: Analog power down: Powers down the analog block in the Serializer. 0: No effect.
		4:3	RSVD			Reserved.
		2	BC Enable	RW	1	Back Channel Enable 0: Disable 1: Enable
		1	Digital Reset 1	RW	0	Digital Reset Resets the entire digital block except registers. This bit is self-clearing. 1: Reset. 0: No effect.
		0	Digital Reset 0	RW	0	Digital Reset Resets the entire digital block including registers. This bit is self-clearing. 1: Reset. 0: No effect.
0x02	General Configuration 0	7	RSVD			Reserved.
		6	RSVD			Reserved.
		5	Auto-Clock	RW	0	1: Output PCLK or OSC clock when not LOCKED. 0: Only PCLK.
		4	SSCG LFMODE	RW	0	1: Selects 8x mode for 10-18 MHz frequency range in SSCG. 0: SSCG running at 4X mode.
		3:0	SSCG	RW	0	SSCG Select. 0000: Normal Operation, SSCG OFF. 0001: fmod (Hz) PCLK/2168, fdev ±0.50%. 0010: fmod (Hz) PCLK/2168, fdev ±1.00%. 0011: fmod (Hz) PCLK/2168, fdev ±1.50%. 0100: fmod (Hz) PCLK/2168, fdev ±2.00%. 0101: fmod (Hz) PCLK/1300, fdev ±0.50%. 0110: fmod (Hz) PCLK/1300, fdev ±1.00%. 0111: fmod (Hz) PCLK/1300, fdev ±1.50%. 1000: fmod (Hz) PCLK/1300, fdev ±2.00%. 1001: fmod (Hz) PCLK/868, fdev ±0.50%. 1010: fmod (Hz) PCLK/868, fdev ±1.00%. 1011: fmod (Hz) PCLK/868, fdev ±1.50%. 1100: fmod (Hz) PCLK/868, fdev ±2.00%. 1101: fmod (Hz) PCLK/650, fdev ±0.50%. 1110: fmod (Hz) PCLK/650, fdev ±1.00%. 1111: fmod (Hz) PCLK/650, fdev ±1.50%. Note: **This register should be changed only after disabling SSCG.**

(1) **To ensure optimum device functionality, It is recommended to NOT write to any RESERVED registers.**

Register Maps (continued)

Table 7. DS90UB914A-Q1 Control Registers(1) (continued)

ADDR (HEX)	NAME	BITS	FIELD	R/W	DEFAULT	DESCRIPTION
0x03	General Configuration 1	7	RX Parity Checker Enable	RW	1	Forward Channel Parity Checker Enable. 1: Enable. 0: Disable.
		6	TX CRC Checker Enable	RW	1	Back Channel CRC Generator Enable. 1: Enable. 0: Disable.
		5	V_{DDIO} Control	RW	1	Auto voltage control. 1: Enable (auto detect mode). 0: Disable.
		4	V_{DDIO} Mode	RW	0	V_{DDIO} voltage set. 1: 3.3 V 0: 1.8 V
		3	I2C Pass-Through	RW	1	I2C Pass-Through Mode. 1: Pass-Through Enabled. SER Alias 0x07 and Slave Alias 0x09- 0x17. 0: Pass-Through Disabled.
		2	AUTO ACK	RW	0	Automatically Acknowledge I2C Remote Write When enabled, I2C writes to the Serializer (or any remote I2C Slave, if I2C PASS ALL is enabled) are immediately acknowledged without waiting for the Serializer to acknowledge the write. The accesses are then remapped to address specified in 0x06. This allows I2C bus without LOCK. 1: Enable. 0: Disable.
		1	Parity Error Reset	RW	0	Parity Error Reset, This bit is NOT self-clearing. 1: Parity Error Reset. 0: No effect.
		0	RRFB	RW	1	Pixel Clock Edge Select. 1: Parallel Interface Data is strobed on the Rising Clock Edge. 0: Parallel Interface Data is strobed on the Falling Clock Edge.
0x04	EQ Feature Control	7:4	EQ level - when AEQ bypass is enabled EQ setting is provided by this register	RW	0000	Equalization gain values listed below are @ maximum line rate (1.4 Gbps). 0000 = ~16.5 dB (minimum) 0001 = ~19.0 dB 0011 = ~20.5 dB 0111 = ~22.0 dB 1111 = ~23.0 dB (maximum)
		3:0	RSVD			Reserved.
0x05	Forward Channel Low Frequency Gain	7:0	LF GAIN	RW	0x00	0x00: Default 0xC0: Beneficial for shorter cable (< 6 meter) applications that have system impedance mismatch. Increases signal-to-noise ratio (SNR) at low frequencies on forward channel to alleviate impedance mismatch.

Register Maps (continued)

Table 7. DS90UB914A-Q1 Control Registers(1) (continued)

ADDR (HEX)	NAME	BITS	FIELD	R/W	DEFAULT	DESCRIPTION
0x06	SER ID	7:1	Remote ID	RW	0x00'h	7-bit **Serializer** Device ID Configures the I2C Slave ID of the remote **Serializer**. A value of 0 in this field disables I2C access to the remote **Serializer**. This field is automatically configured by the Bidirectional Control Channel once RX Lock has been detected. Software may overwrite this value, but should also assert the FREEZE DEVICE ID bit to prevent overwriting by the Bidirectional Control Channel.
		0	Freeze Device ID	RW	0	1: Freeze Serializer Device ID Prevent auto-loading of the Serializer Device ID from the Forward Channel. The ID will be frozen at the value written. 0: Update.
0x07	SER Alias	7:1	Serializer Alias ID	RW	0x00'h	7-bit Remote Serializer Device Alias ID Configures the decoder for detecting transactions designated for an I2C Serializer device. The transaction will be remapped to the address specified in the SER ID register. A value of 0 in this field disables access to the remote I2C Serializer.
		0	RSVD			Reserved.
0x08	Slave ID[0]	7:1	Slave ID0	RW	0x00'h	7-bit Remote Slave Device ID 0 Configures the physical I2C address of the remote I2C Slave device attached to the remote Serializer. If an I2C transaction is addressed to the Slave Alias ID0, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.
		0	RSVD			Reserved.
0x09	Slave ID[1]	7:1	Slave ID1	RW	0x00'h	7-bit Remote Slave Device ID 1 Configures the physical I2C address of the remote I2C Slave device attached to the remote Serializer. If an I2C transaction is addressed to the Slave Alias ID1, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.
		0	RSVD			Reserved.
0x0A	Slave ID[2]	7:1	Slave ID2	RW	0x00'h	7-bit Remote Slave Device ID 2 Configures the physical I2C address of the remote I2C Slave device attached to the remote Serializer. If an I2C transaction is addressed to the Slave Alias ID2, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.
		0	RSVD			Reserved.
0x0B	Slave ID[3]	7:1	Slave ID3	RW	0x00'h	7-bit Remote Slave Device ID 3 Configures the physical I2C address of the remote I2C Slave device attached to the remote Serializer. If an I2C transaction is addressed to the Slave Alias ID3, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.
		0	RSVD			Reserved.

Register Maps (continued)

Table 7. DS90UB914A-Q1 Control Registers[1] (continued)

ADDR (HEX)	NAME	BITS	FIELD	R/W	DEFAULT	DESCRIPTION
0x0C	Slave ID[4]	7:1	Slave ID4	RW	0x00'h	7-bit Remote Slave Device ID 4 Configures the physical I2C address of the remote I2C Slave device attached to the remote Serializer. If an I2C transaction is addressed to the Slave Alias ID4, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.
		0	RSVD			Reserved.
0x0D	Slave ID[5]	7:1	Slave ID5	RW	0x00'h	7-bit Remote Slave Device ID 5 Configures the physical I2C address of the remote I2C Slave device attached to the remote Serializer. If an I2C transaction is addressed to the Slave Alias ID5 , the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.
		0	RSVD			Reserved.
0x0E	Slave ID[6]	7:1	Slave ID6	RW	0x00'h	7-bit Remote Slave Device ID 6 Configures the physical I2C address of the remote I2C Slave device attached to the remote Serializer. If an I2C transaction is addressed to the Slave Alias ID6, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.
		0	RSVD			Reserved.
0x0F	Slave ID[7]	7:1	Slave ID7	RW	0x00'h	7-bit Remote Slave Device ID 7 Configures the physical I2C address of the remote I2C Slave device attached to the remote Serializer. If an I2C transaction is addressed to the Slave Alias ID7, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.
		0	RSVD			Reserved.
0x10	Slave Alias[0]	7:1	Slave Alias ID0	RW	0x00'h	7-bit Remote Slave Device Alias ID 0 Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Serializer. The transaction will be remapped to the address specified in the Slave ID0 register. A value of 0 in this field disables access to the remote I2C Slave.
		0	RSVD			Reserved.
0x11	Slave Alias[1]	7:1	Slave Alias ID1	RW	0x00'h	7-bit Remote Slave Device Alias ID 1 Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Serializer. The transaction will be remapped to the address specified in the Slave ID1 register. A value of 0 in this field disables access to the remote I2C Slave.
		0	RSVD			Reserved.

Register Maps (continued)

Table 7. DS90UB914A-Q1 Control Registers(1) (continued)

ADDR (HEX)	NAME	BITS	FIELD	R/W	DEFAULT	DESCRIPTION
0x12	Slave Alias[2]	7:1	Slave Alias ID2	RW	0x00'h	7-bit Remote Slave Device Alias ID 2 Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Serializer. The transaction will be remapped to the address specified in the Slave ID2 register. A value of 0 in this field disables access to the remote I2C Slave.
		0	RSVD			Reserved.
0x13	Slave Alias[3]	7:1	Slave Alias ID3	RW	0x00'h	7-bit Remote Slave Device Alias ID 3 Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Serializer. The transaction will be remapped to the address specified in the Slave ID3 register. A value of 0 in this field disables access to the remote I2C Slave.
		0	RSVD			Reserved.
0x14	Slave Alias[4]	7:1	Slave Alias ID4	RW	0x00'h	7-bit Remote Slave Device Alias ID 4 Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Serializer. The transaction will be remapped to the address specified in the Slave ID4 register. A value of 0 in this field disables access to the remote I2C Slave.
		0	RSVD			Reserved.
0x15	Slave Alias[5]	7:1	Slave Alias ID5	RW	0x00'h	7-bit Remote Slave Device Alias ID 5 Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Serializer. The transaction will be remapped to the address specified in the Slave ID5 register. A value of 0 in this field disables access to the remote I2C Slave.
		0	RSVD			Reserved.
0x16	Slave Alias[6]	7:1	Slave Alias ID6	RW	0x00'h	7-bit Remote Slave Device Alias ID 6 Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Serializer. The transaction will be remapped to the address specified in the Slave ID6 register. A value of 0 in this field disables access to the remote I2C Slave.
		0	RSVD			Reserved.
0x17	Slave Alias[7]	7:1	Slave Alias ID7	RW	0x00'h	7-bit Remote Slave Device Alias ID 7 Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Serializer. The transaction will be remapped to the address specified in the Slave ID7 register. A value of 0 in this field disables access to the remote I2C Slave.
		0	RSVD			Reserved.
0x18	Parity Errors Threshold	7:0	Parity Error Threshold Byte 0	RW	0x00'h	Parity errors threshold on the Forward channel during normal information. This sets the maximum number of parity errors that can be counted using register 0x1A. Least significant Byte.

Register Maps (continued)

Table 7. DS90UB914A-Q1 Control Registers(1) (continued)

ADDR (HEX)	NAME	BITS	FIELD	R/W	DEFAULT	DESCRIPTION
0x19	Parity Errors Threshold	7:0	Parity Error Threshold Byte 1	RW	0x01'h	Parity errors threshold on the Forward channel during normal operation. This sets the maximum number of parity errors that can be counted using register 0x1B. Most significant Byte.
0x1A	Parity Errors	7:0	Parity Error Byte 0	R	0x00'h	Number of parity errors in the Forward channel during normal operation. Least significant Byte.
0x1B	Parity Errors	7:0	Parity Error Byte 1	R	0x00'h	Number of parity errors in the Forward channel during normal operation. Most significant Byte.
0x1C	General Status	7:4	Rev-ID	R	0x0'h	Revision ID. 0x0: Production Revision ID.
		3	RSVD			Reserved.
		2	Parity Error	R	0	Parity Error detected. 1: Parity Errors detected. 0: No Parity Errors.
		1	Signal Detect	R	0	1: Serial input detected. 0: Serial input not detected.
		0	Lock	R	0	De-Serializer CDR, PLL's clock to recovered clock frequency. 1: De-Serializer locked to recovered clock. 0: De-Serializer not locked.
0x1D	GPIO[1] and GPIO[0] Config	7	GPIO1 Output Value	RW	0	Local GPIO Output Value This value is the output on the GPIO pin when the GPIO function is enabled, the local GPIO direction is Output.
		6	RSVD			Reserved.
		5	GPIO1 Direction	RW	1	Local GPIO Direction. 1: Input. 0: Output.
		4	GPIO1 Enable	RW	1	GPIO Function Enable. 1: Enable GPIO operation. 0: Enable normal operation.
		3	GPIO0 Output Value	RW	0	Local GPIO Output Value This value is output on the GPIO pin when the GPIO function is enabled, the local GPIO direction is Output.
		2	RSVD			Reserved.
		1	GPIO0 Direction	RW	1	Local GPIO Direction. 1: Input. 0: Output.
		0	GPIO0 Enable	RW	1	GPIO Function Enable. 1: Enable GPIO operation. 0: Enable normal operation.

Register Maps (continued)

Table 7. DS90UB914A-Q1 Control Registers(1) (continued)

ADDR (HEX)	NAME	BITS	FIELD	R/W	DEFAULT	DESCRIPTION
0x1E	GPIO[3] and GPIO[2] Config	7	GPIO3 Output Value	RW	0	Local GPIO Output Value This value is the output on the GPIO pin when the GPIO function is enabled, the local GPIO direction is Output.
		6	RSVD			Reserved.
		5	GPIO3 Direction	RW	1	Local GPIO Direction. 1: Input. 0: Output.
		4	GPIO3 Enable	RW	1	GPIO Function Enable. 1: Enable GPIO operation. 0: Enable normal operation.
		3	GPIO2 Output Value	RW	0	Local GPIO Output Value This value is output on the GPIO pin when the GPIO function is enabled, the local GPIO direction is Output.
		2	RSVD			Reserved.
		1	GPIO2 Direction	RW	1	Local GPIO Direction. 1: Input. 0: Output.
		0	GPIO2 Enable	RW	1	GPIO Function Enable. 1: Enable GPIO operation. 0: Enable normal operation.

Register Maps (continued)

Table 7. DS90UB914A-Q1 Control Registers(1) (continued)

ADDR (HEX)	NAME	BITS	FIELD	R/W	DEFAULT	DESCRIPTION
0x1F	Mode and OSS Select	7	OEN_OSS Override	RW	0	Allows overriding OEN and OSS select coming from Pins. 1: Overrides OEN/OSS_SEL selected by pins. 0: Does NOT override OEN/OSS_SEL select by pins.
		6	OEN Select	RW	0	OEN configuration from register.
		5	OSS Select	RW	0	OSS_SEL configuration from register.
		4	MODE_OVERRIDE	RW	0	Allows overriding mode select bits coming from forward-channel. 1: Overrides MODE select bits. 0: Does not override MODE select bits.
		3	PIN_MODE_12–bit HF mode	R	0	Status of mode select pin.
		2	PIN_MODE_10-bit mode	R	0	Status of mode select pin.
		1	MODE_12–bit High Frequency	RW	0	Selects 12-bit high frequency mode. This bit is automatically updated by the mode settings from MODE pin unless MODE_OVERRIDE is SET. 1: 12-bit high frequency mode is selected. 0: 12-bit high frequency mode is not selected. To select 12-bit low frequency mode by register override, set 0x1F[1] = 0x1F[0] = 0
		0	MODE_10–bit mode	RW	0	Selects 10-bit mode. This bit is automatically updated by the mode settings from MODE pin unless MODE_OVERRIDE is SET. 1: Enables 10-bit mode. 0: Disables 10-bit mode.
0x20	BCC Watchdog Control	7:1	BCC Watchdog timer	RW	0x7F'h (111_1111'b)	The watchdog timer allows termination of a control channel transaction if it fails to complete within a programmed amount of time. This field sets the Bidirectional Control Channel Watchdog Timeout value in units of 2ms. This field should not be set to 0.
		0	BCC Watchdog Timer Disable	RW	0	Disable Bidirectional Control Channel Watchdog Timer. 1: Disables BCC Watchdog Timer operation. 0: Enables BCC Watchdog Timer operation.
0x21	I2C Control 1	7	I2C Pass-Through All	RW	0	1: Enable Forward Control Channel pass-through of all I2C accesses to I2C IDs that **do not match** the Deserializer I2C ID. **The I2C accesses are then remapped to address specified in register 0x06 (SER ID).** 0: Enable Forward Control Channel pass-through only of I2C accesses to I2C IDs **matching** either the remote Serializer ID or the remote I2C IDs.
		6:4	I2C SDA Hold Time	RW	0x1'h	Internal SDA Hold Time This field configures the amount of internal hold time provided for the SDA input relative to the SCL input. Units are 50ns.
		3:0	I2C Filter Depth	RW	0x7'h	I2C Glitch Filter Depth This field configures the maximum width of glitch pulses on the SCL and SDA inputs that will be rejected. Units are 10ns.

Register Maps (continued)

Table 7. DS90UB914A-Q1 Control Registers(1) (continued)

ADDR (HEX)	NAME	BITS	FIELD	R/W	DEFAULT	DESCRIPTION
0x22	I2C Control 2	7	Forward Channel Sequence Error	R	0	Control Channel Sequence Error Detected This bit indicates a sequence error has been detected in forward control channel. 1: If this bit is set, an error may have occurred in the control channel operation. 0: No forward channel errors have been detected on the control channel.
		6	Clear Sequence Error	RW	0	1: Clears the Sequence Error Detect bit. 0: No effect.
		5	RSVD			Reserved.
		4:3	SDA Output Delay	RW	00	SDA Output Delay This field configures output delay on the SDA output. Setting this value will increase output delay in units of 50ns. Nominal output delay values for SCL to SDA are: 00 : ~350 ns 01: ~400 ns 10: ~450 ns 11: ~500 ns
		2	Local Write Disable	RW	0	Disable Remote Writes to local registers Setting this bit to a 1 will prevent remote writes to local device registers from across the control channel. This prevents writes to the Deserializer registers from an I2C master attached to the Serializer. Setting this bit does not affect remote access to I2C slaves at the Deserializer.
		1	I2C Bus Timer Speedup	RW	0	Speed up I2C Bus Watchdog Timer. 1: Watchdog Timer expires after approximately 50 µs. 0: Watchdog Timer expires after approximately 1 s.
		0	I2C Bus Timer Disable	RW	0	Disable I2C Bus Watchdog Timer When the I2C Watchdog Timer may be used to detect when the I2C bus is free or hung up following an invalid termination of a transaction. If SDA is high and no signaling occurs for approximately 1 second, the I2C bus will assumed to be free. If SDA is low and no signaling occurs, the device will attempt to clear the bus by driving 9 clocks on SCL.
0x23	General Purpose Control	7:0	GPCR	RW	0x00'h	Scratch Register.
0x24	BIST Control	7:4	RSVD			Reserved.
		3	BIST Pin Configuration	RW	1	Bist Configured through Pin. 1: Bist configured through pin. 0: Bist configured through register bit "reg_24[0]".
		2:1	BIST Clock Source	RW	00	BIST Clock Source. See Table 5
		0	BIST Enable	RW	0	BIST Control. 1: Enabled. 0: Disabled.
0x25	Parity Error Count	7:0	BIST Error Count	R	0x00'h	Number of Forward Channel Parity errors in BIST mode.

Register Maps (continued)

Table 7. DS90UB914A-Q1 Control Registers(1) (continued)

ADDR (HEX)	NAME	BITS	FIELD	R/W	DEFAULT	DESCRIPTION
0x26	Bidirectional Control Channel (BCC) Tuning for Channel 0 (RIN0±)	7:6	RSVD			Reserved.
		5:4	RSVD			Reserved.
		3:2	Termination Resistance Control	RW	00	00: 50 Ω (default) 01: 47.4 Ω 10: 45.3 Ω 11: 37.7 Ω
		1:0	RSVD			Reserved.
0x27	Forward Channel Tuning for Channel 0 (RIN0±)	7:0	Impedance Control	RW	0x00	0x00: Default 0x70: Beneficial for longer cable (> 6 meter) applications that have system impedance mismatch on deserializer side.
0x28 - 0x3B	**Reserved.**					
0x3C	Oscillator output divider select	7:2	RSVD			Reserved.
		1:0	OSC OUT DIVIDER SEL	RW	00	Selects the divider for the OSC clock out on PCLK when system is not locked and selected by OEN/OSS_SEL 0x02[5]: 00: 50 M (±30%) 01: 25 M (±30%) 1X: 12.5 M (±30%)
0x3D - 0x3E	**Reserved.**					
0x3F	CML Output Enable	7:5	RSVD			Reserved.
		4	CML OUT Enable	RW	1	CML Output Driver Enable is Active-Low. 0: CML Loop-through Driver is powered up. 1: CML Loop-through Driver is powered down.
		3:0	RSVD			Reserved.
0x40	SCL High Time	7:0	SCL High Time	RW	0x82'h (1000_0010'b)	I2C Master SCL High Time This field configures the high pulse width of the SCL output when the De-Serializer is the Master on the local I2C bus. Units are 50 ns for the nominal oscillator clock frequency. The default value is set to provide a minimum (4 µs + 0.3 µs of rise time for cases where rise time is very fast) SCL high time with the internal oscillator clock running at 26 MHz rather than the nominal 20 MHz.
0x41	SCL Low Time	7:0	SCL Low Time	RW	0x82'h (1000_0010'b)	I2C SCL Low Time This field configures the low pulse width of the SCL output when the De-Serializer is the Master on the local I2C bus. This value is also used as the SDA setup time by the I2C Slave for providing data prior to releasing SCL during accesses over the Bidirectional Control Channel. Units are 50 ns for the nominal oscillator clock frequency. The default value is set to provide a minimum (4.7 µs + 0.3 µs of fall time for cases where fall time is very fast) SCL low time with the internal oscillator clock running at 26 MHz rather than the nominal 20 MHz.
0x42	CRC Force Error	7:2	RSVD			Reserved.
		1	Force Back Channel Error	RW	0	1: This bit introduces multiple errors into Back channel frame. 0: No effect.
		0	Force One Back Channel Error	RW	0	1: This bit introduces ONLY one error into Back channel frame. Self clearing bit. 0: No effect.
0x43 - 0x45	**Reserved.**					

Register Maps (continued)

Table 7. DS90UB914A-Q1 Control Registers(1) (continued)

ADDR (HEX)	NAME	BITS	FIELD	R/W	DEFAULT	DESCRIPTION
0x46	Bidirectional Control Channel (BCC) Tuning for Channel 1 (RIN1±)	7:6	RSVD			Reserved.
		5:4	RSVD			Reserved.
		3:2	Termination Resistance Control	RW	00	00: 50 Ω (default) 01: 47.4 Ω 10: 45.3 Ω 11: 37.7 Ω
		1:0	RSVD			Reserved.
0x47	Forward Channel Tuning for Channel 1 (RIN1±)	7:0	Impedance Control	RW	0x00	0x00: Default 0x70: Beneficial for longer cable (> 6 meter) applications that have system impedance mismatch on deserializer side.
0x48 - 0x4B	**Reserved.**					
0x4C	SEL Register	7	Pin Channel SEL Override	RW	0	0: SEL pin selects the FPD-III serial input 1: 0x4C[6] selects the FPD-III serial input
		6	Channel SEL	RW	0	0: Channel 0 is selected 1: Channel 1 is selected
		5:0	RSVD			Reserved.
0x4D	AEQ Test Mode Select	7	RSVD			Reserved.
		6	AEQ Bypass	RW	0	Bypass AEQ and use set manual EQ value using register 0x04.
		5:0	RSVD			Reserved.
0x4E	EQ Value	7:4	AEQ / Manual Eq Readback	R	0000	Read back the adaptive and manual EQ level. EQ gain values listed below are @ maximum line rate (1.4 Gbps). 0000 = ~16.5 dB (minimum) 0001 = ~19.0 dB 0011 = ~20.5 dB 0111 = ~22.0 dB 1111 = ~23.0 dB (maximum)
		3:0	RSVD			Reserved.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The DS90UB914A was designed as a deserializer to support automotive camera designs. Automotive cameras are often located in remote positions such as bumpers or trunk lids, and a major component of the system cost is the wiring. For this reason it is desirable to minimize the wiring to the camera. This chipset allows the video data, along with a bidirectional control channel, and power to all be sent over a single coaxial cable. The chipset is also able to transmit over STP and is pin-to-pin/backwards compatible with the DS90UB914Q.

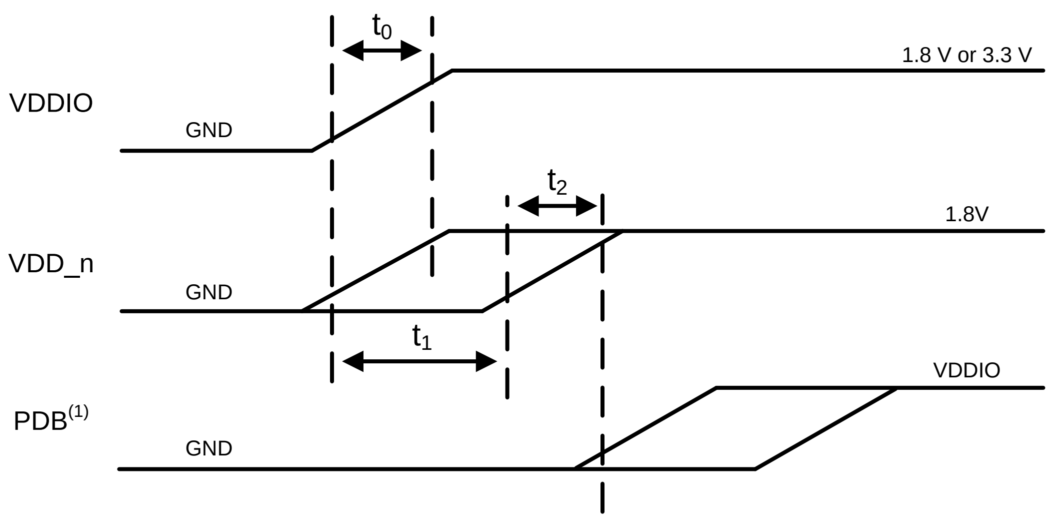
9.1.1 Power Over Coax

See application report *Sending Power over Coax in DS90UB913A Designs* for more details.

9.1.2 Power-Up Requirements and PDB Pin

The PDB pin on the device must be ramped after the V_{DDIO} and V_{DD_n} supplies have reached their required operating voltage levels. It is recommended to assert PDB = HIGH with a control signal from a microcontroller to help ensure proper sequencing of the PDB pin after settling of the power supplies. If a microcontroller is not available, an RC filter network can be used on the PDB pin as an alternative method for asserting the PDB signal. Please refer to *Power Down* for device operation when powered down.

Common applications will tie the V_{DDIO} and V_{DD_n} supplies to the same power source of 1.8 V typically. This is an acceptable method for ramping the V_{DDIO} and V_{DD_n} supplies. The main constraint here is that the V_{DD_n} supply does not lead in ramping before the V_{DDIO} system supply. This is noted in Figure 28 with the requirement of $t_1 \geq 0$. V_{DDIO} should reach the expected operating voltage earlier than V_{DD_n} or at the same time.



(1) It is recommended to assert PDB = HIGH with a microcontroller rather than an RC filter network to help ensure proper sequencing of PDB pin after settling of power supplies.

Figure 28. Suggested Power-Up Sequencing

Application Information (continued)

Table 8. Power-Up Sequencing Constraints for DS90UB914A-Q1

Symbol	Description	Test Conditions	Min	Typ	Max	Units
t_0	V_{DDIO} Rise Time	10% to 90% of nominal voltage on rising edge. Monotonic signal ramp is required	0.05		5	ms
t_1	V_{DDIO} to V_{DD_n} Delay	10% of rising edge (V_{DDIO}) to 10% of rising edge (V_{DD_n})	0			ms
t_2	V_{DD_n} Rise Time	10% to 90% of nominal voltage on rising edge. Monotonic signal ramp is required. V_{PDB} < 10% of V_{DDIO}	0.05		5	ms

If the FPD-Link system is not initialized in the correct sequence, the DS90UB914A-Q1 may need to be reset with signal present at the input to the Deserializer to optimize the link:

1. Toggle the PDB power down reset pin, or:
2. Perform Digital Reset 1 writing register 0x01[1] = 1 over I2C. It resets the entire digital block except registers in the 914A. This is a self-clearing register bit.

For the case of the loss of lock from cable when disconnecting and re-connecting FPD-Link cable, it is recommended to perform either PDB reset or digital reset via I2C when lock drops.

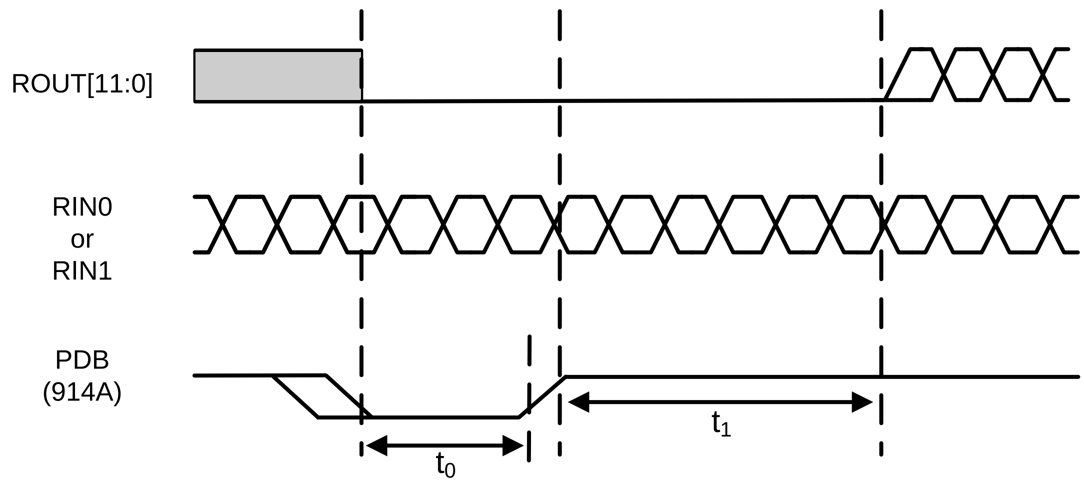


Figure 29. Suggested Timing of PDB RESET for DS90UB914A-Q1 Deserializer

Table 9. PDB RESET Timing Constraints for DS90UB914A-Q1

Symbol	Description	Test Conditions	Min	Typ	Max	Units
t_0	PDB minimum LOW pulse width	10% of falling edge to 10% of rising edge	2	5		ms
t_1	Data Lock Time	90% of rising edge		15	22	ms

9.1.3 AC Coupling

The SER/DES supports only AC-coupled interconnects through an integrated DC-balanced decoding scheme. External AC-coupling capacitors must be placed in series in the FPD-Link III signal path as illustrated in Figure 30. For applications utilizing single-ended 50-Ω coaxial cable, the unused data pin (DOUT–, RIN–) should utilize a 0.047-µF capacitor and should be terminated with a 50-Ω resistor.

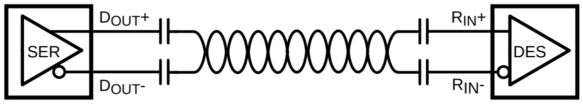


Figure 30. AC-Coupled Connection (STP)

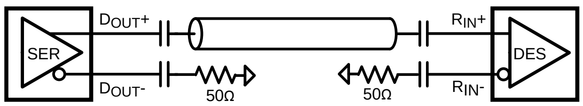


Figure 31. AC-Coupled Connection (Coaxial)

For high-speed FPD–Link III transmissions, the smallest available package should be used for the AC coupling capacitor. This will help minimize degradation of signal quality due to package parasitics. The I/O’s require a 0.1-µF AC coupling capacitors to the line.

9.1.4 Transmission Media

The DS90UB913A/914A chipset is intended to be used in a point-to-point configuration through a shielded coaxial cable. The Serializer and Deserializer provide internal termination to minimize impedance discontinuities. The interconnect (cable and connectors) should have a differential impedance of 100 Ω, or a single-ended impedance of 50 Ω. The maximum length of cable that can be used is dependent on the quality of the cable (gauge, impedance), connector, board(discontinuities, power plane), the electrical environment (for example, power stability, ground noise, input clock jitter, PCLK frequency, etc). The resulting signal quality at the receiving end of the transmission media may be assessed by monitoring the differential eye opening of the serial data stream. A differential probe should be used to measure across the termination resistor at the CMLOUTP/N pins. Figure 8 illustrates the minimum eye width and eye height that is necessary for bit error free operation.

Please refer to *Cable Requirements for the DS90UB913A & DS90UB914A* or contact TI for a channel specification regarding cable loss parameters and further details on adaptive equalizer loss compensation.

9.1.5 Adaptive Equalizer – Loss Compensation

The receiver inputs provide an adaptive equalization filter in order to compensate for signal degradation from the interconnect components. In order to determine the maximum cable reach, factors that affect signal integrity such as jitter, skew, ISI, crosstalk, etc. need to be taken into consideration. The level of equalization can also be manually selected via register controls. The adaptive equalized output can be seen using the CMLOUTP/CMLOUTN pins in the Deserializer.

If the deserializer loses LOCK, the adaptive equalizer will reset and perform the LOCK algorithm again to reacquire the video data stream being sent by the serializer.

9.2 Typical Applications

9.2.1 Coax Application

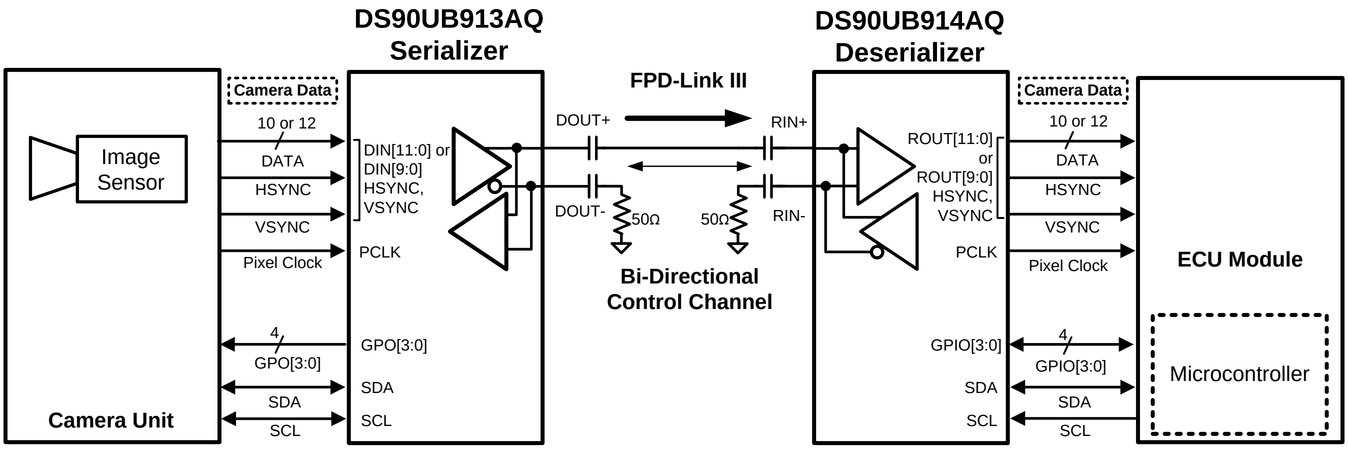


Figure 32. Coax Application Block Diagram

9.2.1.1 Design Requirements

For the typical coax design applications, use the following as input parameters:

Table 10. Coax Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
V_{DDIO}	1.8 V or 3.3 V
V_{DD_n}	1.8 V
AC Coupling Capacitors for RIN±	0.1 µF, 0.047 µF (For the unused data pin, RIN–)
PCLK Frequency	50 MHz (12-bit low frequency), 75 MHz (12-bit high frequency), 100 MHz (10-bit)

9.2.1.2 Detailed Design Procedure

Figure 33 shows a typical connection using a **Coax** interface to the DS90UB914A-Q1 Deserializer.

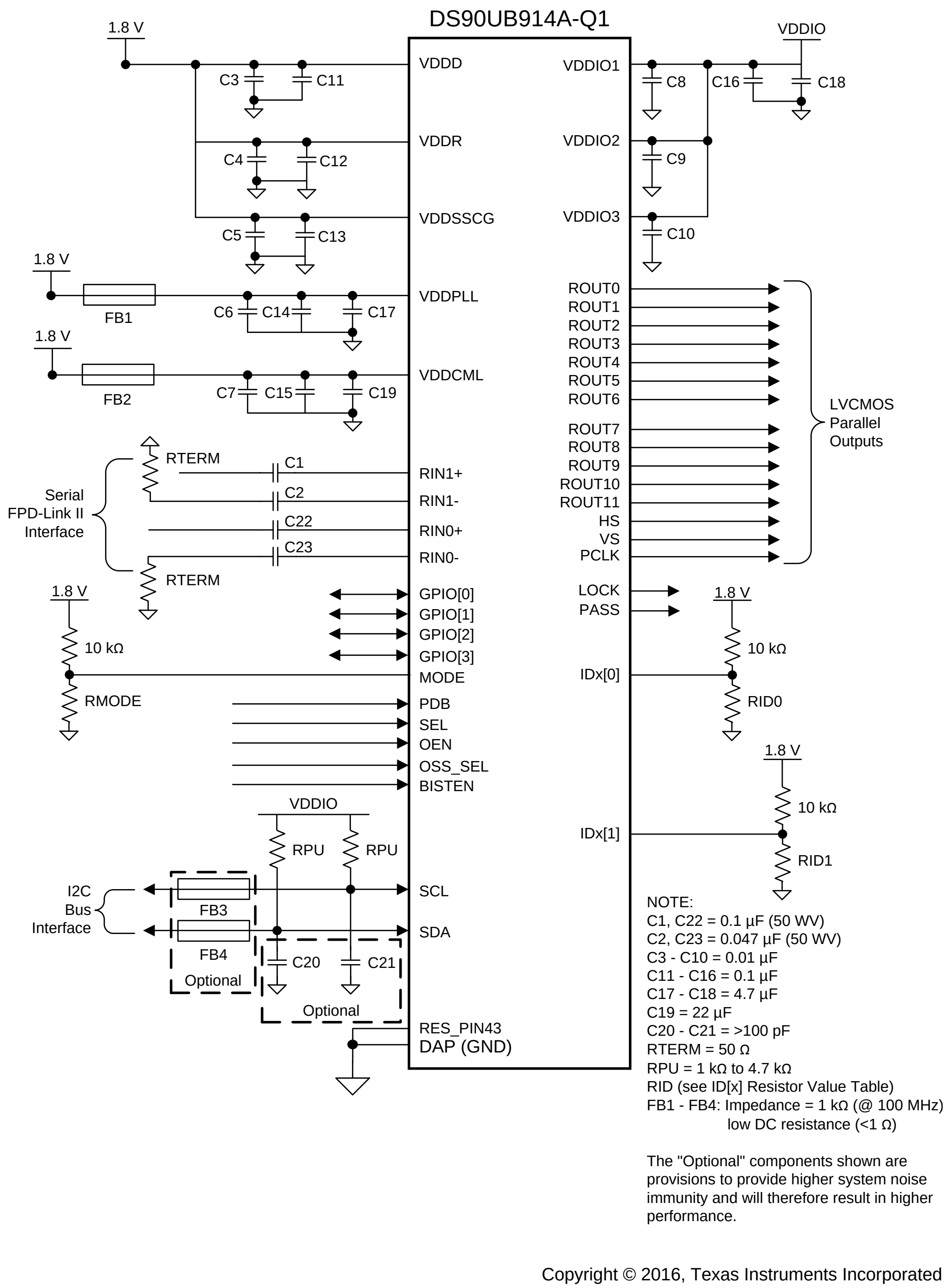


Figure 33. DS90UB914A-Q1 Typical Connection Diagram — Pin Control (Coax)

9.2.1.3 Application Curves

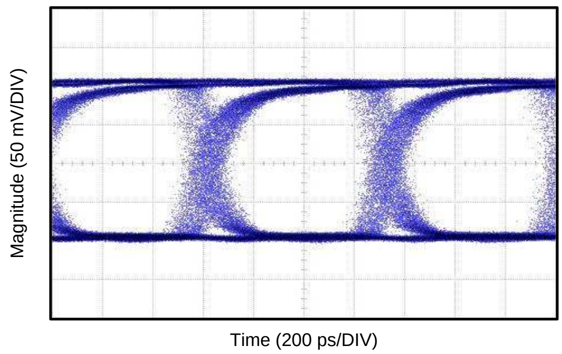


Figure 34. Coax Eye Diagram at 1.4-Gbps Line Rate (100-MHz Pixel Clock) from Deserializer CML Loop-through Output (CMLOUT±)

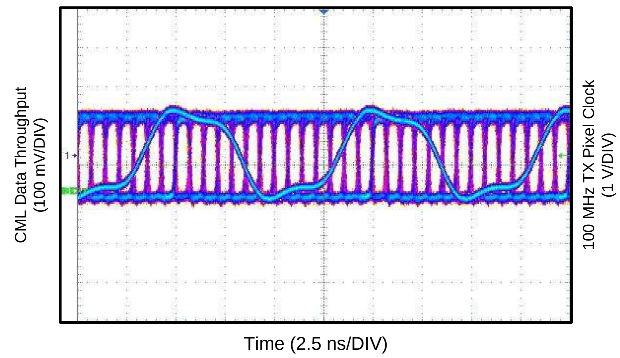


Figure 35. Coax Eye Diagram with 100-MHz TX Pixel Clock Overlay from Deserializer CML Loop-through Output (CMLOUT±)

9.2.2 STP Application

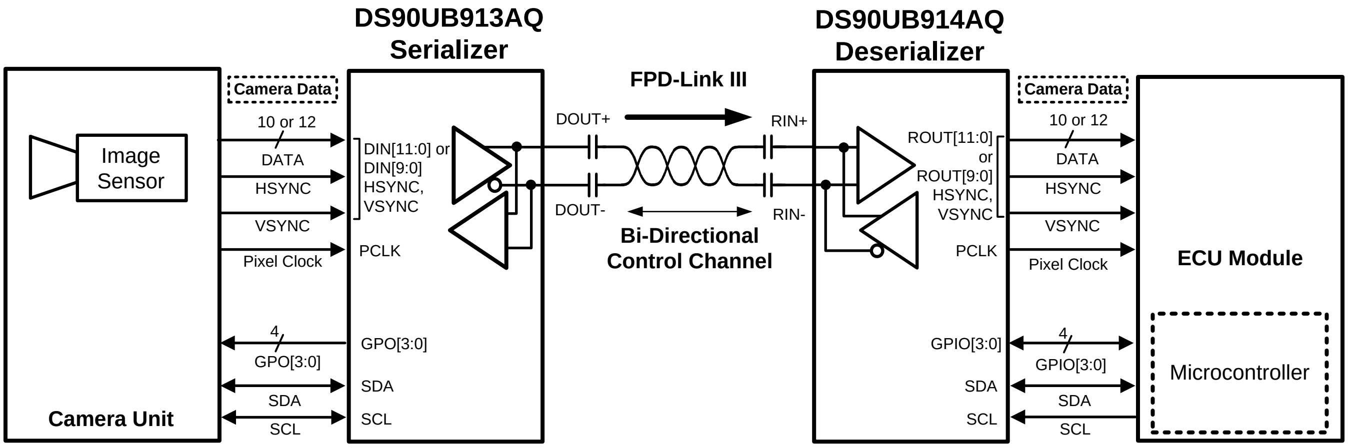


Figure 36. STP Application Block Diagram

9.2.2.1 Design Requirements

For the typical STP design applications, use the following as input parameters

Table 11. STP Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
V_{DDIO}	1.8 V or 3.3 V
V_{DD_n}	1.8 V
AC Coupling Capacitors for RIN±	0.1 µF
PCLK Frequency	50 MHz (12-bit low frequency), 75 MHz (12-bit high frequency), 100 MHz (10-bit)

9.2.2.2 Detailed Design Procedure

Figure 37 shows a typical connection using an **STP** interface to the DS90UB914A-Q1 Deserializer.

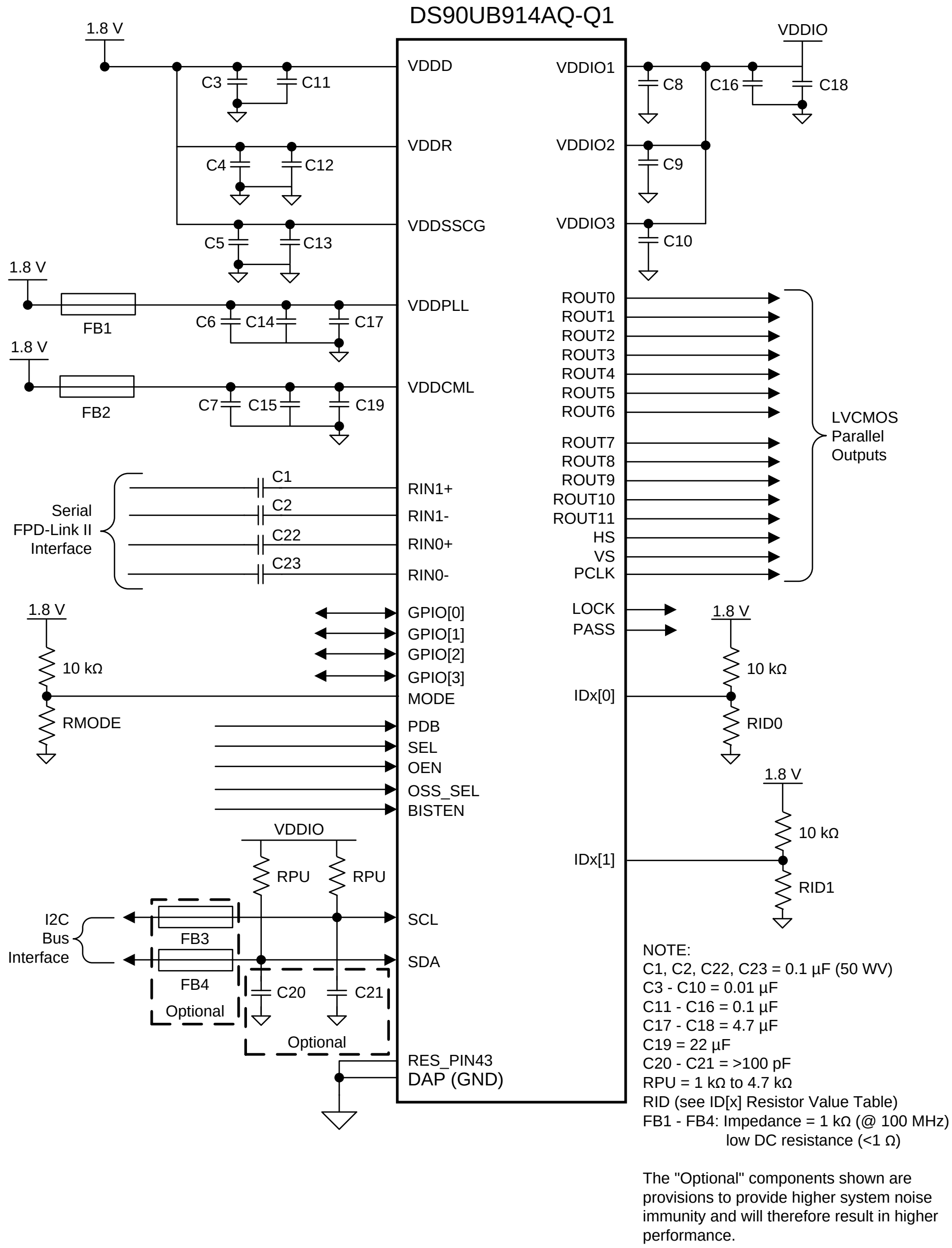


Figure 37. DS90UB914A-Q1 Typical Connection Diagram — Pin Control (STP)

9.2.2.3 Application Curves

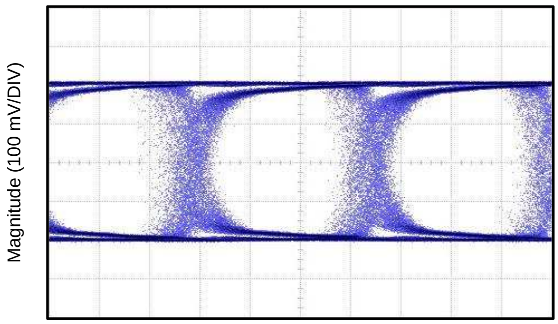


Figure 38. STP Eye Diagram at 1.4-Gbps Line Rate (100-MHz Pixel Clock) from Deserializer CML Loop-through Output (CMLOUT±)

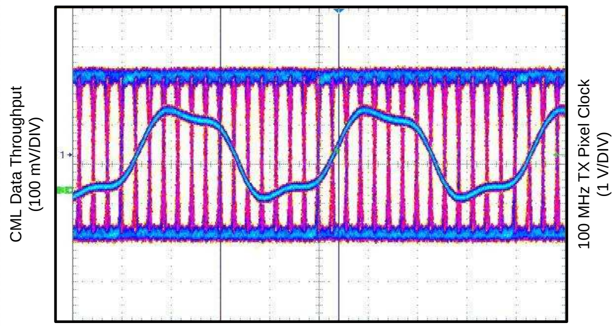


Figure 39. STP Eye Diagram with 100-MHz TX Pixel Clock Overlay from Deserializer CML Loop-through Output (CMLOUT±)

10 Power Supply Recommendations

This device is designed to operate from an input core voltage supply of 1.8 V. Some devices provide separate power and ground terminals for different portions of the circuit. This is done to isolate switching noise effects between different sections of the circuit. Separate planes on the PCB are typically not required. Terminal description tables typically provide guidance on which circuit blocks are connected to which power terminal pairs. In some cases, an external filter may be used to provide clean power to sensitive circuits such as PLLs. The voltage applied on V_{DDIO} (1.8 V, 3.3 V) or other power supplies making up V_{DD_n} (1.8 V) should be at the input pin - any board level DC drop should be compensated (i.e. ferrite beads in the path of the power supply rails).

11 Layout

11.1 Layout Guidelines

Circuit board layout and stack-up for the Ser/Des devices should be designed to provide low-noise power feed to the device. Good layout practice will also separate high frequency or high-level inputs and outputs to minimize unwanted stray noise pickup, feedback and interference. Power system performance may be greatly improved by using thin dielectrics (2 to 4 mils) for power / ground sandwiches. This arrangement provides plane capacitance for the PCB power system with low-inductance parasitics, which has proven especially effective at high frequencies, and makes the value and placement of external bypass capacitors less critical. External bypass capacitors should include both RF ceramic and tantalum electrolytic types. RF capacitors may use values in the range of 0.01 µF to 0.1 µF. Tantalum capacitors may be in the 2.2-µF to 10-µF range. Voltage rating of the tantalum capacitors should be at least 5X the power supply voltage being used.

Surface mount capacitors are recommended due to their smaller parasitics. When using multiple capacitors per supply pin, locate the smaller value closer to the pin. A large bulk capacitor is recommend at the point of power entry. This is typically in the 50-µF to 100-µF range and will smooth low frequency switching noise. It is recommended to connect power and ground pins directly to the power and ground planes with bypass capacitors connected to the plane with via on both ends of the capacitor. Connecting power or ground pins to an external bypass capacitor will increase the inductance of the path.

A small body size X7R chip capacitor, such as 0603, is recommended for external bypass. Its small body size reduces the parasitic inductance of the capacitor. The user must pay attention to the resonance frequency of these external bypass capacitors, usually in the range of 20 to 30 MHz. To provide effective bypassing, multiple capacitors are often used to achieve low impedance between the supply rails over the frequency of interest. At high frequency, it is also a common practice to use two vias from power and ground pins to the planes, reducing the impedance at high frequency.

Some devices provide separate power for different portions of the circuit. This is done to isolate switching noise effects between different sections of the circuit. Separate planes on the PCB are typically not required. Pin Description tables typically provide guidance on which circuit blocks are connected to which power pin pairs. In some cases, an external filter many be used to provide clean power to sensitive circuits such as PLLs.

Use at least a four layer board with a power and ground plane. Locate LVCMOS signals away from the differential lines to prevent coupling from the LVCMOS lines to the differential lines. Closely-coupled differential lines of 100 Ω are typically recommended for differential interconnect. The closely coupled lines help to ensure that coupled noise will appear as common-mode and thus is rejected by the receivers. The tightly coupled lines will also radiate less.

Information on the WQFN style package is provided in TI Application Note: AN-1187 Leadless Leadframe Package (LLP).

11.1.1 Interconnect Guidelines

See AN-1108 Channel-Link PCB and Interconnect Design-In Guidelines for full details.

- Use 100 Ω coupled differential pairs
- Use the S/2S/3S rule in spacings
  - – S = space between the pair
  - – 2S = space between pairs
  - – 3S = space to LVCMOS signal
- Minimize the number of Vias
- Use differential connectors when operating above 500 Mbps line speed
- Maintain balance of the traces
- Minimize skew within the pair

Additional general guidance can be found in the LVDS Owner's Manual - available in PDF format from the Texas Instrument web site at: *www.ti.com/lvds*.

11.2 Layout Example

Stencil parameters such as aperture area ratio and the fabrication process have a significant impact on paste deposition. Inspection of the stencil prior to placement of the WQFN package is highly recommended to improve board assembly yields. If the via and aperture openings are not carefully monitored, the solder may flow unevenly through the DAP. Stencil parameters for aperture opening and via locations are shown below:

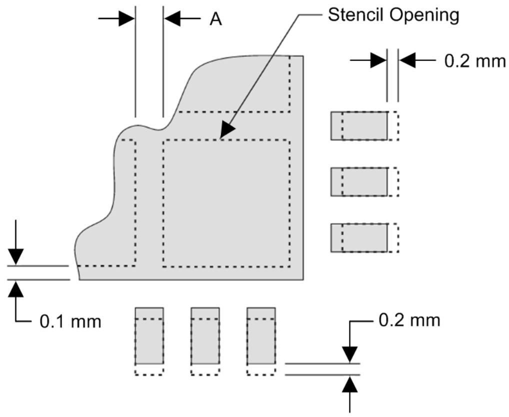


Figure 40. No Pullback WQFN, Single Row Reference Diagram

Table 12. No Pullback WQFN Stencil Aperture Summary for DS90UB914A-Q1

DEVICE	PIN COUNT	MKT DWG	PCB I/O PAD SIZE (mm)	PCB PITCH (mm)	PCB DAP SIZE(mm)	STENCIL I/O APERTURE (mm)	STENCIL DAP APERTURE (mm)	NUMBER OF DAP APERTURE OPENINGS	GAP BETWEEN DAP APERTURE (Dim A mm)
DS90UB914A-Q1	48	RHS	0.25 x 0.6	0.5	5.1 x 5.1	0.25 x 0.7	1.1 x 1.1	16	0.2

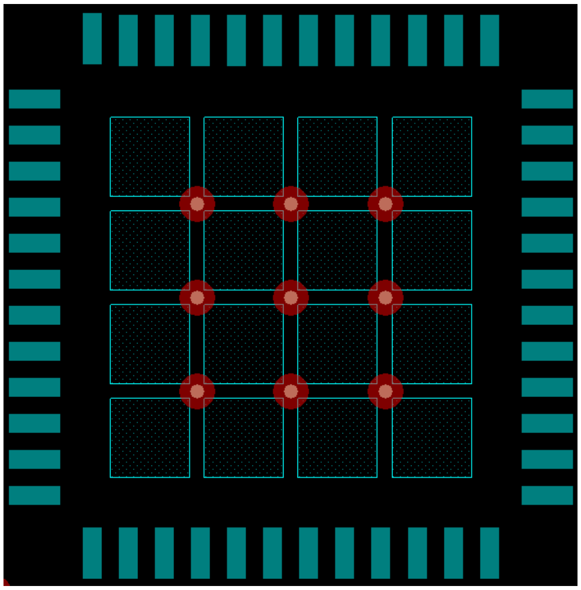


Figure 41. 48-Pin WQFN Stencil Example of Via and Opening Placement

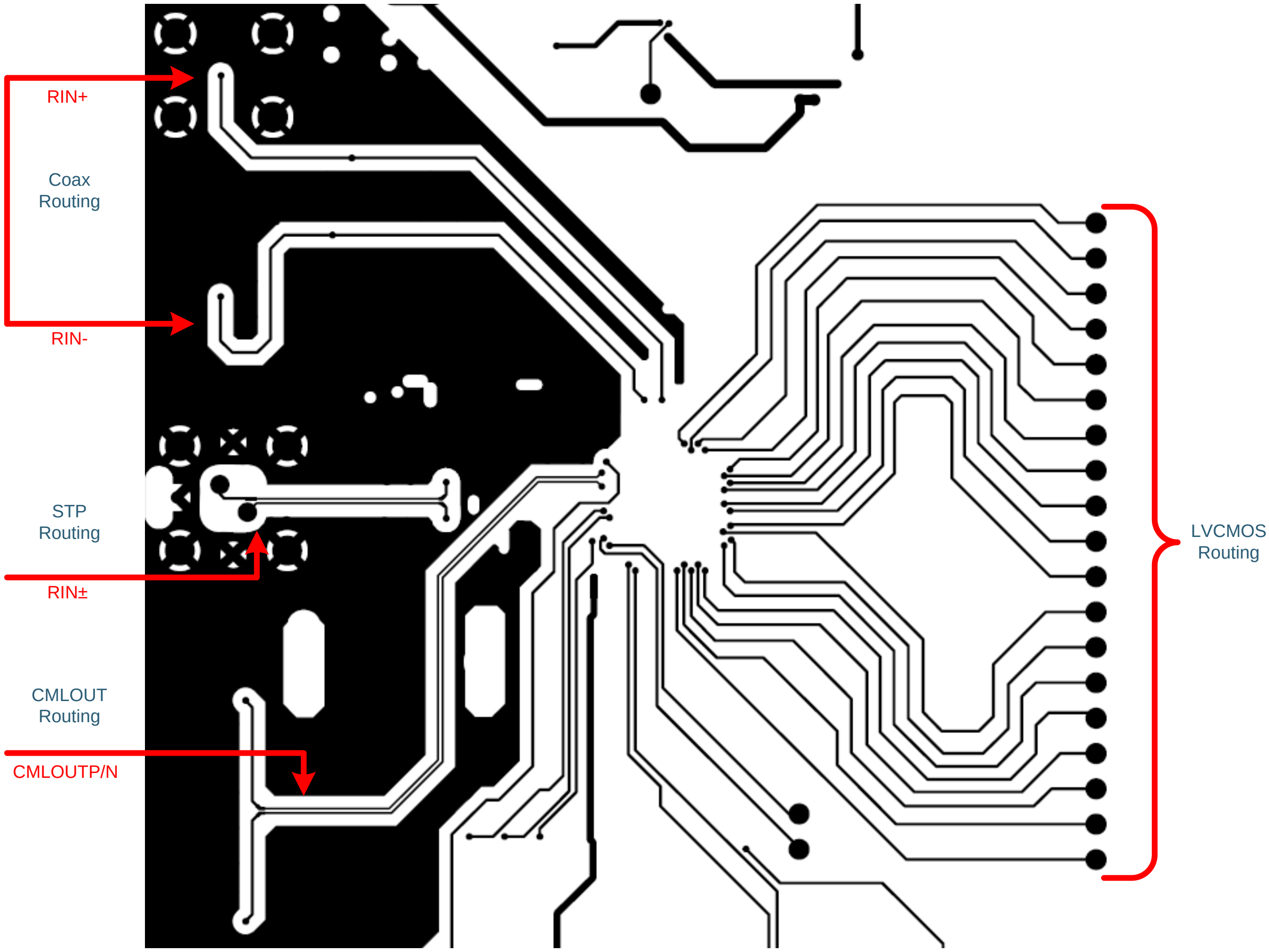


Figure 42. DS90UB914A-Q1 Deserializer Example Layout

The following PCB layout examples are derived from the layout design of the DS90UB914A-Q1 Evaluation Module (DS90UB913A-CXEVM and DS90UB914A-CXEVM REV A User's Guide). These graphics and additional layout description are used to demonstrate both proper routing and proper solder techniques when designing in this Deserializer.

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- *DS90UB913A-CXEVM & DS90UB914A-CXEVM REV A User's Guide*
- *I2C over DS90UB913/4 FPD-Link III with Bidirectional Control Channel*
- *Sending Power Over Coax in DS90UB913A Designs*
- *Soldering Specifications Application Report*
- *IC Package Thermal Metrics Application Report*
- *Leadless Leadframe Package (LLP) Application Report*
- *LVDS Owner's Manual*
- *Cable Requirements for the DS90UB913A & DS90UB914A*

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS90UB914ATRHSJQ1	ACTIVE	WQFN	RHS	48	2500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 105	UB914AQ	Samples
DS90UB914ATRHSRQ1	ACTIVE	WQFN	RHS	48	1000	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 105	UB914AQ	Samples
DS90UB914ATRHSTQ1	ACTIVE	WQFN	RHS	48	250	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 105	UB914AQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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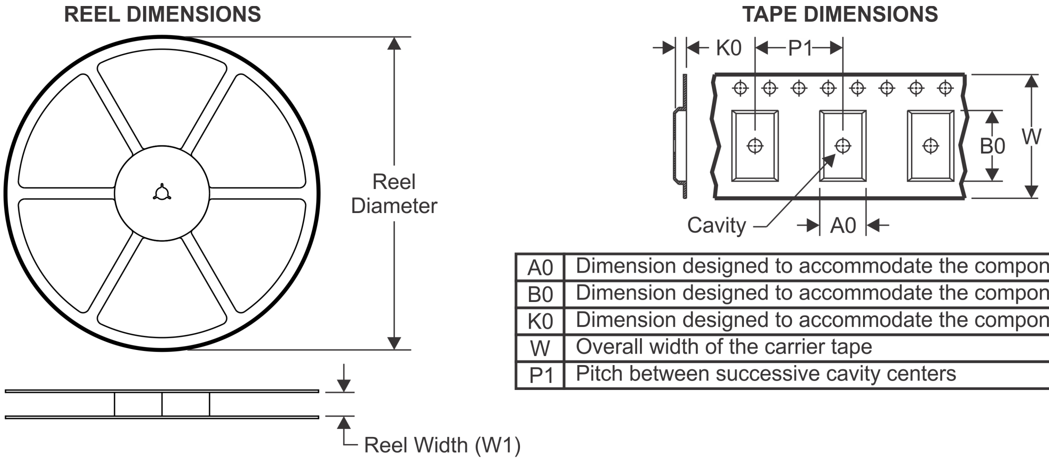
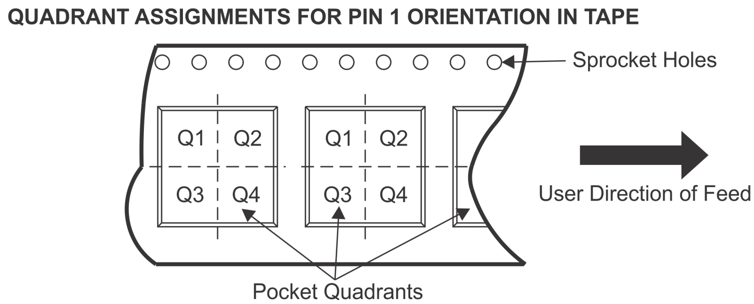
TAPE AND REEL INFORMATION



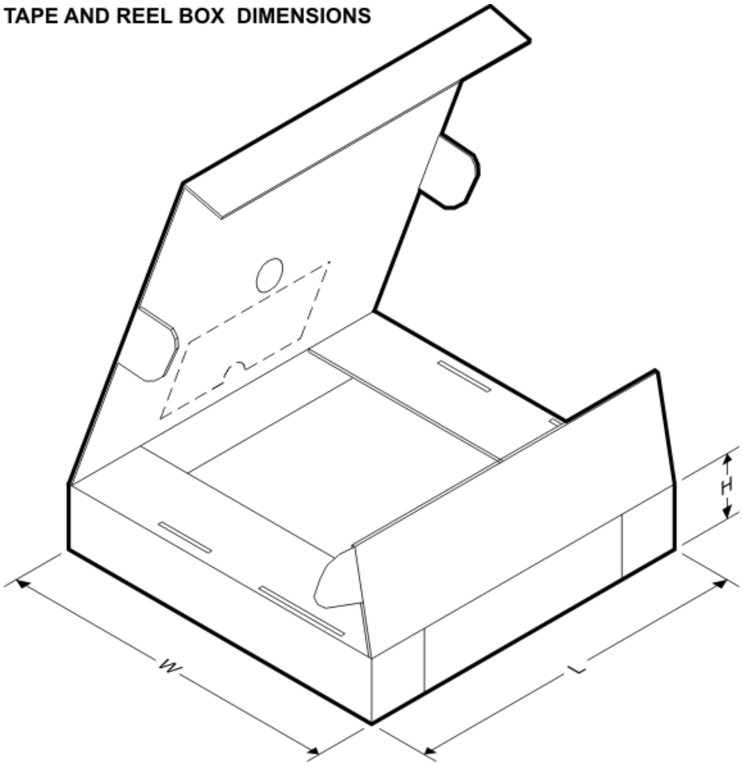
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

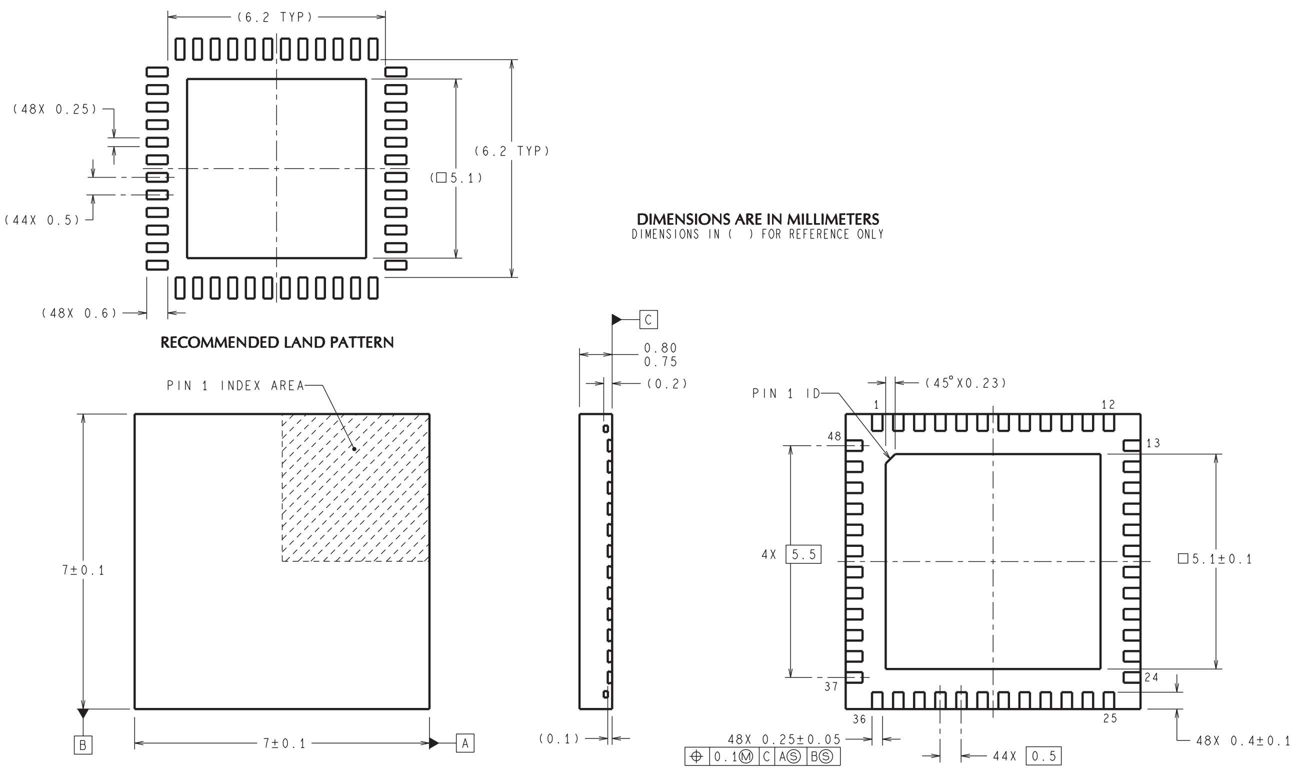
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS90UB914ATRHSJQ1	WQFN	RHS	48	2500	330.0	16.4	7.3	7.3	1.3	12.0	16.0	Q1
DS90UB914ATRHSRQ1	WQFN	RHS	48	1000	330.0	16.4	7.3	7.3	1.3	12.0	16.0	Q1
DS90UB914ATRHSTQ1	WQFN	RHS	48	250	178.0	16.4	7.3	7.3	1.3	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS90UB914ATRHSJQ1	WQFN	RHS	48	2500	367.0	367.0	38.0
DS90UB914ATRHSRQ1	WQFN	RHS	48	1000	367.0	367.0	38.0
DS90UB914ATRHSTQ1	WQFN	RHS	48	250	210.0	185.0	35.0


(6.2 TYP)
(48X 0.25)
(6.2 TYP)
(□5.1)
(44X 0.5)
(48X 0.6)
RECOMMENDED LAND PATTERN
DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY
PIN 1 INDEX AREA
7±0.1
7±0.1
B
A
C
0.80
0.75
(0.2)
(0.1)
PIN 1 ID
(45°X0.23)
1
12
13
24
25
36
37
48
4X 5.5
□5.1±0.1
48X 0.25±0.05
0.1 M C A S B S
44X 0.5
48X 0.4±0.1

SQA48A (Rev B)

IMPORTANT NOTICE