ISO35T Isolated 3.3V RS-485 Transceiver With Integrated Transformer Driver

1 Features

- Designed for RS-485 and RS-422 Applications
- Signaling Rates up to 1 Mbps
- 1/8 Unit Load – up to 256 Nodes on a Bus
- Thermal Shutdown Protection
- Typical Efficiency > 60% (I_{LOAD} = 100 mA) - See *SLUU470*
- Low-Driver Bus Capacitance 16 pF (Typical)
- Fail-Safe Receiver for Bus Open, Short, Idle
- Logic Inputs are 5-V Tolerant
- 50-kV/µs Typical Transient Immunity
- Bus-Pin ESD Protection
  - 16-kV HBM Between Bus-Pins and GND2
  - 6-kV HBM Between Bus-Pins and GND1
- Safety and Regulatory Approvals
  - 4242 V_{PK} Basic Insulation per DIN V VDE V 0884-10 and DIN EN 61010-1
  - 2500 V_{RMS} Isolation for 1 minute per UL 1577
  - CSA Component Acceptance Notice 5A, IEC 60950-1 and IEC 61010-1 Standards

2 Applications

- Isolated RS-485/RS-422 Interfaces
- Factory Automation
- Motor/Motion Control
- HVAC and Building Automation Networks
- Networked Security Stations

3 Description

The ISO35T is an isolated differential line transceiver with integrated oscillator outputs that provide the primary voltage for an isolation transformer. The device is a full-duplex differential line transceiver for RS-485 and RS-422 applications that can easily be configured for half-duplex operation by connecting pin 11 to pin 14, and pin 12 to pin 13.

These devices are ideal for long transmission lines since the ground loop is broken to allow for a much larger common-mode voltage range. The symmetrical isolation barrier of the device is tested to provide 4242V_{PK} of isolation per VDE for 60s between the bus-line transceiver and the logic-level interface.

Any cabled I/O can be subjected to electrical noise transients from various sources. These noise transients can cause damage to the transceiver and/or near-by sensitive circuitry if they are of sufficient magnitude and duration. The ISO35T can significantly reduce the risk of data corruption and damage to expensive control circuits.

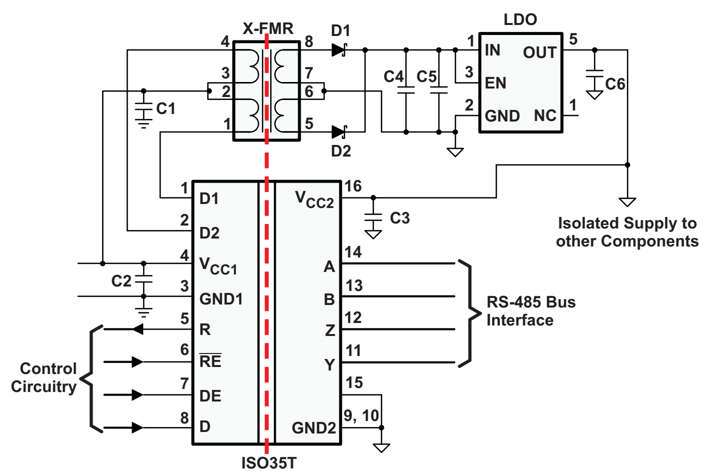
The ISO35T is specified for use from –40°C to 85°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ISO35T	SOIC (16)	10.30 mm × 7.50 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Typical Application Circuit



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (July 2011) to Revision D — **Page**

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- VDE standard changed to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 ... 1

Changes from Revision B (June 2011) to Revision C — **Page**

- Deleted MIN and MAX values from the t_{r_D}, t_{f_D}, and t_{BBM} specifications in theTransformer Driver Chara table. ... 6
- Changed conditions statement from 1.9V to 2.4V; and changed TYP value from 230 to 350 for f_{St} specification in Transformer Driver Characteristics table. ... 6
- Added "D1 and D2 connected to 50-Ω pull-up resistors" to conditions statement for t_{r_D}, t_{f_D}, and t_{BBM} specifications in theTransformer Driver Chara table. ... 6

Changes from Revision A (March 2011) to Revision B — **Page**

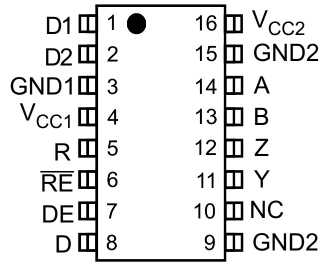
- Changed pin 16 From: V_{CC1} To: V_{CC2} in the DW Package drawing ... 3

Changes from Original (November 2010) to Revision A — **Page**

- Changed the data sheet From: Product Preview To: Production data ... 1

5 Pin Configuration and Functions

DW Package
16-Pin SOIC
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
A	14	I	Non-inverting Receiver Input
B	13	I	Inverting Receiver Input
D	8	I	Driver Input
D1	1	O	Transformer Driver Terminal 1, Open-Drain Output
D2	2	O	Transformer Driver Terminal 2, Open-Drain Output
DE	7	I	Driver Enable Input
GND1	3	–	Logic-side Ground
GND2	9, 15	–	Bus-side Ground. Both pins are internally connected.
NC	10	–	No Connect. This pin is not connected to any internal circuitry.
R	5	O	Receiver Output
$\overline{RE}$	6	I	Receiver Enable Input. This pin has complementary logic.
V_{CC1}	4	–	Logic-side Power Supply
V_{CC2}	16	–	Bus-side Power Supply
Y	11	O	Non-inverting Driver Output
Z	12	O	Inverting Driver Output

6 Specifications

6.1 Absolute Maximum Ratings

See [(1)]

		MIN	MAX	UNIT
V_{CC1},V_{CC2}	Input supply voltage[(2)]	–0.3	6	V
V_A,V_B,V_Y,V_Z	Voltage at any bus I/O terminal (A, B, Y, Z)	–9	14	V
V_{D1},V_{D2}	Voltage at D1, D2		14	V
$V_{(TRANS)}$	Voltage input, transient pulse through 100Ω, see Figure 22 (A,B,Y,Z)	–50	50	V
V_I	Voltage input at any D, DE or $\overline{RE}$ terminal	–0.5	7	V
I_O	Receiver output current	–10	10	mA
I_{D1},I_{D2}	Transformer Driver Output Current		450	mA
T_J	Maximum junction temperature		170	°C
T_{STG}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values except differential I/O bus voltages are with respect to network ground terminal and are peak voltage values.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 [1]	Bus pins and GND1	±6000	V
			Bus pins and GND2	±16000	
			All pins	±4000	
		Charged-device model (CDM), per JEDEC specification JESD22-C101 [2]		±1500	
		Machine model (MM), ANSI/ESDS5.2-1996		±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC1},V_{CC2}	Supply Voltage		3	3.3	3.6	V
V_I or V_{IC}	Voltage at any bus terminal (separately or common-mode)		–7		12	V
V_{IH}	High-level input voltage	D, DE, $\overline{RE}$	2		V_{CC}	V
V_{IL}	Low-level input voltage		0		0.8	
V_{ID}	Differential input voltage	A with respect to B	–12		12	V
R_L	Differential load resistance		54	60		Ω
I_O	Output Current	Driver	–60		60	mA
		Receiver	–8		8	
T_A	Ambient temperature		-40		85	°C
T_J	Operating junction temperature		–40		150	°C
$1 / t_{UI}$	Signaling Rate				1	Mbps

6.4 Thermal Information

THERMAL METRIC [1]		ISO35T DW (SOIC) 16 PINS	UNIT
$R_{θJA}$	Junction-to-ambient thermal resistance	80.5	°C/W
$R_{θJC(top)}$	Junction-to-case (top) thermal resistance	43.8	°C/W
$R_{θJB}$	Junction-to-board thermal resistance	49.7	°C/W
$ψ_{JT}$	Junction-to-top characterization parameter	13.8	°C/W
$ψ_{JB}$	Junction-to-board characterization parameter	41.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Power Ratings

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	VALUE	UNIT
P_D	Maximum device power dissipation	V_{CC1} = V_{CC2} = 3.6 V, T_J = 150°C, R_L = 54 Ω, C_L = 50 pF (Driver), C_L = 15 pF (Receiver), Input a 0.5-MHz 50% duty cycle square wave to Driver and Receiver	373	mW

6.6 Supply Current and Common Mode Transient Immunity

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC1} (1)	Logic-side quiescent supply current	DE & $\overline{RE}$ = 0V or V_{CC1} (Driver and Receiver Enabled or Disabled), D = 0 V or V_{CC1}, No load		4.5	8	mA
I_{CC2} (1)	Bus-side quiescent supply current	$\overline{RE}$ = 0 V or V_{CC1}, DE = 0 V (driver disabled), No load		7.5	13	mA
		$\overline{RE}$ = 0 V or V_{CC1}, DE = V_{CC1} (driver enabled), D = 0 V or V_{CC1}, No Load		9	16	
CMTI	Common-mode transient immunity	See Figure 23	25	50		kV/μs

(1) I_{CC1} and I_{CC2} are measured when device is connected to external power supplies, V_{CC1} & V_{CC2}. In this case, D1 & D2 are open and disconnected from external transformer.

6.7 RS-485 Driver Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$\|V_{OD}\|$	Differential output voltage magnitude	I_O = 0 mA (No Load)		2.5		V_{CC2}	V
		R_L = 54 Ω (RS-485), See Figure 11		1.5	2		
		R_L = 100 Ω (RS-422) (1), See Figure 11		2	2.3		
		V_{test} = –7 V to +12 V, See Figure 12		1.5			
$\Delta\|V_{OD}\|$	Change in magnitude of the differential output voltage	See Figure 11 and Figure 12		–0.2	0	0.2	V
$V_{OC(SS)}$	Steady-state common-mode output voltage	See Figure 13		1	2.6	3	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage	See Figure 13		–0.1		0.1	V
$V_{OC(pp)}$	Peak-to-peak common-mode output voltage	See Figure 13			0.25		V
I_I	Input current, D & DE	V_I at 0 V or V_{CC1}		–10		10	μA
I_{OZ}	High-impedance state output current	V_Y or V_Z = 12V, V_{CC} = 0 V or 3 V, DE = 0 V	Other input at 0 V			90	μA
		V_Y or V_Z = –7 V, V_{CC} = 0 V or 3 V, DE = 0 V		–10			
$I_{OS(P)}$ (2)	Peak short-circuit output current	V_Y or V_Z = –7 V to +12 V, See Figure 14	Other input at 0 V		300		mA
$I_{OS(SS)}$ (2)	Steady-state short-circuit output current	V_Y or V_Z = –7 V to +12 V, See Figure 14		-250		250	mA
$C_{(OD)}$	Differential output capacitance	V_I = 0.4 sin (4E6πt) + 0.5V, DE at 0 V			16		pF

(1) V_{CC2} = 3.3 V ± 5%
(2) This device has thermal shutdown and output current-limiting features to protect in short-circuit fault condition.

6.8 RS-485 Receiver Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{IT(+)}$	Positive-going input threshold voltage	I_O = -8 mA				–20	mV
$V_{IT(–)}$	Negative-going input threshold voltage	I_O = 8 mA		–200			mV
V_{hys}	Hysteresis voltage (V_{IT+} – $V_{IT–}$)				50		mV
V_{OH}	High-level output voltage	See Figure 18; V_{ID} = +200 mV, I_O = -8 mA		2.4			V
V_{OL}	Low-level output voltage	See Figure 18; V_{ID} = –200 mV, I_O = 8 mA				0.4	V
$I_{O(Z)}$	High-impedance state output current	V_O = 0 or V_{CC1}, $\overline{RE}$ = V_{CC1}		–1		1	µA
I_A, I_B	Bus input current	V_A or V_B = 12 V	Other input at 0 V		50	100	µA
		V_A or V_B = 12 V, V_{CC2} = 0 V			60	100	
		V_A or V_B = –7 V		–100	–40		
		V_A or V_B = -7 V, V_{CC2} = 0 V		–100	–30		
I_{IH}	High-level input current, $\overline{RE}$	V_{IH} = 2. V		–10		10	µA
I_{IL}	Low-level input current, $\overline{RE}$	VIL = 0.8 V		–10		10	
R_{ID}	Differential input resistance	Measured between A & B		96			kΩ
C_{ID}	Differential input capacitance	V_I = 0.4 sin (4E6πt) + 0.5V, DE at 0 V			2		pF

6.9 Transformer Driver Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{OSC}	Oscillator frequency	V_{CC1} = 3.3V ± 10%, D1 and D2 connected to Transformer	300	400	550	kHz
R_{ON}	Switch on resistance	D1 and D2 connected to 50Ω pull-up resistors		1	2.5	Ω
t_{r_D}	D1, D2 output rise time	V_{CC1} = 3.3V ± 10%, see Figure 24, D1 and D2 connected to 50-Ω pull-up resistors.		70		ns
t_{f_D}	D1, D2 output fall time	V_{CC1} = 3.3V ± 10%, see Figure 24, D1 and D2 connected to 50-Ω pull-up resistors.		80		ns
f_{St}	Startup frequency	V_{CC1} = 2.4 V, D1 and D2 connected to Transformer		350		kHz
t_{BBM}	Break before make time delay	V_{CC1} = 3.3V ± 10%, see Figure 24, D1 & D2 connected to 50-Ω pull-up resistors.		140		ns

6.10 RS-485 Driver Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay	See Figure 15		205	340	ns
$t_{sk(p)}$	Pulse skew (|t_{PHL} – t_{PLH}|)			1.5		
t_r	Differential output signal rise time		120	185	300	
t_f	Differential output signal fall time		120	180	300	
t_{PHZ}	Propagation delay, high-level-to-high-impedance output	See Figure 16			205	ns
t_{PZH}	Propagation delay, high-impedance-to-high-level output				530	
t_{PLZ}	Propagation delay, low-level to high-impedance output	See Figure 17			330	
t_{PZL}	Propagation delay, high-impedance-to-low-level output				530	

6.11 RS-485 Receiver Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay	See Figure 19		85	115	ns
$t_{sk(p)}$	Pulse skew ($\|t_{PHL} – t_{PLH}\|$)				13	
t_r	Output signal rise time			1	4	
t_f	Output signal fall time			1	4	
t_{PHZ}, t_{PZH}	Propagation delay, high-level to high-impedance output Propagation delay, high-impedance to high-level output	See Figure 20, DE at 0 V		13	25	ns
t_{PLZ} t_{PZL}	Propagation delay, low-level to high-impedance output Propagation delay, high-impedance to low-level output	See Figure 21, DE at 0 V		13	25	

6.12 Typical Characteristics

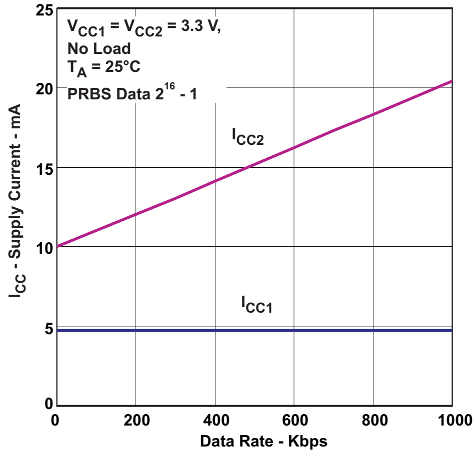


Figure 1. Supply Current vs Data Rate With No Load

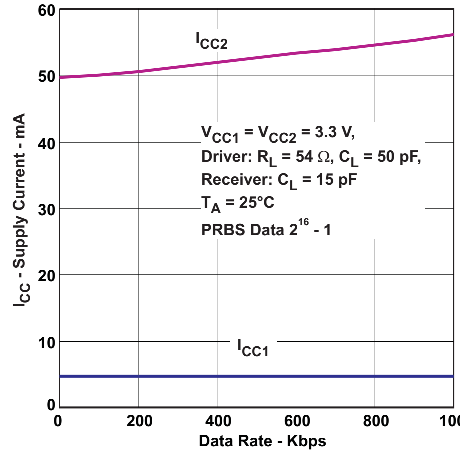


Figure 2. Supply Current vs Data Rate With Load

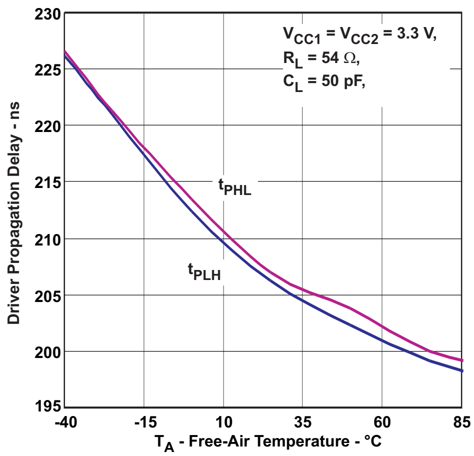


Figure 3. Driver Propagation Delay vs Free-Air Temperature

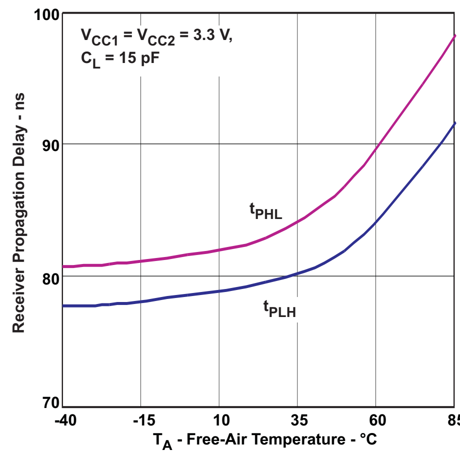


Figure 4. Receiver Propagation Delay vs Free-Air Temperature

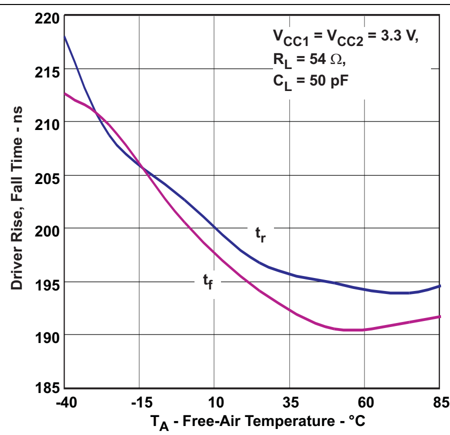


Figure 5. Driver Rise, Fall Time vs Free-Air Temperature

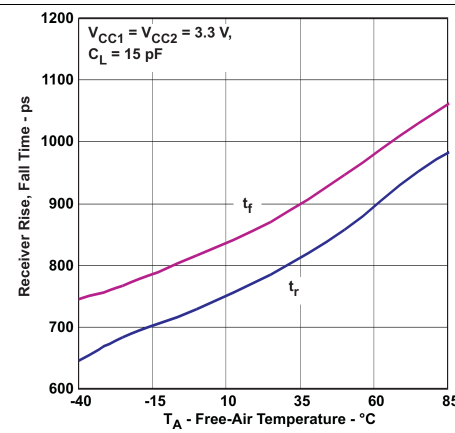


Figure 6. Receiver Rise, Fall Time vs Free-Air Temperature

Typical Characteristics (continued)

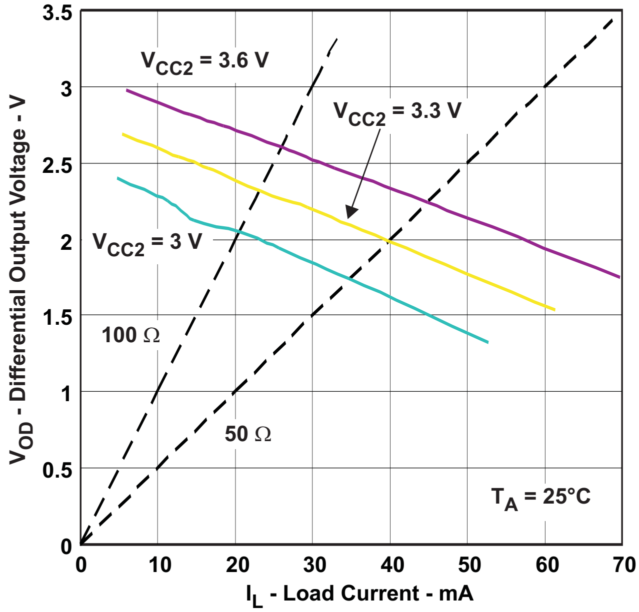


Figure 7. Differential Output Voltage vs Load Current

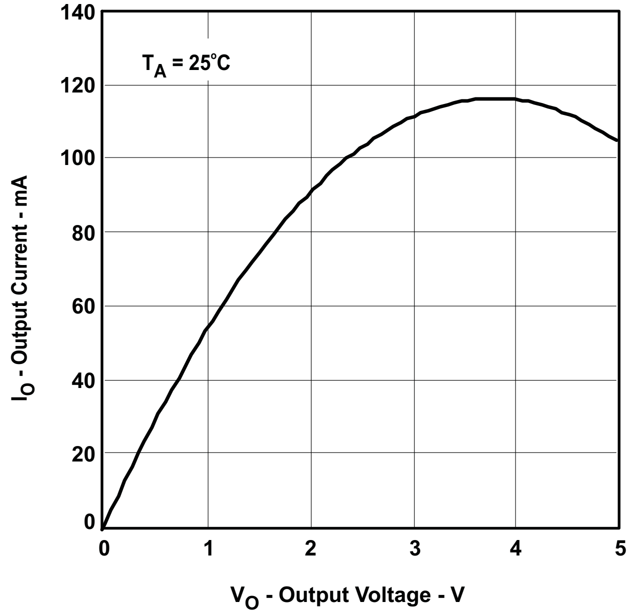


Figure 8. Receiver Low-Level Output Current vs Low-Level Output Voltage

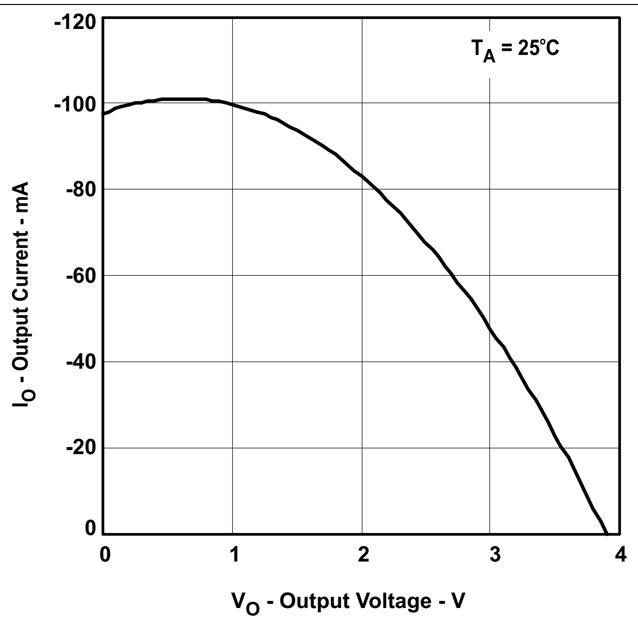


Figure 9. Receiver High-Level Output Current vs High-Level Output Voltage

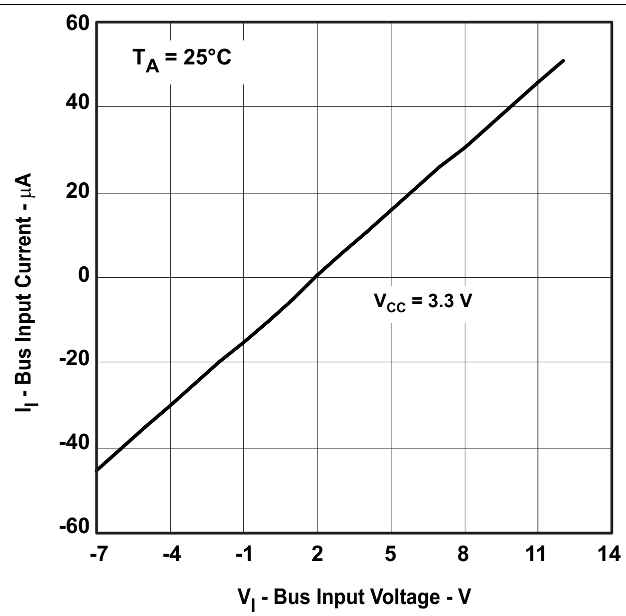


Figure 10. Bus Input Current vs Input Voltage

7 Parameter Measurement Information

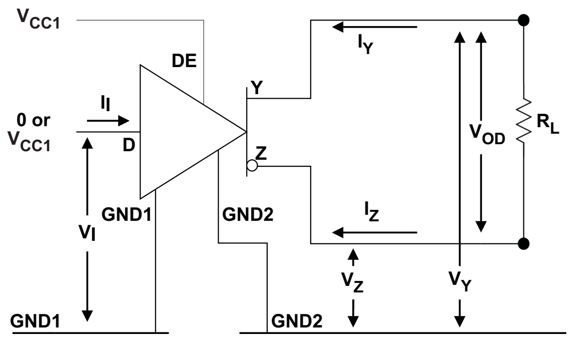


Figure 11. Driver V_{OD} Test and Current Definitions

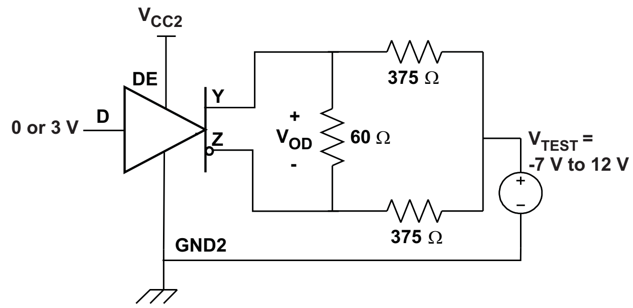


Figure 12. Driver V_{OD} With Common-Mode Loading Test Circuit

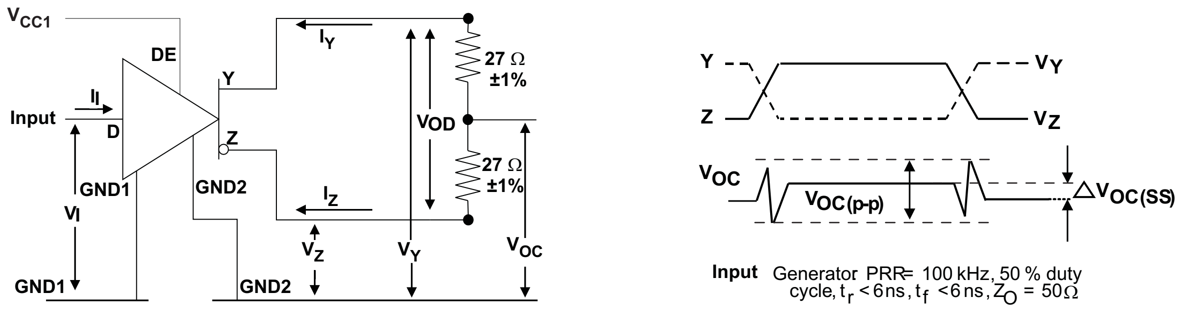


Figure 13. Test Circuit and Waveform Definitions For The Driver Common-Mode Output Voltage

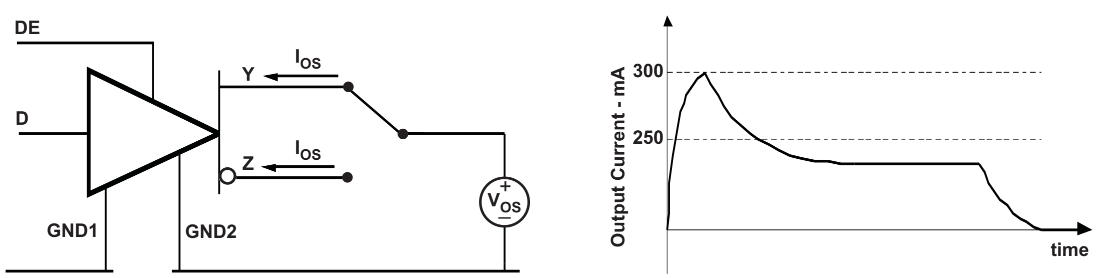


Figure 14. Driver Short-Circuit Test Circuit and Waveforms (Short Circuit applied at Time t=0

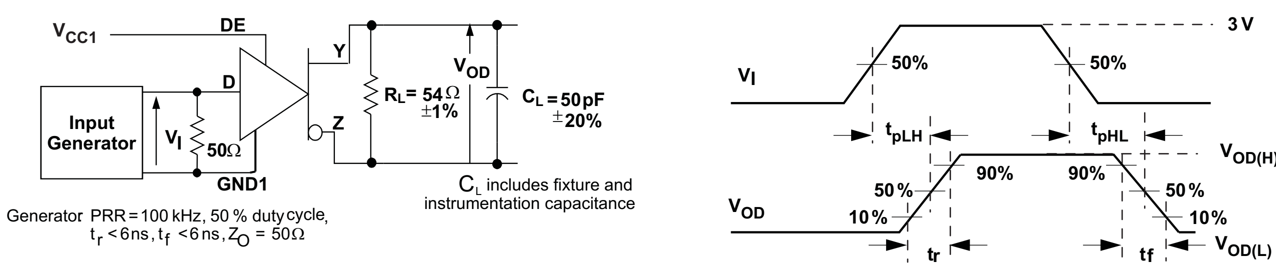


Figure 15. Driver Switching Test Circuit and Voltage Waveforms

Parameter Measurement Information (continued)

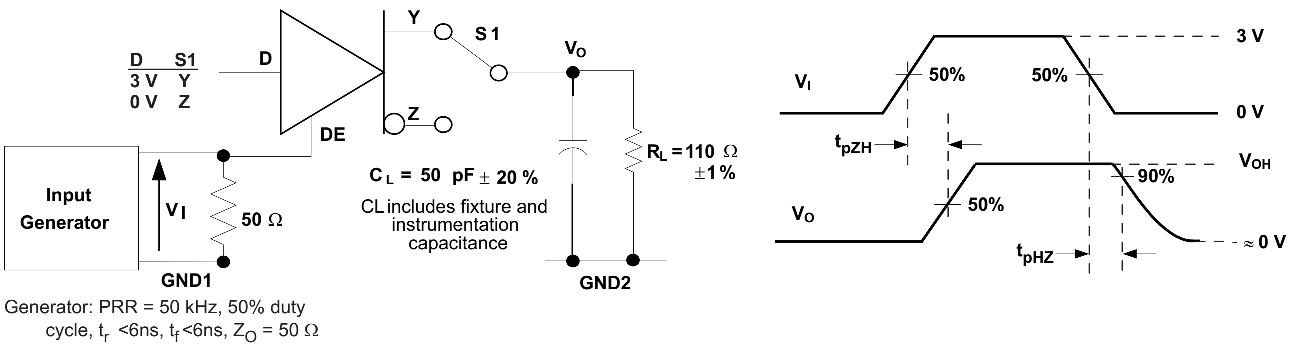


Figure 16. Driver High-Level Output Enable and Disable Time Test Circuit and Voltage Waveforms

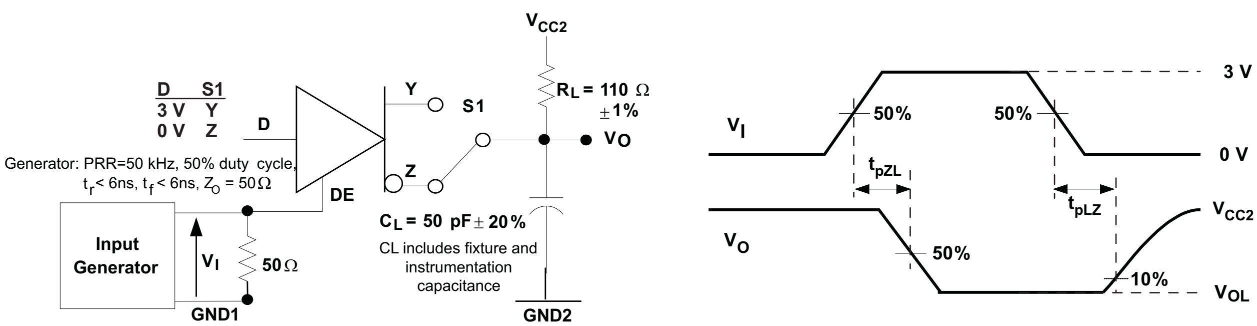


Figure 17. Driver Low-Level Output Enable and Disable Time Test Circuit and Voltage Waveform

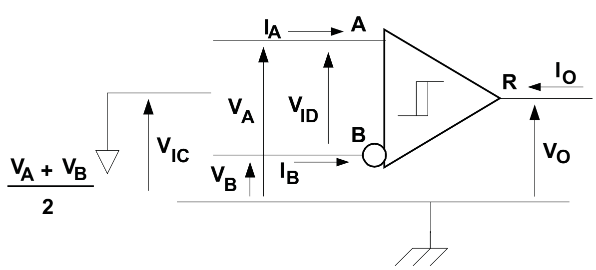


Figure 18. Receiver Voltage and Current Definitions

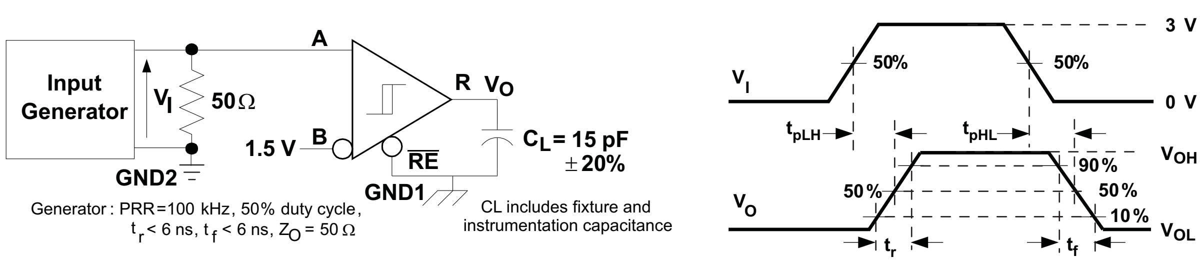


Figure 19. Receiver Switching Test Circuit and Waveforms

Parameter Measurement Information (continued)

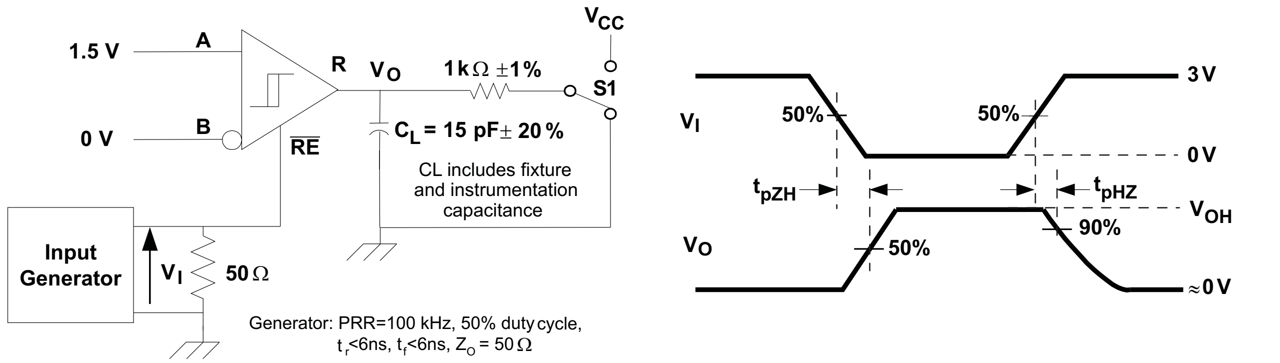


Figure 20. Receiver Enable Test Circuit and Waveforms, Data Output High

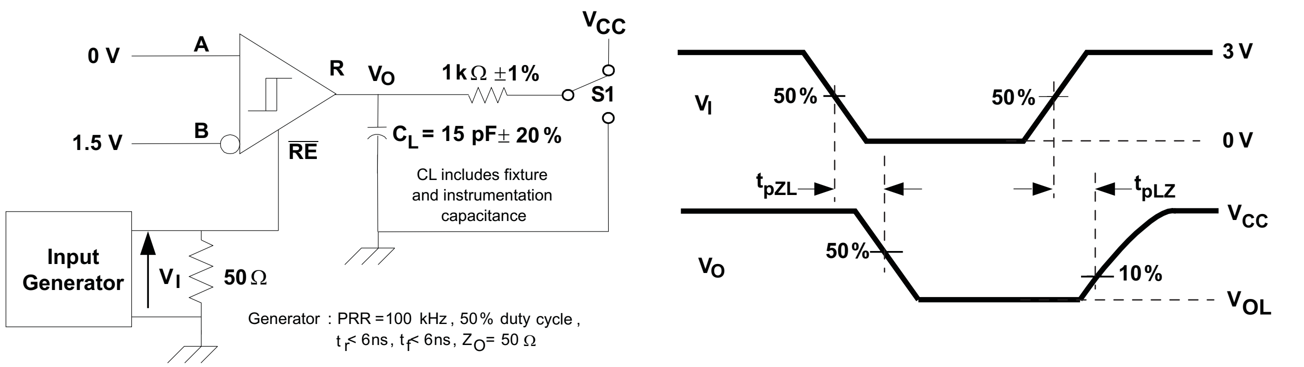


Figure 21. Receiver Enable Test Circuit and Waveforms, Data Output Low

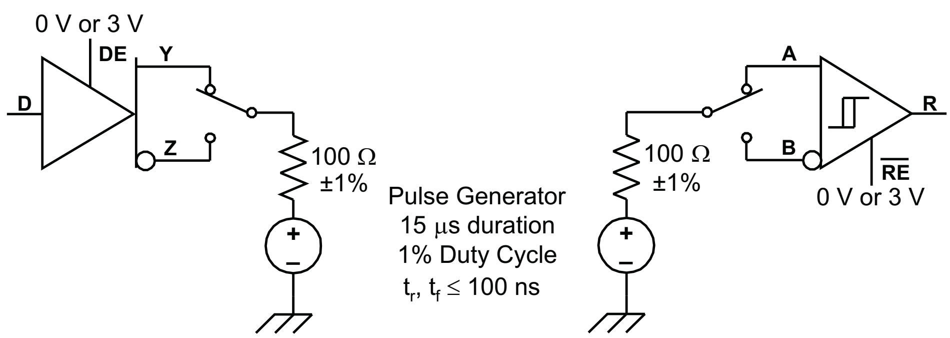


Figure 22. Transient Over-Voltage Test Circuit

Parameter Measurement Information (continued)

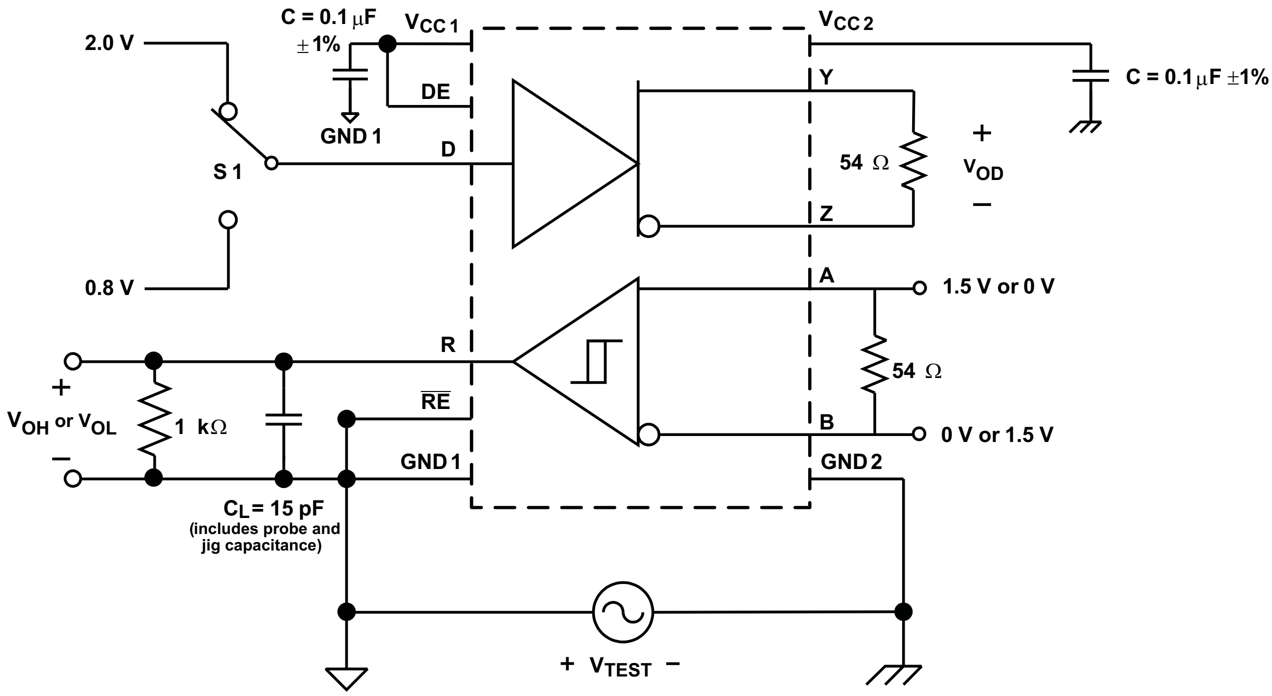


Figure 23. Common-Mode Transient Immunity Test Circuit

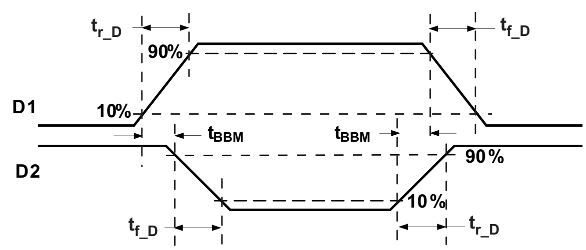


Figure 24. Transition Times and Break-Before-Make Time Delay for D1, D2 Outputs

8 Detailed Description

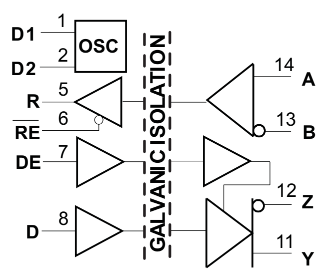
8.1 Overview

ISO35T is an isolated full-duplex differential transceiver with integrated transformer driver. The integrated transformer driver supports elegant secondary power supply design. This device is rated to provide galvanic isolation up to 4242 V_{PK} per VDE and 2500 V_{RMS} per UL. It has active-high driver enable and active-low receiver enable to control the data flow. It is suitable for data transmission up to 1 Mbps.

When the driver enable pin, DE, is logic high, the differential outputs Y and Z follow the logic states at data input D. A logic high at D causes Y to turn high and Z to turn low. In this case the differential output voltage defined as $V_{OD} = V_{(Y)} – V_{(Z)}$ is positive. When D is low, the output states reverse, Z turns high, Y becomes low, and V_{OD} is negative. When DE is low, both outputs turn high-impedance. In this condition the logic state at D is irrelevant. The DE pin has an internal pulldown resistor to ground, thus when left open the driver is disabled (high-impedance) by default. The D pin has an internal pullup resistor to V_{CC}, thus, when left open while the driver is enabled, output Y turns high and Z turns low.

When the receiver enable pin, $\overline{RE}$, is logic low, the receiver is enabled. When the differential input voltage defined as $V_{ID} = V_{(A)} – V_{(B)}$ is positive and higher than the positive input threshold, V_{IT+}, the receiver output, R, turns high. When V_{ID} is negative and lower than the negative input threshold, $V_{IT–}$, the receiver output, R, turns low. If V_{ID} is between V_{IT+} and $V_{IT–}$ the output is indeterminate. When $\overline{RE}$ is logic high or left open, the receiver output is high-impedance and the magnitude and polarity of V_{ID} are irrelevant. Internal biasing of the receiver inputs causes the output to go failsafe-high when the transceiver is disconnected from the bus (open-circuit), the bus lines are shorted (short-circuit), or the bus is not actively driven (idle bus).

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Insulation and Safety Related Specifications for 16-DW Package

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
L(I01)	Minimum air gap (Clearance[(1)])	Shortest terminal to terminal distance through air	8			mm
L(I02)	Minimum external tracking (Creepage[(1)])	Shortest terminal to terminal distance across the package surface	8			mm
CTI	Comparative Tracking Index (Tracking resistance)	DIN EN 60112 (VDE 0303-11); IEC 60112	400			V
DTI	Distance through the insulation	Minimum Internal Gap (Internal Clearance)	0.008			mm
R_{IO}	Isolation resistance	Input to output, V_{IO} = 500 V, all pins on each side of the barrier tied together creating a two-terminal device, T_A = 25 °C		$>10^{12}$		Ω
C_{IO}	Barrier capacitance Input to output	V_{IO} = 0.4 sin (2πft), f = 1 MHz		2		pF
C_I	Input capacitance to ground	$V_I = V_{CC}/2$ + 0.4 sin (2πft), f = 1 MHz, V_{CC} = 5 V		2		pF

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed circuit board do not reduce this distance. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.

8.3.2 IEC 60664-1 Ratings Table

PARAMETER	TEST CONDITIONS	SPECIFICATION
Material group		II
Overvoltage category / Installation classification for basic insulation	Rated mains voltage ≤ 150 V_{RMS}	I-IV
	Rated mains voltage ≤ 300 V_{RMS}	I-III

8.3.3 DIN V VDE V 0884-10 Insulation Characteristics (1)

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SPECIFICATION	UNIT
V_{IORM}	Maximum working isolation voltage		566	V_{PK}
V_{PR}	Input to output test voltage	Method b1, $V_{PR} = V_{IORM} \times 1.875$, 100% Production test with t = 1 s, Partial discharge < 5 pC	1062	V_{PK}
		Method a, After environmental tests subgroup 1, $V_{PR} = V_{IORM} \times 1.6$, t = 10 s, Partial discharge < 5pC	906	
		After Input/Output Safety Test Subgroup 2/3, $V_{PR} = V_{IORM}$ x 1.2, t = 10 s, Partial discharge < 5 pC	680	
V_{IOTM}	Maximum transient isolation voltage	t = 60 s (Qualification) t = 1 s (100% Production)	4242	V_{PK}
V_{IOSM}	Maximum surge isolation voltage	Tested per IEC 60065, 1.2/50 µs waveform, V_{TEST} = 1.3 x V_{IOSM} = 4000 V_{PK}(Qualification Test)	3077	V_{PK}
R_S	Isolation resistance	V_{IO} = 500 V at T_S = 150 °C	> 10^9	Ω
	Pollution degree		2	

(1) Climatic Classification 40/125/21

8.3.4 Regulatory Information

VDE	CSA	UL
Certified according to DIN V VDE V 0884-10(VDE V 0884-10):2006-12 and DIN EN 61010-1 (VDE 0411-1)	Approved according to CSA Component Acceptance Notice 5A, IEC 60959-1 and IEC 61010-1	Approved under UL 1577 Component Recognition Program
Basic Insulation Maximum Transient Isolation Voltage, 4242 V_{PK} Maximum Surge Isolation Voltage, 3077 V_{PK} Maximum Working Isolation Voltage, 566 V_{PK}	3000 V_{RMS} Isolation Rating; Reinforced insulation per CSA 61010-1-04 and IEC 61010-1 2nd Ed. 150 V_{RMS} working voltage; Basic insulation per CSA 61010-1-04 and IEC 61010-1 2nd Ed. 600 V_{RMS} working voltage; Basic insulation per CSA 60950-1-07 and IEC 60950-1 2nd Ed. 760 V_{RMS} working voltage	Single Protection, 2500 V_{RMS} (1)
Certificate Number: 40016131	Master Contract Number: 220991	File Number: E181974

(1) Production tested ≥ 3000 V_{RMS} for 1 second in accordance with UL 1577.

8.3.5 Safety Limiting Values

Safety limiting intends to prevent potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the IO can allow low resistance to ground or the supply. Without current limiting, sufficient power is dissipated to overheat the die and damage the isolation barrier—potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	DW-16	θ_{JA} = 80.5°C/W, V_I = 3.6V, T_J = 170°C, T_A = 25°C			500	mA
T_S	Maximum safety temperature					150	°C

The safety-limiting constraint is the maximum junction temperature specified for the device. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in *Thermal Information* is that of a device installed on the High-K Test Board for Leaded Surface Mount Packages. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

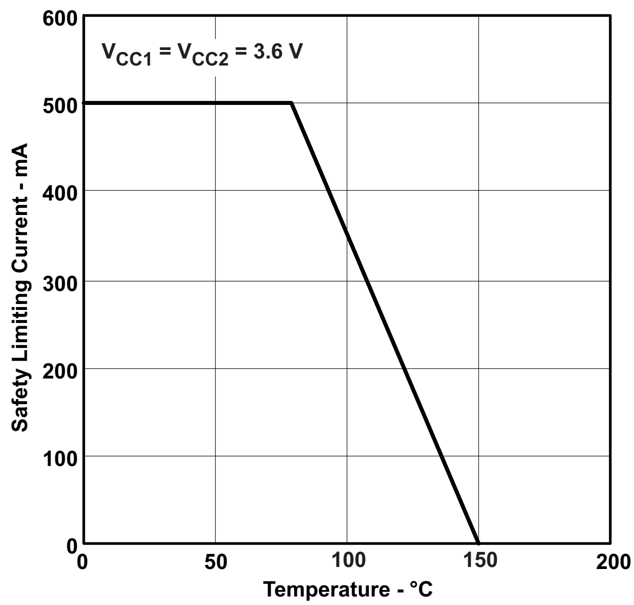


Figure 25. Thermal Derating Curve Per VDE

8.4 Device Functional Modes

Table 1 and Table 2 are the function tables for the ISO35T driver and receiver.

Table 1. Driver Function Table(1)

INPUT	ENABLE	OUTPUTS	
(D)	(DE)	Y	Z
H	H	H	L
L	H	L	H
X	L	hi-Z	hi-Z
X	OPEN	hi-Z	hi-Z
OPEN	H	H	L

(1) H = High Level, L= Low Level, X = Don't Care, hi-Z = High Impedance (Off)

Table 2. Receiver Function Table(1)

DIFFERENTIAL INPUT $V_{ID} = (V_A – V_B)$	ENABLE $(\overline{RE})$	OUTPUT (R)
–0.02 V ≤ V_{ID}	L	H
–0.2 V < V_{ID} –0.02 V	L	?
V_{ID} ≤ –0.2 V	L	L
X	H	hi-Z
X	OPEN	hi-Z
Open circuit	L	H

(1) H = High Level, L= Low Level, X = Don't Care, hi-Z = High Impedance (Off), ? = Indeterminate

Table 2. Receiver Function Table[(1)] (continued)

DIFFERENTIAL INPUT $V_{ID} = (V_A - V_B)$	ENABLE ($\overline{RE}$)	OUTPUT (R)
Short Circuit	L	H
Idle (terminated) bus	L	H

8.4.1 Device I/O Schematics

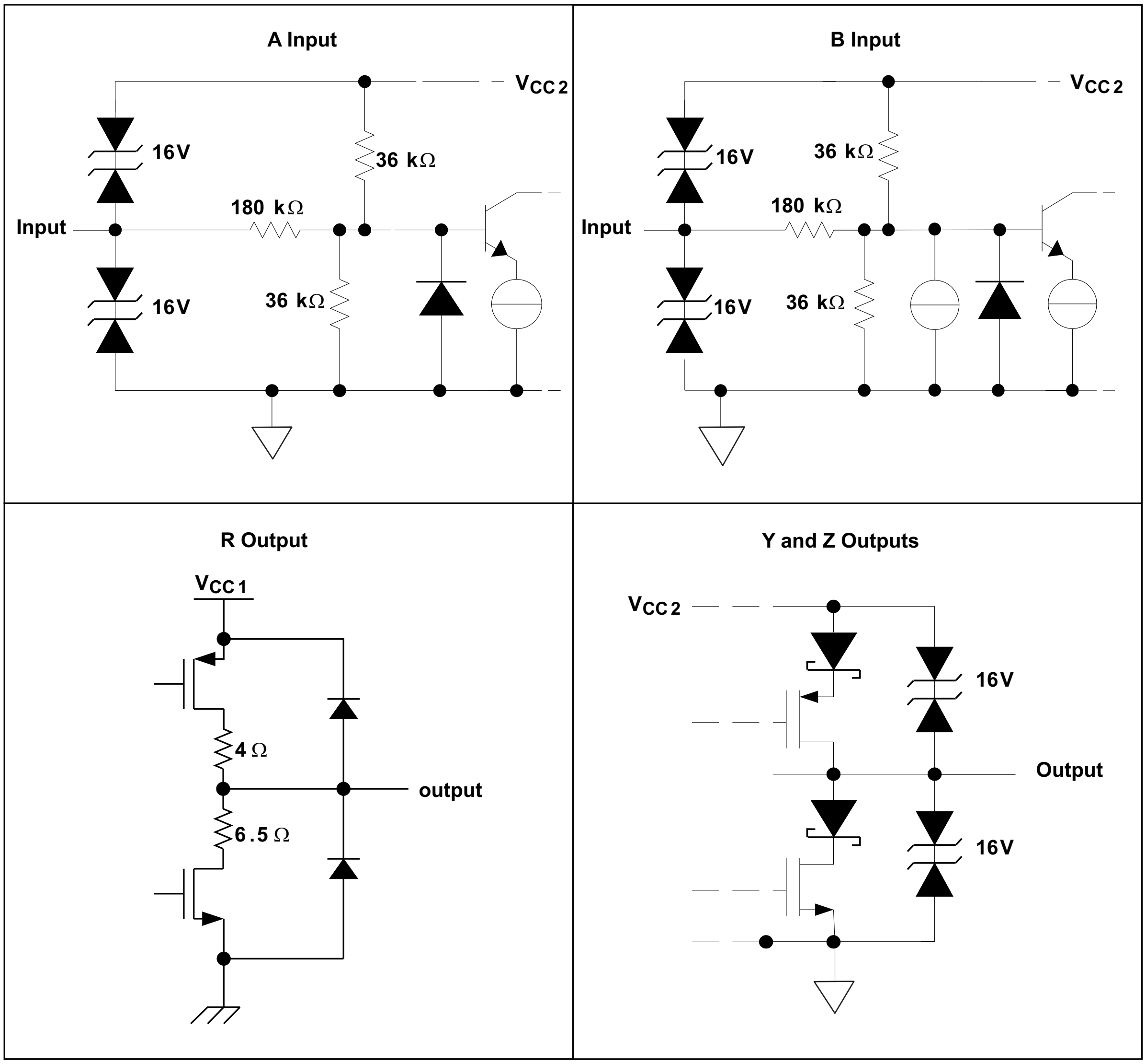


Figure 26. Equivalent Circuit Schematics

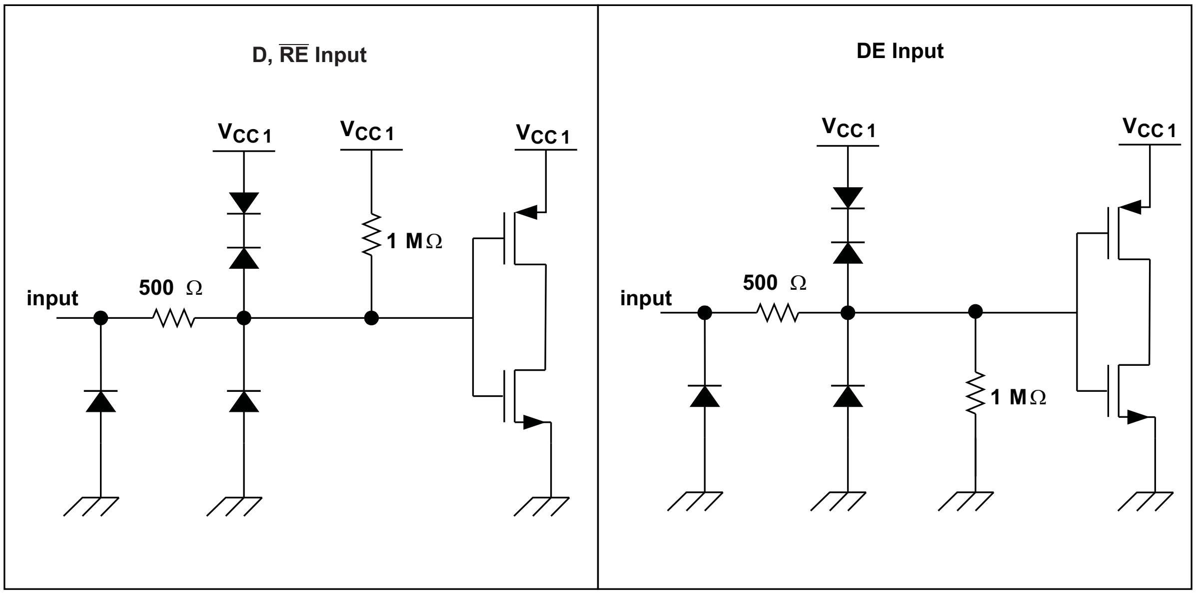


Figure 27. Equivalent Circuit Schematics

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

ISO35T is a full-duplex RS-485 transceiver commonly used for asynchronous data transmission. Full-duplex implementation requires two signal pairs (four wires), and allows each node to transmit data on one pair while simultaneously receiving data on the other pair. To eliminate line reflections, each cable end is terminated with a termination resistor, R(T), whose value matches the characteristic impedance, Z0, of the cable. This method, known as parallel termination, allows for higher data rates over longer cable length.

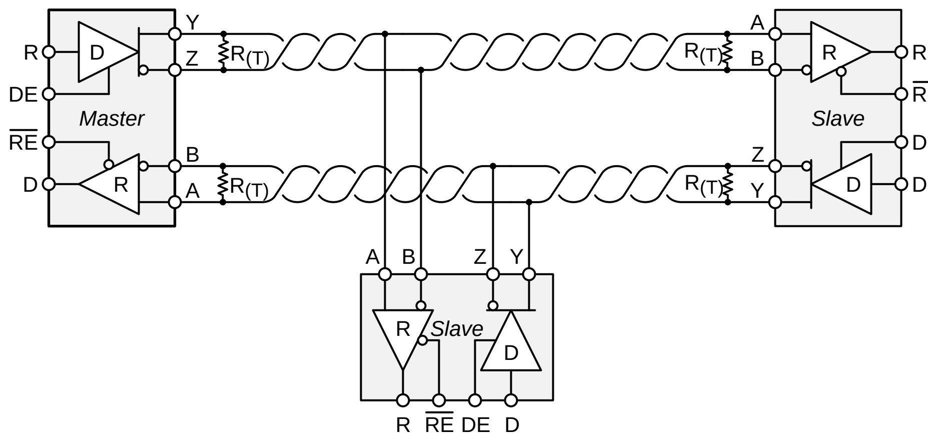


Figure 28. Typical RS-485 Network With Full-Duplex Transceivers

9.2 Typical Application

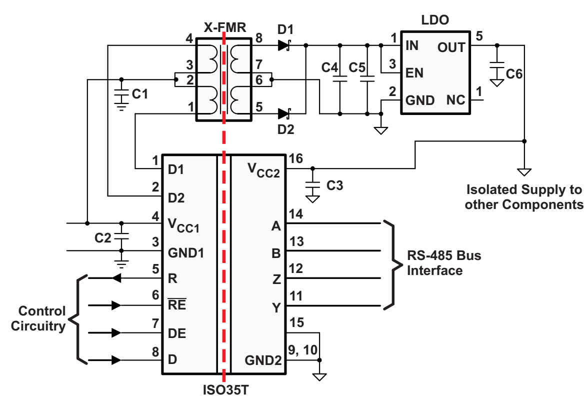


Figure 29. Typical Application Circuit

Typical Application (continued)

9.2.1 Design Requirements

RS-485 is a robust electrical standard suitable for long-distance networking that may be used in a wide range of applications with varying requirements, such as distance, data rate, and number of nodes.

Table 3. Design Parameters

PARAMETER	VALUE
Pullup and Pulldown Resistors	1 kΩ to 10 kΩ
Decoupling Capacitors	100 nF

9.2.2 Detailed Design Procedure

9.2.2.1 Transient Voltages

Isolation of a circuit insulates it from other circuits and earth so that noise develops across the insulation rather than circuit components. The most common noise threat to data-line circuits is voltage surges or electrical fast transients that occur after installation and the transient ratings of ISO35T are sufficient for all but the most severe installations. However, some equipment manufacturers use their ESD generators to test transient susceptibility of their equipment and can easily exceed insulation ratings. ESD generators simulate static discharges that may occur during device or equipment handling with low-energy but very high voltage transients.

Figure 30 models the ISO35T bus IO connected to a noise generator. C_{IN} and R_{IN} is the device and any other stray or added capacitance or resistance across the A or B pin to GND2, C_{ISO} and R_{ISO} is the capacitance and resistance between GND1 and GND2 of ISO35T plus those of any other insulation (transformer, etc.), and we assume stray inductance negligible. From this model, the voltage at the isolated bus return is shown in Equation 1 and will always be less than 16 V from V_N.

$$v_{GND2} = v_N \frac{Z_{ISO}}{Z_{ISO} + Z_{IN}} \tag{1}$$

If ISO35T is tested as a stand-alone device, R_{IN}= 6 × 10^4Ω, C_{IN}= 16 × 10^{-12} F, R_{ISO}= 10^9Ω and C_{ISO}= 10^{-12} F.

In Figure 30 the resistor ratio determines the voltage ratio at low frequency and it is the inverse capacitance ratio at high frequency. In the stand-alone case and for low frequency, use Equation 2, or essentially all noise appears across the barrier.

$$\frac{v_{GND2}}{v_N} = \frac{R_{ISO}}{R_{ISO} + R_{IN}} = \frac{10^9}{10^9 + 6 \times 10^4} \tag{2}$$

At very high frequency, Equation 3 is true and 94% of V_N appears across the barrier.

$$\frac{v_{GND2}}{v_N} = \frac{\frac{1}{C_{ISO}}}{\frac{1}{C_{ISO}} + \frac{1}{C_{IN}}} = \frac{1}{1 + \frac{C_{ISO}}{C_{IN}}} = \frac{1}{1 + \frac{1}{16}} = 0.94 \tag{3}$$

As long as R_{ISO} is greater than R_{IN} and C_{ISO} is less than C_{IN}, most of transient noise appears across the isolation barrier, as it should.

We recommend the reader not test equipment transient susceptibility with ESD generators or consider product claims of ESD ratings above the barrier transient ratings of an isolated interface. ESD is best managed through recessing or covering connector pins in a conductive connector shell and installer training.

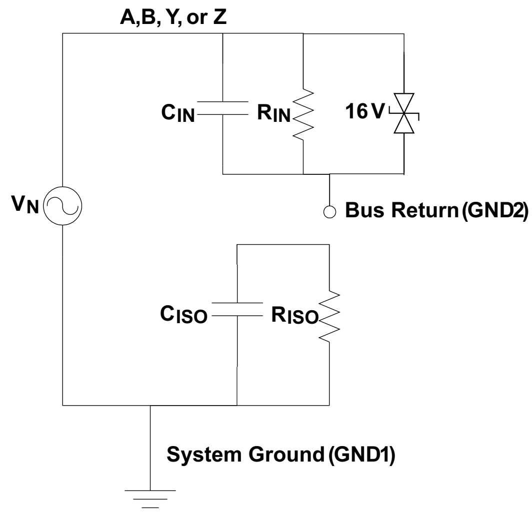


Figure 30. Noise Model

9.2.3 Application Curve

At maximum working voltage, ISO3086T isolation barrier has more than 28 years of life.

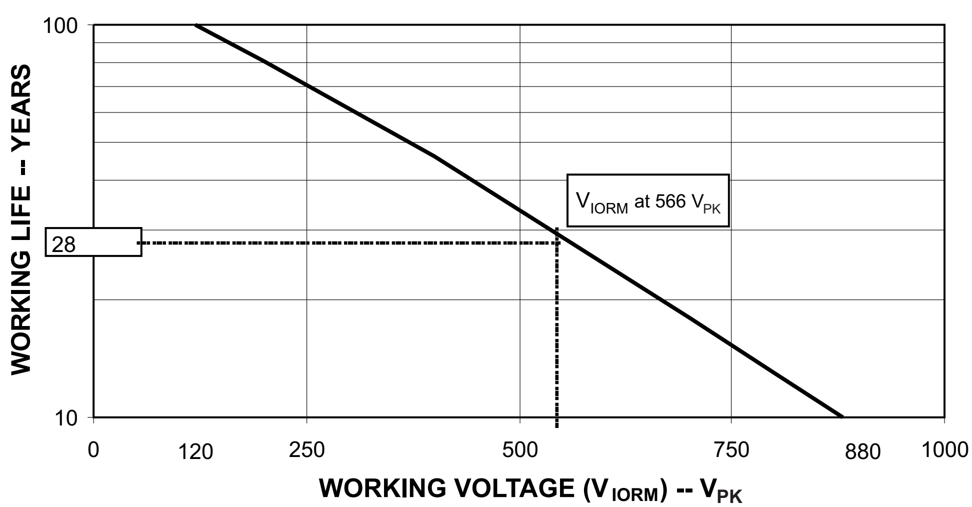


Figure 31. Time-Dependent Dielectric Breakdown Test Results

10 Power Supply Recommendations

To ensure reliable operation at all data rates and supply voltages, TI recommends a 0.1-µF bypass capacitor at input and output supply pins (V_{CC1} and V_{CC2}). The capacitors should be placed as close to the supply pins as possible. This device is used in applications where only a single primary-side power supply is available. Isolated power can be generated for the secondary-side with the help of integrated transformer driver.

11 Layout

11.1 Layout Guidelines

ON-chip IEC-ESD protection is good for laboratory and portable equipment but never sufficient for EFT and surge transients occurring in industrial environments. Therefore, robust and reliable bus node design requires the use of external transient protection devices. Because ESD and EFT transients have a wide frequency bandwidth from approximately 3-MHz to 3-GHz, high-frequency layout techniques must be applied during PCB design. A minimum of four layers is required to accomplish a low EMI PCB design (see Figure 32).

- Layer stacking should be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane, and low-frequency signal layer.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100 pF/in^2.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.
- Place the protection circuitry close to the bus connector to prevent noise transients from penetrating your board.
- Use V_{CC} and ground planes to provide low-inductance. High-frequency currents might follow the path of least inductance and not necessarily the path of least resistance.
- Design the protection components into the direction of the signal path. Do not force the transient currents to divert from the signal path to reach the protection device.
- Apply 0.1-µF bypass capacitors as close as possible to the V_{CC}-pins of transceiver, UART, and controller ICs on the board.
- Use at least two vias for V_{CC} and ground connections of bypass capacitors and protection devices to minimize effective via-inductance.
- Use 1-kΩ to 10-kΩ pullup and pulldown resistors for enable lines to limit noise currents in these lines during transient events.
- Insert pulse-proof resistors into the A and B bus lines if the TVS clamping voltage is higher than the specified maximum voltage of the transceiver bus pins. These resistors limit the residual clamping current into the transceiver and prevent it from latching up.
- While pure TVS protection is sufficient for surge transients up to 1 kV, higher transients require metal-oxide varistors (MOVs) which reduce the transients to a few hundred volts of clamping voltage, and transient blocking units (TBUs) that limit transient current to less than 1 mA.
- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.

If an additional supply voltage plane or signal layer is needed, add a second power and ground plane system to the stack to keep it symmetrical. This makes the stack mechanically stable and prevents it from warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

NOTE

For detailed layout recommendations, see Application Note *Digital Isolator Design Guide*, SLLA284.

11.2 Layout Example

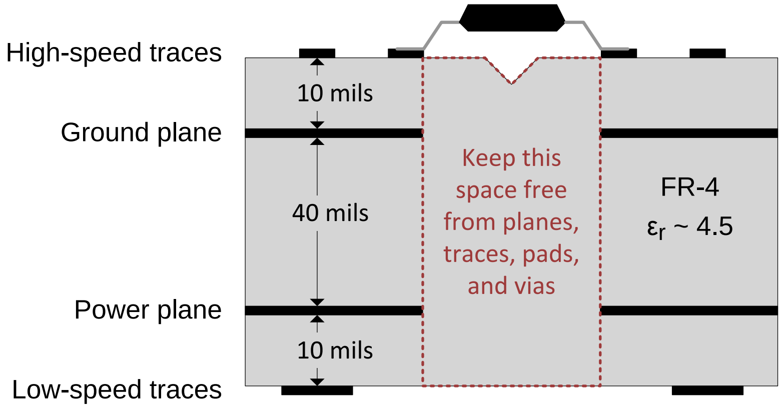


Figure 32. Recommended Layer Stack

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- *Isolated, Full-Duplex, 1-Mbps, 3.3-V to 3.3-V RS-485 Interface* (*SLUU470*)
- *Digital Isolator Design Guide* (SLLA284)
- *Isolation Glossary* (SLLA353)

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ISO35TDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ISO35TDW	Samples
ISO35TDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ISO35TDW	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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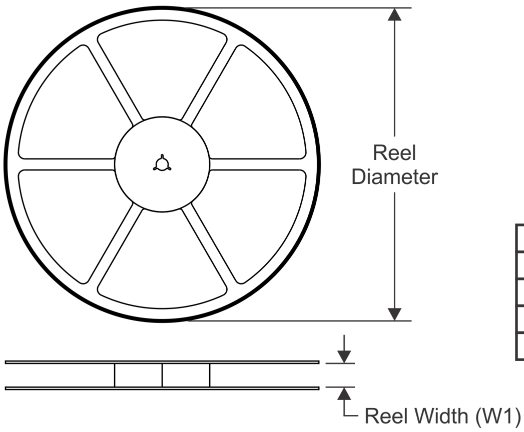
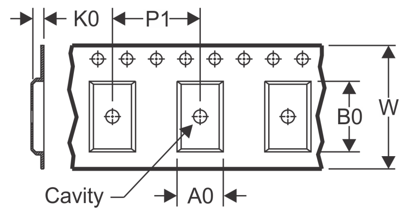
TAPE AND REEL INFORMATION

REEL DIMENSIONS

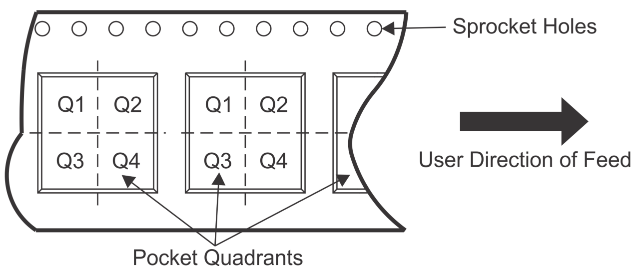


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

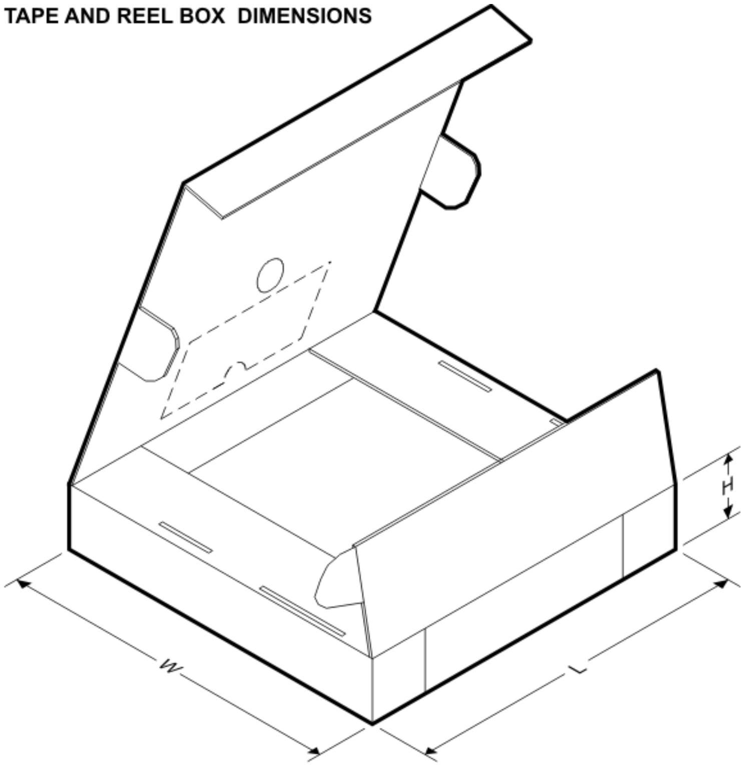
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO35TDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

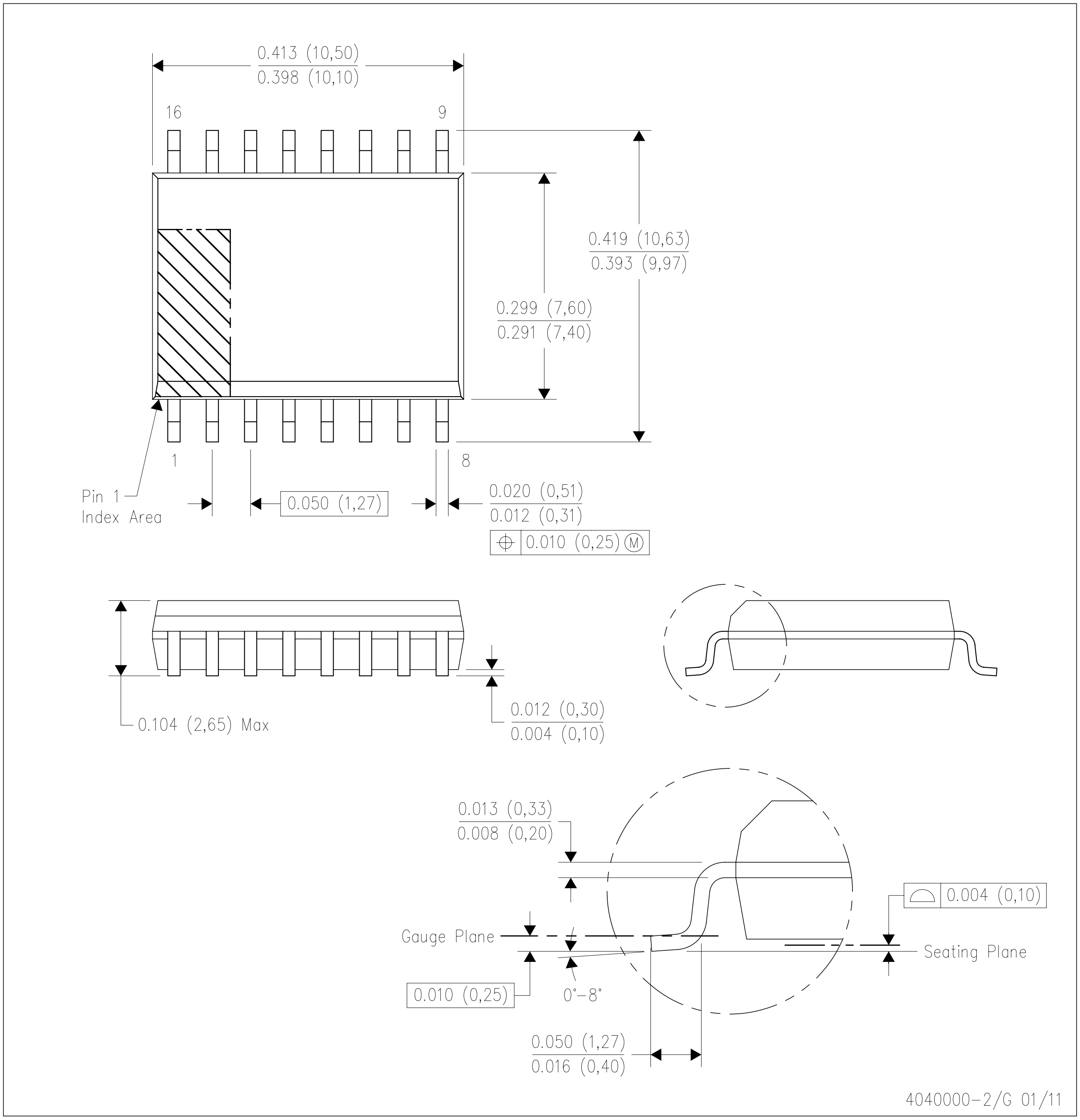
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

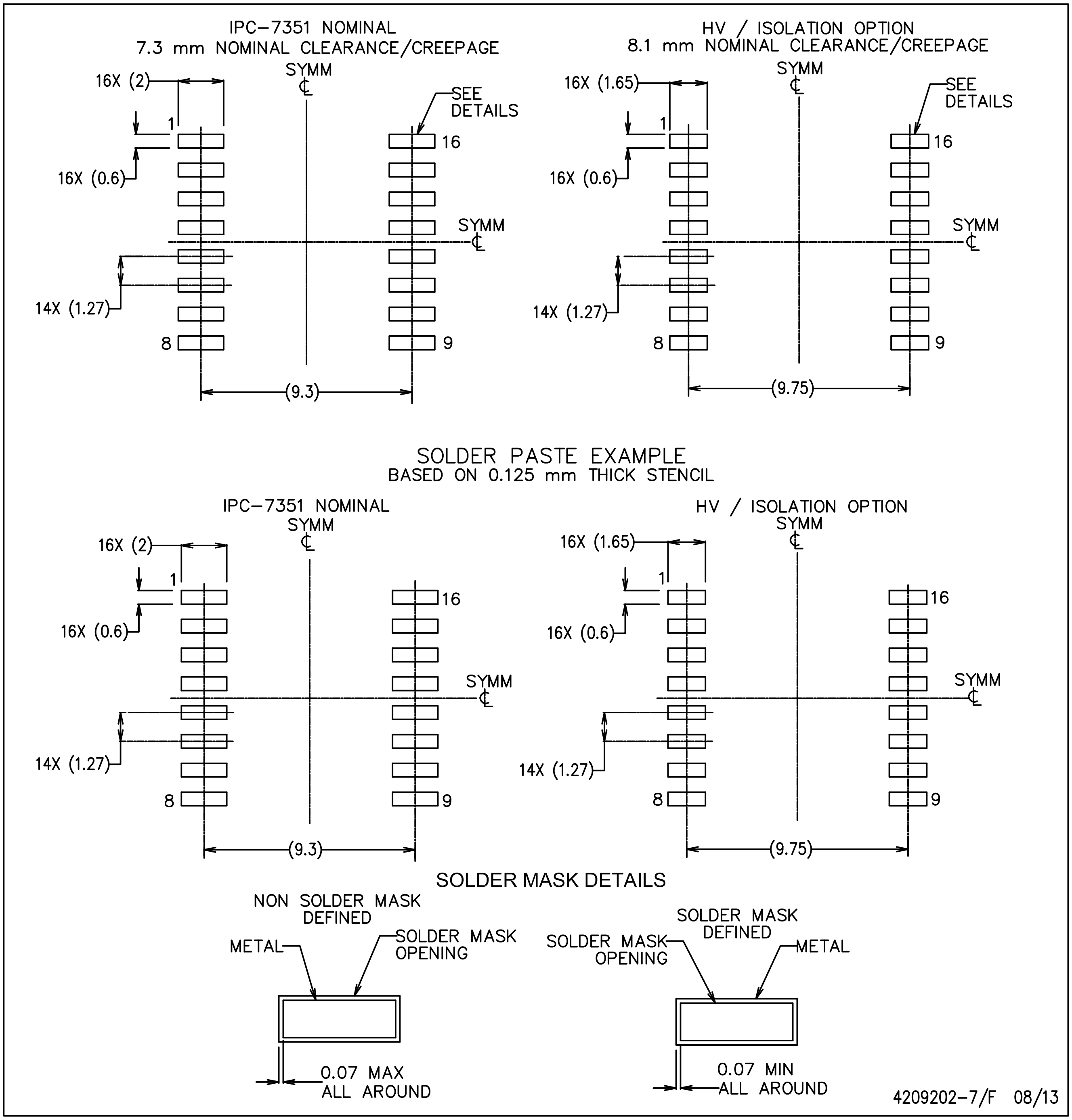
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO35TDWR	SOIC	DW	16	2000	367.0	367.0	38.0

DW (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS–013 variation AA.

DW (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Refer to IPC7351 for alternate board design.
D. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
E. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC–7525 may have alternate design recommendations.
F. Board assembly site may have different recommendations for stencil design.