SNOSBH7F – APRIL 1999 – REVISED SEPTEMBER 2014

LF412-N Low Offset, Low Drift Dual JFET Input Operational Amplifier

1 Features

- Internally Trimmed Offset Voltage: 1 mV (Max)
- Input Offset Voltage Drift: 7 µV/°C (Typ)
- Low Input Bias Current: 50 pA
- Low Input Noise Current: 0.01 pA / $\sqrt{Hz}$
- Wide Gain Bandwidth: 3 MHz (Min)
- High Slew Rate: 10V/µs (Min)
- Low Supply Current: 1.8 mA/Amplifier
- High Input Impedance: $10^{12}\Omega$
- Low Total Harmonic Distortion: ≤0.02%
- Low 1/f Noise Corner: 50 Hz
- Fast Settling Time to 0.01%: 2 µs

2 Applications

- High Speed Integrators
- Fast D/A Converters
- Sample and Hold Circuits

3 Description

These devices are low cost, high speed, JFET input operational amplifiers with very low input offset voltage and input offset voltage drift. They require low supply current yet maintain a large gain bandwidth product and fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF412-N dual is pin compatible with the LM1558, allowing designers to immediately upgrade the overall performance of existing designs.

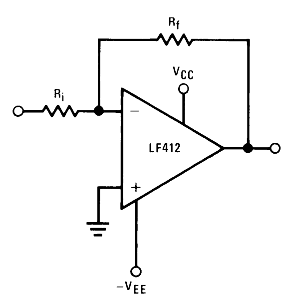
These amplifiers may be used in applications such as high speed integrators, fast D/A converters, sample and hold circuits and many other circuits requiring low input offset voltage and drift, low input bias current, high input impedance, high slew rate and wide bandwidth.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LF412ACN	PDIP	9.59 mm x 6.35 mm
LF412CN	PDIP	9.59 mm x 6.35 mm
LF412MH	TO	9.14 mm diameter

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Inverting Amplifier



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (March 2014) to Revision F — **Page**

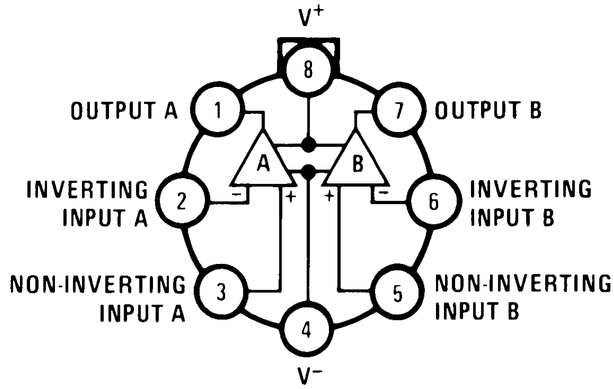
- Updated datasheet to new TI layout 1
- Deleted note. 5
- Deleted $\Delta V_{OS}/\Delta T$ Max specification for LF412A. 5
- Deleted $\Delta V_{OS}/\Delta T$ Max specification for LF412. 5
- Added Application Note 14

Changes from Revision D (March 2013) to Revision E — **Page**

- Changed layout of National Data Sheet to TI format 14

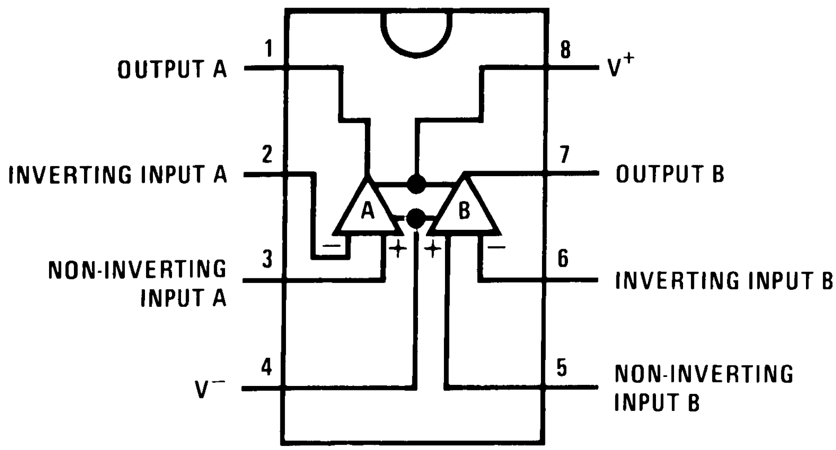
5 Pin Configuration and Functions

TO Package
See Package Number NEV0008A
Top View



Note. Pin 4 connected to case.

PDIP/CDIP Package
See Package Number P0008E or NAB0008A
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
Output A	1	O	Amplifier A Output
Inverting Input A	2	I	Amplifier A Inverting Input
Non-Inverting Input A	3	I	Amplifier A Non-Inverting Input
V-	4	P	Negative Supply
Non-Inverting Input B	5	I	Amplifier B Non-Inverting Input
Inverting Input B	6	I	Amplifier B Inverting Input
Output B	7	O	Amplifier B Output
V+	8	P	Positive Supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1][2]

	LF412A		LF412		UNIT
	MIN	MAX	MIN	MAX	
Supply Voltage	–22	22	–18	18	V
Differential Input Voltage	–38	38	–30	30	V
Input voltage Range[3]					
Output Short Circuit Duration[4]	Continuous		Continuous		
	TO Package		PDIP Package		
Power Dissipation[5]	See [6]		670		mW
T_j max	150		115		°C
Operating Temp. Range	See [7]		See [7]		
Lead Temp. (Soldering, 10 sec.)	260		260		°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Refer to RETS412X for LF412MH and LF412MJ military specifications.
(3) Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.
(4) Any of the amplifier outputs can be shorted to ground indefintely, however, more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.
(5) Max. Power Dissipation is defined by the package characteristics. Operating the part near the Max. Power Dissipation may cause the part to operate outside guaranteed limits.
(6) For operating at elevated temperature, these devices must be derated based on a thermal resistance of θ_{jA}.
(7) These devices are available in both the commercial temperature range $0°C \le T_A \le 70°C$ and the military temperature range $-55°C \le T_A \le 125°C$. The temperature range is designated by the position just before the package type in the device number. A “C” indicates the commercial temperature range and an “M” indicates the military temperature range. The military temperature range is available in TO package only. In all cases the maximum operating temperature is limited by internal junction temperature T_j max.

6.2 Handling Ratings

			TO and PDIP Package		UNIT
			MIN	MAX	
T_{stg}	Storage temperature range		−65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	-1700	1700[2]	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[3]			

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) Human body model, 1.5 kΩ in series with 100 pF.
(3) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply Voltage LF412A			±20	V
Supply Voltage LF412			±15	V

6.4 Thermal Information

THERMAL METRIC[1]		TO Package	PDIP Package	UNIT
$R_{θJA}$	Junction-to-ambient thermal resistance (Typical)	152	115	°C/W
$R_{θJC(top)}$	Junction-to-case (top) thermal resistance			
$R_{θJB}$	Junction-to-board thermal resistance			
$ψ_{JT}$	Junction-to-top characterization parameter			
$ψ_{JB}$	Junction-to-board characterization parameter			
$R_{θJC(bot)}$	Junction-to-case (bottom) thermal resistance			

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 DC Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		LF412A[1]			LF412[1]			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	R_S=10 kΩ, T_A=25°C			0.5	1.0		1.0	3.0	mV
$ΔV_{OS}/ΔT$	Average TC of Input Offset Voltage	R_S=10 kΩ			7			7		μV/°C
I_{OS}	Input Offset Current	V_S=±15V[1][2]	T_j=25°C		25	100		25	100	pA
			T_j=70°C			2			2	nA
			T_j=125°C			25			25	nA
I_B	Input Bias Current	V_S=±15V[1][2]	T_j=25°C		50	200		50	200	pA
			T_j=70°C			4			4	nA
			T_j=125°C			50			50	nA
R_{IN}	Input Resistance	T_j=25°C			10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	R_L=2k, T_A=25°C, V_S=±15V, V_O=±10V		50	200		25	200		V/mV
		Over Temperature		25	200		15	200		
V_O	Output Voltage Swing	V_S=±15V, R_L=10k		±12	±13.5		±12	±13.5		V
V_{CM}	Input Common-Mode Voltage Range			±16	+19.5		±11	+14.5		V
					−16.5			−11.5		V
CMRR	Common-Mode Rejection Ratio	R_S≤10k		80	100		70	100		dB
PSRR	Supply Voltage Rejection Ratio	See[3]		80	100		70	100		dB
I_S	Supply Current	V_O = 0V, R_L = ∞			3.6	5.6		3.6	6.5	mA

(1) Unless otherwise specified, the specifications apply over the full temperature range and for V_S=±20V for the LF412A and for V_S=±15V for the LF412. V_{OS}, I_B, and I_{OS} are measured at V_{CM}=0.
(2) The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_j. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. $T_j=T_A+θ_{jA} P_D$ where $θ_{jA}$ is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.
(3) Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice. V_S = ±6V to ±15V.

6.6 AC Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	LF412A[1]			LF412[1]			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Amplifier to Amplifier Coupling	T_A=25°C, f=1 Hz-20 kHz (Input Referred)		−120			−120		dB

(1) Unless otherwise specified, the specifications apply over the full temperature range and for V_S=±20V for the LF412A and for V_S=±15V for the LF412. V_{OS}, I_B, and I_{OS} are measured at V_{CM}=0.

AC Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	LF412A[1]			LF412[1]			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew Rate	V_S=±15V, T_A=25°C	10	15		8	15		V/μs
GBW	Gain-Bandwidth Product	V_S=±15V, T_A=25°C	3	4		2.7	4		MHz
THD	Total Harmonic Dist	A_V=+10, R_L=10k, V_O=20 Vp-p, BW=20 Hz-20 kHz		≤0.02%			≤0.02%		
e_n	Equivalent Input Noise Voltage	T_A=25°C, R_S=100Ω, f=1 kHz		25			25		nV / √Hz
i_n	Equivalent Input Noise Current	T_A=25°C, f=1 kHz		0.01			0.01		pA / √Hz

6.7 Typical Characteristics

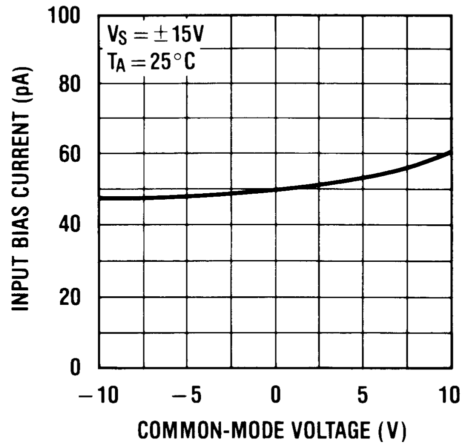


Figure 1. Input Bias Current

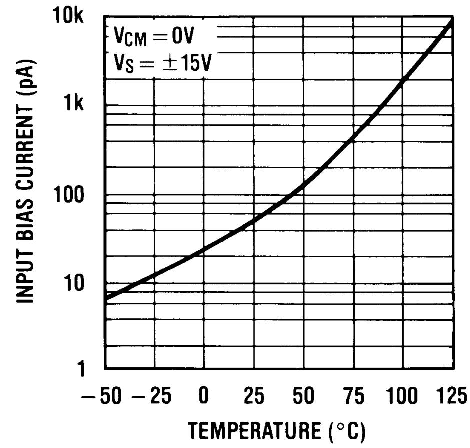


Figure 2. Input Bias Current

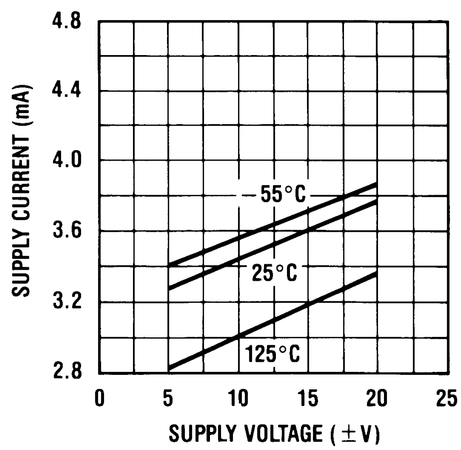


Figure 3. Supply Current

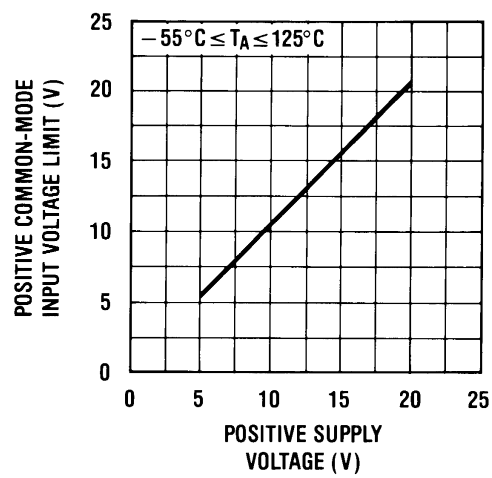


Figure 4. Positive Common-Mode Input Voltage Limit

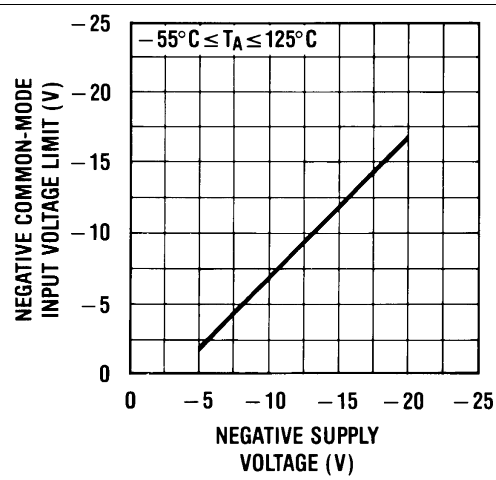


Figure 5. Negative Common-Mode Input Voltage Limit

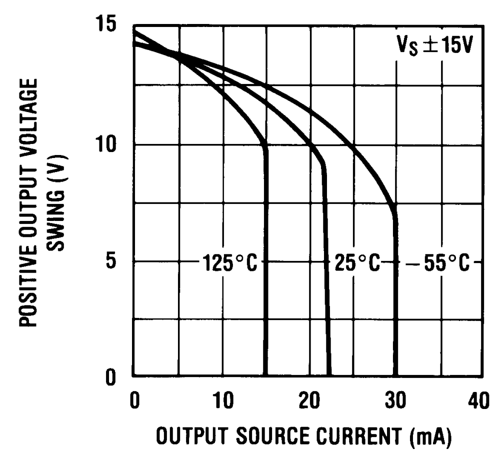


Figure 6. Positive Current Limit

Typical Characteristics (continued)

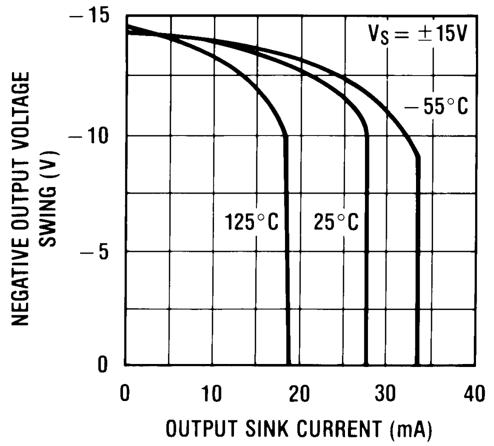


Figure 7. Negative Current Limit

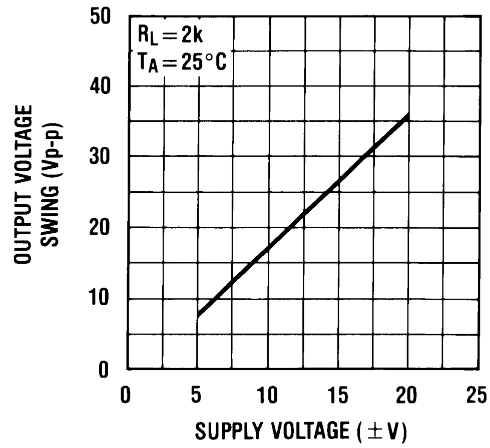


Figure 8. Output Voltage Swing

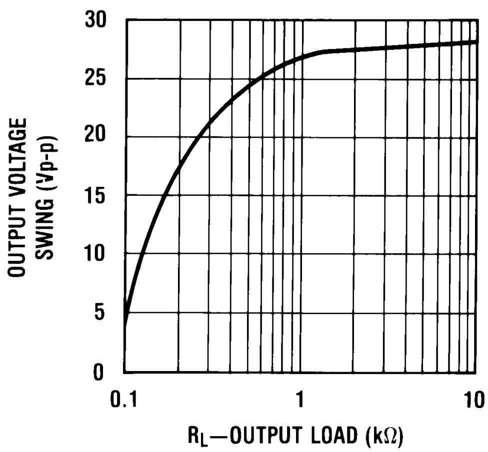


Figure 9. Output Voltage Swing

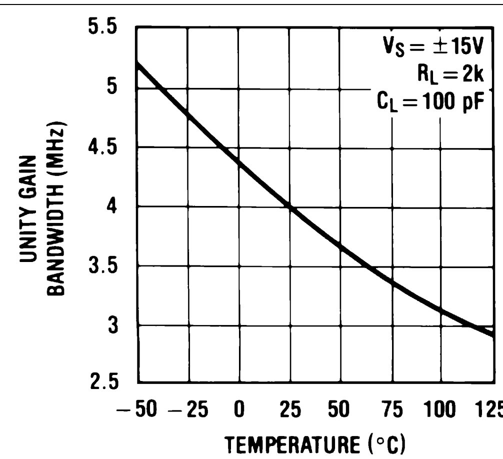


Figure 10. Gain Bandwidth

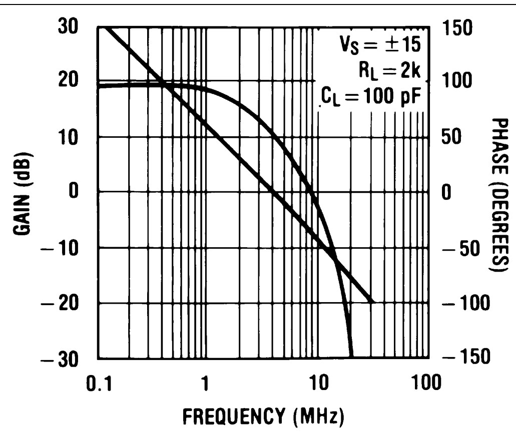


Figure 11. Bode Plot

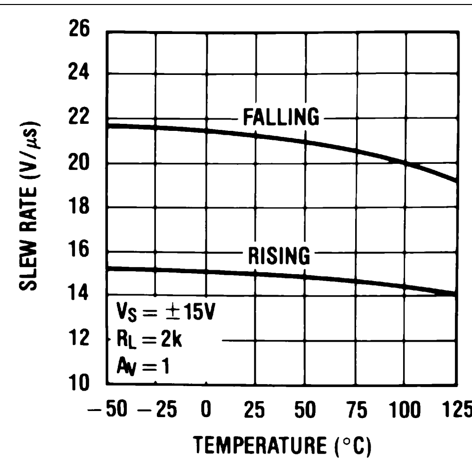


Figure 12. Slew Rate

Typical Characteristics (continued)

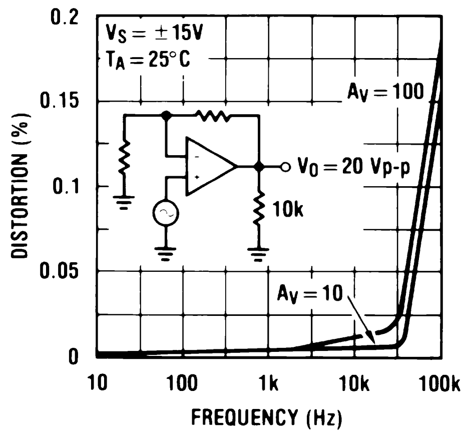


Figure 13. Distortion vs Frequency

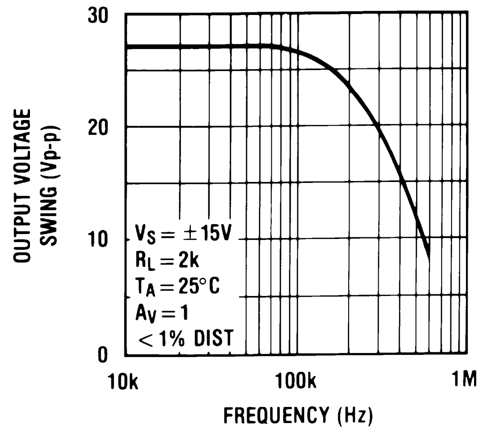


Figure 14. Undistorted Output Voltage Swing

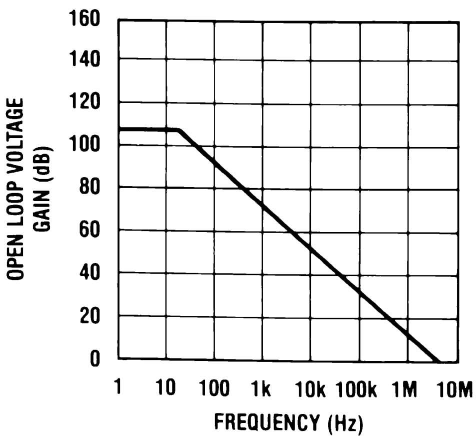


Figure 15. Open Loop Frequency Response

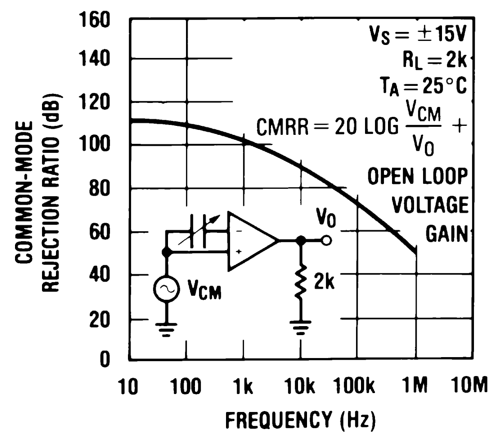


Figure 16. Common-Mode Rejection Ratio

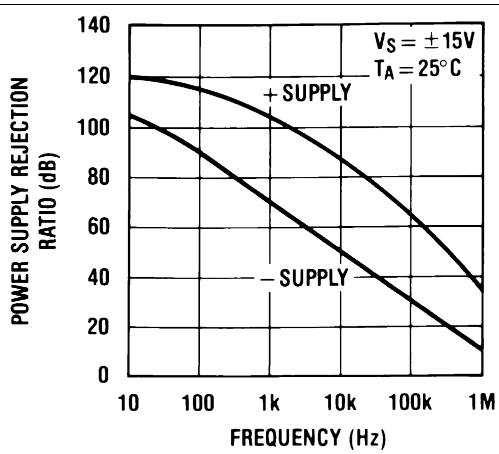


Figure 17. Power Supply Rejection Ratio

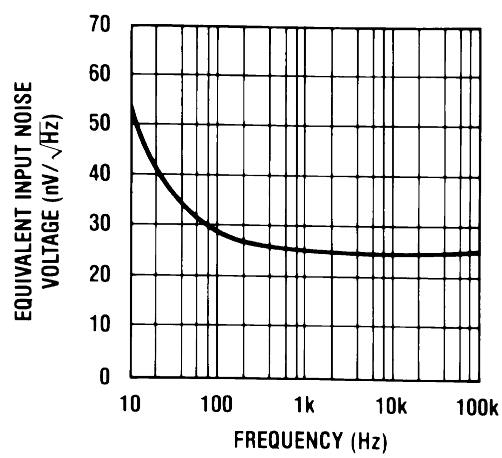


Figure 18. Equivalent Input Noise Voltage

Typical Characteristics (continued)

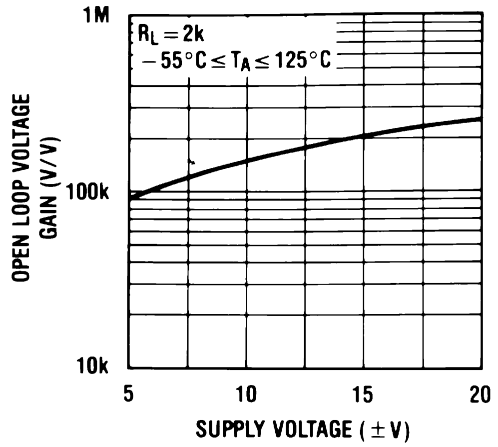


Figure 19. Open Loop Voltage Gain

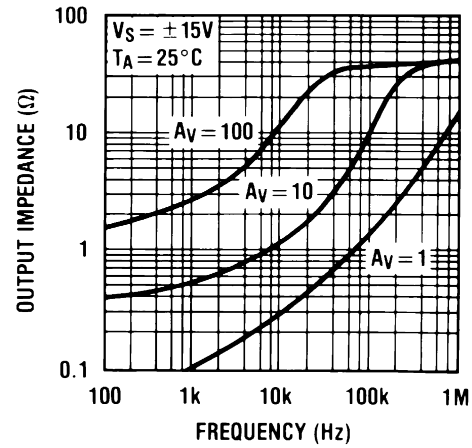


Figure 20. Output Impedance

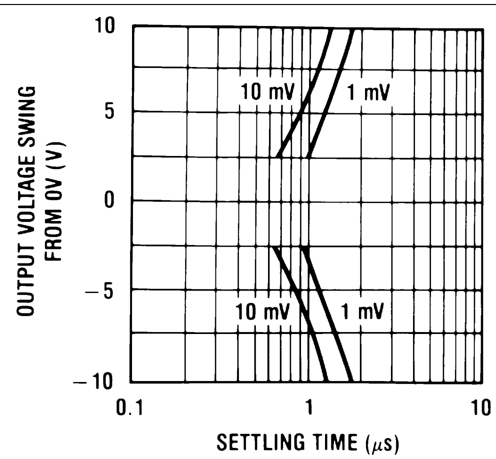


Figure 21. Inverter Settling Time

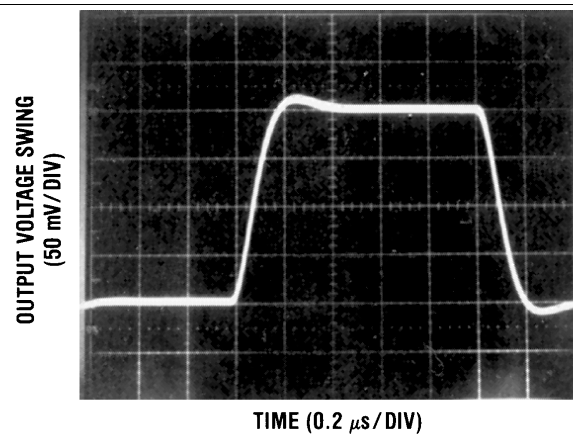


Figure 22. Small Signal Inverting (R_L = 2 kΩ, C_L = 10 pF)

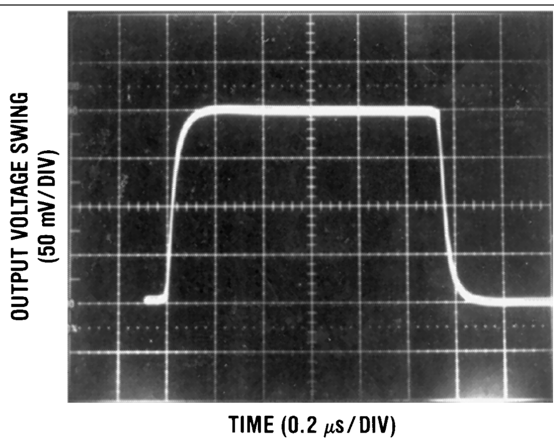


Figure 23. Small Signal Non-Inverting (R_L = 2 kΩ, C_L = 10 pF)

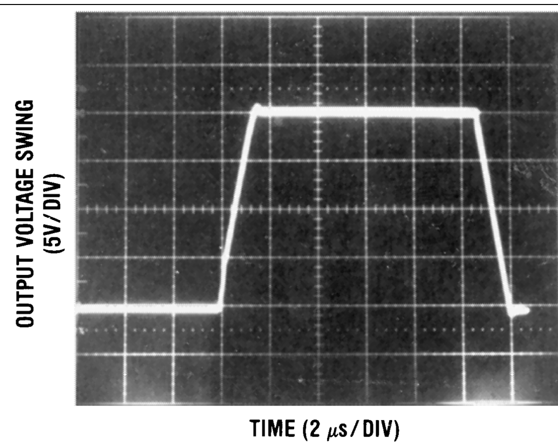


Figure 24. Large Signal Inverting (R_L = 2 kΩ, C_L = 10 pF)

Typical Characteristics (continued)

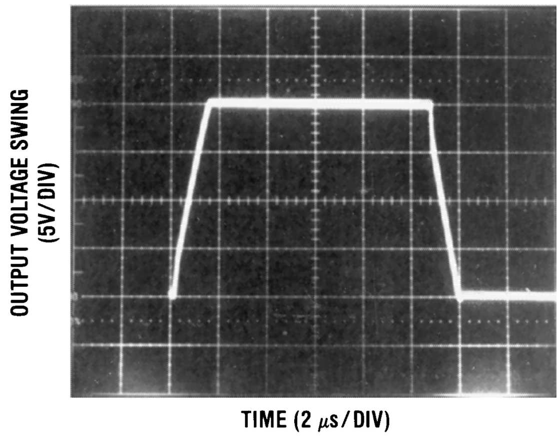


Figure 25. Large Signal Non-Inverting (R_L = 2 kΩ, C_L = 10 pF)

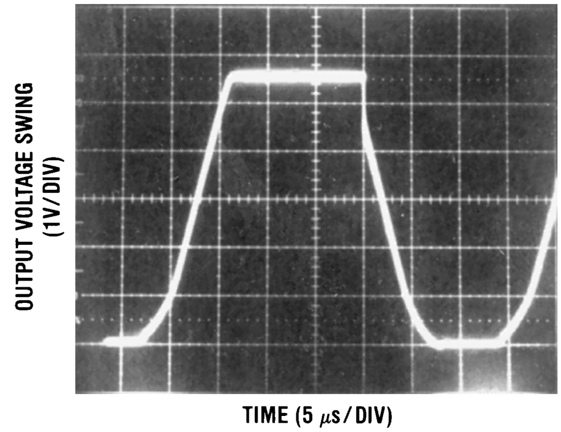


Figure 26. Current Limit (R_L=100Ω) (C_L = 10 pF)

7 Detailed Description

7.1 Overview

The LF412 devices are low cost, high speed, JFET input operational amplifiers with very low input offset voltage and input offset voltage drift. They require low supply current yet maintain a large gain bandwidth product and fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF412-N dual is pin compatible with the LM1558, allowing designers to immediately upgrade the overall performance of existing designs.

These amplifiers may be used in applications such as high speed integrators, fast D/A converters, sample and hold circuits and many other circuits requiring low input offset voltage and drift, low input bias current, high input impedance, high slew rate and wide bandwidth.

7.2 Functional Block Diagram

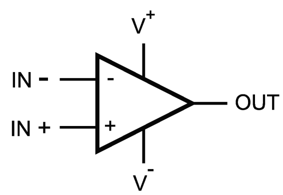


Figure 27. Each Amplifier

7.3 Feature Description

The amplifier's differential inputs consist of a non-inverting input (+IN) and an inverting input (-IN). The amplifier amplifies only the difference in voltage between the two inputs, which is called the differential input voltage. The output voltage of the op-amp V_{OUT} is given by the equation $V_{OUT} = A_{OL}(IN+ - IN-)$.

7.4 Device Functional Modes

7.4.1 Input and Output Stage

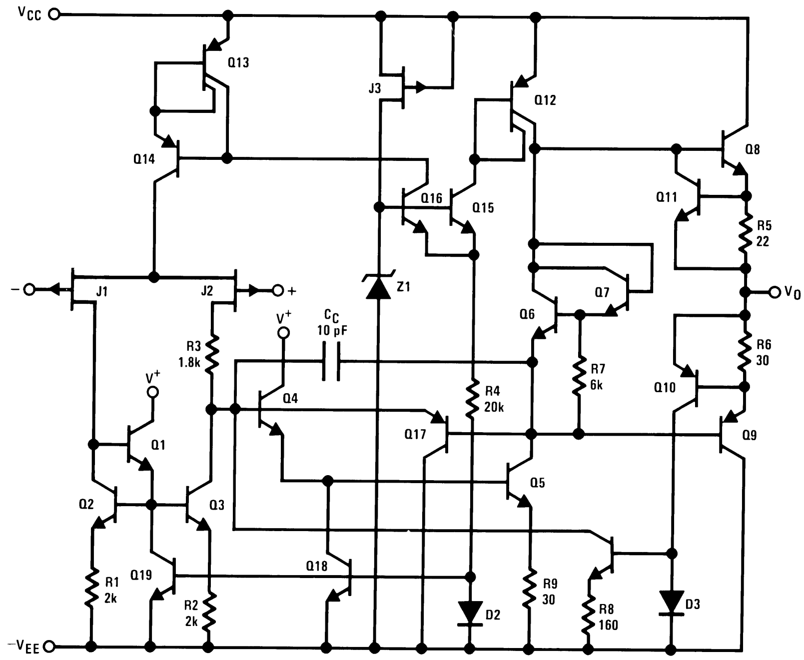


Figure 28. 1/2 Dual LF412

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LF412-N series of JFET input dual op amps are internally trimmed (BI-FET II™) providing very low input offset voltages and input offset voltage drift. These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

8.2 Typical Application

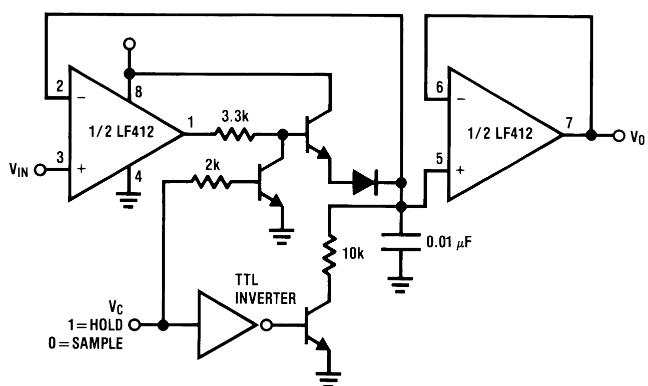


Figure 29. Single Supply Sample and Hold

8.2.1 Design Requirements

Single supply.

8.2.2 Detailed Design Procedure

Exceeding the negative common-mode limit on either input will cause a reversal of the phase to the output and force the amplifier output to the corresponding high or low state.

Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output, however, if both inputs exceed the limit, the output of the amplifier may be forced to a high state.

The amplifiers will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

Each amplifier is individually biased by a zener reference which allows normal circuit operation on ±6.0V power supplies. Supply voltages less than these may result in lower gain bandwidth and slew rate.

The amplifiers will drive a 2 kΩ load resistance to ±10V over the full temperature range. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

Typical Application (continued)

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize “pick-up” and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

8.2.3 Application Curves

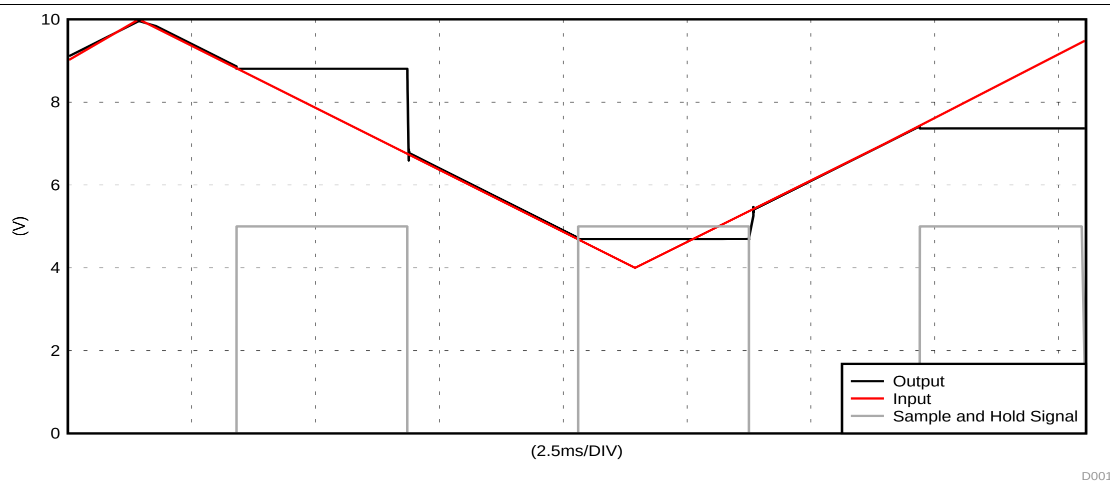


Figure 30. Sample and Hold Waveforms

9 Power Supply Recommendations

For proper operation, the power supplies must be properly decoupled. For decoupling the supply lines it is suggested that 0.1µF capacitors be placed as close as possible to the op amp power supply pins. The minimum power supply voltage is ±5V.

10 Layout

10.1 Layout Guidelines

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

10.2 Layout Example

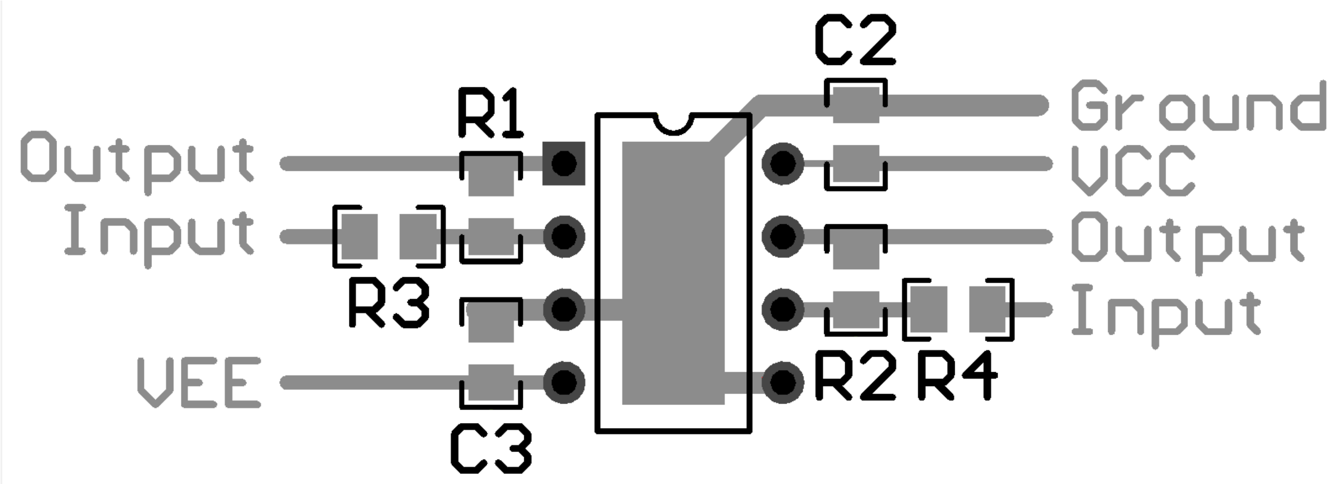


Figure 31. LF412 Layout

11 Device and Documentation Support

11.1 Trademarks

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11.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LF412ACN/NOPB	ACTIVE	PDIP	P	8	40	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM	0 to 70	LF 412ACN	Samples
LF412CN/NOPB	ACTIVE	PDIP	P	8	40	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM	0 to 70	LF 412CN	Samples
LF412MH	ACTIVE	TO-99	LMC	8	500	TBD	Call TI	Call TI	-55 to 125	(LF412MH ~ LF412MH)	Samples
LF412MH/NOPB	ACTIVE	TO-99	LMC	8	500	Green (RoHS & no Sb/Br)	Call TI	Level-1-NA-UNLIM	-55 to 125	(LF412MH ~ LF412MH)	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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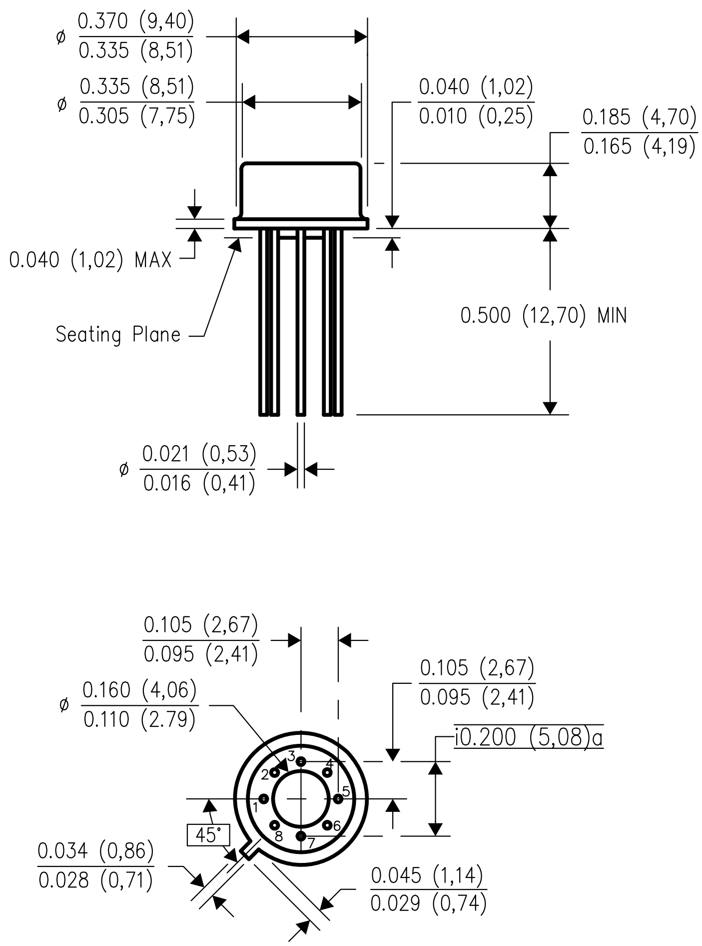
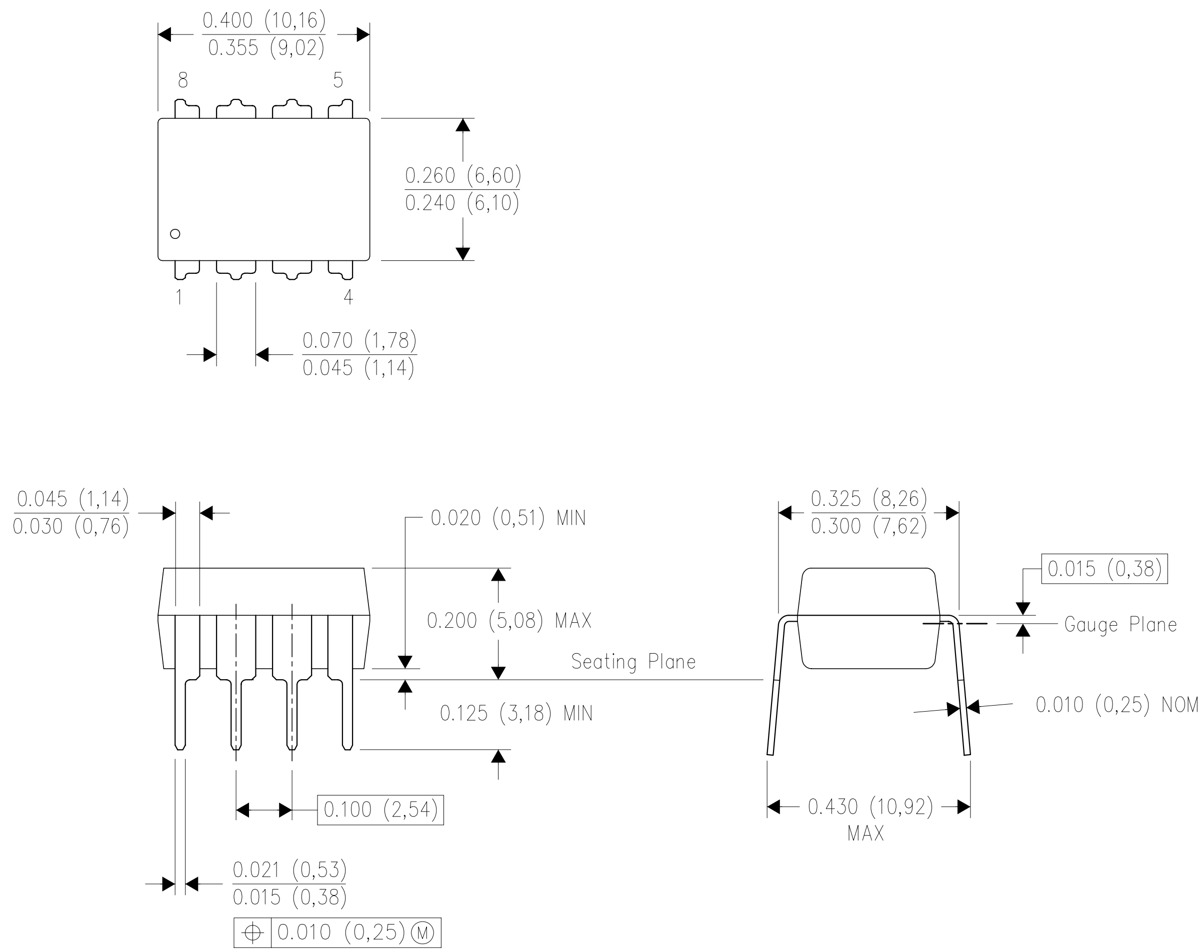
LMC (O-MBCY-W8) METAL CYLINDRICAL PACKAGE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Leads in true position within 0.010 (0,25) R @ MMC at seating plane.
- D. Pin numbers shown for reference only. Numbers may not be marked on package.
- E. Falls within JEDEC MO-002/TO-99.

P (R-PDIP-T8) PLASTIC DUAL-IN-LINE PACKAGE



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