LMx85-1.2, LM385B-1.2 Micropower Voltage References

1 Features

- Operating Current Range
  - LM285-1.2: 10 µA to 20 mA
  - LM385-1.2: 15 µA to 20 mA
  - LM385B-1.2: 15 µA to 20 mA
- 1% and 2% Initial Voltage Tolerance
- Reference Impedance
  - LM385-1.2: 1 Ω MAX at 25°C
  - All devices: 1.5 Ω MAX over Full Temperature Range
- Very Low Power Consumption
- Interchangeable with Industry Standard LM285-1.2 and LM385-1.2

2 Applications

- Portable Meter References
- Portable Test Instruments
- Battery-Operated Systems
- Current-Loop Instrumentation
- Panel Meters

3 Description

These micropower, two-terminal, band-gap voltage references operate over a 10-µA to 20-mA current range and feature exceptionally low dynamic impedance and good temperature stability. On-chip trimming provides tight voltage tolerance. The band-gap reference for these devices has low noise and long-term stability.

The design makes these devices exceptionally tolerant of capacitive loading and, thus, easier to use in most reference applications. The wide dynamic operating temperature range accommodates varying current supplies, with excellent regulation.

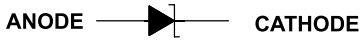
The extremely low power drain of this series makes them useful for micropower circuitry. These voltage references can be used to make portable meters, regulators, or general-purpose analog circuitry, with battery life approaching shelf life. The wide operating current range allows them to replace older references with tighter-tolerance parts.

Device Information(1)

PART NUMBER	PACKAGE (PIN)	BODY SIZE (NOM)
LMx85-1.2	SOIC (8)	4.90 mm × 3.91 mm
	SOP (8)	6.20 mm × 5.30 mm
	TSSOP (8)	3.00 mm × 4.40 mm
	TO-226 (3)	4.30 mm × 4.30 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

4 Simplified Schematic



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

5 Revision History

Changes from Revision I (December 2005) to Revision J **Page**

- Added *Applications*, *Device Information* table, *Pin Functions* table, *ESD Ratings* table, *Thermal Information* table, *Typical Characteristics*, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1
- Deleted *Ordering Information* table. ... 1

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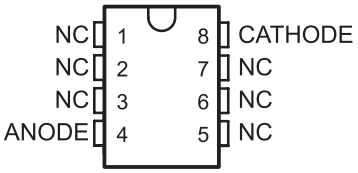
6 Pin Configuration and Functions

LM285-1.2 . . . D PACKAGE
LM385-1.2 . . . D, PS, OR PW PACKAGE
LM385B-1.2 . . . D OR PW PACKAGE
(TOP VIEW)



NC – No internal connection

LM285-1.2, LM385-1.2, LM385B-1.2 . . . LP PACKAGE
(TOP VIEW)

NC – No internal connection

Pin Functions

PIN			TYPE	DESCRIPTION
NAME	LP	D, PS or PW		
ANODE	1	4	I	Shunt Current/Voltage input
CATHODE	2	8	O	Common pin, normally connected to ground
NC	3	1, 2, 3, 5, 6, 7	—	No internal connection

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
I_R	Reverse Current		30	mA
I_F	Forward Current		10	mA
T_J	Operating virtual junction temperature		150	°C
T_{stg}	Storage temeprature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
I_{ZZ}	Reference current		0.01	20	mA
T_A	Operating free-air temperature	LM285-1.2	–40	85	°C
		LM385-1.2, LM385B-1.2	0	70	

7.4 Thermal Information

THERMAL METRIC(1)		LMx85-1.2				UNIT
		D	LP	PS	PW	
		8 PINS	3 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	97	140	95	149	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

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7.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A (1)	LM285-1.2			LM385-1.2			LM385B-1.2			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_Z	Reference voltage	I_Z = I(min) to 20 mA (2)	25°C	1.223	1.235	1.247	1.21	1.235	1.26	1.223	1.235	1.247	V
α_{VZ}	Average temperature coefficient of reference voltage (3)	I_Z = I(min) to 20 mA (2)	Full Range		±20			±20			±20		ppm/°C
Δ_{VZ}	Change in reference voltage with current	I_Z = I(min) to 1 mA (2)	25°C			1			1			1	mV
			Full Range			1.5			1.5			1.5	
		I_Z = I(min) to 20 mA	25°C			12			20			20	
			Full Range			30			30			30	
$\Delta V_Z/\Delta t$	Long-term change in reference voltage	I_Z = 100 µA	25°C		±20			±20			±20		ppm/khr
I_Z(min)	Minimum reference current		Full Range		8	10		8	15		8	15	µA
Z_Z	Reference impedance	I_Z = 100 µA, f = 25 Hz	25°C		0.2	0.6		0.4	1		0.4	1	Ω
			Full Range			1.5			1.5			1.5	
V_n	Broadband noise voltage	I_Z = 100 µA, f = 10 Hz to 10 kHz	25°C		60			60			60		µV

(1) Full range is −40°C to 85°C for the LM285-1.2 and 0°C to 70°C for the LM385-1.2 and LM385B-1.2.
(2) I(min) = 10 µA for the LM285-1.2 and 15 µA for the LM385-1.2 and LM385B-1.2
(3) The average temperature coefficient of reference voltage is defined as the total change in reference voltage divided by the specified temperature range.

7.6 Typical Characteristics

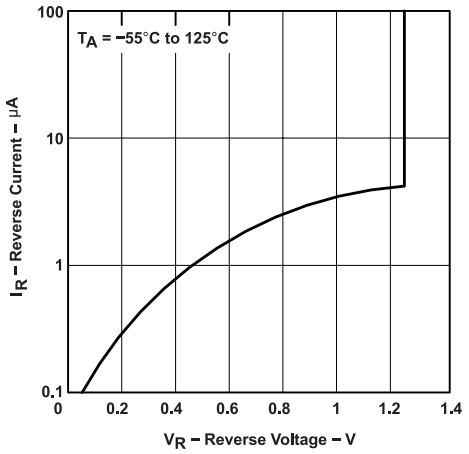

Figure 1. Reverse Current vs Reverse Voltage

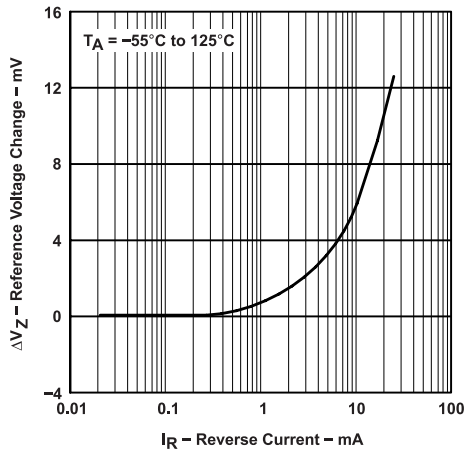

Figure 2. Reference Voltage Change vs Reverse Current

Typical Characteristics (continued)

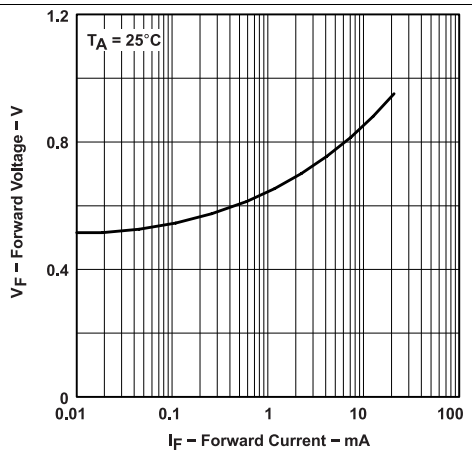

Figure 3. Forward Voltage vs Forward Current

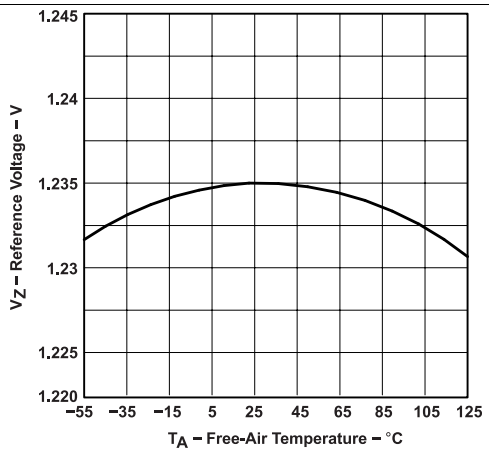

Figure 4. Reference Voltage vs Free-Air Temperature

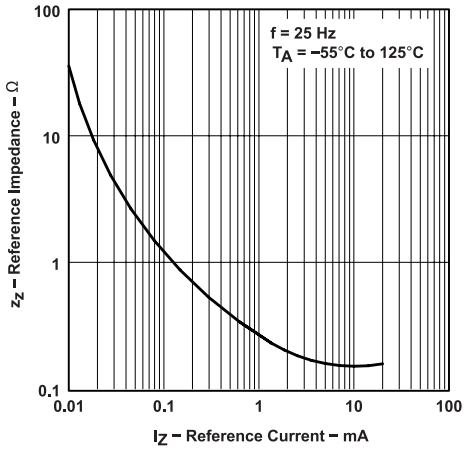

Figure 5. Reference Impedance vs Reference Current

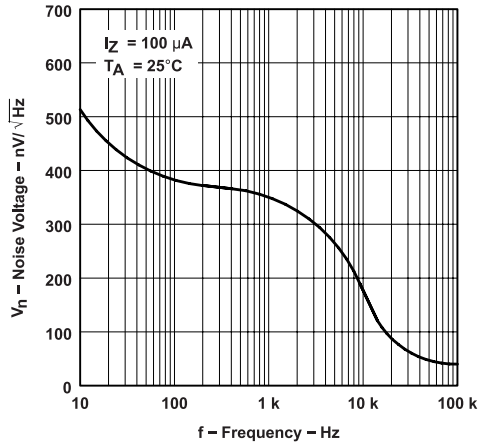

Figure 6. Noise Voltage vs Frequency

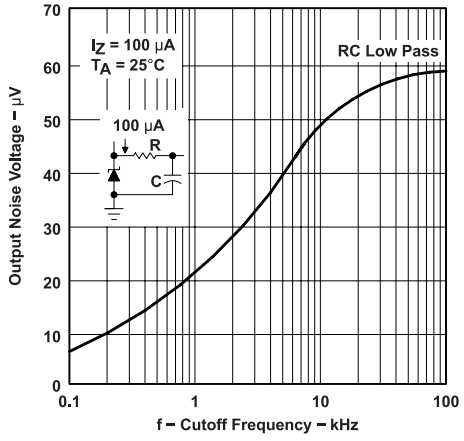

Figure 7. Output Noise Voltage vs Cutoff Frequency

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8 Detailed Description

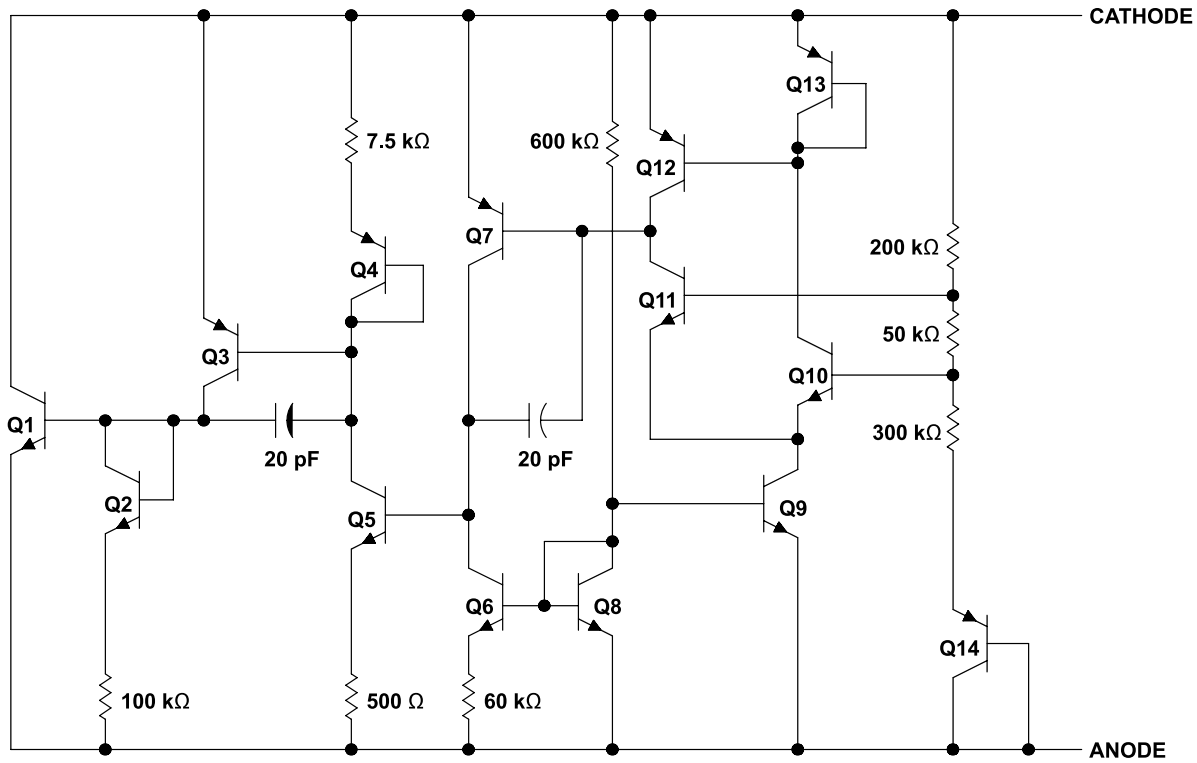
8.1 Overview

The LM285-1.2, LM385-1.2, and LM385-1.2 devices are micropower, two-terminal, band-gap voltage references which operate over a 10-μA to 20-mA current range. On-chip trimming provides tight voltage tolerance. The band-gap reference for these devices has low noise and long-term stability.

The design makes these devices exceptionally tolerant of capacitive loading and, thus, easier to use in most reference applications. The wide dynamic operating temperature range accommodates varying current supplies, with excellent regulation.

The extremely low power drain of this series makes them useful for micropower circuitry. These voltage references can be used to make portable meters, regulators, or general-purpose analog circuitry, with battery life approaching shelf life.

8.2 Functional Block Diagram



A. Component values shown are nominal.

8.3 Feature Description

A band gap voltage reference controls high gain amplifier and shunt pass element to maintain a nearly constant voltage between cathode and anode. Regulation occurs after a minimum current is provided to power the voltage divider and amplifier. Internal frequency compensation provides a stable loop for all capacitor loads. Floating shunt design is useful for both positive and negative regulation applications.

8.4 Device Functional Modes

LM285-1.2, LM385-1.2, and LM385-1.2 devices will operate in one mode, which is as a fixed voltage reference that cannot be adjusted.

In order for a proper Reverse Voltage to be developed, current must be sourced into the cathode of LM285. The minimum current needed for proper regulation is denoted in *Electrical Characteristics* as $I_{Z,min}$.

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The The LM285-1.2, LM385-1.2, and LM385-1.2 devices create a voltage reference for to be used for a variety of applications including amplifiers, power supplies, and current-sensing circuits. The following application shows how to use these devices to establish a voltage reference.

9.2 Typical Application

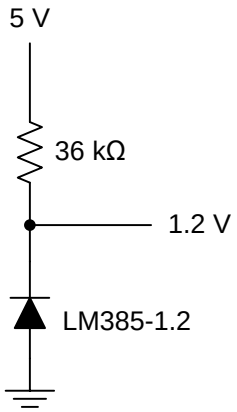

Figure 8. Generating Reference Voltage with a Resistive Current Source

9.2.1 Design Requirements

The key design requirement when using this device as a voltage reference is to supply the LM385 with a minimum Cathode Current (I_Z), as indicated in *Electrical Characteristics*.

9.2.2 Detailed Design Procedure

In order to generate a constant and stable reference voltage, a current greater than $I_{Z(MIN)}$ must be sourced into the cathode of this device. This can be accomplished using a current regulating device such as LM334 or a simple resistor. For a resistor, its value should be equal to or greater than $(V_{supply} - V_{reference}) \div I_{Z(MIN)}$.

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Typical Application (continued)

9.2.3 Application Curves

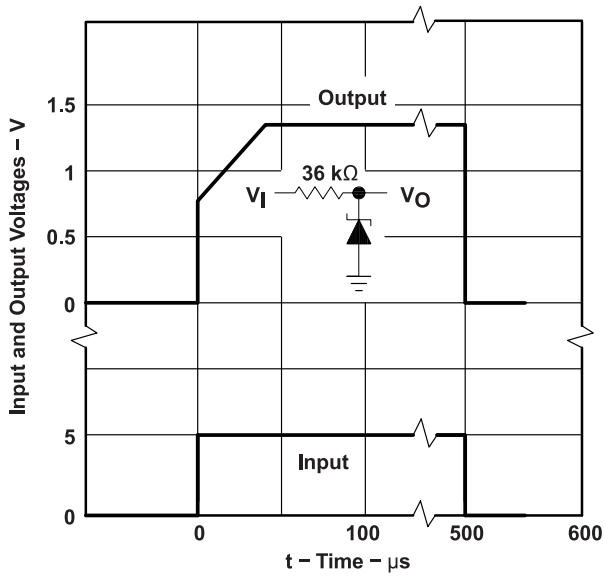
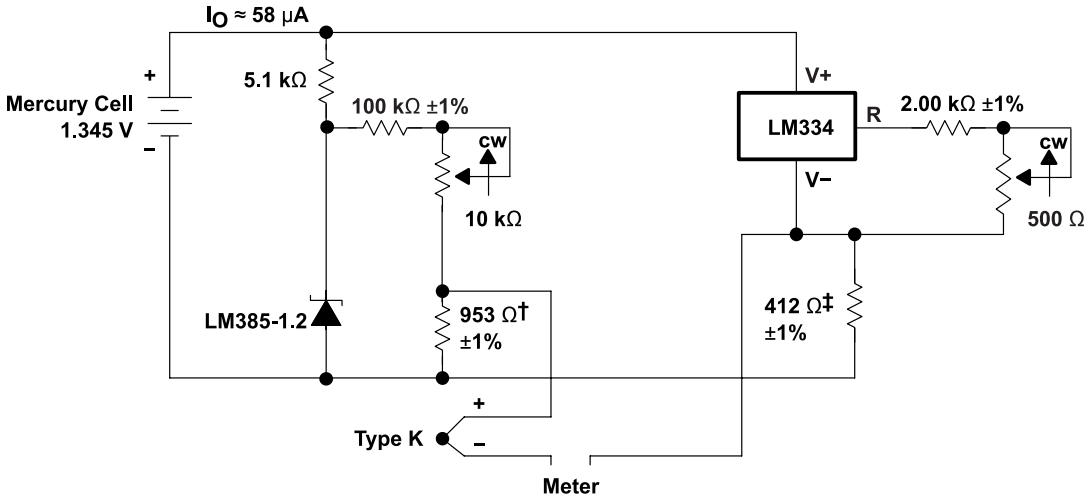


Figure 9. Transient Response

9.3 System Examples

9.3.1 Thermocouple Cold-Junction Compensator



† Adjust for 11.15 mV at 25°C across 953 Ω
‡ Adjust for 12.17 mV at 25°C across 412 Ω

Figure 10. Thermocouple Cold-Junction Compensator

9.3.2 Generating Reference Voltage with a Constant Current Source

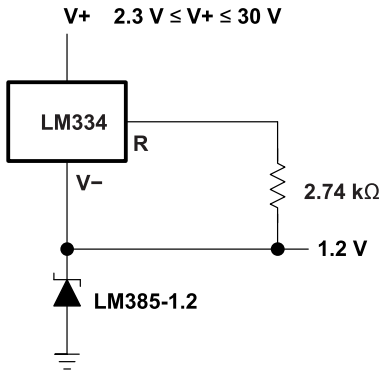


Figure 11. Generating Reference Voltage with a Constant Current Source Device

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10 Power Supply Recommendations

In order to not exceed the maximum cathode current, be sure that the supply voltage is current limited.

For applications shunting high currents (30 mA max), pay attention to the cathode and anode trace lengths, adjusting the width of the traces to have the proper current density.

11 Layout

11.1 Layout Guidelines

Figure 12 shows an example of a PCB layout of LMx85x-1.2. Some key V_{ref} niose considerations are:

- Connect a low-ESR, 0.1-µF (C_L) ceramic bypass capacitor on the cathode pin node.
- Decouple other active devices in the system per the device specifications.
- Using a solid ground plane helps distribute heat and reduces electromagnetic interference (EMI) noise pickup.
- Place the external components as close to the device as possible. This configuration prevents parasitic errors (such as the Seebeck effect) from occurring.
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible and only make perpendicular crossings when absolutely necessary.

11.2 Layout Example

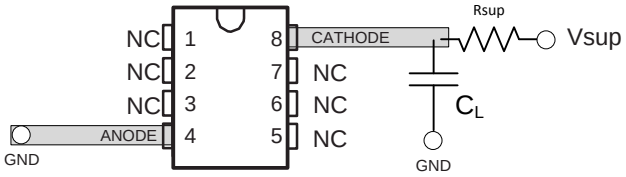

Figure 12. Layout Diagram

12 Device and Documentation Support

12.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LM285-1.2	Click here	Click here	Click here	Click here	Click here
LM385-1.2	Click here	Click here	Click here	Click here	Click here
LM385B-1.2	Click here	Click here	Click here	Click here	Click here

12.2 Trademarks

All trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM285D-1-2	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	285-12	Samples
LM285DE4-1-2	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	285-12	Samples
LM285DG4-1-2	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	285-12	Samples
LM285DR-1-2	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	285-12	Samples
LM285DRE4-1-2	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	285-12	Samples
LM285DRG4-1-2	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	285-12	Samples
LM285LP-1-2	ACTIVE	TO-92	LP	3	1000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	-40 to 85	285-12	Samples
LM285LPE3-1-2	ACTIVE	TO-92	LP	3	1000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	-40 to 85	285-12	Samples
LM285LPRE3-1-2	ACTIVE	TO-92	LP	3	2000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	-40 to 85	285-12	Samples
LM385-1.2-MWC	ACTIVE	WAFERSALE	YS	0	1	Green (RoHS & no Sb/Br)	Call TI	Level-1-NA-UNLIM	-40 to 85		Samples
LM385BD-1-2	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	385B12	Samples
LM385BDE4-1-2	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	385B12	Samples
LM385BDG4-1-2	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	385B12	Samples
LM385BDR-1-2	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	385B12	Samples
LM385BDRG4-1-2	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	385B12	Samples
LM385BLP-1-2	ACTIVE	TO-92	LP	3	1000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 70	385B12	Samples
LM385BLPE3-1-2	ACTIVE	TO-92	LP	3	1000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 70	385B12	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM385BLPR-1-2	ACTIVE	TO-92	LP	3	2000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 70	385B12	Samples
LM385BLPRE3-1-2	ACTIVE	TO-92	LP	3	2000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 70	385B12	Samples
LM385BPW-1-2	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	385B12	Samples
LM385BPWR-1-2	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	385B12	Samples
LM385D-1-2	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	385-12	Samples
LM385DG4-1-2	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	385-12	Samples
LM385DR-1-2	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	385-12	Samples
LM385DRG4-1-2	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	385-12	Samples
LM385LP-1-2	ACTIVE	TO-92	LP	3	1000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 70	385-12	Samples
LM385LPE3-1-2	ACTIVE	TO-92	LP	3	1000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 70	385-12	Samples
LM385LPR-1-2	ACTIVE	TO-92	LP	3	2000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 70	385-12	Samples
LM385LPRE3-1-2	ACTIVE	TO-92	LP	3	2000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 70	385-12	Samples
LM385PW-1-2	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	385-12	Samples
LM385PWE4-1-2	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	385-12	Samples
LM385PWR-1-2	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	385-12	Samples
LM385PWRE4-1-2	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	385-12	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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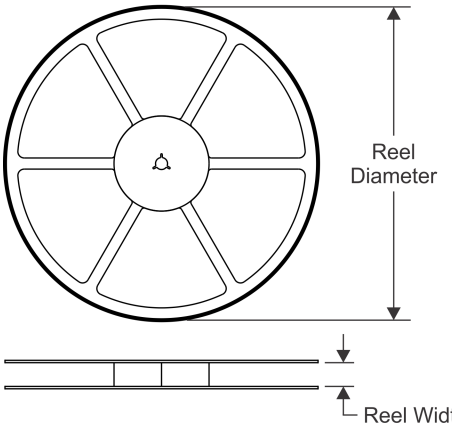
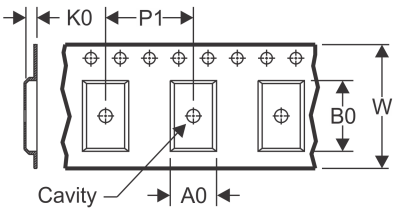
TAPE AND REEL INFORMATION

REEL DIMENSIONS

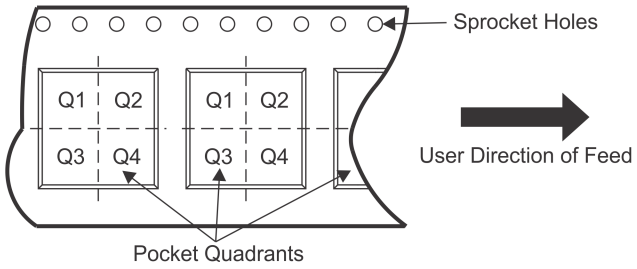


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

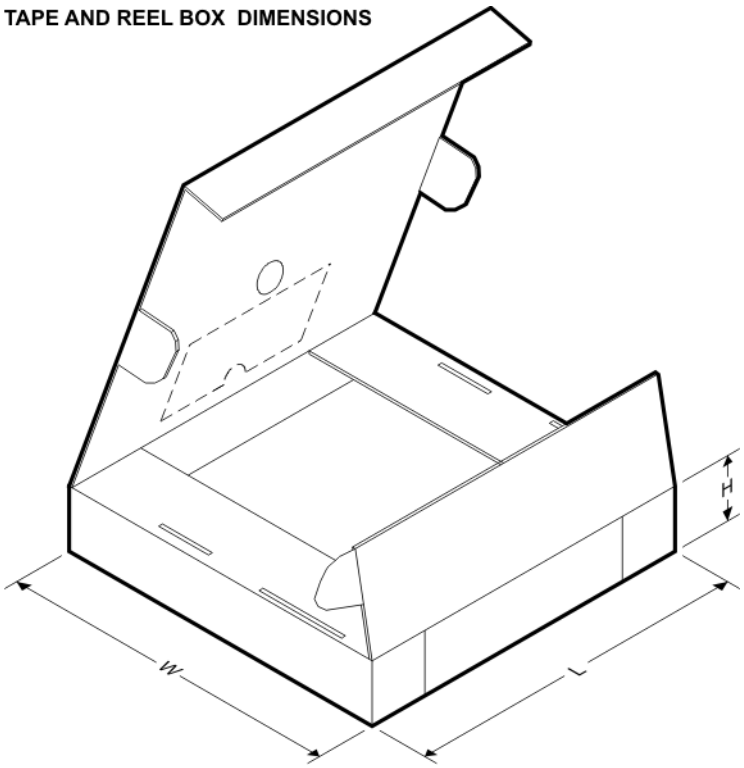
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM285DR-1-2	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM385BDR-1-2	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM385BPWR-1-2	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM385DR-1-2	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM385PWR-1-2	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

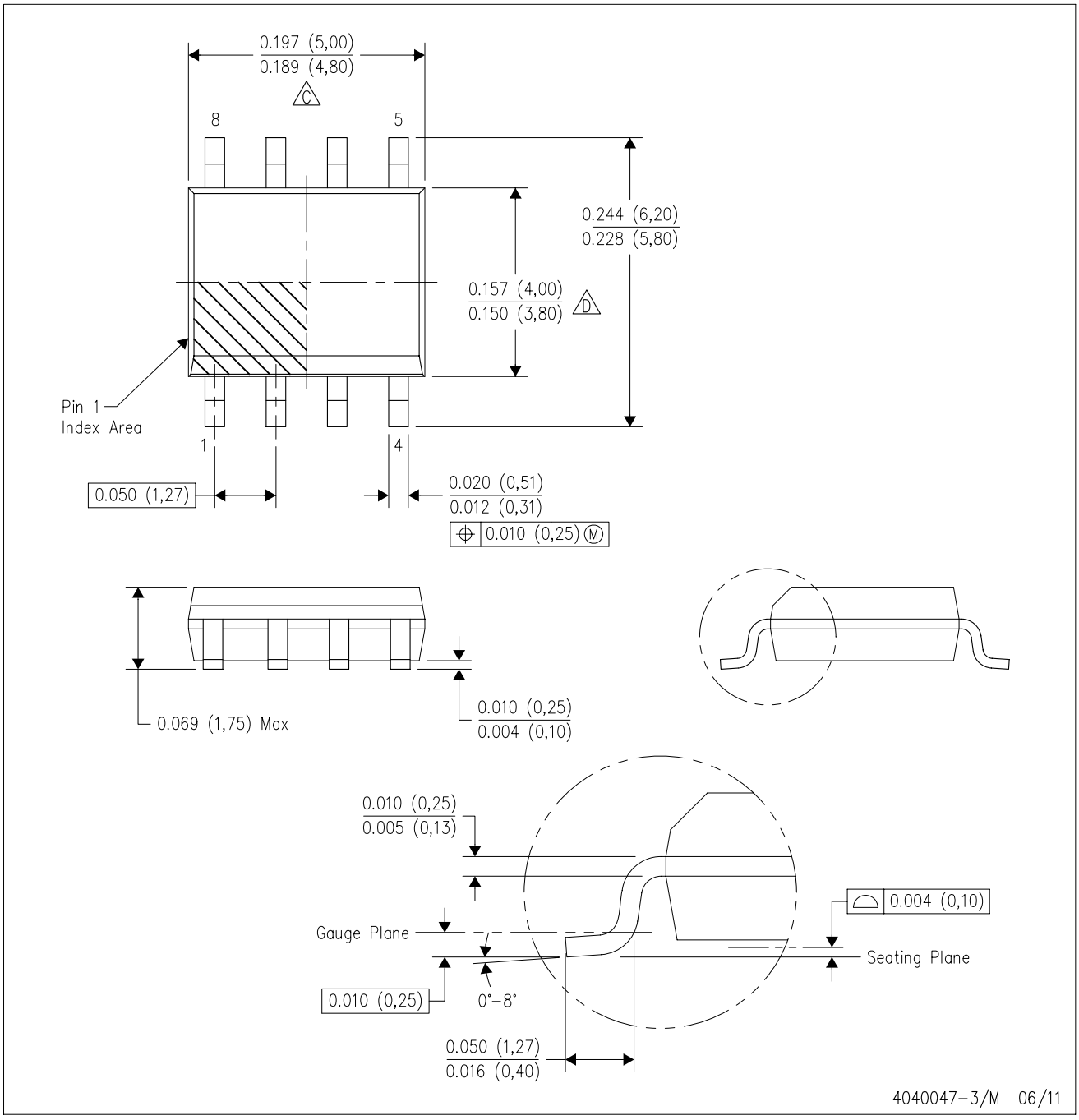
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

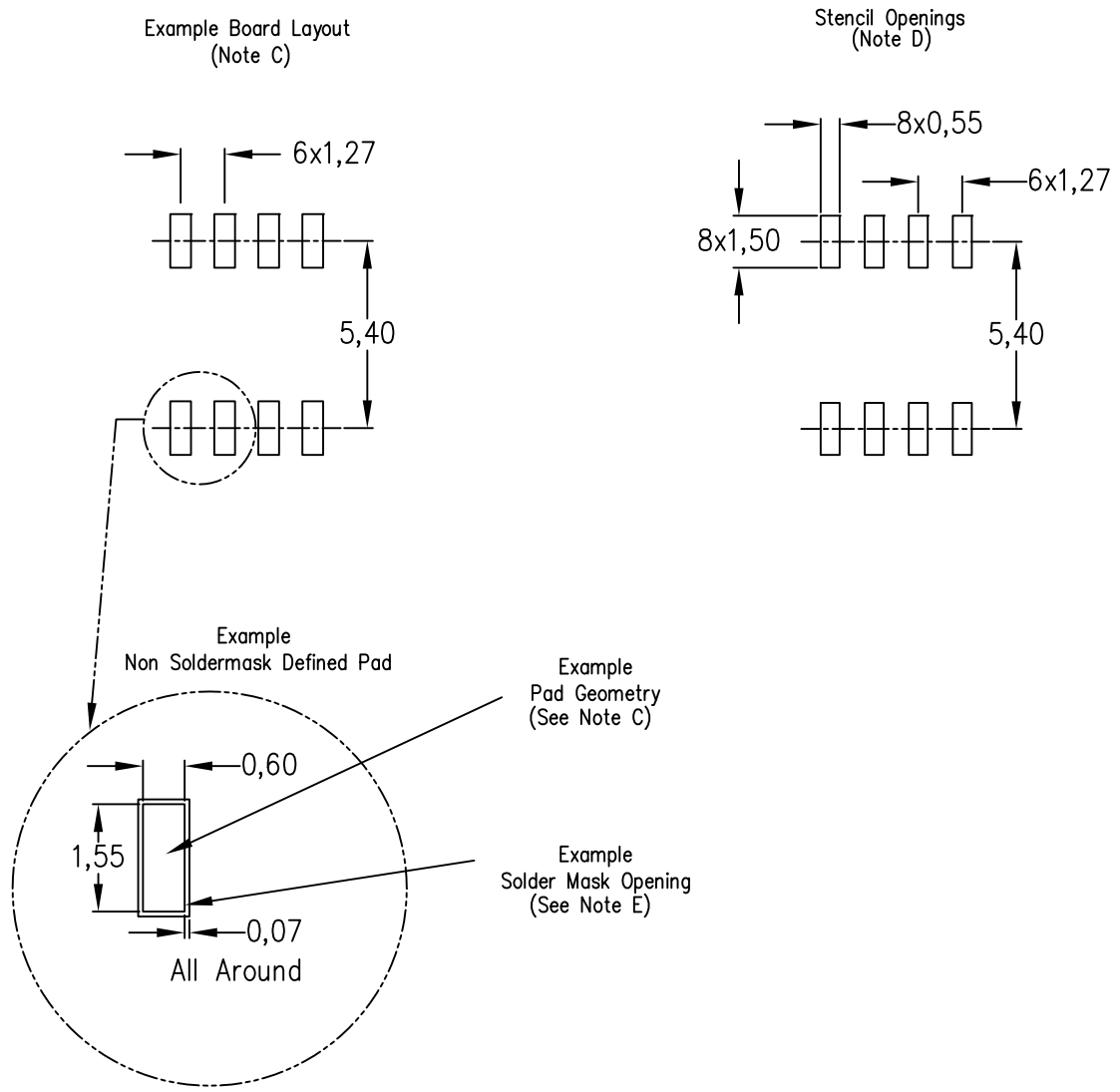
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM285DR-1-2	SOIC	D	8	2500	340.5	338.1	20.6
LM385BDR-1-2	SOIC	D	8	2500	340.5	338.1	20.6
LM385BPWR-1-2	TSSOP	PW	8	2000	367.0	367.0	35.0
LM385DR-1-2	SOIC	D	8	2500	340.5	338.1	20.6
LM385PWR-1-2	TSSOP	PW	8	2000	367.0	367.0	35.0

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



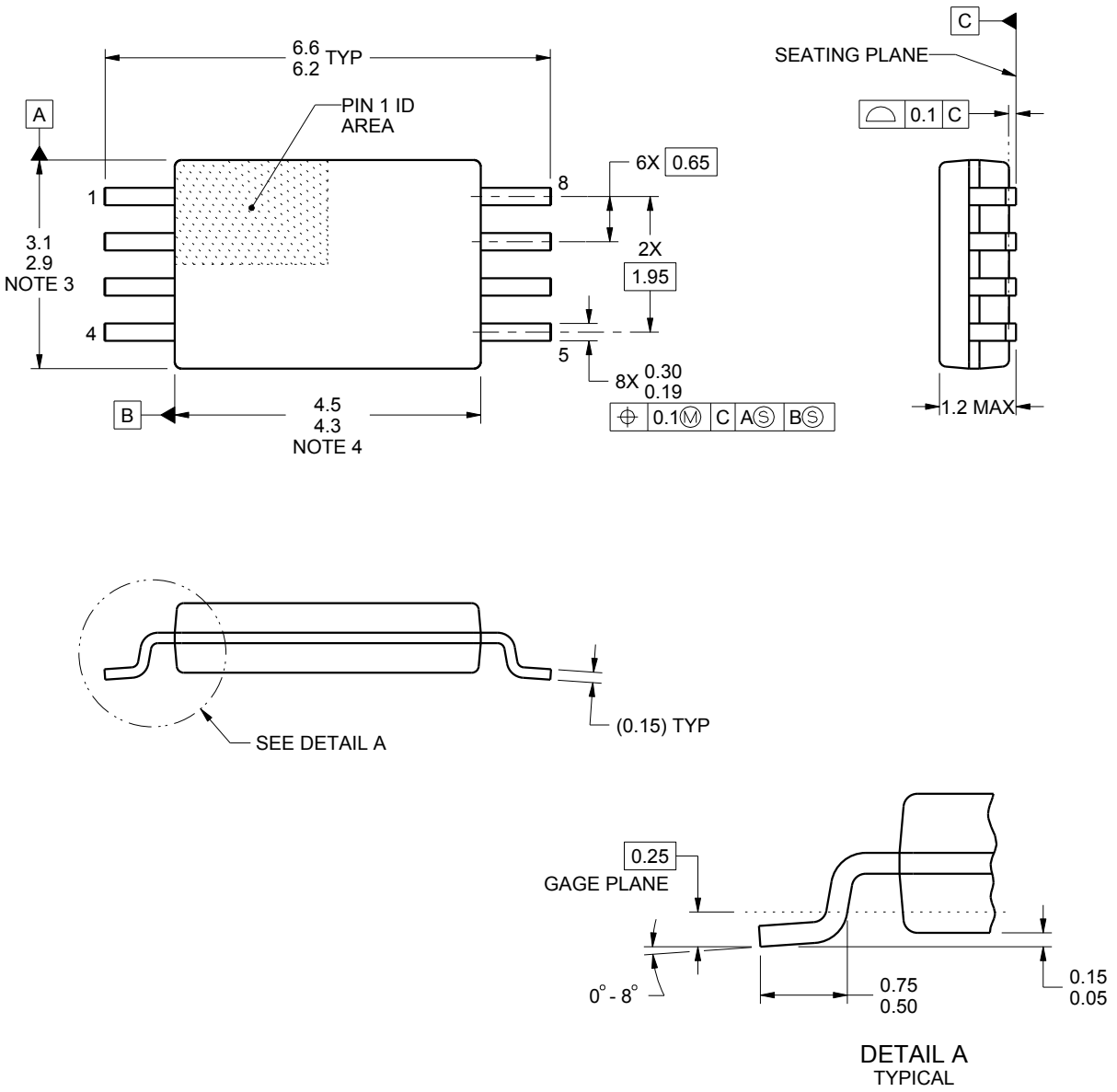
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PACKAGE OUTLINE

PW0008A

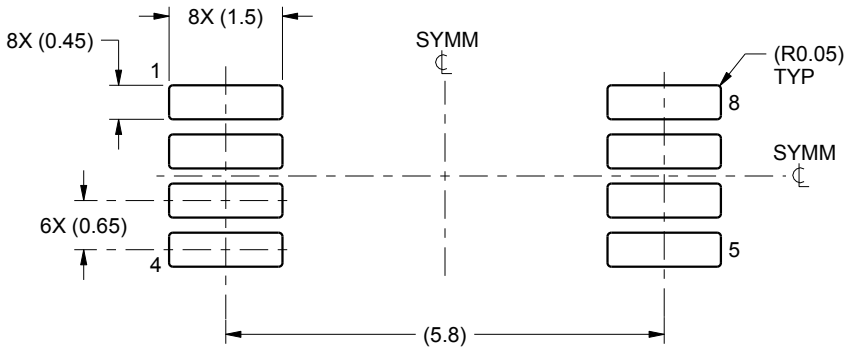
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

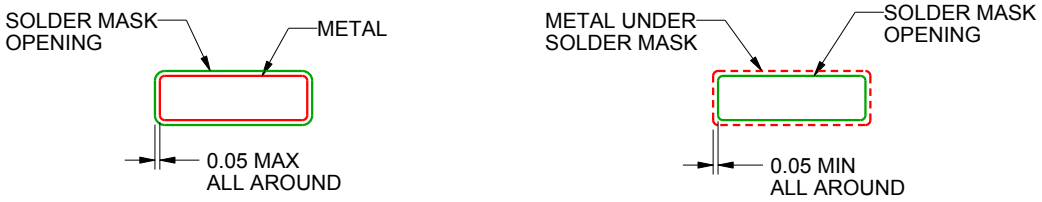


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X

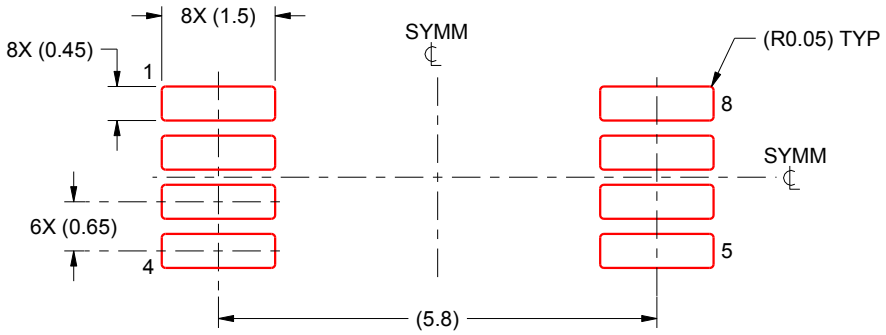


SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

LP 3 TO-92 - 5.34 mm max height

TRANSISTOR OUTLINE

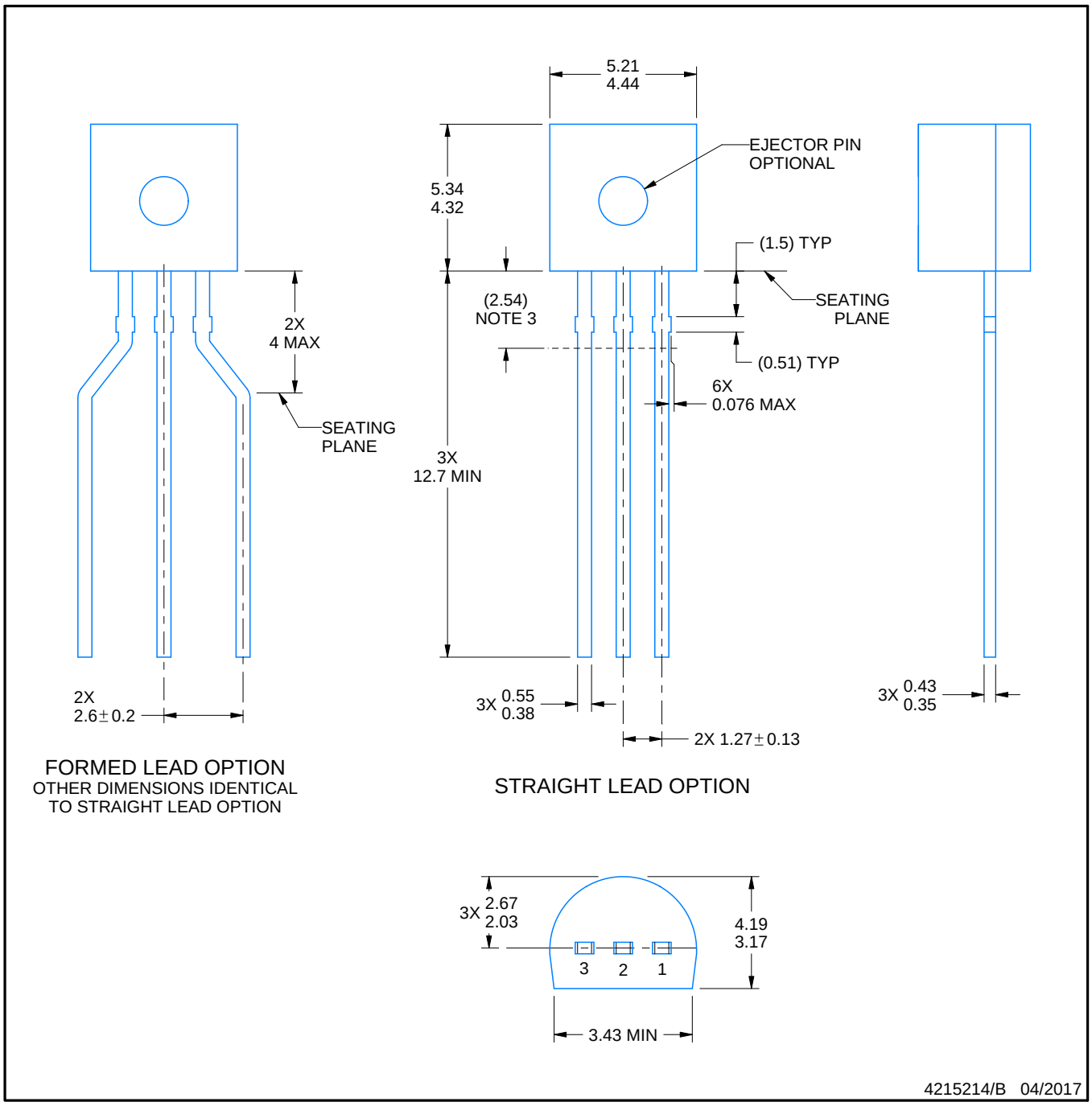
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

LP0003A

PACKAGE OUTLINE

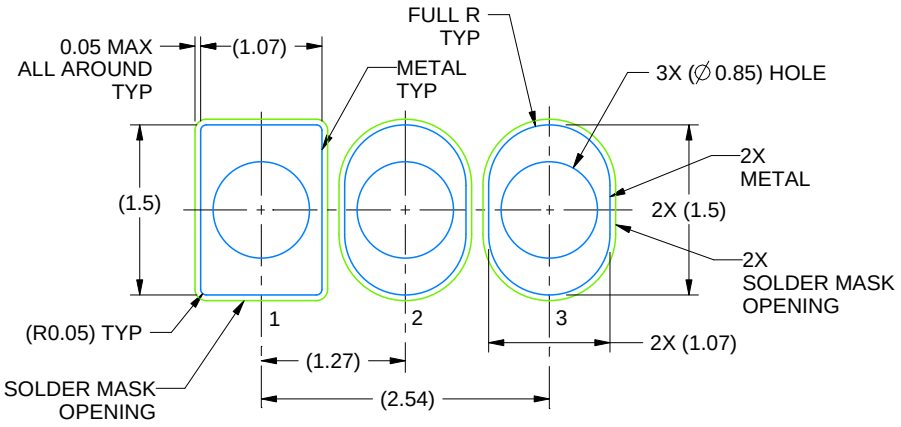
TO-92 - 5.34 mm max height

TO-92

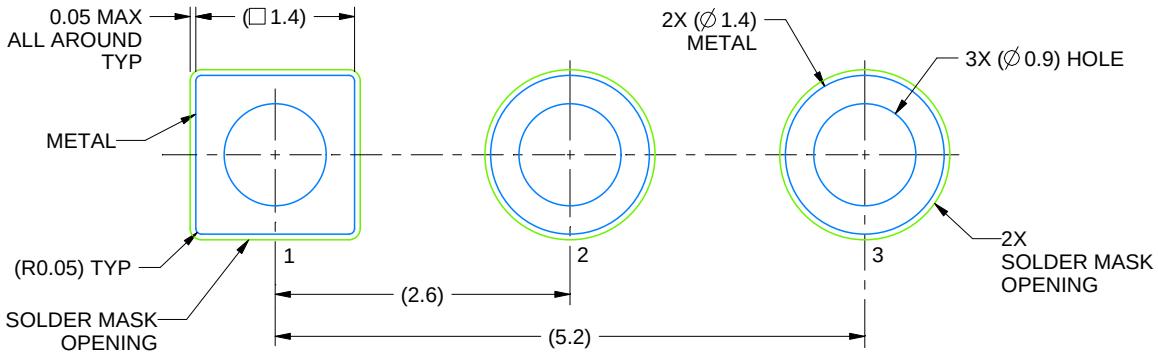


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Lead dimensions are not controlled within this area.
4. Reference JEDEC TO-226, variation AA.
5. Shipping method:
   a. Straight lead option available in bulk pack only.
   b. Formed lead option available in tape and reel or ammo pack.
   c. Specific products can be offered in limited combinations of shipping medium and lead options.
   d. Consult product folder for more information on available options.



LAND PATTERN EXAMPLE
STRAIGHT LEAD OPTION
NON-SOLDER MASK DEFINED
SCALE:15X



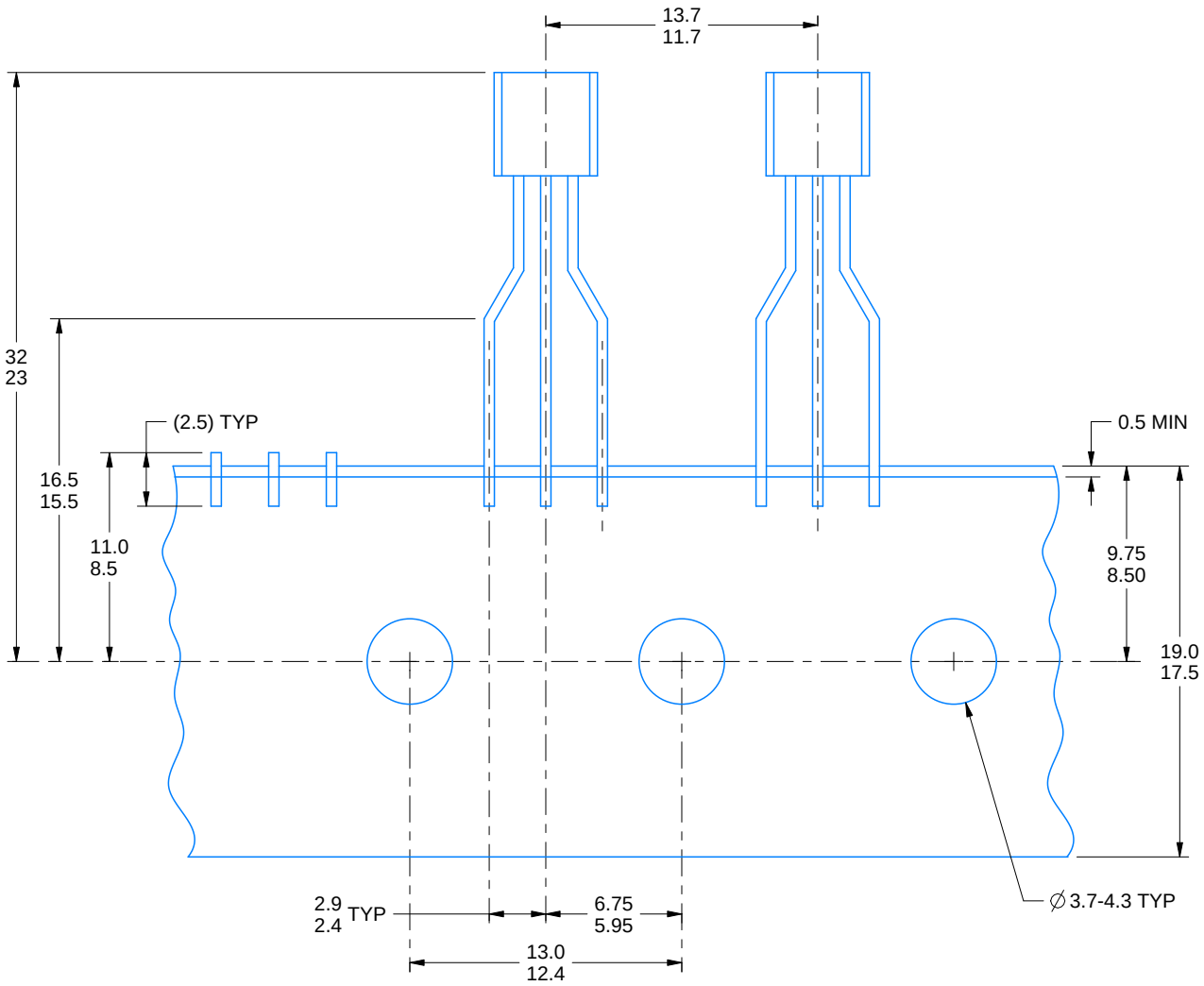
LAND PATTERN EXAMPLE
FORMED LEAD OPTION
NON-SOLDER MASK DEFINED
SCALE:15X

4215214/B 04/2017

LP0003A

TO-92 - 5.34 mm max height

TO-92



FOR FORMED LEAD OPTION PACKAGE

4215214/B 04/2017

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