# LMH6702 1.7-GHz Ultra-Low Distortion Wideband Op Amp

## 1 Features

$V_S$ = ±5 V, $T_A$ = 25°C, $A_V$ = 2V/V, $R_L$ = 100 Ω, $V_{OUT}$ = 2 $V_{PP}$, Typical Unless Noted:

- 2nd and 3rd Harmonics (5 MHz, SOT-23) −100/−96 dBc
- −3-dB Bandwidth ($V_{OUT}$ = 0.5 $V_{PP}$) 1.7 GHz
- Low Noise 1.83 nV/√Hz
- Fast Settling to 0.1% 13.4 ns
- Fast Slew Rate 3100 V/µs
- Supply Current 12.5 mA
- Output Current 80 mA
- Low Intermodulation Distortion (75 MHz) −67 dBc
- Improved Replacement for CLC409 and CLC449

## 2 Applications

- Flash A-D Driver
- D-A Transimpedance Buffer
- Wide Dynamic Range IF Amp
- Radar and Communication Receivers
- Line Driver
- High Resolution Video

## 3 Description

The LMH6702 is a very wideband, DC-coupled monolithic operational amplifier designed specifically for wide dynamic range systems requiring exceptional signal fidelity. Benefitting from current feedback architecture, the LMH6702 offers unity gain stability at exceptional speed without need for external compensation.

With its 720-MHz bandwidth ($A_V$ = 2 V/V, $V_O$ = 2 $V_{PP}$), 10-bit distortion levels through 60-MHz ($R_L$ = 100 Ω), 1.83-nV/√Hz input referred noise and 12.5-mA supply current, the LMH6702 is the ideal driver or buffer for high-speed flash A-D and D-A converters.

Wide dynamic range systems such as radar and communication receivers that require a wideband amplifier offering exceptional signal purity will find the low input referred noise and low harmonic and intermodulation distortion of the LMH6702 an attractive high speed solution.

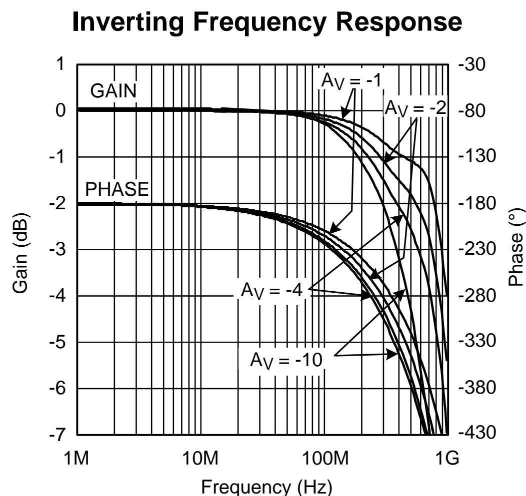
The LMH6702 is constructed using VIP10™ complimentary bipolar process and proven current feedback architecture. The LMH6702 is available in SOIC and SOT-23 packages.

**Device Information(1)**

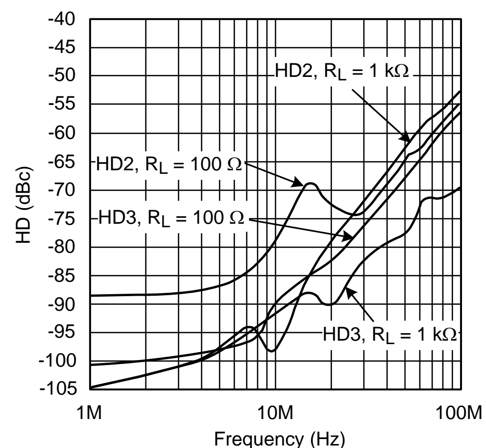
| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| LMH6702 | SOIC (8) | 4.90 mm × 3.91 mm |
| | SOT-23 (5) | 2.90 mm × 1.60 mm |

(1) For all available packages, see the orderable addendum at the end of the datasheet.

**Inverting Frequency Response**




**Harmonic Distortion vs Load and Frequency**



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

**Changes from Revision G (October 2014) to Revision H** — **Page**

- Updated *Thermal Information* ... 4
- Changed non-inverting input bias (with no test conditions) current maximum value from ±15 μA to –15 μA ... 6
- Changed non-inverting input bias (-40 ≤ $T_J$ ≤ 85) current maximum value from ±21 μA to –21 μA ... 6
- Added *Community Resources* section ... 17

**Changes from Revision F (March 2013) to Revision G** — **Page**

- Added, updated, or renamed the following sections: *Device Information*; *Specifications; Application and Implementation*; *Power Supply Recommendations*; *Layout*; *Device and Documentation Support*; *Mechanical, Packaging, and Ordering Information* ... 1
- Changed ±5 V to ±4 V in *Recommended Operating Conditions* ... 4

**Changes from Revision E (March 2013) to Revision F** — **Page**

- Changed layout of National Data Sheet to TI format ... 1


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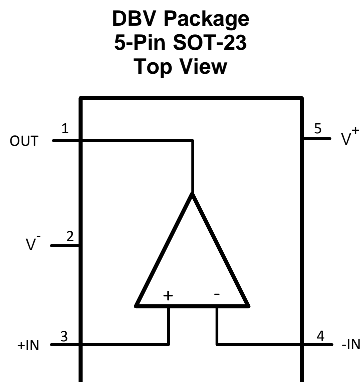
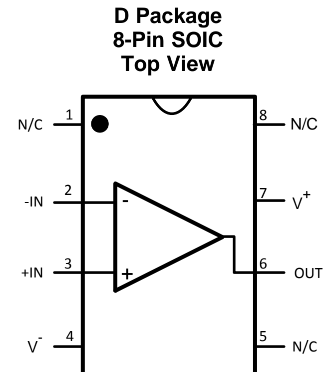
# 5 Pin Configuration and Functions

**DBV Package**
**5-Pin SOT-23**
**Top View**




**D Package**
**8-Pin SOIC**
**Top View**




NC: No internal connection

**Pin Functions**

| PIN | | | I/O | DESCRIPTION |
|---|---|---|---|---|
| NAME | NUMBER | | | |
| | D | DBV | | |
| -IN | 2 | 4 | I | Inverting input voltage |
| +IN | 3 | 3 | I | Non-inverting input voltage |
| N/C | 1, 5, 8 | – | – | No connection |
| OUT | 6 | 1 | O | Output |
| V- | 4 | 2 | I | Negative supply |
| V+ | 7 | 5 | I | Positive supply |

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) [1][2]

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_S$ | | | ±6.75 | V |
| $I_{OUT}$ | | | See[3] | |
| Common mode input voltage | | | $V^-$ to $V^+$ | V |
| Maximum junction temperature | | | 150 | °C |
| Storage temperature | | −65 | 150 | °C |
| Soldering information | Infrared or convection (20 s) | | 235 | °C |
| | Wave soldering (10 s) | | 260 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.
(3) The maximum output current ($I_{OUT}$) is determined by device power dissipation limitations.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1] | ±2000 | V |
| | | Machine Model (MM), per JEDEC specification JESD22-C101, all pins[2] | ±200 | |

(1) Human body model: 1.5 kΩ in series with 100 pF. JEDEC document JEP155 states that 2000-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 2000-V HBM is possible with the necessary precautions. Pins listed as ±2000 V may actually have higher performance.
(2) Machine model: 0 Ω in series with 200 pF. JEDEC document JEP157 states that 200-V MM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 200-V MM is possible with the necessary precautions. Pins listed as ±200 V may actually have higher performance.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)[1]

| | MIN | MAX | UNIT |
|---|---|---|---|
| Operating temperature | −40 | 85 | °C |
| Nominal supply voltage | ±4 | ±6 | V |

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications, see the Electrical Characteristics tables.

## 6.4 Thermal Information

| THERMAL METRIC[1] | | LMH6702 | | UNIT |
|---|---|---|---|---|
| | | DBV (SOT-23) | D (SOIC) | |
| | | 5 PINS | 8 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 182 | 133 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 139 | 79 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 40 | 73 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 28 | 28 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 40 | 73 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).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## 6.5 Electrical Characteristics

at $A_V$ = 2, $V_S$ = ±5 V, $R_L$ = 100 Ω, $R_F$ = 237 Ω (unless otherwise noted)[1]

| PARAMETER | | TEST CONDITIONS | MIN[2] | TYP[3] | MAX[2] | UNIT |
|---|---|---|---|---|---|---|
| **FREQUENCY DOMAIN PERFORMANCE** | | | | | | |
| $SSBW_{SM}$ | -3-dB Bandwidth | $V_{OUT}$ = 0.5 $V_{PP}$ | | 1700 | | MHz |
| $SSBW_{LG}$ | | $V_{OUT}$ = 2 $V_{PP}$ | | 720 | | |
| $LSBW_{LG}$ | | $V_{OUT}$ = 4 $V_{PP}$ | | 480 | | |
| $SSBW_{HG}$ | | $V_{OUT}$ = 2 $V_{PP}$, $A_V$ = +10 | | 140 | | |
| $GF_{0.1dB}$ | 0.1-dB gain flatness | $V_{OUT}$ = 2 $V_{PP}$ | | 120 | | MHz |
| LPD | Linear phase deviation | DC to 100 MHz | | 0.09 | | deg |
| DG | Differential gain | $R_L$ =150 Ω, 3.58 MHz | | 0.024% | | |
| | | $R_L$ =150 Ω, 4.43 MHz | | 0.021% | | |
| DP | Differential phase | $R_L$ = 150 Ω, 3.58 MHz | | 0.004 | | deg |
| | | $R_L$ = 150 Ω, 4.43 MHz | | 0.007 | | |
| **TIME DOMAIN RESPONSE** | | | | | | |
| $t_R$ | Rise time | 2-V Step, TRS | | 0.87 | | ns |
| | | 2-V Step, TRL | | 0.77 | | |
| $t_F$ | Fall time | 6-V Step, TRS | | 1.70 | | ns |
| | | 6-V Step, TRL | | 1.70 | | |
| OS | Overshoot | 2-V Step | | 0% | | |
| SR | Slew rate | 6 $V_{PP}$, 40% to 60%[4] | | 3100 | | V/µs |
| $T_s$ | Settling time to 0.1% | 2-V Step | | 13.4 | | ns |
| **DISTORTION AND NOISE RESPONSE** | | | | | | |
| HD2L | 2nd Harmonic distortion | 2 $V_{PP}$, 5 MHz[5] (SOT-23) | | −100 | | dBc |
| | | 2 $V_{PP}$, 5 MHz[5] (SOIC) | | −87 | | |
| HD2 | | 2$V_{PP}$, 20 MHz[5] (SOT-23) | | −79 | | dBc |
| | | 2$V_{PP}$, 20 MHz[5] (SOIC) | | −72 | | |
| HD2H | | 2$V_{PP}$, 60 MHz[5] (SOT-23) | | −63 | | dBc |
| | | 2$V_{PP}$, 60 MHz[5] (SOIC) | | −64 | | |
| HD3L | 3rd Harmonic distortion | 2$V_{PP}$, 5 MHz[5] (SOT-23) | | −96 | | dBc |
| | | 2$V_{PP}$, 5 MHz[5] (SOIC) | | −98 | | |
| HD3 | | 2$V_{PP}$, 20 MHz[5] (SOT-23) | | −88 | | dBc |
| | | 2$V_{PP}$, 20 MHz[5] (SOIC) | | −82 | | |
| HD3H | | 2$V_{PP}$, 60 MHz[5] (SOT-23) | | −70 | | dBc |
| | | 2$V_{PP}$, 60 MHz[5] (SOIC) | | −65 | | |
| OIM3 | IMD | 75 MHz, $P_O$ = 10dBm/ tone | | −67 | | dBc |
| $V_N$ | Input referred voltage noise | >1 MHz | | 1.83 | | nV/√Hz |
| $I_N$ | Input referred inverting noise current | >1 MHz | | 18.5 | | pA/√Hz |
| $I_{NN}$ | Input referred non-inverting noise current | >1 MHz | | 3.0 | | pA/√Hz |
| SNF | Total input noise floor | >1 MHz | | −158 | | $dBm_{1Hz}$ |
| INV | Total integrated input noise | 1 MHz to 150 MHz | | 35 | | µV |

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J$ = $T_A$. No guarantee of parametric performance is indicated in the electrical tables under conditions of internal self-heating where $T_J$ > $T_A$. Min/Max ratings are based on production testing unless otherwise specified.
(2) All limits are ensured by testing or statistical analysis.
(3) Typical numbers are the most likely parametric norm.
(4) Slew Rate is the average of the rising and falling edges.
(5) Harmonic distortion is strongly influenced by package type (SOT-23 or SOIC). See Application Note section under *Harmonic Distortion* for more information.

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## Electrical Characteristics (continued)

at $A_V$ = 2, $V_S$ = ±5 V, $R_L$ = 100 Ω, $R_F$ = 237 Ω (unless otherwise noted)(1)

| PARAMETER | | TEST CONDITIONS | | MIN(2) | TYP(3) | MAX(2) | UNIT |
|---|---|---|---|---|---|---|---|
| **STATIC, DC PERFORMANCE** | | | | | | | |
| $V_{IO}$ | Input offset voltage | | | | ±1.0 | ±4.5 | mV |
| | | | -40 ≤ $T_J$ ≤ 85 | | | ±6.0 | |
| $DV_{IO}$ | Input offset voltage average drift | See(6) | | | −13 | | μV/°C |
| $I_{BN}$ | Input bias current | Non-Inverting(7) | | | −6 | –15 | μA |
| | | | -40 ≤ $T_J$ ≤ 85 | | | –21 | |
| $DI_{BN}$ | Input bias current average drift | Non-Inverting(6) | | | +40 | | nA/°C |
| $I_{BI}$ | Input bias current | Inverting(7) | | | −8 | ±30 | μA |
| | | | -40 ≤ $T_J$ ≤ 85 | | | ±34 | |
| $DI_{BI}$ | Input bias current average drift | Inverting(6) | | | −10 | | nA/°C |
| PSRR | Power supply rejection ratio | DC | | 47 | 52 | | dB |
| | | | -40 ≤ $T_J$ ≤ 85 | 45 | | | |
| CMRR | Common mode rejection ration | DC | | 45 | 48 | | dB |
| | | | -40 ≤ $T_J$ ≤ 85 | 44 | | | |
| $I_{CC}$ | Supply current | $R_L$ = ∞ | | 11.0 | 12.5 | 16.1 | mA |
| | | | -40 ≤ $T_J$ ≤ 85 | 10.0 | | 17.5 | |
| **MISCELLANEOUS PERFORMANCE** | | | | | | | |
| $R_{IN}$ | Input resistance | Non-Inverting | | | 1.4 | | MΩ |
| $C_{IN}$ | Input capacitance | Non-Inverting | | | 1.6 | | pF |
| $R_{OUT}$ | Output resistance | Closed Loop | | | 30 | | mΩ |
| $V_{OL}$ | Output voltage range | $R_L$ = 100 Ω | | ±3.3 | ±3.5 | | V |
| | | | -40 ≤ $T_J$ ≤ 85 | ±3.2 | | | |
| CMIR | Input voltage range | Common Mode | | ±1.9 | ±2.2 | | V |
| $I_O$ | Output current | | | 50 | 80 | | mA |

(6) Drift determined by dividing the change in parameter at temperature extremes by the total temperature change.
(7) Negative input current implies current flowing out of the device.


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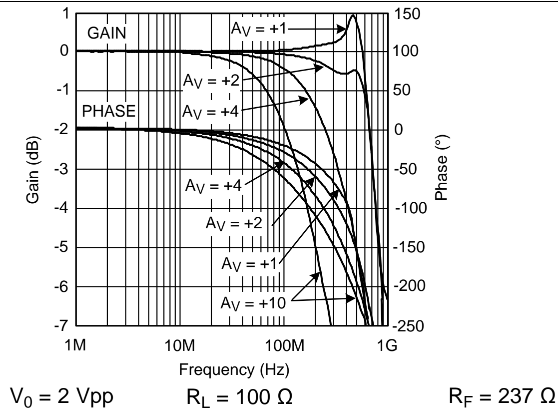
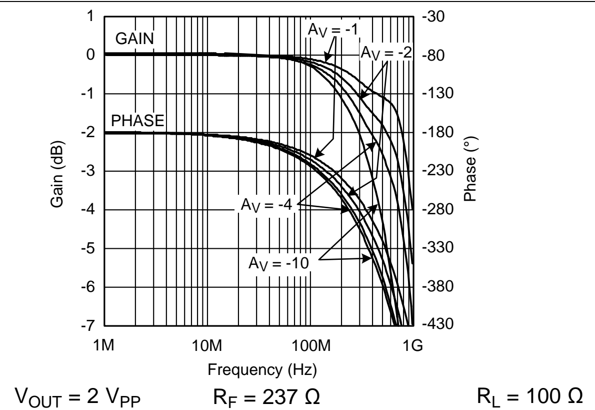
## 6.6 Typical Characteristics

$T_A$ = 25°C, $V_S$ = ±5 V, $R_L$ = 100 Ω, $R_f$ = 237 Ω (unless otherwise noted)



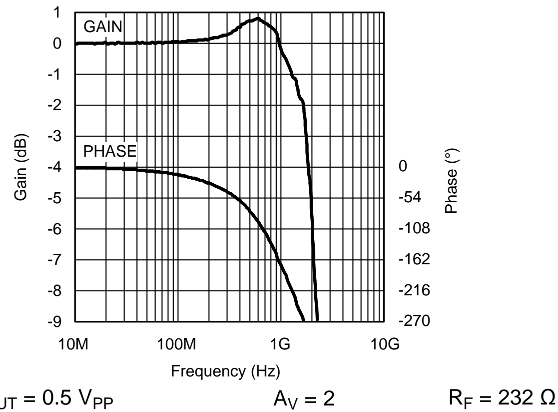

$V_0$ = 2 Vpp  $R_L$ = 100 Ω  $R_F$ = 237 Ω

**Figure 1. Non-Inverting Frequency Response**



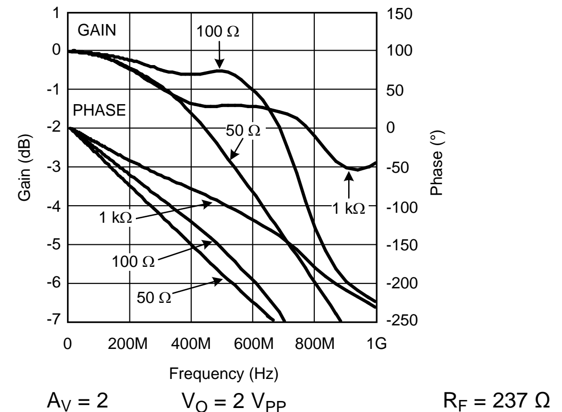

$V_{OUT}$ = 2 $V_{PP}$  $R_F$ = 237 Ω  $R_L$ = 100 Ω

**Figure 2. Inverting Frequency Response**



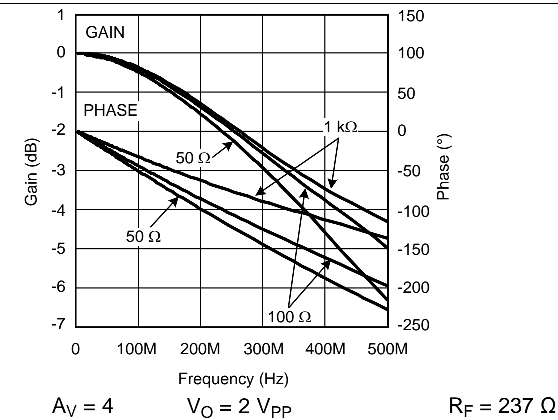

$V_{OUT}$ = 0.5 $V_{PP}$  $A_V$ = 2  $R_F$ = 232 Ω

**Figure 3. Small Signal Bandwidth**



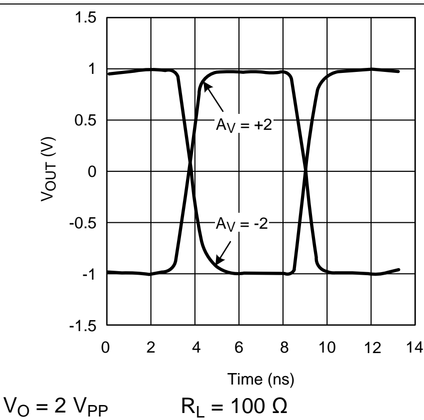

$A_V$ = 2  $V_O$ = 2 $V_{PP}$  $R_F$ = 237 Ω

**Figure 4. Frequency Response for Various $R_L$s, $A_V$ = 2**




$A_V$ = 4  $V_O$ = 2 $V_{PP}$  $R_F$ = 237 Ω

**Figure 5. Frequency Response for Various $R_L$s, $A_V$ = 4**




$V_O$ = 2 $V_{PP}$  $R_L$ = 100 Ω

**Figure 6. Step Response, 2 $V_{PP}$**

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## Typical Characteristics (continued)

$T_A$ = 25°C, $V_S$ = ±5 V, $R_L$ = 100 Ω, $R_f$ = 237 Ω (unless otherwise noted)

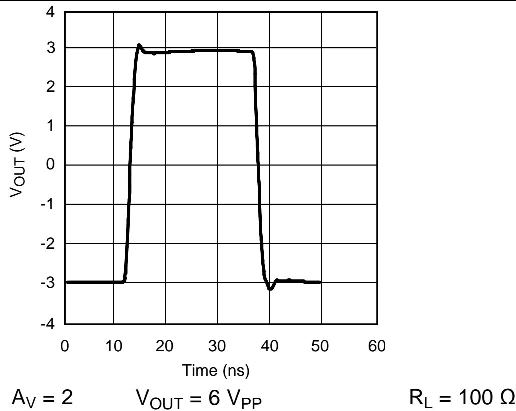


**Figure 7. Step Response, 6 $V_{PP}$**

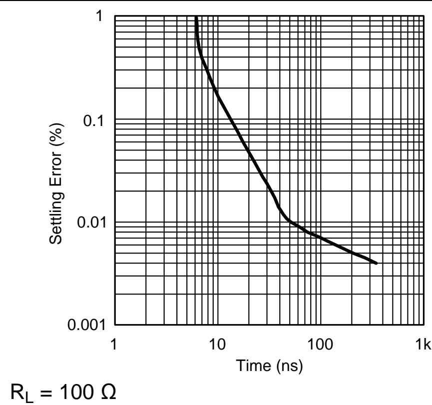


**Figure 8. Percent Settling vs Time**

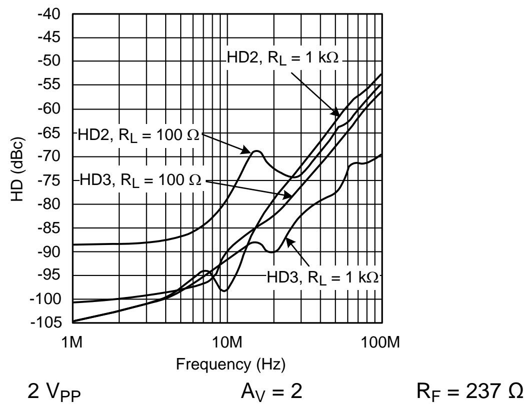


**Figure 9. Harmonic Distortion vs Load and Frequency (SOIC Package)**

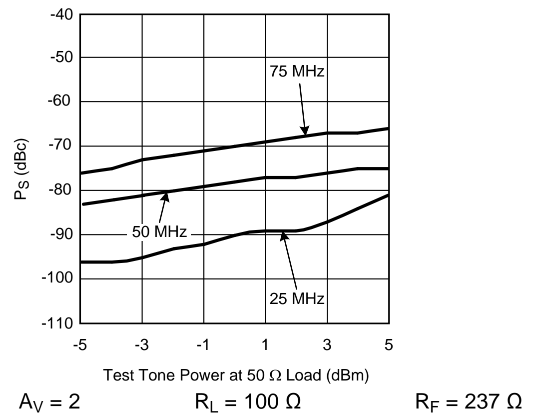


**Figure 10. 2 Tone 3rd Order Spurious Level (SOIC Package)**

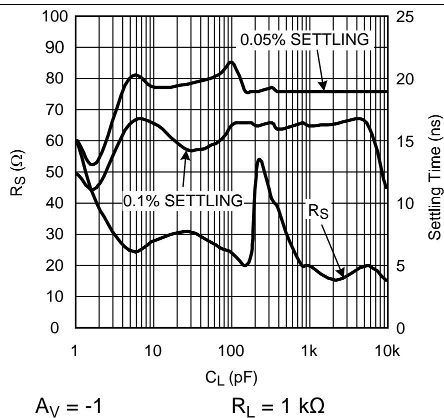


**Figure 11. $R_S$ and Settling Time vs $C_L$**

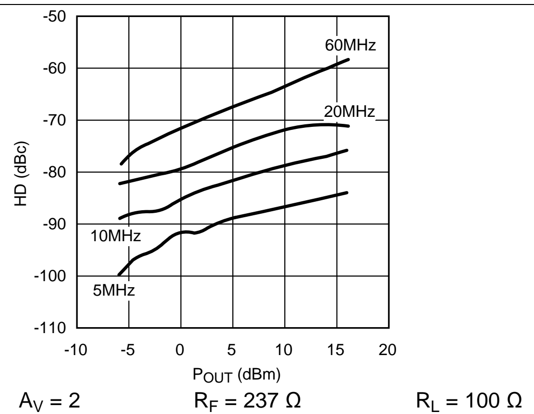


**Figure 12. HD2 vs Output Power (Across 100 Ω) (SOIC Package)**


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## Typical Characteristics (continued)

$T_A$ = 25°C, $V_S$ = ±5 V, $R_L$ = 100 Ω, $R_f$ = 237 Ω (unless otherwise noted)

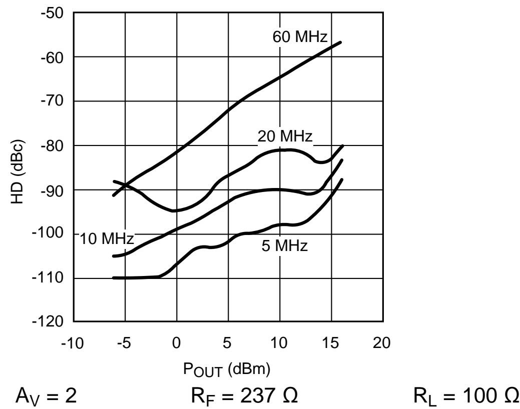



**Figure 13. HD3 vs Output Power (Across 100 Ω) (SOIC Package)**

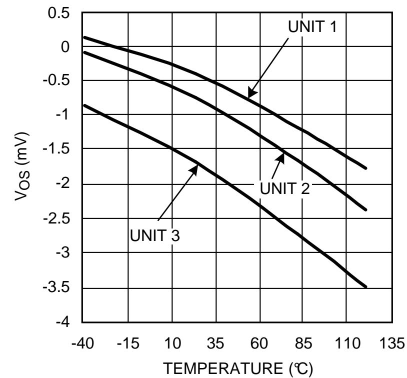



**Figure 14. Input Offset for 3 Representative Units**

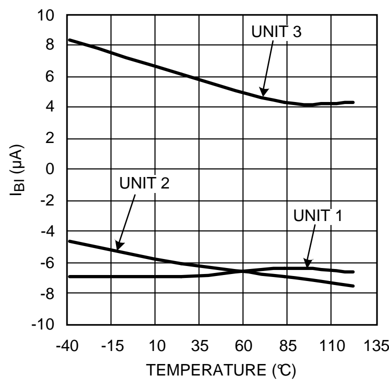



**Figure 15. Inverting Input Bias for 3 Representative Units**

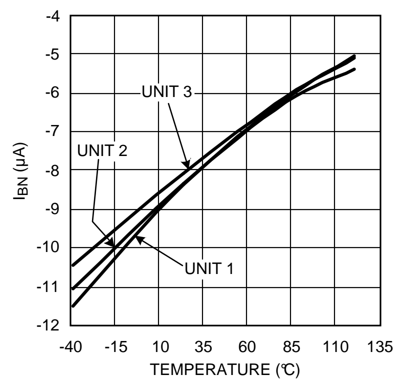



**Figure 16. Non-Inverting Input Bias for 3 Representative Units**

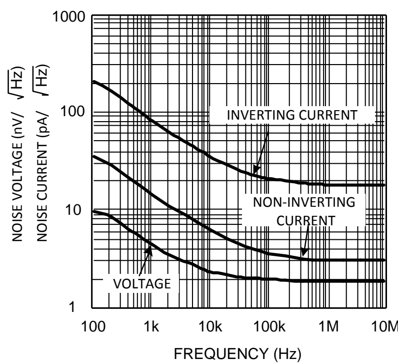



**Figure 17. Noise**

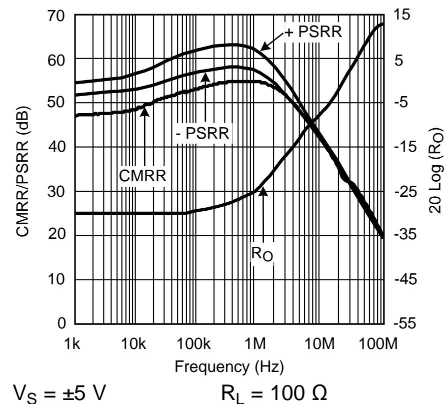
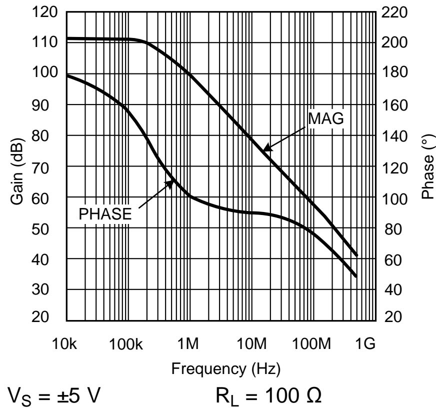



**Figure 18. CMRR, PSRR, $R_{OUT}$**

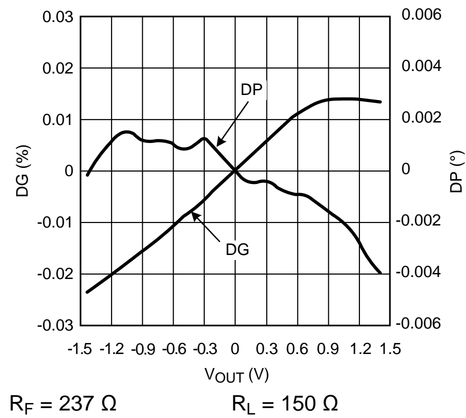
## Typical Characteristics (continued)

$T_A$ = 25°C, $V_S$ = ±5 V, $R_L$ = 100 Ω, $R_f$ = 237 Ω (unless otherwise noted)



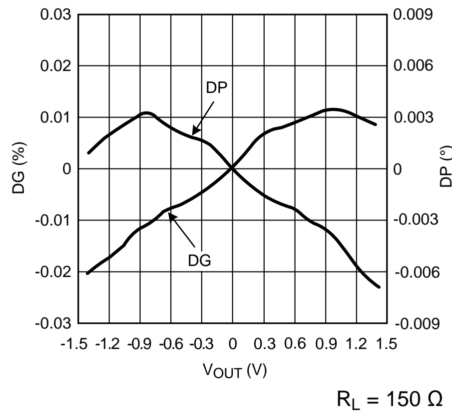

$V_S$ = ±5 V $R_L$ = 100 Ω

Figure 19. Transimpedance




$R_F$ = 237 Ω $R_L$ = 150 Ω

Figure 20. DG/DP (NTSC)




$R_F$ = 237 Ω $R_L$ = 150 Ω

Figure 21. DG/DP (PAL)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# 7 Detailed Description

## 7.1 Overview

The LMH6702 has been optimized for exceptionally low harmonic distortion while driving very demanding resistive or capacitive loads. Generally, when used as the input amplifier to very high speed flash ADCs, the distortions introduced by the converter will dominate over the low LMH6702 distortions shown in *Typical Characteristics*.

## 7.2 Feature Description

### 7.2.1 Harmonic Distortion

The capacitor $C_{SS}$, shown across the supplies in Figure 24 and Figure 25, is critical to achieving the lowest 2nd harmonic distortion. For absolute minimum distortion levels, it is also advisable to keep the supply decoupling currents (ground connections to $C_{POS}$, and $C_{NEG}$ in Figure 24 and Figure 25) separate from the ground connections to sensitive input circuitry (such as $R_G$, $R_T$, and $R_{IN}$ ground connections). Splitting the ground plane in this fashion and separately routing the high frequency current spikes on the decoupling caps back to the power supply (similar to *Star Connection* layout technique) ensures minimum coupling back to the input circuitry and results in best harmonic distortion response (especially 2nd order distortion).

If this layout technique has not been observed on a particular application board, designer may actually find that supply decoupling caps could adversely affect HD2 performance by increasing the coupling phenomenon already mentioned. Figure 22 shows actual HD2 data on a board where the ground plane is *shared* between the supply decoupling capacitors and the rest of the circuit. Once these capacitors are removed, the HD2 distortion levels reduce significantly, especially between 10 MHz to 20 MHz, as shown in Figure 22:

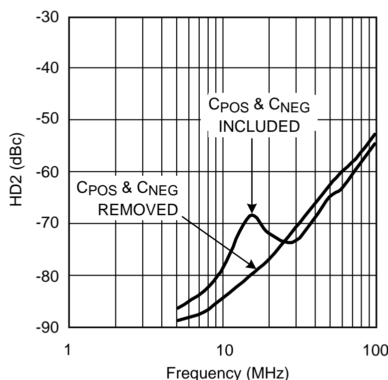


**Figure 22. Decoupling Current Adverse Effect on a Board with Shared Ground Plane**

At these extremely low distortion levels, the high frequency behavior of decoupling capacitors themselves could be significant. In general, lower value decoupling caps tend to have higher resonance frequencies making them more effective for higher frequency regions. A particular application board which has been laid out correctly with ground returns *split* to minimize coupling, would benefit the most by having low value and higher value capacitors paralleled to take advantage of the effective bandwidth of each and extend low distortion frequency range.

Another important variable in getting the highest fidelity signal from the LMH6702 is the package itself. As already noted, coupling between high frequency current transients on supply lines and the device input can lead to excess harmonic distortion. An important source of this coupling is in fact through the device bonding wires. A smaller package, in general, will have shorter bonding wires and therefore lower coupling. This is true in the case of the SOT-23 compared to the SOIC package where a marked improvement in HD can be measured in the SOT-23 package. Figure 23 shows the HD comparing SOT-23 to SOIC package:

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## Feature Description (continued)

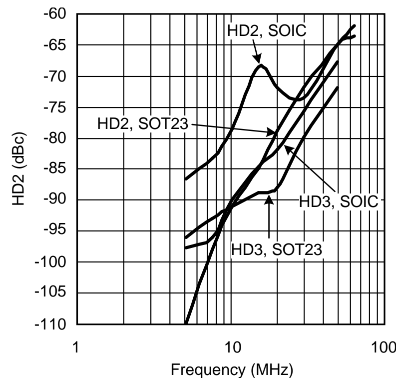


**Figure 23. SOIC and SOT-23 Packages Distortion Terms Compared**

The LMH6702 data sheet shows both SOT-23 and SOIC data in *Electrical Characteristics* to aid in selecting the right package. *Typical Characteristics* shows SOIC package plots only.

## 7.3 Device Functional Modes

### 7.3.1 2-Tone 3rd Order Intermodulation

Figure 10 shows a relatively constant difference between the test power level and the spurious level with the difference depending on frequency. The LMH6702 does not show an intercept type performance, (where the relative spurious levels change at a 2X rate versus the test tone powers), due to an internal full power bandwidth enhancement circuit that boosts the performance as the output swing increases while dissipating negligible quiescent power under low output power conditions. This feature enhances the distortion performance and full power bandwidth to match that of much higher quiescent supply current parts.

### 7.3.2 DC Accuracy and Noise

The example in Equation 1 shows the output offset computation equation for the non-inverting configuration using the typical bias current and offset specifications for $A_V$ = 2:

Output Offset:

$$V_O = (\pm I_{BN} \cdot R_{IN} \pm V_{IO}) (1 + R_F/R_G) \pm I_{BI} \cdot R_F$$

where

- $R_{IN}$ is the equivalent input impedance on the non-inverting input. (1)

Example computation for $A_V$ = +2, $R_F$ = 237Ω, $R_{IN}$ = 25Ω:

$$V_O = (\pm 6\ \mu A \times 25\ \Omega \pm 1mV) (1 + 237/237) \pm 8\ \mu A \times 237 = \pm 4.20\ mV \quad (2)$$

A good design, however, should include a worst case calculation using min/max numbers in the data sheet tables, in order to ensure *worst case* operation.

Further improvement in the output offset voltage and drift is possible using the composite amplifiers described in Application Note OA--07, *Current Feedback Op Amp Applications Circuit Guide* (SNOA365). The two input bias currents are physically unrelated in both magnitude and polarity for the current feedback topology. It is not possible, therefore, to cancel their effects by matching the source impedance for the two inputs (as is commonly done for matched input bias current devices).

The total output noise is computed in a similar fashion to the output offset voltage. Using the input noise voltage and the two input noise currents, the output noise is developed through the same gain equations for each term but combined as the square root of the sum of squared contributing elements. See Application Note OA-12, *Noise Analysis for Comlinear Amplifiers* (SNOA375) for a full discussion of noise calculations for current feedback amplifiers.


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# 8 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 8.1 Application Information

The LMH6702 achieves its excellent pulse and distortion performance by using the current feedback topology. The loop gain for a current feedback op amp, and hence the frequency response, is predominantly set by the feedback resistor value. The LMH6702 is optimized for use with a 237-Ω feedback resistor. Using lower values can lead to excessive ringing in the pulse response while a higher value will limit the bandwidth.

## 8.2 Typical Application

### 8.2.1 Feedback Resistor

The LMH6702 achieves its excellent pulse and distortion performance by using the current feedback topology. The loop gain for a current feedback op amp, and hence the frequency response, is predominantly set by the feedback resistor value. The LMH6702 is optimized for use with a 237-Ω feedback resistor. Using lower values can lead to excessive ringing in the pulse response while a higher value will limit the bandwidth.

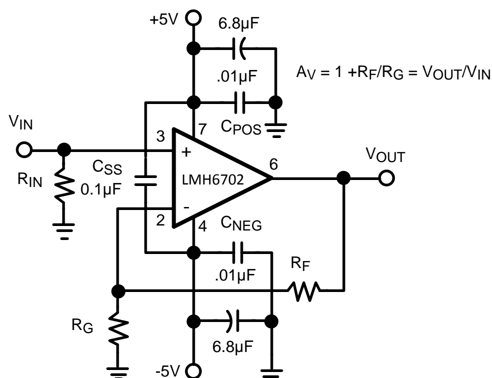


**Figure 24. Recommended Non-Inverting Gain Circuit**

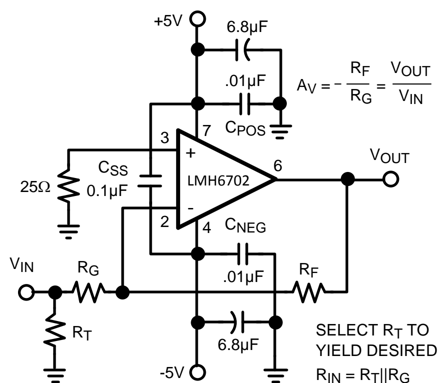


**Figure 25. Recommended Inverting Gain Circuit**

## Typical Application (continued)

### 8.2.2 Design Requirements

The exceptional performance and uniquely targeted superior technical specifications of the LMH6702 make it a natural choice for high speed data acquisition applications as a front end amplifier driving the input of a high performance ADC. Of these specifications, the following can be discussed in more detail:

1. A bandwidth of 1.7 GHz and relative insensitivity of bandwidth to closed loop gain (characteristic of Current Feedback architecture when compared to the traditional voltage feedback architecture) as shown in Figure 1.
2. Ultra-low distortion approaching -87 dBc at the lower frequencies and exceptional noise performance (see Figure 9 and Figure 17).
3. Fast settling in less than 20 ns (see Figure 27).

As the input of an ADC could be capacitive in nature and could also alternate in capacitance value during a typical acquisition cycle, the driver amplifier (LMH6702 in this case) should be designed so that it avoids instability, peaking, or other undesirable artifacts.

For Capacitive Load Drive, see Figure 26, which shows a typical application using the LMH6702 to drive an ADC.

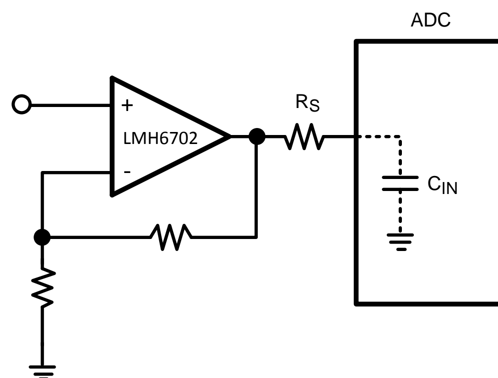


**Figure 26. Input Amplifier to ADC**

### 8.2.3 Detailed Design Procedure

The series resistor, $R_S$, between the amplifier output and the ADC input is critical to achieving best system performance. This load capacitance, if applied directly to the output pin, can quickly lead to unacceptable levels of ringing in the pulse response. Figure 27 in *Application Curve* ($R_S$ and Settling Time vs $C_L$) is an excellent starting point for selecting $R_S$. The value derived in that plot minimizes the step settling time into a fixed discrete capacitive load with the output driving a very light resistive load (1 kΩ). Sensitivity to capacitive loading is greatly reduced once the output is loaded more heavily. Therefore, for cases where the output is heavily loaded, $R_S$ value may be reduced. The exact value may best be determined experimentally for these cases.

In applications where the LMH6702 is replacing the CLC409, care must be taken when the device is lightly loaded and some capacitance is present at the output. Due to the much higher frequency response of the LMH6702 compared to the CLC409, there could be increased susceptibility to low value output capacitance (parasitic or inherent to the board layout or otherwise being part of the output load). As already mentioned, this susceptibility is most noticeable when the LMH6702's resistive load is light. Parasitic capacitance can be minimized by careful lay out. Addition of an output snubber R-C network will also help by increasing the high frequency resistive loading.

Referring back to Figure 26, it must be noted that several additional constraints should be considered in driving the capacitive input of an ADC. There is an option to increase $R_S$, band-limiting at the ADC input for either noise or Nyquist band-limiting purposes. However, increasing $R_S$ too much can induce an unacceptably large input glitch due to switching transients coupling through from the *convert* signal. Also, $C_{IN}$ is oftentimes a voltage dependent capacitance. This input impedance non-linearity will induce distortion terms that will increase as $R_S$ is increased. Only slight adjustments up or down from the recommended $R_S$ value should therefore be attempted in optimizing system performance.


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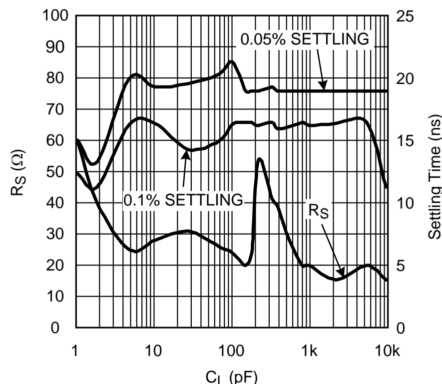
## Typical Application (continued)

### 8.2.4 Application Curve




$A_V$ = -1 $R_L$ = 1 kΩ

**Figure 27. $R_S$ and Settling Time vs $C_L$**

# 9 Power Supply Recommendations

The LMH6702 can operate off a single supply or with dual supplies as long as the input CM voltage range (CMIR) has the required headroom to either supply rail. Supplies should be decoupled with low inductance, often ceramic, capacitors to ground less than 0.5 inches from the device pins. The use of ground plane is recommended, and as in most high speed devices, it is advisable to remove ground plane close to device sensitive pins such as the inputs.

# 10 Layout

## 10.1 Layout Guidelines

Generally, a good high frequency layout will keep power supply and ground traces away from the inverting input and output pins. Parasitic capacitances on these nodes to ground will cause frequency response peaking and possible circuit oscillations. See *Frequent Faux Pas in Applying Wideband Current Feedback Amplifiers*, Application Note OA-15 (SNOA367). Texas Instruments suggests the following evaluation boards as a guide for high frequency layout and as an aid in device testing and characterization. See Table 1 for details.

The LMH6702 evaluation board(s) is a good example of high frequency layout techniques as a reference. General high-speed, signal-path layout suggestions include:

- Continuous ground planes are preferred for signal routing with matched impedance traces for longer runs. However, open up both ground and power planes around the capacitive sensitive input and output device pins as shown in Figure 28. After the signal is sent into a resistor, parasitic capacitance becomes more of a bandlimiting issue and less of a stability issue.
- Use good, high-frequency decoupling capacitors (0.1 μF) on the ground plane at the device power pins as shown in Figure 28. Higher value capacitors (2.2 μF) are required, but may be placed further from the device power pins and shared among devices. For best high-frequency decoupling, consider X2Y supply-decoupling capacitors that offer a much higher self-resonance frequency over standard capacitors.
- When using differential signal routing over any appreciable distance, use microstrip layout techniques with matched impedance traces.
- The input summing junction is very sensitive to parasitic capacitance. Connect any Rf, and Rg elements into the summing junction with minimal trace length to the device pin side of the resistor, as shown in Figure 29. The other side of these elements can have more trace length if needed to the source or to ground.

## 10.2 Layout Example

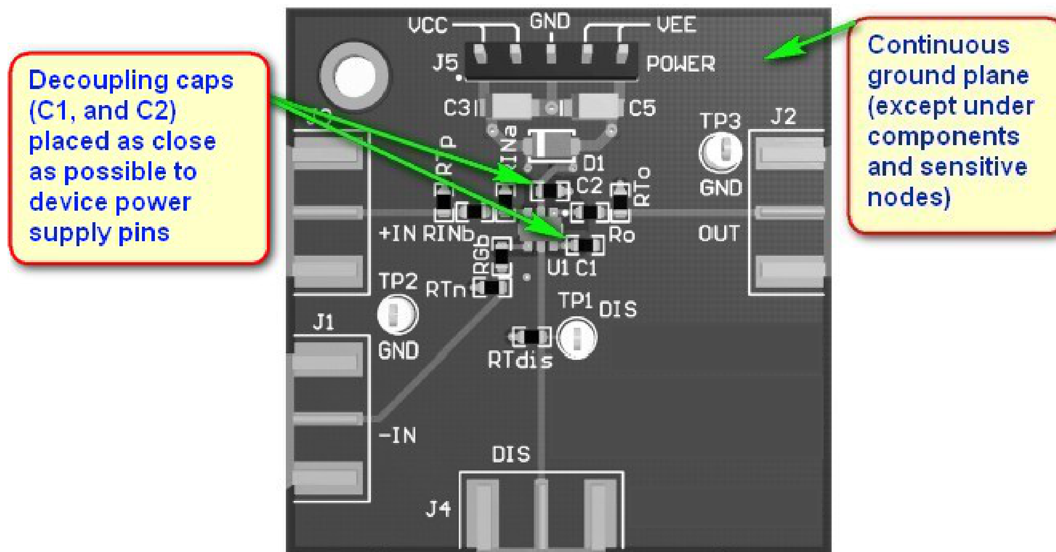



Figure 28. LMH6702 Evaluation Board Layer 1

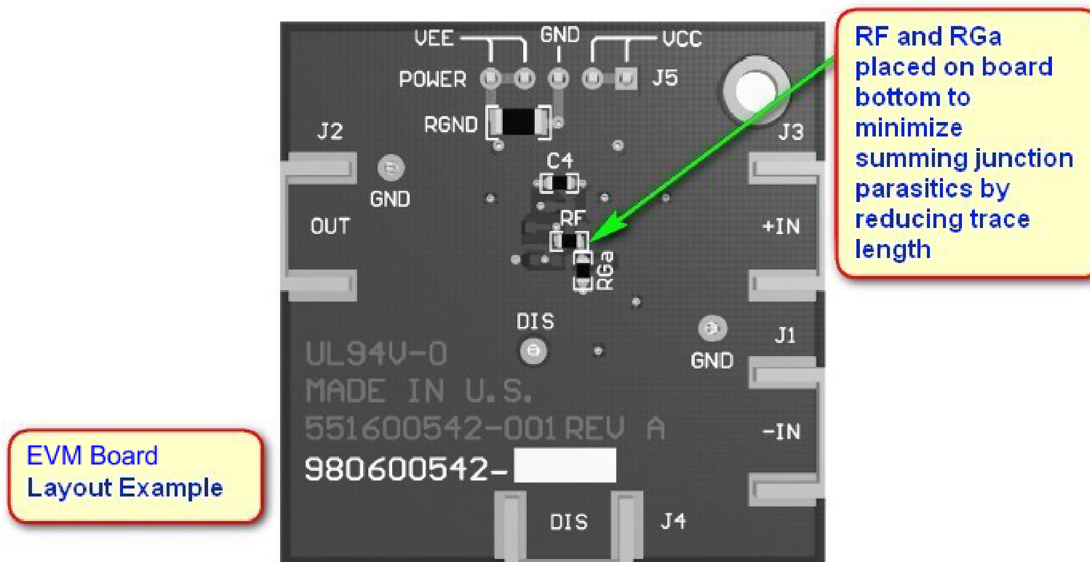



Figure 29. LMH6702 Evaluation Board Layer 2

Table 1. Evaluation Board Comparison

| DEVICE | PACKAGE | EVALUATION BOARD PART NUMBER |
|---|---|---|
| LMH6702MF | SOT-23 | LMH730216 |
| LMH6702MA | SOIC | LMH730227 |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# 11 Device and Documentation Support

## 11.1 Documentation Support

### 11.1.1 Related Documentation

For related documentation, see the following:

- *Absolute Maximum Ratings for Soldering* (SNOA549)
- *Current Feedback Op Amp Applications Circuit Guide*, Application Note OA--07 (SNOA365)
- *Frequent Faux Pas in Applying Wideband Current Feedback Amplifiers*, Application Note OA-15 (SNOA367)
- *Noise Analysis for Comlinear Amplifiers*, Application Note OA-12 (SNOA375)
- *Semiconductor and IC Package Thermal Metrics* (SPRA953)

## 11.2 Community Resources

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**Design Support** ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

## 11.3 Trademarks

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All other trademarks are the property of their respective owners.

## 11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## 11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| LMH6702 MDC | ACTIVE | DIESALE | Y | 0 | 754 | Green (RoHS & no Sb/Br) | Call TI | Level-1-NA-UNLIM | -40 to 85 | | Samples |
| LMH6702MA | NRND | SOIC | D | 8 | 95 | TBD | Call TI | Call TI | -40 to 85 | LMH67 02MA | |
| LMH6702MA/NOPB | ACTIVE | SOIC | D | 8 | 95 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 85 | LMH67 02MA | Samples |
| LMH6702MAX/NOPB | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 85 | LMH67 02MA | Samples |
| LMH6702MF/NOPB | ACTIVE | SOT-23 | DBV | 5 | 1000 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 85 | A83A | Samples |
| LMH6702MFX/NOPB | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 85 | A83A | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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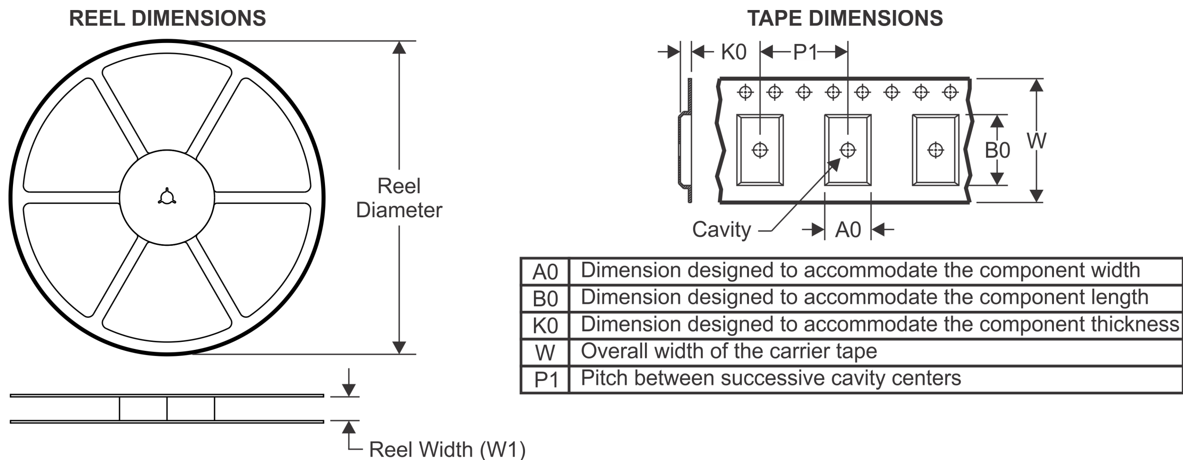
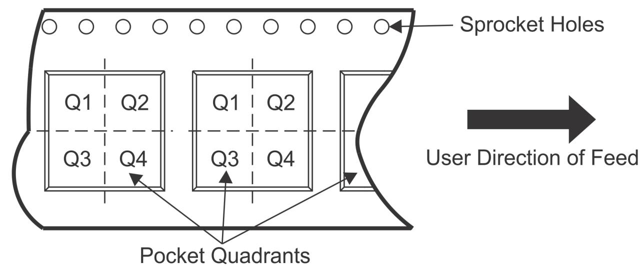
## TAPE AND REEL INFORMATION




| A0 | Dimension designed to accommodate the component width |
|---|---|
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

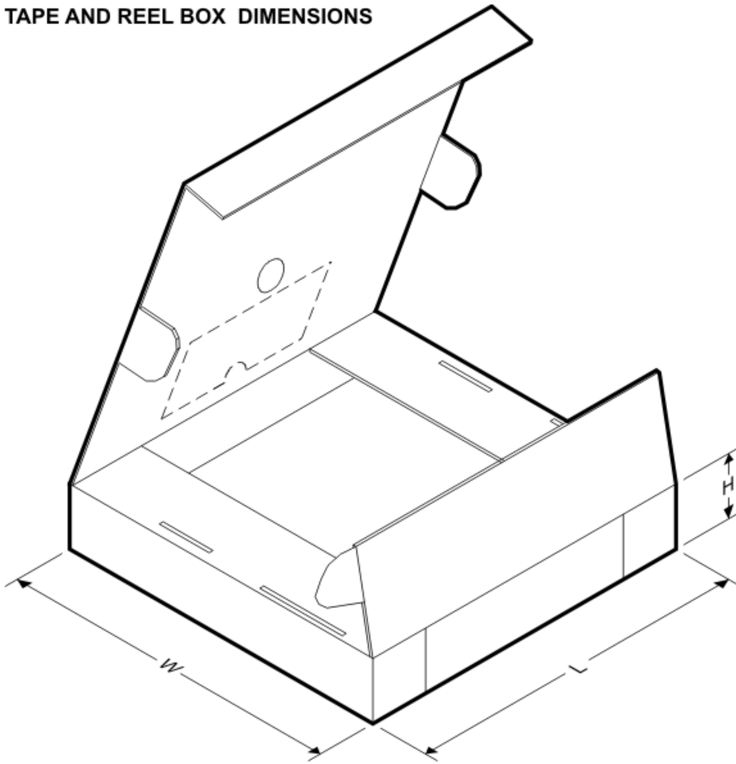
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LMH6702MAX/NOPB | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.5 | 5.4 | 2.0 | 8.0 | 12.0 | Q1 |
| LMH6702MF/NOPB | SOT-23 | DBV | 5 | 1000 | 178.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| LMH6702MFX/NOPB | SOT-23 | DBV | 5 | 3000 | 178.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |

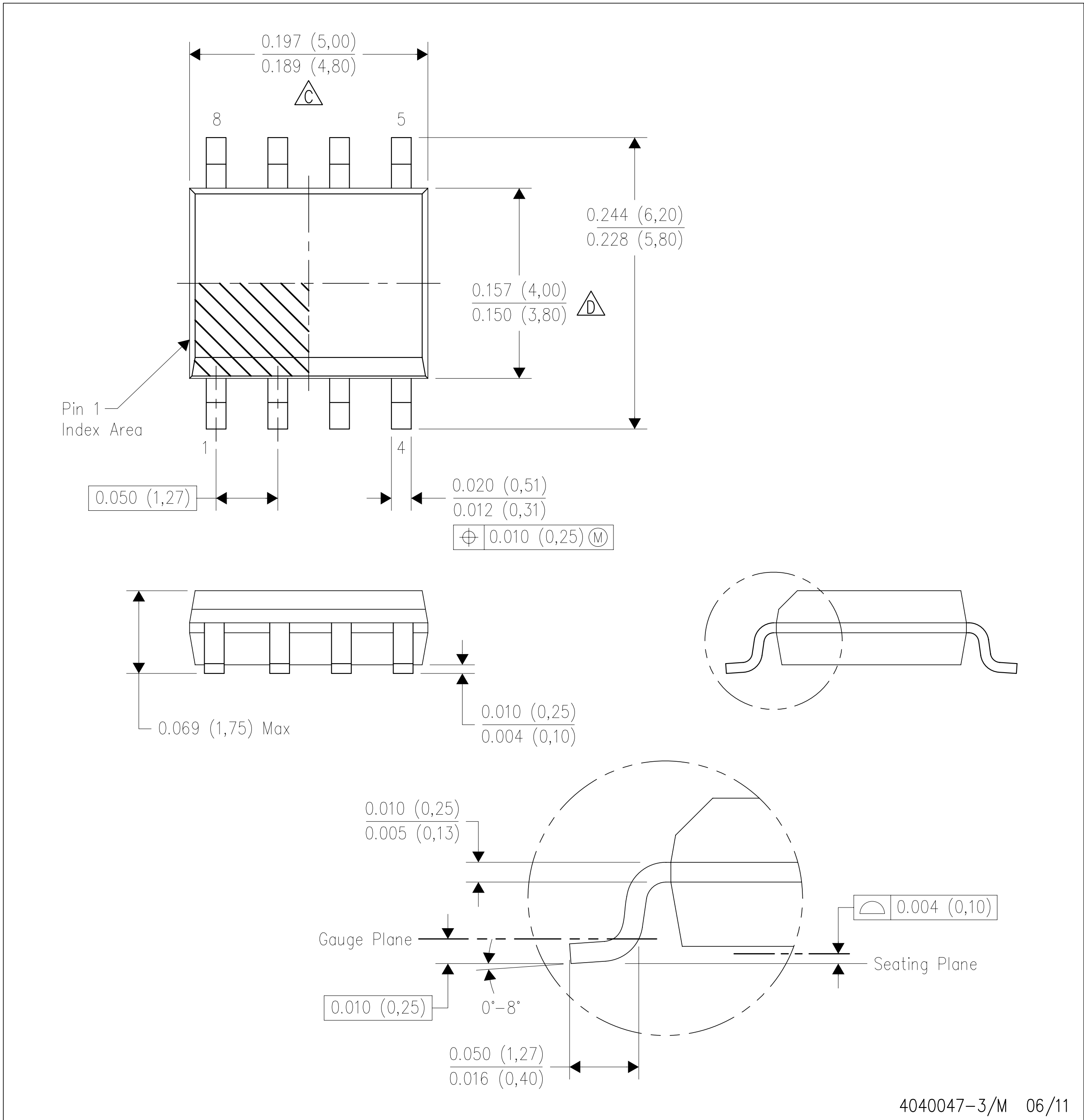
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

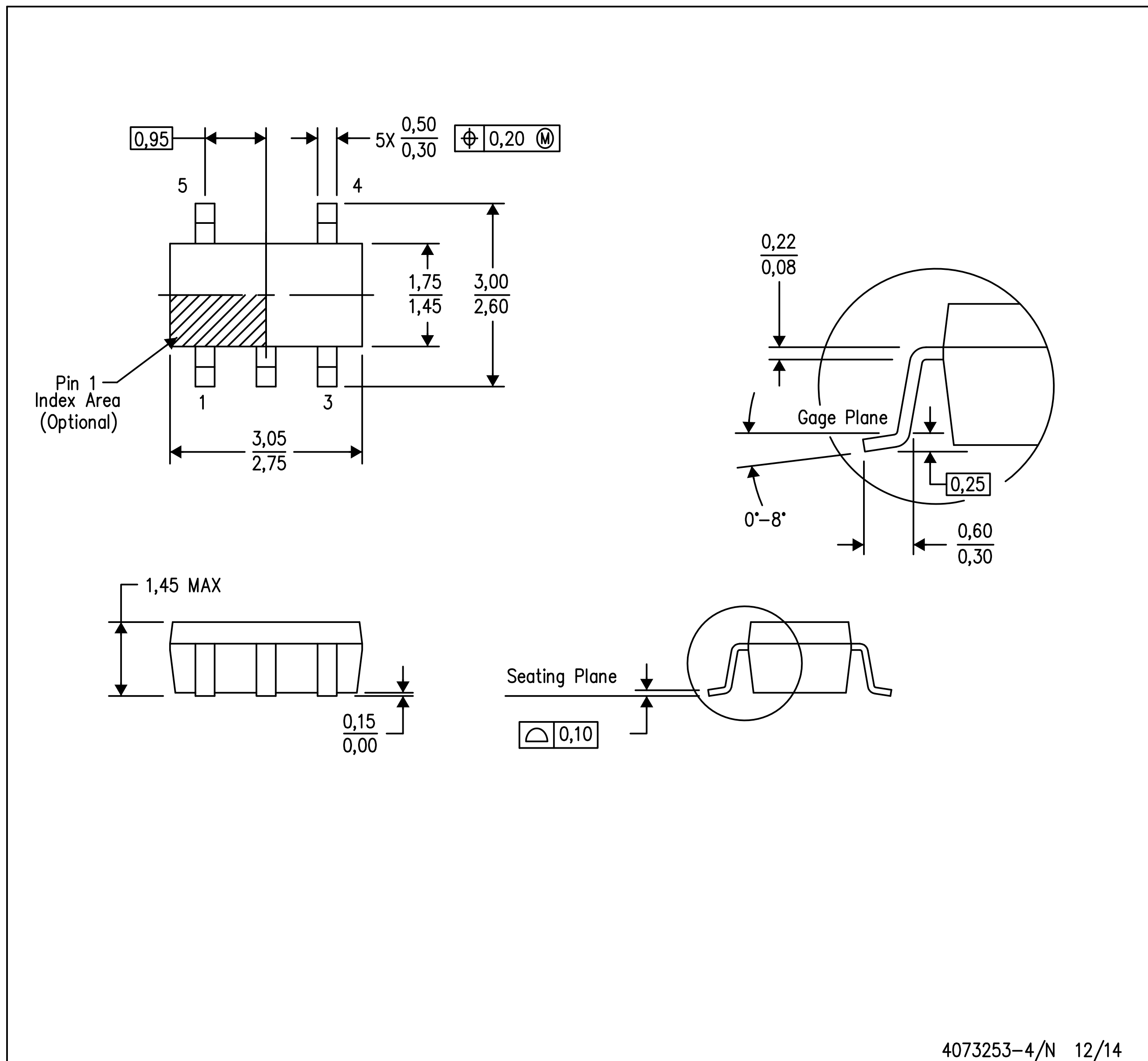
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| LMH6702MAX/NOPB | SOIC | D | 8 | 2500 | 367.0 | 367.0 | 35.0 |
| LMH6702MF/NOPB | SOT-23 | DBV | 5 | 1000 | 210.0 | 185.0 | 35.0 |
| LMH6702MFX/NOPB | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |

D (R-PDSO-G8) PLASTIC SMALL OUTLINE



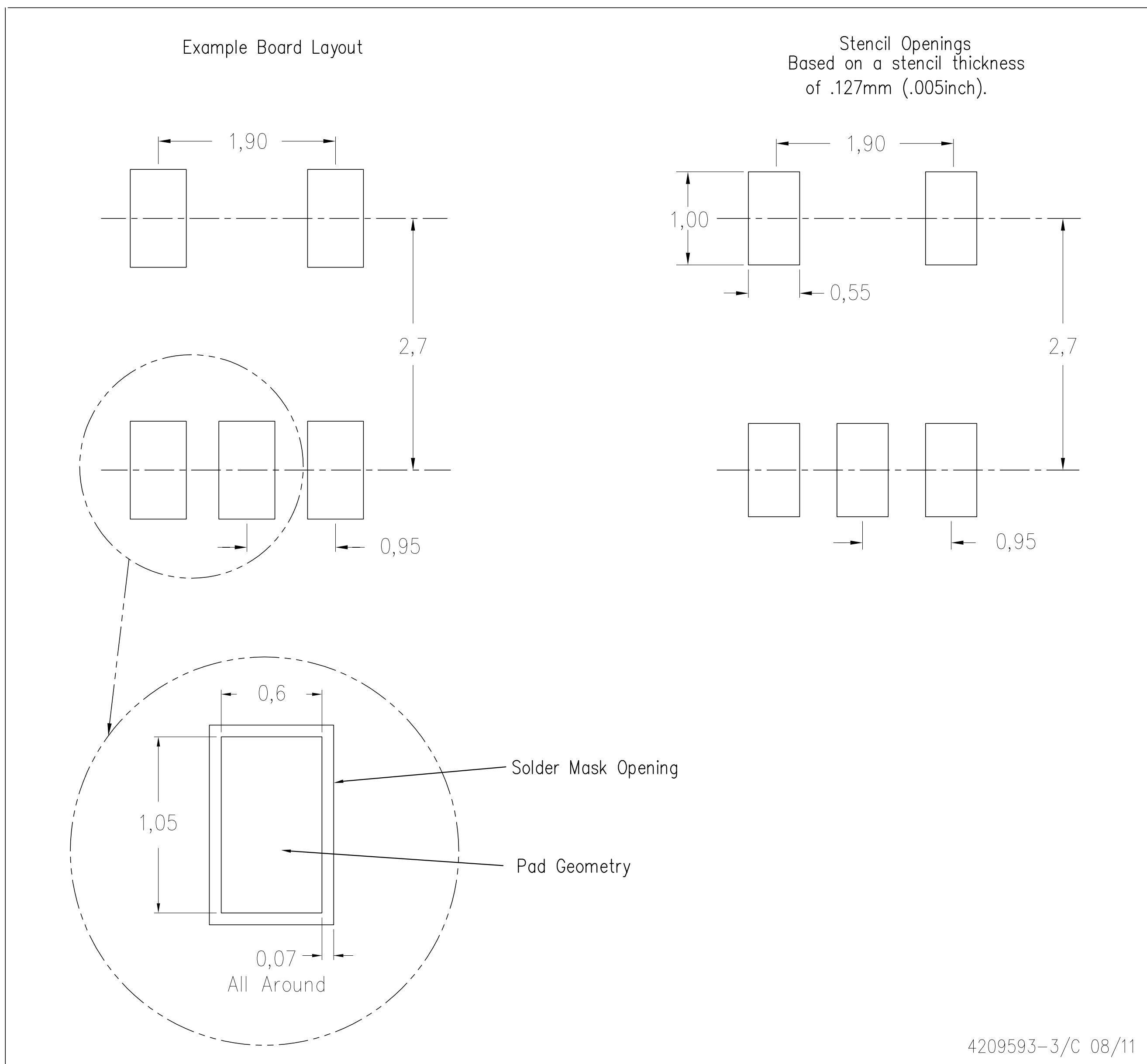

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AA.

DBV (R-PDSO-G5) PLASTIC SMALL-OUTLINE PACKAGE




NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Falls within JEDEC MO-178 Variation AA.

DBV (R-PDSO-G5) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC-7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

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