LMK04828 Evaluation Module

(ACTIVE) LMK04828BEVM

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Key Document

- LMK04826/28 User's Guide (Rev. A) (PDF 2669 KB)
  27 Jun 2013 659 views Read Abstract

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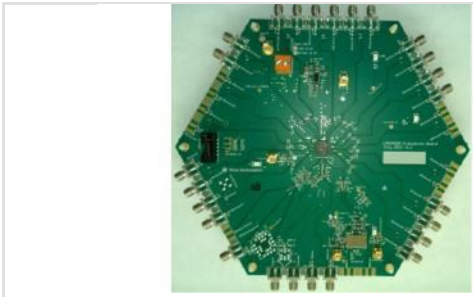

LMK04828BEVM Top View

Description

The LMK04828BEVM and LMK04826BEVM supports the LMK04820 family of products, the industry's highest performance clock conditioners with JEDEC JESD204B support. The dual loop PLLatinum™ architecture enables sub-100 fs jitter (12 kHz to 20 MHz) using a low noise VCXO module. The dual loop architecture consists of two high-performance phase-locked loops (PLL), a low-noise crystal oscillator circuit, and a high-performance voltage controlled oscillator (VCO).

The first PLL (PLL1) provides a low-noise jitter cleaner function while the second PLL (PLL2) performs the clock and SYSREF generation. PLL1 can be configured to either work with an external VCXO module or the integrated crystal oscillator with an external tunable crystal and varactor diode. When used with a very narrow loop bandwidth, PLL1 uses the superior close-in phase noise (offsets below 50 kHz) of the VCXO module or the tunable crystal to clean the input clock. The output of PLL1 is used as the clean input reference to PLL2 where it locks the integrated VCO.

The loop bandwidth of PLL2 can be optimized to clean the far-out phase noise (offsets above 50 kHz) where the integrated VCO outperforms the VCXO module or tunable crystal used in PLL1.

Features

- JEDEC JESD204B Support
- Ultra-low RMS Jitter Performance
- Dual loop Architecture
- 3 redundant input clocks with LOS
- Precision digital delay, fixed or dynamically adjustable

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LMK04828BEVM: LMK04828/26 Evaluation Module	$499.00(USD) In Stock Typically Ships in 1 to 3 Business Days Buy from TI	Pricing may vary. Buy from distributor	ACTIVE	Yes	Yes	Yes	NA	NA	NA	NA	No	No	No

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Technical Documents

Datasheet (1)

Title	Abstract	Type	Size (KB)	Date	Views
LMK0482x Ultra Low-Noise JESD204B Compliant Clock Jitter Cleaner with Dual Loop PLLs (Rev. AQ)		PDF	2954	17 Aug 2014	

User Guides (1)

Title	Abstract	Type	Size (KB)	Date	Views	TI Recommends
LMK04826/28 User's Guide (Rev. A)	Read Abstract	PDF	2669	27 Jun 2013	659	✓

Related Products

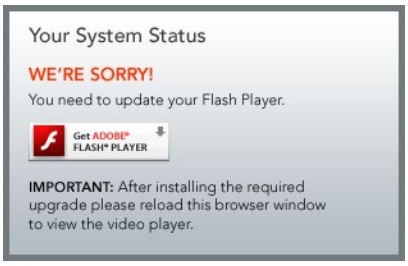
Design Kits & Evaluation Modules (1)

Name	Part Number	Tool Type
TSW38J84 Evaluation Module	TSW38J84EVM	Evaluation Modules & Boards

TI Devices (1)

Part Number	Name	Product Family
LMK04828	Ultra Low Jitter Synthesizer and Jitter Cleaner	Clock Jitter Cleaners

Videos



LMK04826/8: JESD204B-compliant clock jitter cleaners

Timothy demonstrates how to use the LMK0482x devices in JESD204B applications, illustrates the benefits of designing with the JESD204B interface, and focuses on device highlights

Posted: 23-May-2014
Duration: 10:38
Views: 137
Tags: JESD204B, lmk04828, clock and timing, clock, clock jitter cleaner, jitter cleaner, lmk04826, clocks, English, clocks & timers
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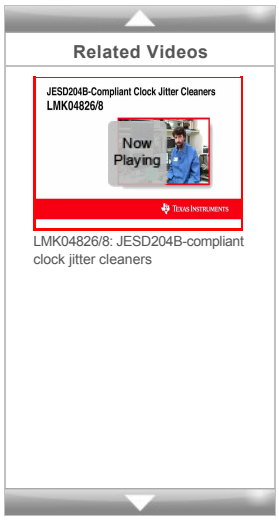

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