LMP7721 3-Femtoampere Input Bias Current Precision Amplifier

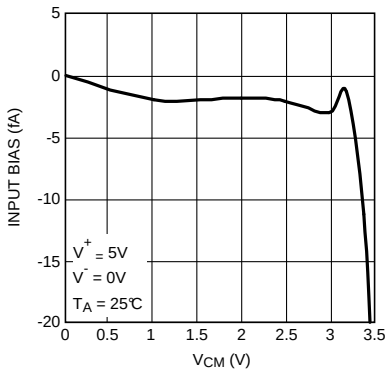
1 Features

- Unless Otherwise Noted, Typical Values at T_A = 25°C, V_S = 5 V.
- Input Bias Current (V_{CM} = 1 V)
  - Maximum at 25°C ±20 fA
  - Maximum at 85°C ±900 fA
- Offset Voltage ±26 µV
- Offset Voltage Drift −1.5 µV/°C
- DC Open-Loop Gain 120 dB
- DC CMRR 100 dB
- Input Voltage Noise (at f = 1 kHz) 6.5 nV/√Hz
- THD 0.0007%
- Supply Current 1.3 mA
- GBW 17 MHz
- Slew Rate (Falling Edge) 12.76 V/µs
- Supply Voltage 1.8 V to 5.5 V
- Operating Temperature Range −40°C to 125°C
- 8-Pin SOIC

2 Applications

- Photodiode Amplifier
- High Impedance Sensor Amplifier
- Ion Chamber Amplifier
- Electrometer Amplifier
- pH Electrode Amplifier
- Transimpedance Amplifier

Ultra-Low Input Bias Current



3 Description

The LMP7721 is the industry's lowest specified input bias current precision amplifier. The ultra-low input bias current is 3 fA, with a specified limit of ±20 fA at 25°C and ±900 fA at 85°C. This is achieved with the latest patent-pending technology of input bias current cancellation amplifier circuitry. This technology also maintains the ultra-low input bias current over the entire input common-mode voltage range of the amplifier.

Other outstanding features, such as low voltage noise (6.5 nV/√Hz), low DC-offset voltage (±150 µV maximum at 25°C) and low-offset voltage temperature coefficient (−1.5 µV/°C), improve system sensitivity and accuracy in high-precision applications. With a supply voltage range of 1.8 V to 5.5 V, the LMP7721 is the ideal choice for battery-operated, portable applications. The LMP7721 is part of the LMP™ precision amplifier family.

As part of Texas Instruments' PowerWise™ products, the LMP7721 provides the remarkably wide-gain bandwidth product (GBW) of 17 MHz while consuming only 1.3 mA of current. This wide GBW along with the high open-loop gain of 120 dB enables accurate signal conditioning. With these specifications, the LMP7721 has the performance to excel in a wide variety of applications such as electrochemical cell amplifiers and sensor interface circuits.

The LMP7721 is offered in an 8-pin SOIC package with a special pinout that isolates the amplifier's input from the power supply and output pins. With proper board layout techniques, the unique pinout of the LMP7721 will prevent PCB leakage current from reaching the input pins. Thus system error will be further reduced.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LMP7721	SOIC (8)	4.90 mm × 3.90 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (March 2013) to Revision E **Page**

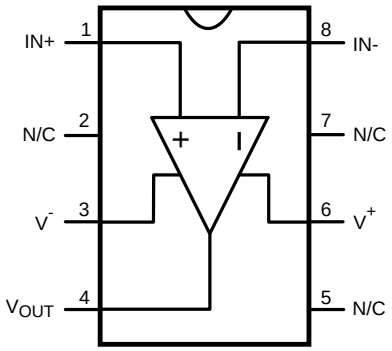
- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

Changes from Revision C (March 2013) to Revision D **Page**

- Changed layout of National Data Sheet to TI format ... 25

5 Pin Configuration and Functions

8-Pin
SOIC Package
Top View



Note: Non-standard single pinout. Substitutions may require a new layout.

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
IN+	1	I	Non-Inverting Input
N/C	2	-	No Internal Connection (1)
V-	3	P	Negative Power Supply
VOUT	4	O	Output
N/C	5	-	No Internal Connection
V+	6	P	Positive Power Supply
N/C	7	-	No Internal Connection (1)
IN-	8	I	Inverting Input

(1) Recommeded to connect to system guard trace.

6 Specifications

6.1 Absolute Maximum Ratings[1][2]

	MIN	MAX	UNIT
V_{IN} Differential	–0.3	0.3	V
Supply Voltage ($V_S = V^+ – V^–$) [3]	–0.3	6.0	V
Voltage on Input/Output Pins	V^+ + 0.3	$V^–$ − 0.3	V
Junction Temperature [4]		150	°C
Soldering Information			
Infrared or Convection (20 sec)		235	°C
Wave Soldering Lead Temp. (10 sec)		260	°C
Storage temperature, T_{stg}	−65	150	°C

(1) *Absolute Maximum Ratings*[1][2] indicate limits beyond which damage to the device may occur. *Recommended Operating Conditions* indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics Tables.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) The voltage on any pin should not exceed 6V relative to any other pins.
(4) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly onto a PC Board.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

	MIN	MAX	UNIT
Temperature Range[1]	–40	125	°C
Supply Voltage ($V_S = V^+ – V^–$):			
0°C ≤ T_A ≤ 125°C	1.8	5.5	V
−40°C ≤ T_A ≤ 125°C	2.0	5.5	V

(1) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly onto a PC Board.

6.4 Thermal Information

THERMAL METRIC[1]		LMP7721 D 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	190	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics: 2.5 V

Unless otherwise specified, all limits are specified for T_A = 25°C, V^+ = 2.5 V, V^- = 0 V, V_{CM} = (V^+ + V^-)/2.

PARAMETER		TEST CONDITIONS		MIN(1)	TYP(2)	MAX(1)	UNIT
V_{OS}	Input Offset Voltage			–180	±50	180	µV
		–40°C ≤ T_J ≤ 125°C		–480		480	
TC V_{OS}	Input Offset Voltage Drift (3)				–1.5	–4	µV/°C
I_{BIAS}	Input Bias Current	V_{CM} = 1 V (4) (5)	25°C	–20	±3	20	fA
			−40°C to 85°C	–900		900	
			−40°C to 125°C	–5		5	pA
I_{OS}	Input Offset Current	V_{CM} = 1 V (5)			±6	±40	fA
CMRR	Common-Mode Rejection Ratio	0 V ≤ V_{CM} ≤ 1.4 V		83	100		dB
		0 V ≤ V_{CM} ≤ 1.4 V, –40°C ≤ T_J ≤ 125°C		80			
PSRR	Power Supply Rejection Ratio	1.8 V ≤ V^+ ≤ 5.5 V, V^- = 0 V, V_{CM} = 0		84	92		dB
		1.8 V ≤ V^+ ≤ 5.5 V, V^- = 0 V, V_{CM} = 0, –40°C ≤ T_J ≤ 125°C		80			
CMVR	Input Common-Mode Voltage Range	CMRR ≥ 80 dB		−0.3		1.5	V
		CMRR ≥ 78 dB, –40°C ≤ T_J ≤ 125°C		–0.3		1.5	
A_{VOL}	Large Signal Voltage Gain	V_O = 0.15 V to 2.2 V, R_L = 2 kΩ to V^+/2		88	107		dB
		V_O = 0.15 V to 2.2 V, R_L = 2 kΩ to V^+/2, –40°C ≤ T_J ≤ 125°C		82			
		V_O = 0.15 V to 2.2 V, R_L = 10 kΩ to V^+/2		92	120		
		V_O = 0.15 V to 2.2 V, R_L = 10 kΩ to V^+/2, –40°C ≤ T_J ≤ 125°C		88			
V_O	Output Swing High	R_L = 2 kΩ to V^+/2		70	25		mV from V^+
		R_L = 2 kΩ to V^+/2, –40°C ≤ T_J ≤ 125°C		77			
		R_L = 10 kΩ to V^+/2		60	20		
		R_L = 10 kΩ to V^+/2, –40°C ≤ T_J ≤ 125°C		66			
	Output Swing Low	R_L = 2 kΩ to V^+/2			30	70	mV
		R_L = 2 kΩ to V^+/2, –40°C ≤ T_J ≤ 125°C				73	
		R_L = 10 kΩ to V^+/2			15	60	
		R_L = 10 kΩ to V^+/2, –40°C ≤ T_J ≤ 125°C				62	
I_O	Output Short Circuit Current	Sourcing to V^-, V_{IN} = 200 mV (6)		36	46		mA
		Sourcing to V^-, V_{IN} = 200 mV (6), –40°C ≤ T_J ≤ 125°C		30			
		Sinking to V^+, V_{IN} = −200 mV (6)		7.5	15		
		Sinking to V^+, V_{IN} = −200 mV (6), –40°C ≤ T_J ≤ 125°C		5.0			
I_S	Supply Current				1.1	1.5	mA
		–40°C ≤ T_J ≤ 125°C				1.75	
SR	Slew Rate	A_V = +1, Rising (10% to 90%)			9.3		V/µs
		A_V = +1, Falling (90% to 10%)			10.8		
GBW	Gain Bandwidth Product				15		MHz
e_n	Input-Referred Voltage Noise	f = 400 Hz			8		nV/√Hz
		f = 1 kHz			7		

(1) Limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlations using the Statistical Quality Control (SQC) method.
(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not specified on shipped production material.
(3) Offset voltage average drift is determined by dividing the change in V_{OS} at the temperature extremes by the total temperature change.
(4) Positive current corresponds to current flowing into the device.
(5) This parameter is specified by design and/or characterization and is not tested in production.
(6) The short circuit test is a momentary open loop test.

Electrical Characteristics: 2.5 V (continued)

Unless otherwise specified, all limits are specified for T_A = 25°C, V^+ = 2.5 V, V^- = 0 V, V_{CM} = (V^+ + V^-)/2.

PARAMETER		TEST CONDITIONS	MIN(1)	TYP(2)	MAX(1)	UNIT
I_n	Input-Referred Current Noise	f = 1 kHz		0.01		pA/√Hz
THD+N	Total Harmonic Distortion + Noise	f = 1 kHz, A_V = 2, R_L = 100 kΩ V_O = 0.9 V_{PP}		0.003%		
		f = 1 kHz, A_V = 2, R_L = 600 Ω V_O = 0.9 V_{PP}		0.003%		

6.6 Electrical Characteristics: 5 V

Unless otherwise specified, all limits are specified for T_A = 25°C, V^+ = 5 V, V^- = 0 V, V_{CM} = (V^+ + V^-)/2.

PARAMETER		TEST CONDITIONS		MIN(1)	TYP(2)	MAX(1)	UNIT
V_{OS}	Input Offset Voltage			–150	±26	150	µV
		–40°C ≤ T_J ≤ 125°C		450		450	
TC V_{OS}	Input Offset Average Drift (3)				–1.5	–4	µV/°C
I_{BIAS}	Input Bias Current	V_{CM} = 1 V (4) (5)	25°C	–20	±3	20	fA
			−40°C to 85°C	–900		900	
			−40°C to 125°C	–5		5	pA
I_{OS}	Input Offset Current	(5)			±6	±40	fA
CMRR	Common-Mode Rejection Ratio	0 V ≤ V_{CM} ≤ 3.7 V		84	100		dB
		0 V ≤ V_{CM} ≤ 3.7 V, –40°C ≤ T_J ≤ 125°C		82			
PSRR	Power Supply Rejection Ratio	1.8 V ≤ V^+ ≤ 5.5 V, V^- = 0 V, V_{CM} = 0		84	96		dB
		1.8 V ≤ V^+ ≤ 5.5 V, V^- = 0 V, V_{CM} = 0, –40°C ≤ T_J ≤ 125°C		80			
CMVR	Input Common-Mode Voltage Range	CMRR ≥ 80 dB		−0.3		4	V
		CMRR ≥ 78 dB, –40°C ≤ T_J ≤ 125°C		–0.3		4	
A_{VOL}	Large Signal Voltage Gain	V_O = 0.3 V to 4.7 V, R_L = 2 kΩ to V^+/2		88	111		dB
		V_O = 0.3 V to 4.7 V, R_L = 2 kΩ to V^+/2, –40°C ≤ T_J ≤ 125°C		82			
		V_O = 0.3 V to 4.7 V, R_L = 10 kΩ to V^+/2		92	120		
		V_O = 0.3 V to 4.7 V, R_L = 10 kΩ to V^+/2, –40°C ≤ T_J ≤ 125°C		88			
V_O	Output Swing High	R_L = 2 kΩ to V^+/2		70	30		mV from V^+
		R_L = 2 kΩ to V^+/2, –40°C ≤ T_J ≤ 125°C		77			
		R_L = 10 kΩ to V^+/2		60	20		
		R_L = 10 kΩ to V^+/2, –40°C ≤ T_J ≤ 125°C		66			
	Output Swing Low	R_L = 2 kΩ to V^+/2			31	70	mV
		R_L = 2 kΩ to V^+/2, –40°C ≤ T_J ≤ 125°C				73	
		R_L = 10 kΩ to V^+/2			20	60	
		R_L = 10 kΩ to V^+/2, –40°C ≤ T_J ≤ 125°C				62	

(1) Limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlations using the Statistical Quality Control (SQC) method.
(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not specified on shipped production material.
(3) Offset voltage average drift is determined by dividing the change in V_{OS} at the temperature extremes by the total temperature change.
(4) Positive current corresponds to current flowing into the device.
(5) This parameter is specified by design and/or characterization and is not tested in production.

Electrical Characteristics: 5 V (continued)

Unless otherwise specified, all limits are specified for T_A = 25°C, V^+ = 5 V, V^- = 0 V, V_{CM} = (V^+ + V^-)/2.

	PARAMETER	TEST CONDITIONS	MIN(1)	TYP(2)	MAX(1)	UNIT
I_O	Output Short Circuit Current	Sourcing to V^-, V_{IN} = 200 mV (6)	46	60		mA
		Sourcing to V^-, V_{IN} = 200 mV (6), –40°C ≤ T_J ≤ 125°C	38			
		Sinking to V^+, V_{IN} = −200 mV (6)	10.5	22		
		Sinking to V^+, V_{IN} = −200 mV (6), –40°C ≤ T_J ≤ 125°C	6.5			
I_S	Supply Current			1.3	1.7	mA
		–40°C ≤ T_J ≤ 125°C			1.95	
SR	Slew Rate	A_V = +1, Rising (10% to 90%)		10.43		V/µs
		A_V = +1, Falling (90% to 10%)		12.76		
GBW	Gain Bandwidth Product			17		MHz
e_n	Input-Referred Voltage Noise	f = 400 Hz		7.5		nV/√Hz
		f = 1 kHz		6.5		
I_n	Input-Referred Current Noise	f = 1 kHz		0.01		pA/√Hz
THD+N	Total Harmonic Distortion + Noise	f = 1 kHz, A_V = 2, R_L = 100 kΩ V_O = 4 V_{PP}		0.0007%		
		f = 1 kHz, A_V = 2, R_L = 600Ω V_O = 4 V_{PP}		0.0007%		

(6) The short circuit test is a momentary open loop test.

6.7 Typical Characteristics

Unless otherwise specified: T_A = 25°C, V_{CM} = (V^+ + V^-)/2.

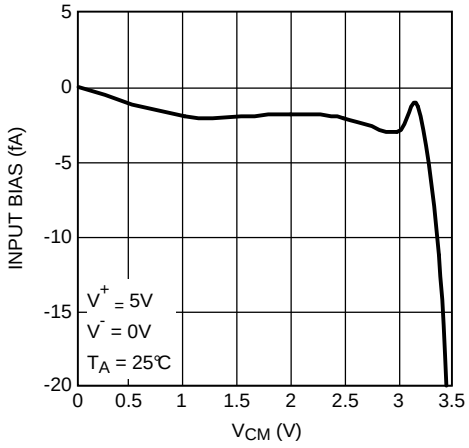


Figure 1. Input Bias Current vs. V_{CM}

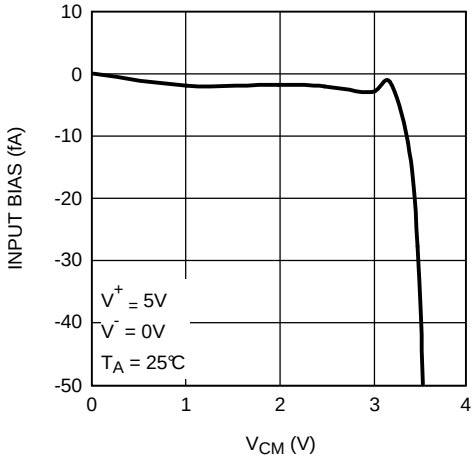


Figure 2. Input Bias Current vs. V_{CM}

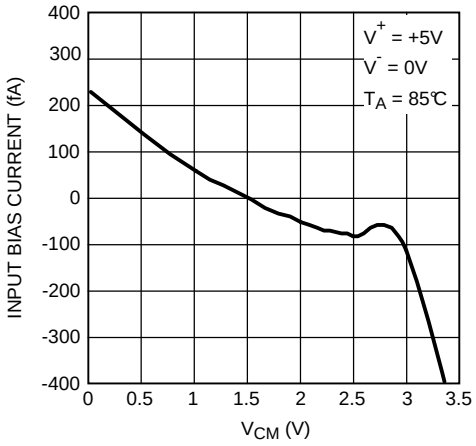


Figure 3. Input Bias Current vs. V_{CM}

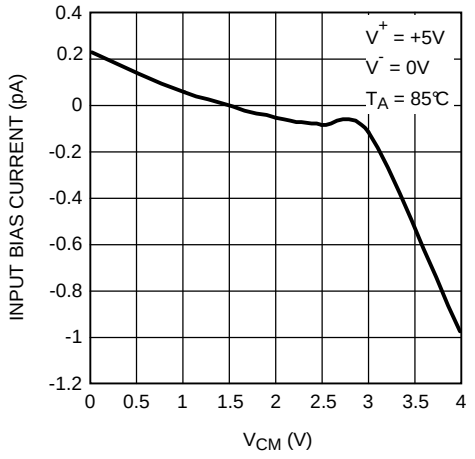


Figure 4. Input Bias Current vs. V_{CM}

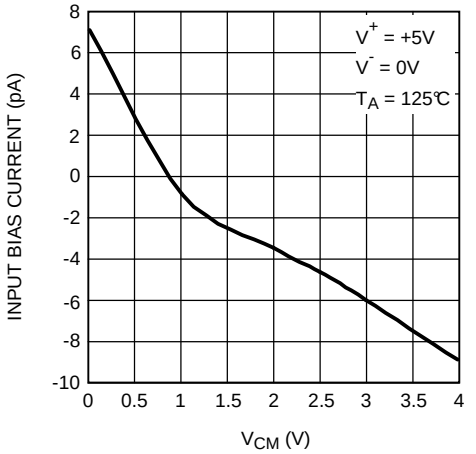


Figure 5. Input Bias Current vs. V_{CM}

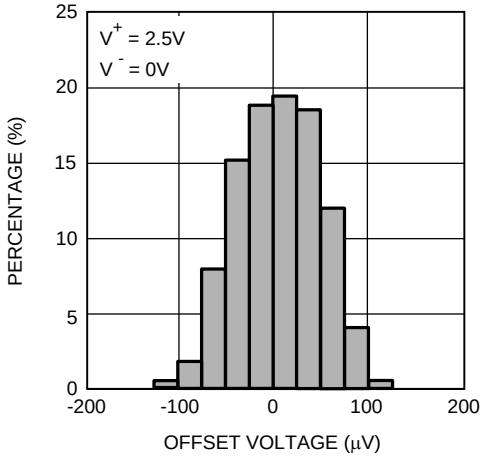


Figure 6. Offset Voltage Distribution

Typical Characteristics (continued)

Unless otherwise specified: T_A = 25°C, V_{CM} = (V^+ + V^-)/2.

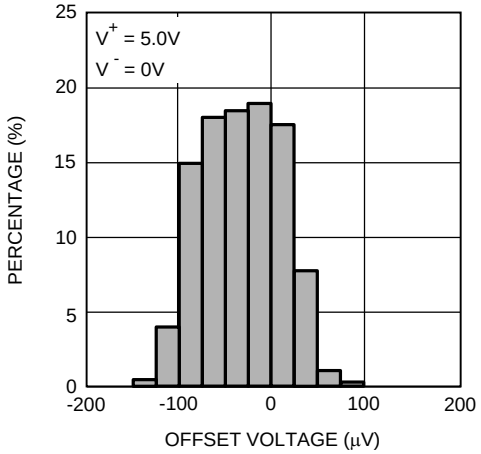


Figure 7. Offset Voltage Distribution

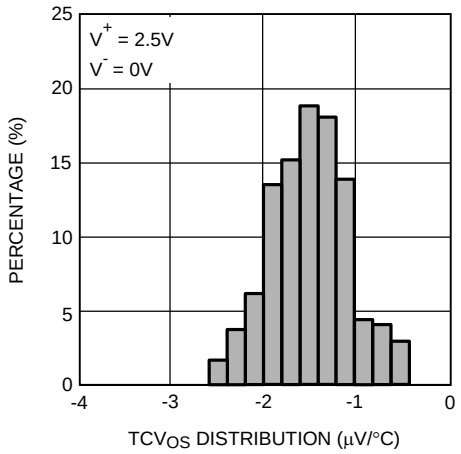


Figure 8. TCV_{OS} Distribution

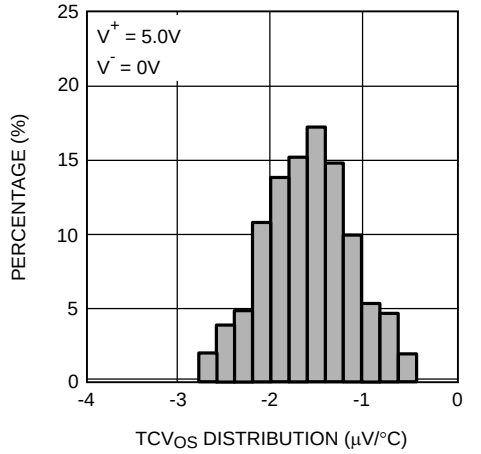


Figure 9. TCV_{OS} Distribution

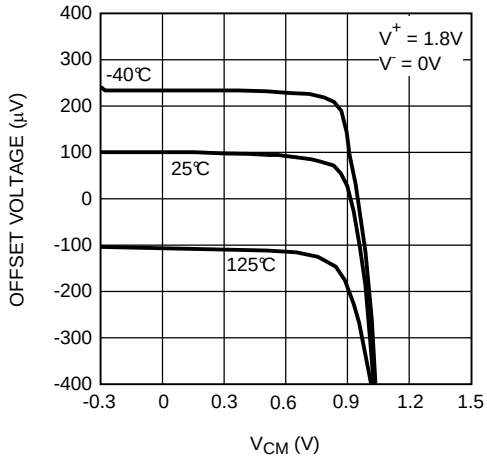


Figure 10. Offset Voltage vs. V_{CM}

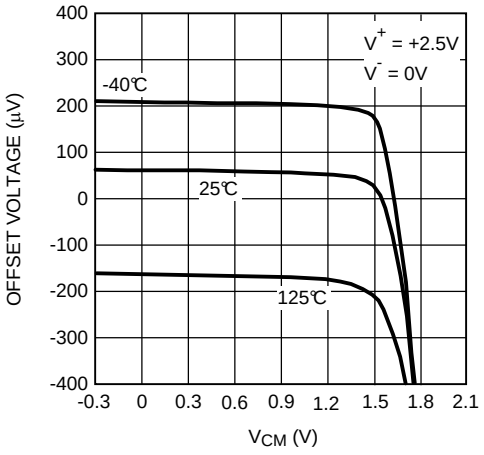


Figure 11. Offset Voltage vs. V_{CM}

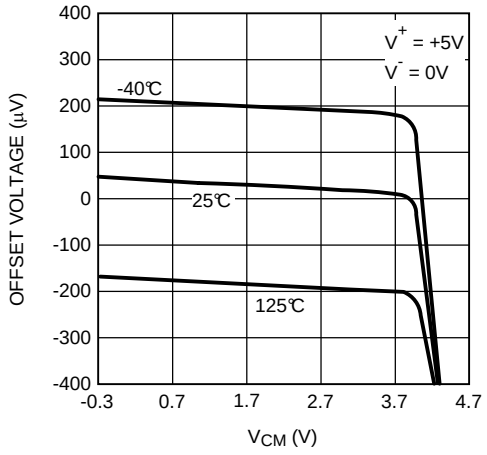


Figure 12. Offset Voltage vs. V_{CM}

Typical Characteristics (continued)

Unless otherwise specified: T_A = 25°C, V_{CM} = (V^+ + V^-)/2.

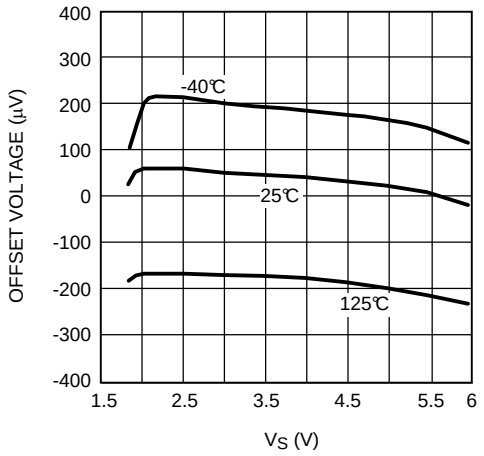


Figure 13. Offset Voltage vs. Supply Voltage

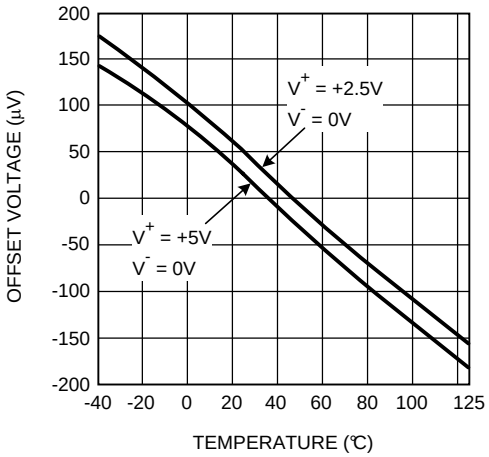


Figure 14. Offset Voltage vs. Temperature

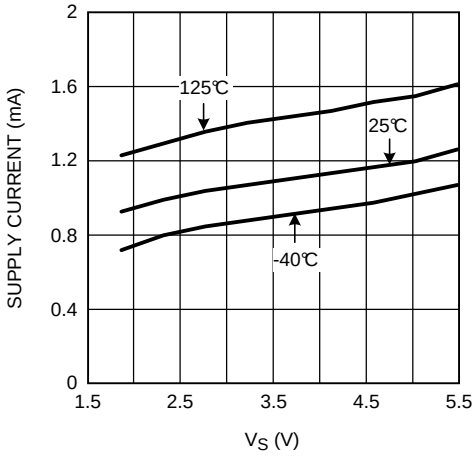


Figure 15. Supply Current vs. Supply Voltage

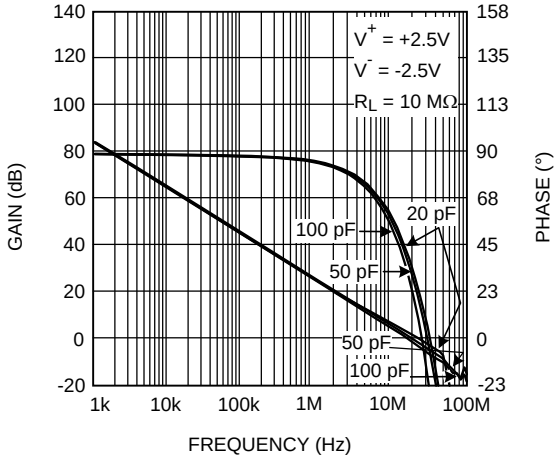


Figure 16. Open-Loop Frequency Response Gain and Phase

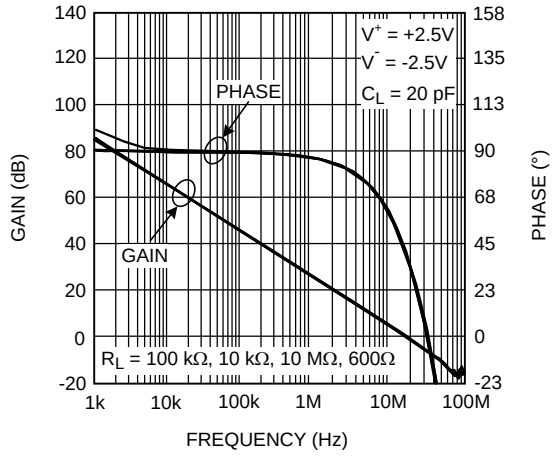


Figure 17. Open-Loop Frequency Response Gain and Phase

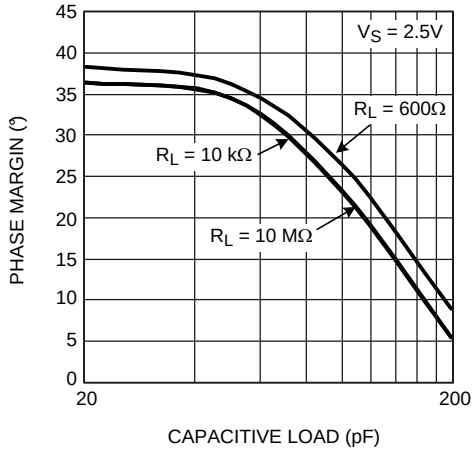


Figure 18. Phase Margin vs. Capacitive Load

Typical Characteristics (continued)

Unless otherwise specified: T_A = 25°C, V_{CM} = (V^+ + V^-)/2.

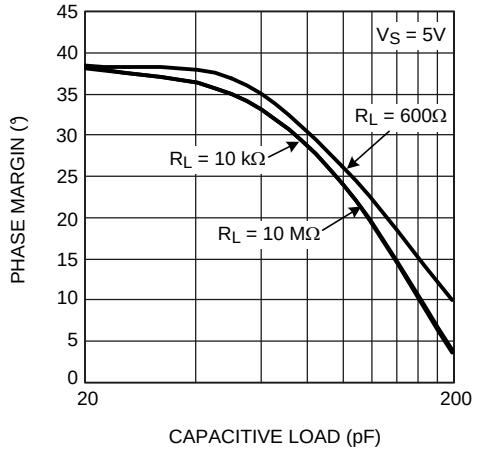


Figure 19. Phase Margin vs. Capacitive Load

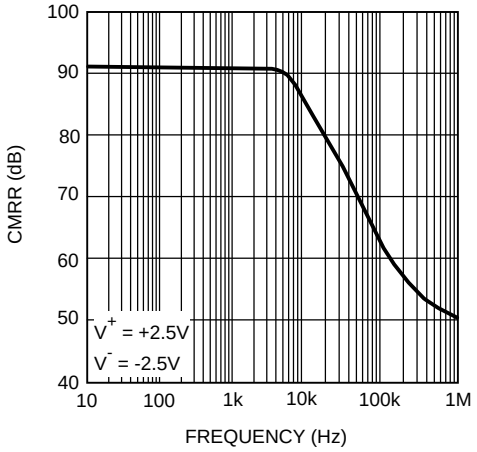


Figure 20. CMRR vs. Frequency

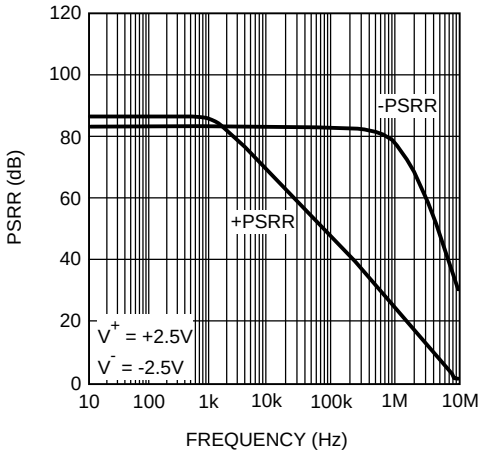


Figure 21. PSRR vs. Frequency

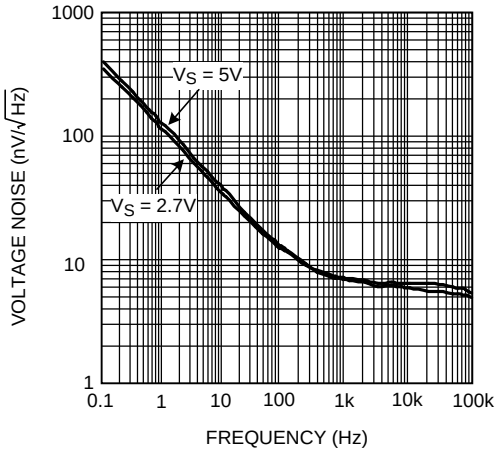


Figure 22. Input-Referred Voltage Noise vs. Frequency

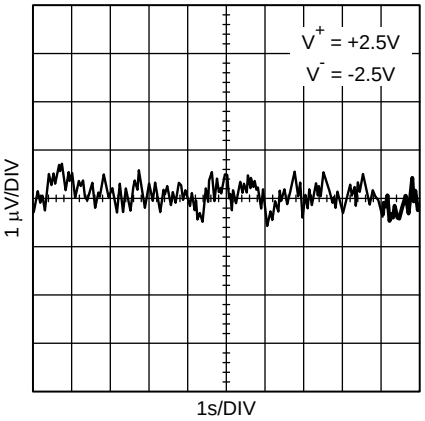


Figure 23. Time Domain Voltage Noise

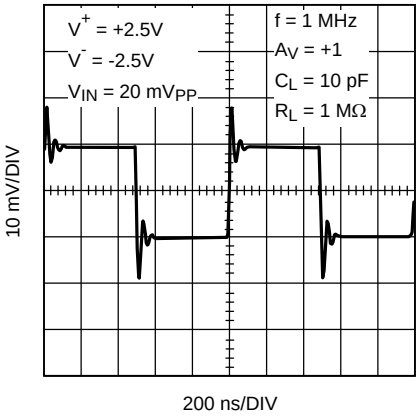


Figure 24. Small Signal Step Response

Typical Characteristics (continued)

Unless otherwise specified: T_A = 25°C, V_{CM} = (V^+ + V^-)/2.

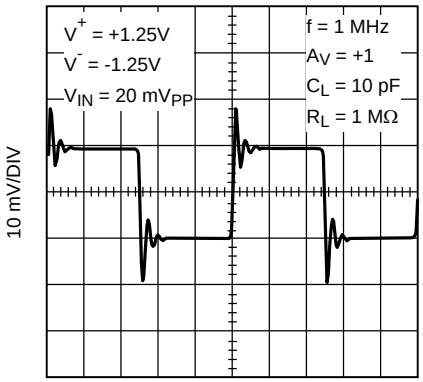


Figure 25. Small Signal Step Response

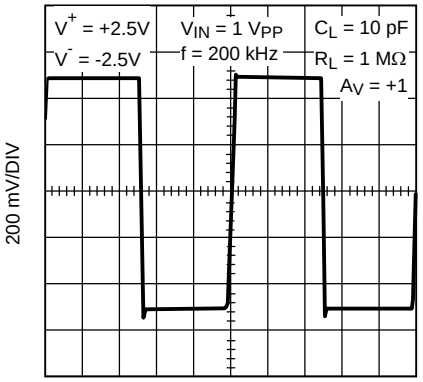


Figure 26. Large Signal Step Response

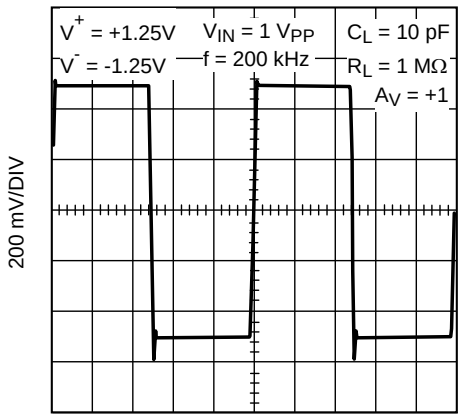


Figure 27. Large Signal Step Response

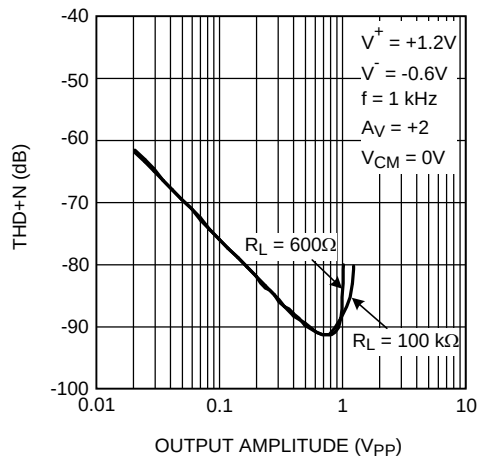


Figure 28. THD+N vs. Output Voltage

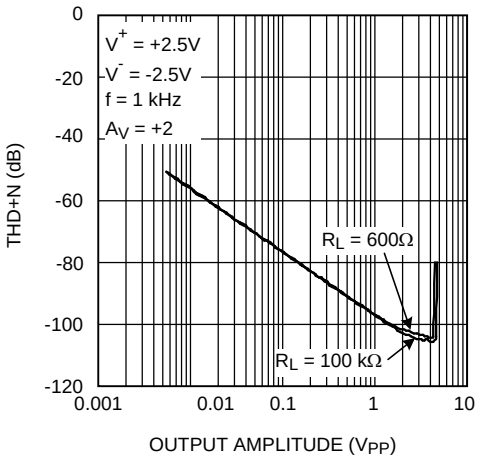


Figure 29. THD+N vs. Output Voltage

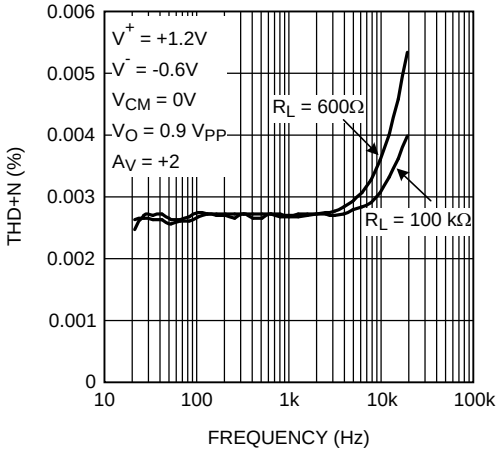


Figure 30. THD+N vs. Frequency

Typical Characteristics (continued)

Unless otherwise specified: T_A = 25°C, V_{CM} = (V^+ + V^-)/2.

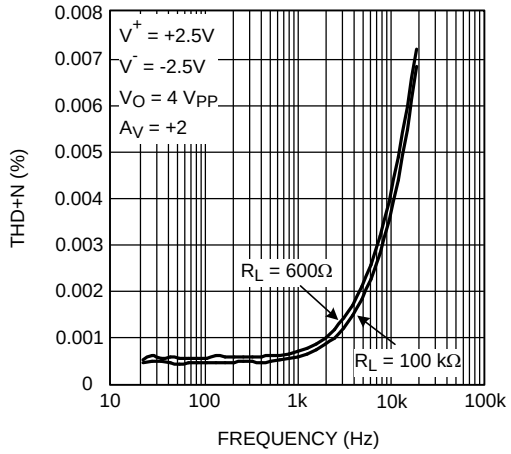


Figure 31. THD+N vs. Frequency

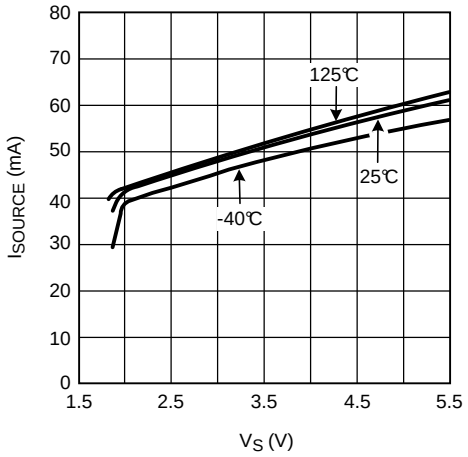


Figure 32. Sourcing Current vs. Supply Voltage

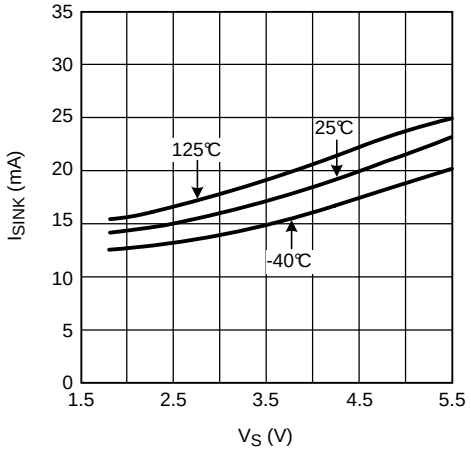


Figure 33. Sinking Current vs. Supply Voltage

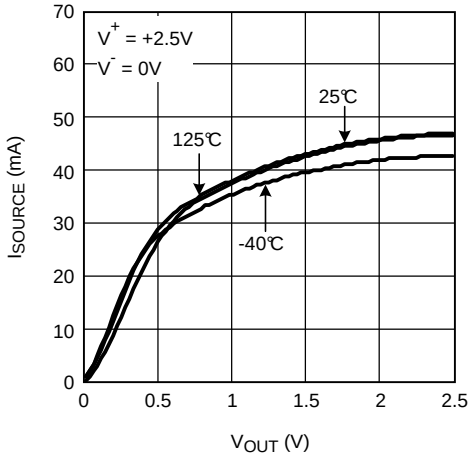


Figure 34. Sourcing Current vs. Output Voltage

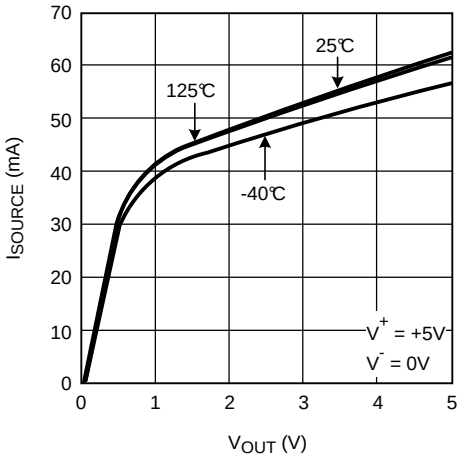


Figure 35. Sourcing Current vs. Output Voltage

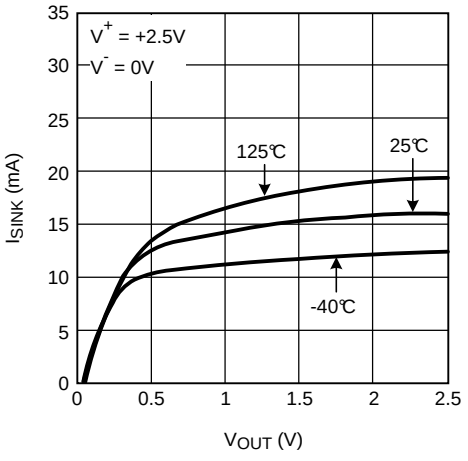


Figure 36. Sinking Current vs. Output Voltage

Typical Characteristics (continued)

Unless otherwise specified: T_A = 25°C, V_{CM} = (V^+ + V^-)/2.

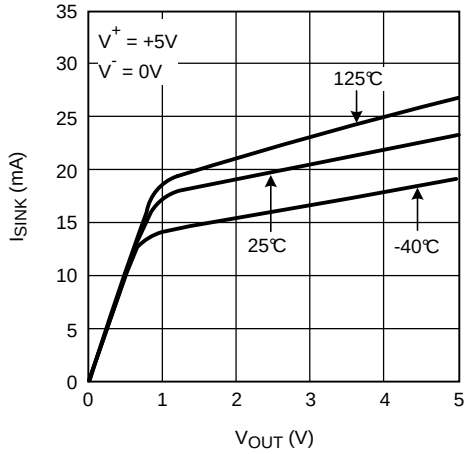


Figure 37. Sinking Current vs. Output Voltage

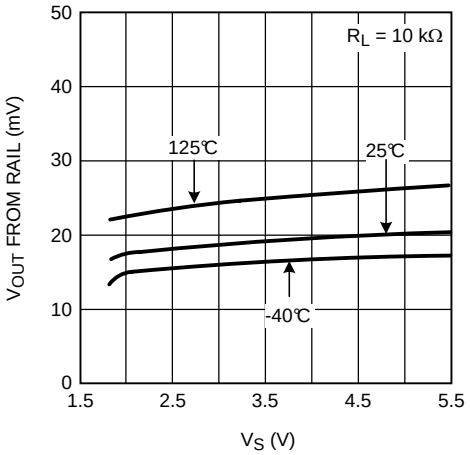


Figure 38. Output Swing High vs. Supply Voltage

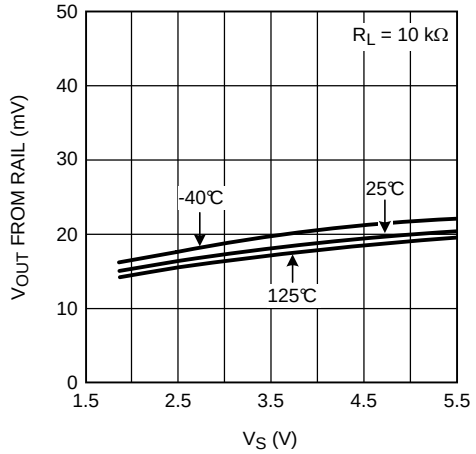


Figure 39. Output Swing Low vs. Supply Voltage

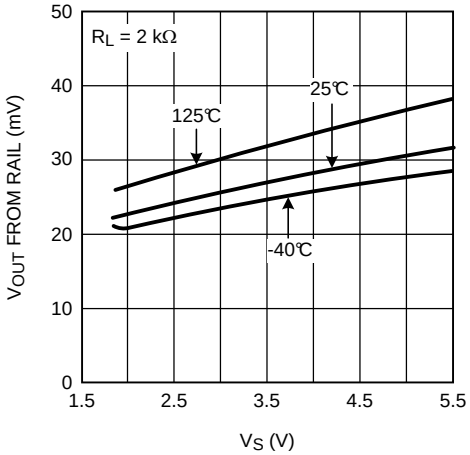


Figure 40. Output Swing High vs. Supply Voltage

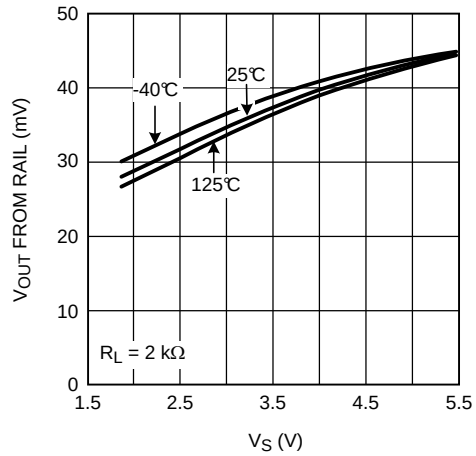


Figure 41. Output Swing Low vs. Supply Voltage

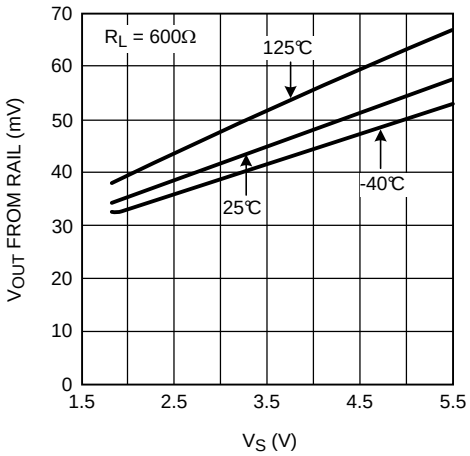


Figure 42. Output Swing High vs. Supply Voltage

Typical Characteristics (continued)

Unless otherwise specified: T_A = 25°C, V_{CM} = (V^+ + V^-)/2.

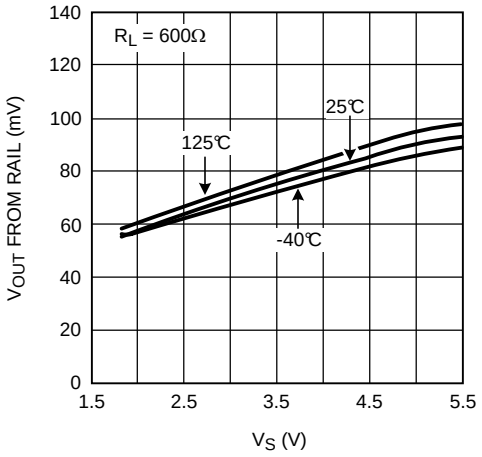


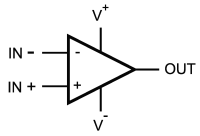
Figure 43. Output Swing Low vs. Supply Voltage

7 Detailed Description

7.1 Overview

The LMP7721 combines a patented input bias current cancelling circuitry along with an optimized pinout to provide and ultra-low maximum specified bias current of ±20 fA.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Ultra-Low Input Bias Current

The LMP7721 has the industry's lowest specified input bias current. The ultra-low input bias current is typically 3 fA, with a specified limit of ±20 fA at 25°C, ±900 fA at 85°C and ±5 pA at 125°C when V_{CM} = 1 V with a 5-V or a 2.5-V power supply.

7.3.2 Wide Bandwidth at Low-Supply Current

The LMP7721 is a high-performance amplifier that provides a 17-MHz unity gain bandwidth while drawing only 1.3 mA of current. This makes the LMP7721 ideal for wideband amplification in portable applications.

7.3.3 Low Input Referred Noise

The LMP7721 has a low input-referred voltage noise density (6.5 nV/$\sqrt{\text{Hz}}$ at 1 kHz with 5-V supply). Its MOS input stage ensures a very low input-referred current noise density (0.01 pA/$\sqrt{\text{Hz}}$).

The low input-referred noise and the ultra-low input bias current make the LMP7721 stand out in maintaining signal fidelity. This quality makes the LMP7721 a suitable candidate for sensor-based applications.

7.3.4 Low-Supply Voltage

The LMP7721 has performance specified at 2.5-V and 5-V power supplies. The LMP7721 is ensured to be functional at all supply voltages between 2 V to 5.5 V, for ambient temperatures ranging from −40°C to 125°C. This means that the LMP7721 has a long operational span over the battery's lifetime. The LMP7721 is also specified to be functional at 1.8-V supply voltage, for ambient temperatures ranging from 0°C to 125°C. This makes the LMP7721 ideal for use in low-voltage commercial applications.

7.3.5 Rail-to-Rail Output and Ground Sensing

Rail-to-rail output swing provides the maximum possible output dynamic range. This is particularly important when operating at low-supply voltages. An innovative positive feedback scheme is created to boost the LMP7721's output current drive capability. This allows the LMP7721 to source 30 mA to 40 mA of current at 1.8-V power supply.

The LMP7721's input common-mode range includes the negative supply rail which makes direct sensing at ground possible in single-supply operation.

Feature Description (continued)

7.3.6 Unique Pinout

The LMP7721 has been designed with the IN+ and IN−, V^+ and V^- pins on opposite sides of the package. There are isolation pins between IN+ and V^-, IN− and V+. This unique pinout makes it easy to guard the LMP7721's input. This pinout design reduces the input bias current's dependence on common mode or supply bias.

The SOIC package features low leakage and it has large pin spacing. This lowers the probability of dust particles settling down between two pins thus reducing the resistance between the pins which can be a problem.

The two No Connect (N/C) isolation pins are not internally connected and may be tied to the guard trace to provide down-into-the-package level guarding of the inputs.

7.3.7 Input Protection

The LMP7721 input stage is protected from seeing excessive differential input voltage by a pair of back-to-back diodes attached between the inputs. This limits the differential voltage and hence prevents phase inversion as well as any performance drift. These diodes can conduct current when the input signal has a really fast edge, and, if necessary, should be isolated (using a resistor or a current follower) in such cases. Under normal feedback operation, the average differential voltage is less than 1 mV and these diodes do not affect the normal operation of the device. This clamp also limits the use as a comparator, which is not a recommended function for operational amplifiers.

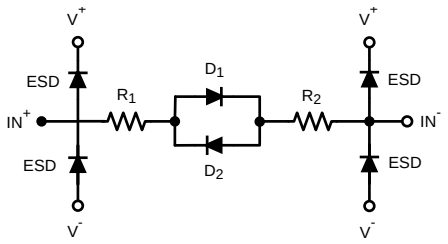


Figure 44. Input Protection Diodes

7.4 Device Functional Modes

7.4.1 Compensating Input Capacitance

The high-input resistance of the LMP7721 allows the use of large feedback and source resistor values without losing gain accuracy due to loading. However, the circuit will be especially sensitive to its layout when these large-value resistors are used.

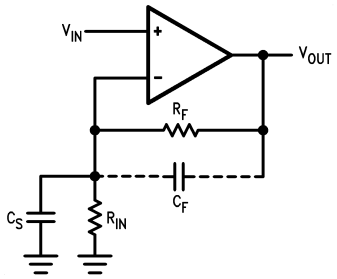


Figure 45. General Operational Amplifier Circuit

Every amplifier has some capacitance between each input and AC ground, and also some differential capacitance between the inputs. When the feedback network around an amplifier is resistive, this input capacitance (along with any additional capacitance due to circuit board traces, the socket, etc.) and the feedback resistors create a pole in the feedback path. This pole can cause gain "peaking" or outright oscillations.

Device Functional Modes (continued)

In the General Operational Amplifier circuit, Figure 45 the frequency of this pole is:

$$f_p = \frac{1}{2\pi C_S R_P} \tag{1}$$

where:

- C_S is the total capacitance at the inverting input, including amplifier input capacitance and any stray capacitance from the circuit board traces.
- R_P is the parallel combination of R_F and R_{IN}

The typical input capacitance of the LMP7721 is about 11pF. This formula, as well as all formulas derived below, apply to inverting and non-inverting op amp configurations.

When the feedback resistors are smaller than a few kΩ, the frequency of the feedback pole will be quite high, since C_S is generally less than 15 pF. If the frequency of the feedback pole is much higher than the "ideal" closed-loop bandwidth (the nominal closed-loop bandwidth in the absence of C_S), the pole will have a negligible effect on stability, as it will add only a small amount of phase shift.

However, if the feedback pole is less than approximately 6 to 10 times the "ideal" −3 dB frequency, a feedback capacitor, C_F, should be connected between the output and the inverting input of the op amp. This condition can also be stated in terms of the amplifier's low-frequency noise gain: To maintain stability a feedback capacitor will probably be needed if

$$\left(\frac{R_F}{R_{IN}} + 1\right) \leq \sqrt{6 \times 2\pi \times GBW \times R_F \times C_S} \tag{2}$$

where

$$\left(\frac{R_F}{R_{IN}} + 1\right) \tag{3}$$

is the amplifier's low-frequency noise gain and GBW is the amplifier's gain bandwidth product. An amplifier's low-frequency noise gain is represented by the formula

$$\left(\frac{R_F}{R_{IN}} + 1\right) \tag{4}$$

regardless of whether the amplifier is being used in inverting or noninverting mode. Note that a feedback capacitor is more likely to be needed when the noise gain is low and/or the feedback resistor is large.

If the above condition is met (indicating a feedback capacitor will probably be needed), and the noise gain is large enough that:

$$\left(\frac{R_F}{R_{IN}} + 1\right) \geq 2\sqrt{GBW \times R_F \times C_S} \tag{5}$$

the following value of feedback capacitor is recommended:

$$C_F = \frac{C_S}{2\left(\frac{R_F}{R_{IN}} + 1\right)} \tag{6}$$

If

Device Functional Modes (continued)

$$\left(\frac{R_F}{R_{IN}} + 1 \right) < 2\sqrt{GBW \times R_F \times C_S} \tag{7}$$

the feedback capacitor should be:

$$C_F = \sqrt{\frac{C_S}{GBW \times R_F}} \tag{8}$$

Note that these capacitor values are usually significant smaller than those given by the older, more conservative formula:

$$C_F = \frac{C_S R_{IN}}{R_F} \tag{9}$$

NOTE

C_S consists of the amplifier's input capacitance plus any stray capacitance from the circuit board. C_F compensates for the pole caused by C_S and the feedback resistors.

Using the smaller capacitors will give much higher bandwidth with little degradation of transient response. It may be necessary in any of the above cases to use a somewhat larger feedback capacitor to allow for unexpected stray capacitance, or to tolerate additional phase shifts in the loop, or excessive capacitive load, or to decrease the noise or bandwidth, or simply because the particular circuit implementation needs more feedback capacitance to be sufficiently stable. For example, a printed circuit board's stray capacitance may be larger or smaller than the breadboard's, so the actual optimum value for C_F may be different from the one estimated using the breadboard. In most cases, the values of C_F should be checked on the actual circuit, starting with the computed value.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LMP7721 is specified for operation from 1.8 V to 5.5 V. Many of the specifications apply from –40°C to 125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Typical Characteristics* section.

8.1.1 Using a Guard

In order to take full advantage of the LMP7721's ultra-low input bias current, a "Guard" trace is recommended when designing sub-nanoamp systems.

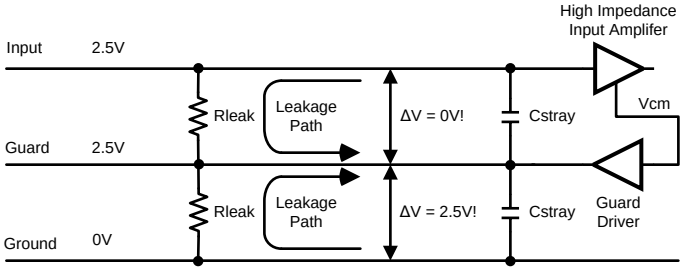


Figure 46. Guarding Theory

A "Guard" is a driven trace or shield that physically surrounds the input trace and feedback circuitry that is held at a potential equal to the average input signal potential. Since the input circuitry and the guard are kept at the same potential, the leakage current between the two nodes is practically zero. The guard is a low-impedance node, so any external leakages will "leak" into the guard and not into the protected input. One benefit of using a guard is it cancels the effect of the added stray and cable capacitance at low frequencies (but cannot cancel the sensor or amplifier input capacitance).

The guard potential may be taken from the inverting input (summing node) in noninverting and buffer applications. An example of this is shown in Figure 47 If the guarding needs to extend beyond the immediate local area around the IC, then a buffer should be used to drive the guard to prevent adding additional capacitance to the inverting node.

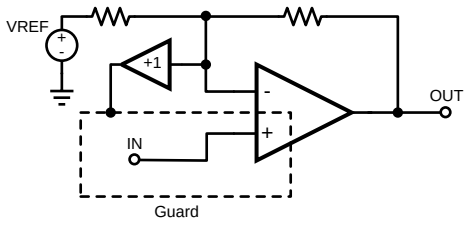


Figure 47. Guarding the Noninverting Configuration

The guard potential may be taken from the noninverting input or reference voltage in inverting or transimpedance applications. An example of this is shown in Figure 48

Application Information (continued)

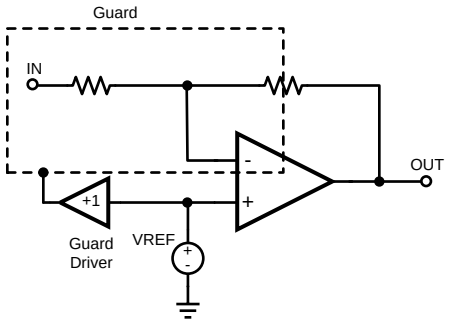


Figure 48. Guarding the Inverting or Transimpedance Configuration

The gain of the buffer should be slightly less than one to prevent oscillations and should be current limited to protect against short circuits. The buffer amplifier should also be capable of driving large capacitive loads. To satisfy these two requirements, a small series output resistor is usually placed on the buffer output in the range of 100 Ω to 1 kΩ.

For optimum results, the guard should completely enclose the input circuitry within a conductive "cocoon", including above and below the circuitry. A cover or shield connected to the guard should protect the circuitry above (or below) the PC board. Do not forget about thru-hole devices (like leaded photodiodes or connectors) that may expose high-impedance nodes to the opposite side of the board.

The guard trace should not be relied upon as the only method of shielding. A ground plane or shield should surround and protect the guard from large external leakages and noise, as the guard trace has the potential to couple noise back into the input. For more information on guarding, please see the articles referenced in *Related Documentation*.

8.1.2 Use Triaxial Cable

A triaxial cable or connector is similar to a coaxial cable or connector and is often referred to as “triax”. The triaxial cable extends the guard protection through the length of the cable by adding a second internal guard "shield" around the center conductor in addition to the outer ground shield. Figure 49 shows the structure of the triax connector.

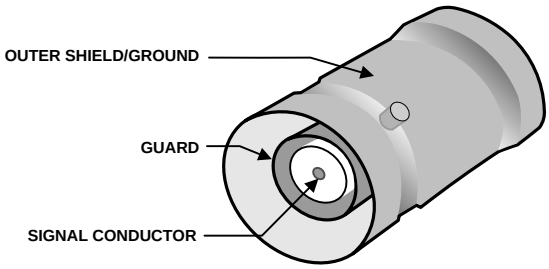


Figure 49. The Structure of a Triax

8.1.3 Properly Clean the Assembly

Proper cleaning of the board is very critical to providing the expected sub-picoamp performance. Properly cleaning the board and components takes a few extra steps over conventional board cleaning methods. Leftover flux residue, moisture and cleaning solvent residues will severely degrade the low-current performance.

Application Information (continued)

If using "water soluble" or "no clean" flux, a second cleaning step is needed. These fluxes still leave a film behind that can attract contaminates and dust. The board should be washed with fresh isopropyl alcohol or methanol and baked to make sure all remaining traces of moisture are removed from the board. Areas between the component leads should be scrubbed and areas under surface mount devices thoroughly flushed. The board should be re-cleaned after any rework to components within the guarded areas. Boards should be handled by the edges and stored in sealed containers with desiccant.

8.2 Typical Application

The following application examples highlight only a few of the circuits where the LMP7721 can be used.

A CMOS input stage with ultra-low input bias current, negligible input current noise, and low input voltage noise allows the LMP7721 to provide high fidelity amplification. In addition, the LMP7721 has a 17 MHz gain bandwidth product, which enables high gain at wide bandwidth. A rail-to-rail output swing at 5.5-V power supply allows detection and amplification of a wide range of input currents. These properties make the LMP7721 ideal for transimpedance amplification.

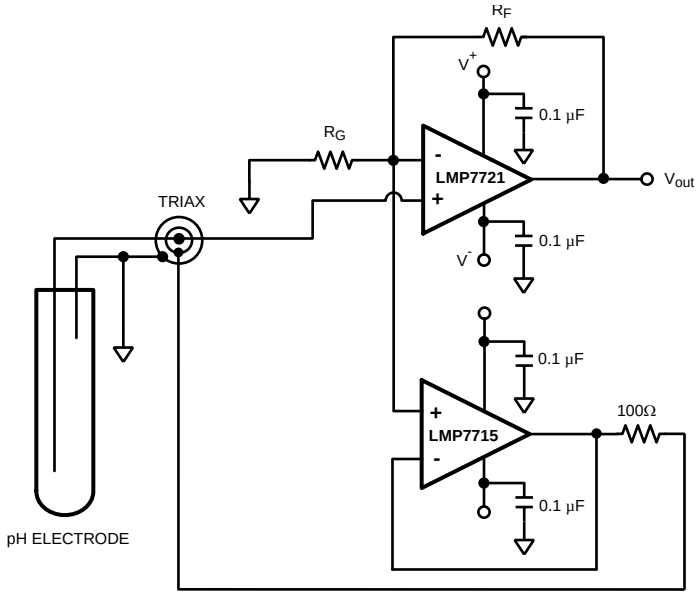


Figure 50. LMP7721 as pH Electrode Amplifier

8.2.1 Design Requirements

The output of a pH electrode is typically 59.16 mV per pH unit at 25°C, for an output range of 414 mV to −414 mV as the pH changes from 0 to 14 at 25°C.

Typical Application (continued)

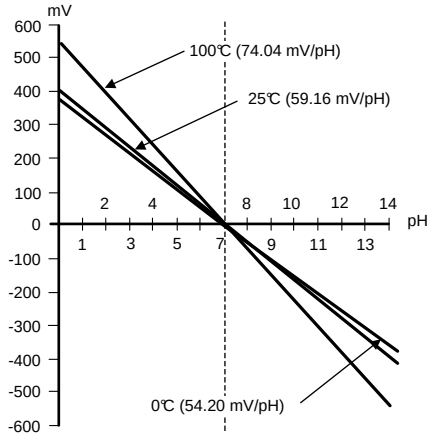


Figure 51. pH Electrode Transfer Function

The output impedance of a pH electrode is extremely high, ranging from 10 MΩ to 1000 MΩ. The ultra low input bias current of the LMP7721 allows the voltage error produced by the input bias current and electrode resistance to be minimal. For example, the output impedance of the pH electrode used is 10 MΩ, if an op amp with 3 nA of I_{bias} is used, the error caused due to this amplifier's input bias current and the source resistance of the pH electrode is 30 mV! This error can be greatly reduced to 30 nV by using the LMP7721.

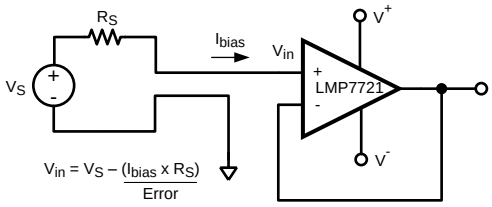


Figure 52. Error Caused by Amplifier's Input Bias Current and Sensor Source Impedance

8.2.2 Detailed Design Procedure

The output voltage of the pH electrode will range from 54.2 mV/pH at 0°C, to 74.04 mV/pH at 100°C. The maximum input voltage will then be ±74.04 mV * 7 = ±518.3 mV. Allowing for output swing and offset headroom, the maximum output swing should be limited to ±2.4V. The amplifier gain would then be 2.4 V / 0.5183 V = 4.6 V/V.

With R_F = 3.57 kΩ and R_G = 1 kΩ, the gain would be 4.57 V/V.

The output voltage from the pH electrode is fed to the signal conductor of the triax and then sent to the non-inverting input of the LMP7721. In this application, the inverting input is a low impedance node and hence is used to drive the LMP7715 which acts as a guard driver. The output of the guard driver is connected to the guard of the triax through a 100-Ω isolation resistor.

Figure 50 is an example of the LMP7721 used as a pH sensor amplifier.

Typical Application (continued)

8.2.3 Application Curve

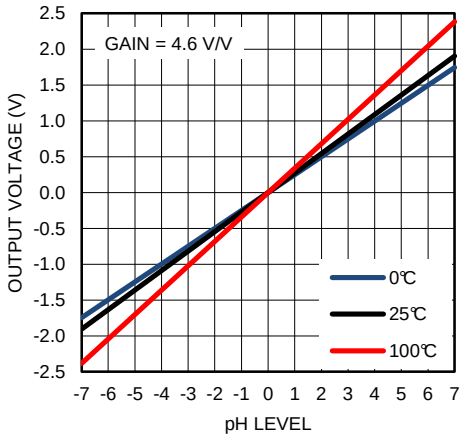


Figure 53. Output Voltage vs. pH Level

9 Power Supply Recommendations

For high-sensitivity applications, the power supply rails should be as clean as possible.

Noise on the power supply lines can modulate the tiny capacitance (about 0.5 pF) of the ESD structure on each input. While this is not a major concern for most applications, charge-sensitive or high-gain, high-impedance applications can be affected. Common results are power line "hum" or high-frequency switcher "hash" imposed on the signal.

TI recommends using a very low noise linear regulator and add a dedicated filter network to the LMP7721 power supply pins consisting of a series resistor of about 100 Ω, and a bypass capacitor of 100 uF or larger. Series inductors or ferrite beads may be required if high frequency switcher noise is present.

10 Layout

10.1 Layout Guidelines

In order to capitalize on the LMP7721's ultra-low input bias current, careful circuit layout and assembly are required. Guarding techniques are highly recommended to reduce parasitic leakage current by isolating the LMP7721's input from large voltage gradients across the PC board. A guard is a low-impedance conductor that surrounds an input line and its potential is raised to the input line's voltage. The input pins should be fully guarded as shown in Figure 54. The guard traces should completely encircle the input connections. In addition, they should be located on both sides of the PCB and be connected together.

To further guard the inputs from the supply pins, the two N/C pins may be connected to the guard trace which will provide guarding down to the leadframe level.

Solder mask should not cover the input and the guard area including guard traces on either side of the PCB.

Keep switching power supplies and other noise-producing devices away from the input area.

10.2 Layout Example

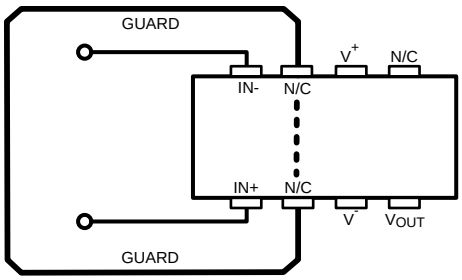


Figure 54. Layout Example Showing Guard Trace

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

- LMP7721 PSPICE Model, SNOM096
- TINA-TI SPICE Based Circuit Simulation Software (free download), http://www.ti.com/tool/tina-ti
- TI FilterPro Filter Design software, http://www.ti.com/tool/filterpro

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation, see the following:

- LMP7721 Multi-Function Evaluation Board (current evaluation board), SNOU004
- AN-1796 LMP7721 Evaluation Board (obsolete evaluation board - for reference only), SNOA513
- AN-1798 Designing with Electro-Chemical Sensors, SNOA514
- AN-1803 Design Considerations for a Transimpedance Amplifier, SNOA515
- AN-1852 Designing With pH Electrodes, SNOA529
- Compensate Transimpedance Amplifiers Intuitively, SBOA055
- Transimpedance Considerations for High-Speed Operational Amplifiers, SBOA112
- Noise Analysis of FET Transimpedance Amplifiers, SBOA060
- Circuit Board Layout Techniques - SLOA089
- Handbook of Operational Amplifier Applications - SBOA092
- Low Level Measurements Handbook, Keithley Instruments, Inc., Latest Edition. Available: www.keithley.com
- Grohe, P., "Design femtoampere circuits with low leakage, Part 1", EDN Magazine, November 7, 2011. Available: www.edn.com
- Grohe, P., "Design femtoampere circuits with low leakage, Part 2", EDN Magazine, June 15, 2012. Available: www.edn.com
- Grohe, P., "Design femtoampere circuits with low leakage, Part 3", EDN Magazine, September 7, 2012. Available: www.edn.com

11.3 Trademarks

LMP, PowerWise are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMP7721MA/NOPB	ACTIVE	SOIC	D	8	95	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LMP77 21MA	Samples
LMP7721MAX/NOPB	ACTIVE	SOIC	D	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LMP77 21MA	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

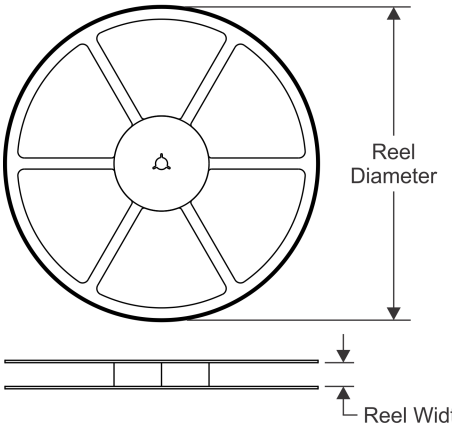
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

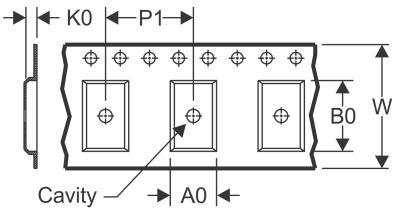
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

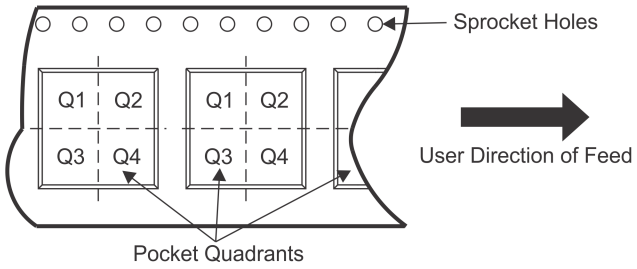


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

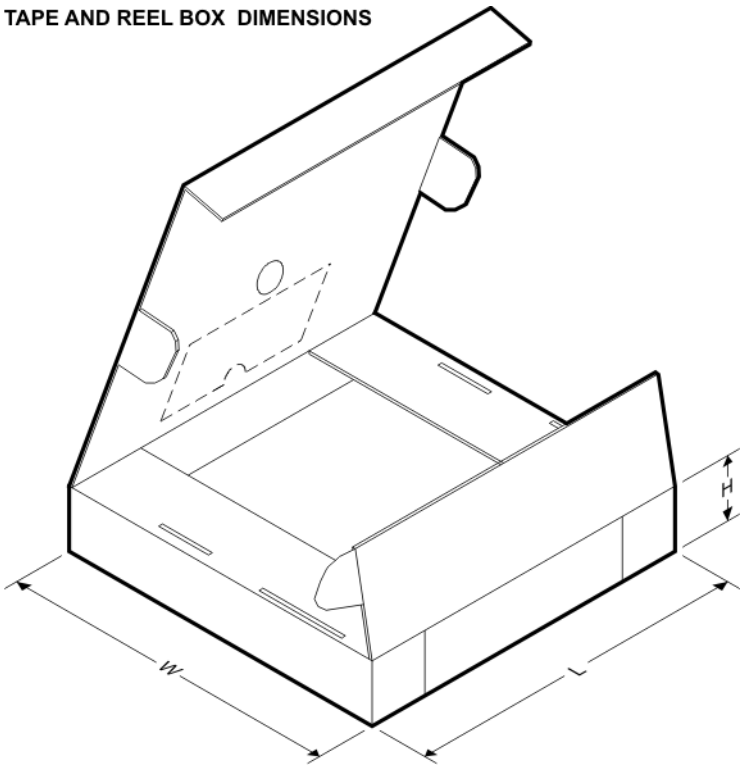
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

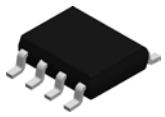
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMP7721MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMP7721MAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

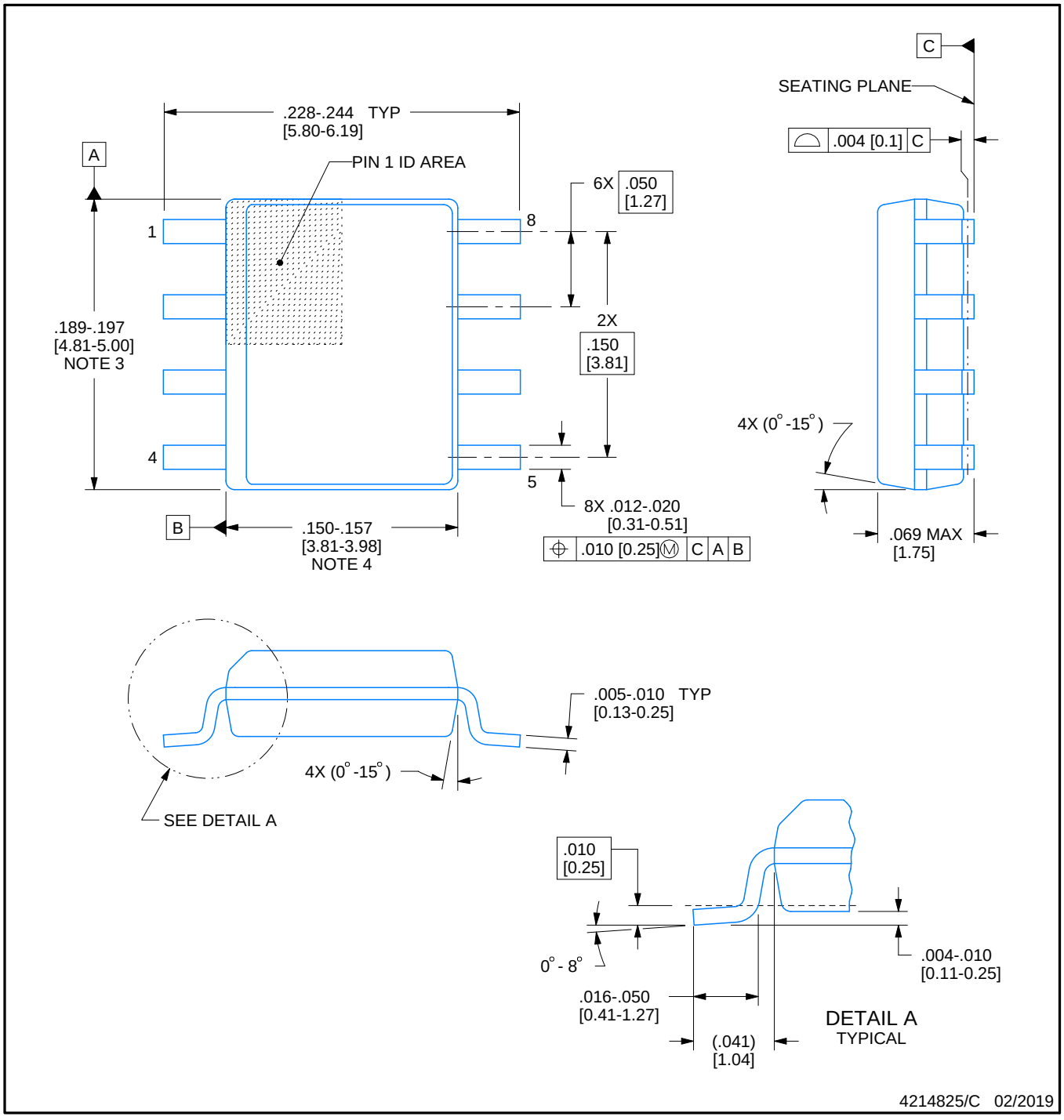


PACKAGE OUTLINE

D0008A

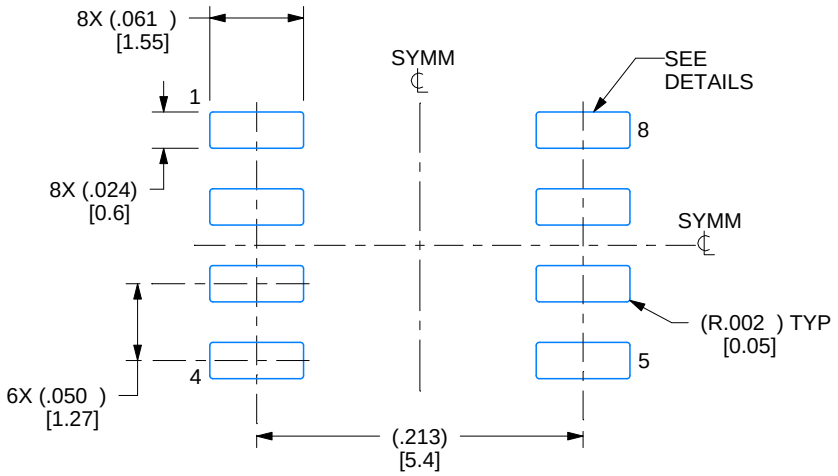
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

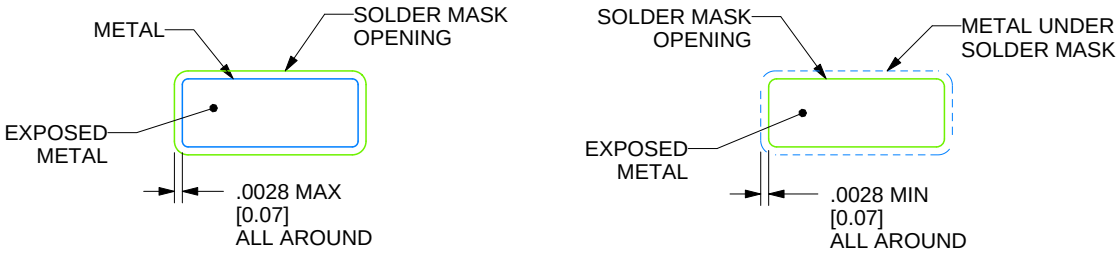


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

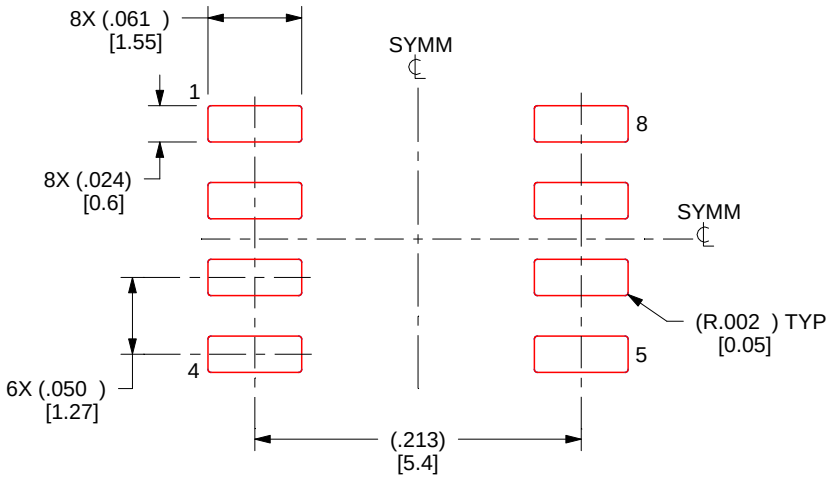
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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