LMV76x and LMV762Q-Q1 Low-Voltage, Precision Comparator With Push-Pull Output

1 Features

- V_S = 5 V, T_A = 25°C, Typical Values Unless Specified
- Input Offset Voltage 0.2 mV
- Input Offset Voltage (Maximum Over Temp) 1 mV
- Input Bias Current 0.2 pA
- Propagation Delay (OD = 50 mV) 120 ns
- Low Supply Current 300 µA
- CMRR 100 dB
- PSRR 110 dB
- Extended Temperature Range −40°C to +125°C
- Push-Pull Output
- Ideal for 2.7-V and 5-V Single-Supply Applications
- Available in Space-Saving Packages:
  - 6-Pin SOT-23 (Single With Shutdown)
  - 8-Pin SOIC (Single With Shutdown)
  - 8-Pin SOIC and VSSOP (Dual Without Shutdown)
- LMV762Q-Q1 is Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 1: –40°C to +125°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level 1C
  - Device CDM ESD Classification Level M2

2 Applications

- Portable and Battery-Powered Systems
- Scanners
- Set-Top Boxes
- High-Speed Differential Line Receiver
- Window Comparators
- Zero-Crossing Detectors
- High-Speed Sampling Circuits
- Automotive

3 Description

The LMV76x devices are precision comparators intended for applications requiring low noise and low input offset voltage. The LMV761 single has a shutdown pin that can be used to disable the device and reduce the supply current. The LMV761 is available in a space-saving 6-pin SOT-23 or 8-Pin SOIC package. The LMV762 dual is available in 8-pin SOIC or VSSOP package. The LMV762Q-Q1 is available VSSOP and SOIC packages.

These devices feature a CMOS input and push-pull output stage. The push-pull output stage eliminates the need for an external pullup resistor.

The LMV76x are designed to meet the demands of small size, low power and high performance required by portable and battery-operated electronics.

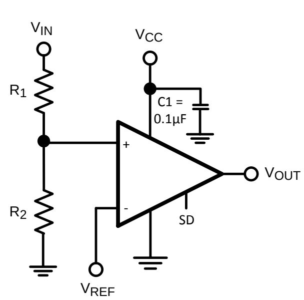
The input offset voltage has a typical value of 200 µV at room temperature and a 1-mV limit over temperature.

Device Information(1)

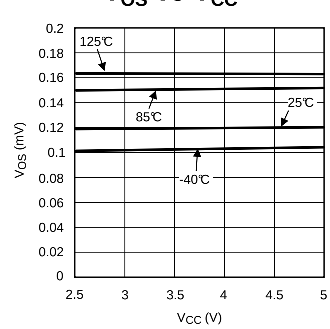
PART NUMBER	PACKAGE	BODY SIZE (NOM)
LMV761	SOIC (8)	4.90 mm × 3.91 mm
	SOT-23 (6)	2.90 mm × 1.60 mm
LMV762 LMV762Q-Q1	SOIC (8)	4.90 mm × 3.91 mm
	VSSOP (8)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Threshold Detector



V_{OS} vs V_{CC}



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4 Revision History

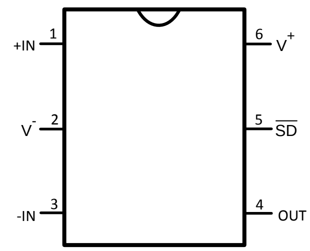
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision H (March 2013) to Revision I	Page
• Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

Changes from Revision G (March 2013) to Revision H	Page
• Changed layout of National Data Sheet to TI format	15

5 Pin Configuration and Functions

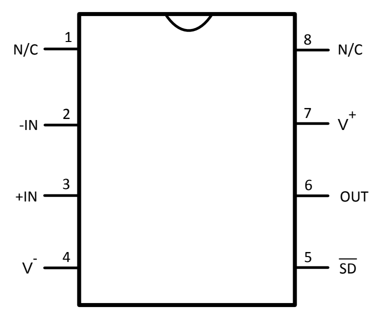
LMV761 (Single) DBV Package
6-Pin SOT-23
Top View



Pin Functions for SOT-23

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	+IN	I	Noninverting input
2	V^-	P	Negative power terminal
3	-IN	I	Inverting input
4	OUT	O	Output
5	SDB	I	Shutdown (active low)
6	V^+	P	Positive power terminal

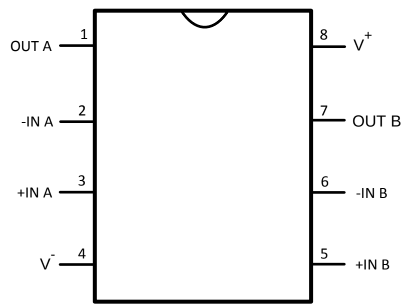
LMV761 (Single) D Package
8-Pin SOIC
Top View



Pin Functions for SOIC (Single)

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	N/C	—	No Connect (not internally connected)
2	-IN	I	Inverting Input
3	+IN	I	Noninverting Input
4	V^-	P	Negative Power Terminal
5	SDB	I	Shutdown (active low)
6	OUT	O	Output
7	V^+	P	Positive Power Terminal
8	N/C	—	No Connect (not internally connected)

LMV762, LMV762Q-Q1 (Dual) DBV or DGK Package
8-Pin SOIC or VSSOP
Top View



Pin Functions for SOIC and VSSOP (Dual)

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	OUTA	O	Channel A Output
2	-INA	I	Channel A Inverting Input
3	+INA	I	Channel A Noninverting Input
4	V^-	P	Negative Power Terminal
5	+INB	I	Channel B Noninverting Input
6	-INB	I	Channel B Inverting Input
7	OUTB	O	Channel B Output
8	V^+	P	Positive Power Terminal

6 Specifications

6.1 Absolute Maximum Ratings

See (1)(2)

		MIN	MAX	UNIT
Supply voltage ($V^+ – V^-$)			5.5	V
Differential input voltage		Supply Voltage		
Voltage between any two pins		Supply Voltage		
Output short circuit duration(3)	Current at input pin		±5	mA
Soldering information	Infrared or convection (20 sec.)		235	°C
	Wave soldering (10 sec.) (Lead temp)		260	°C
Junction temperature			150	°C
Storage temperature, T_{stg}		−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) Applies to both single supply and split supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output current in excess of ±25 mA over long term may adversely affect reliability.

6.2 ESD Ratings: LMV761, LMV762

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge(1)	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(2)	± 2000	V
		Machine model	± 200	

(1) Unless otherwise specified human body model is 1.5 kΩ in series with 100 pF. Machine model 200 pF.
(2) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 ESD Ratings: LMV762Q-Q1

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	± 2000	V
		Machine model	± 200	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.4 Recommended Operating Conditions

	MIN	MAX	UNIT
Supply voltage ($V^+ – V^−$)	2.7	5.25	V
Temperature range	−40	125	°C

6.5 Thermal Information

THERMAL METRIC(1)		LMV761	LMV762, LMV762Q-Q1		UNIT
		D (SOIC)	DBV (SOT-23)	DGK (VSSOP)	
		8 PINS	6 PINS	8 PINS	
$R_{θJA}$	Junction-to-ambient thermal resistance (2)	190	265	235	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) The maximum power dissipation is a function of $T_{J(MAX)}$, $θ_{JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} – T_A)\ R_{θJA}$. All numbers apply for packages soldered directly into a PCB.

6.6 2.7-V Electrical Characteristics

Unless otherwise specified, all limited ensured for T_J = 25°C, $V_{CM} = V^+ / 2$, V^+ = 2.7 V, $V^−$ = 0 V.

PARAMETER		TEST CONDITIONS		MIN(1)	TYP(2)	MAX(1)	UNIT
V_{OS}	Input offset voltage				0.2		mV
		apply at the temperature extremes(3)				1	
I_B	Input bias current(4)				0.2	50	pA
I_{OS}	Input offset current(4)				0.001	5	pA
CMRR	Common-mode rejection ratio	$0\text{ V} < V_{CM} < V_{CC} – 1.3\text{ V}$		80	100		dB
PSRR	Power supply rejection ratio	V^+ = 2.7 V to 5 V		80	110		dB
CMVR	Input common-mode voltage range	CMRR > 50 dB	apply at the temperature extremes(3)	−0.3		1.5	V
V_O	Output swing high	I_L = 2 mA, V_{ID} = 200 mV		$V^+ – 0.35$	$V^+ – 0.1$		V
	Output swing low	I_L = −2 mA, V_{ID} = –200 mV			90	250	mV
I_{SC}	Output short circuit current(5)	Sourcing, V_O = 1.35 V, V_{ID} = 200 mV		6	20		mA
		Sinking, V_O = 1.35 V, V_{ID} = –200 mV		6	15		

(1) All limits are specified by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm.
(3) Maximum temperature ensured range is −40°C to +125°C.
(4) Specified by design.
(5) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No ensured specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$. See *Recommended Operating Conditions* for information on temperature de-rating of this device. Absolute Maximum Rating indicate junction temperature limits beyond which the device may be permanently degraded, either mechanically or electrically.

2.7-V Electrical Characteristics (continued)

Unless otherwise specified, all limited ensured for T_J = 25°C, V_{CM} = V^+ / 2, V^+ = 2.7 V, V^- = 0 V^-.

PARAMETER		TEST CONDITIONS	MIN(1)	TYP(2)	MAX(1)	UNIT
I_S	Supply current LMV761 (single comparator)			275	700	µA
	LMV762, LMV762Q-Q1 (both comparators)			550		µA
		apply at the temperature extremes(3)			1400	
$I_{OUT\ LEAKAGE}$	Output leakage I at shutdown	$\overline{SD}$ = GND, V_O = 2.7 V		0.2		µA
$I_{S\ LEAKAGE}$	Supply leakage I at shutdown	$\overline{SD}$ = GND, V_{CC} = 2.7 V		0.2	2	µA

6.7 5-V Electrical Characteristics

Unless otherwise specified, all limited ensured for T_J = 25°C, V_{CM} = V^+ / 2, V^+ = 5 V, V^- = 0 V^-.

PARAMETER		TEST CONDITIONS		MIN(1)	TYP(2)	MAX(1)	UNIT
V_{OS}	Input offset voltage				0.2		mV
		apply at the temperature extremes(3)				1	
I_B	Input bias current(4)				0.2	50	pA
I_{OS}	Input offset current(4)				0.01	5	pA
CMRR	Common-mode rejection ratio	0 V < V_{CM} < V_{CC} – 1.3 V		80	100		dB
PSRR	Power supply rejection ratio	V^+ = 2.7 V to 5 V		80	110		dB
CMVR	Input common-mode voltage range	CMRR > 50 dB	apply at the temperature extremes(3)	−0.3		3.8	V
V_O	Output swing high	I_L = 4 mA, V_{ID} = 200 mV		V^+ – 0.35	V^+ – 0.1		V
	Output swing low	I_L = –4 mA, V_{ID} = –200 mV			120	250	mV
I_{SC}	Output short circuit current(5)	Sourcing, V_O = 2.5 V, V_{ID} = 200 mV		6	60		mA
		Sinking, V_O = 2.5 V, V_{ID} = −200 mV		6	40		
I_S	Supply current LMV761 (single comparator)				225	700	µA
	LMV762, LMV762Q-Q1 (both comparators)				450		µA
		apply at the temperature extremes(3)				1400	
$I_{OUT\ LEAKAGE}$	Output leakage I at shutdown	$\overline{SD}$ = GND, V_O = 5 V			0.2		µA
$I_{S\ LEAKAGE}$	Supply leakage I at shutdown	$\overline{SD}$ = GND, V_{CC} = 5 V			0.2	2	µA

(1) All limits are specified by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm.
(3) Maximum temperature ensured range is −40°C to +125°C.
(4) Specified by design.
(5) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T_J = T_A. No ensured specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where T_J > T_A. See *Recommended Operating Conditions* for information on temperature de-rating of this device. Absolute Maximum Rating indicate junction temperature limits beyond which the device may be permanently degraded, either mechanically or electrically.

6.8 2-V Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

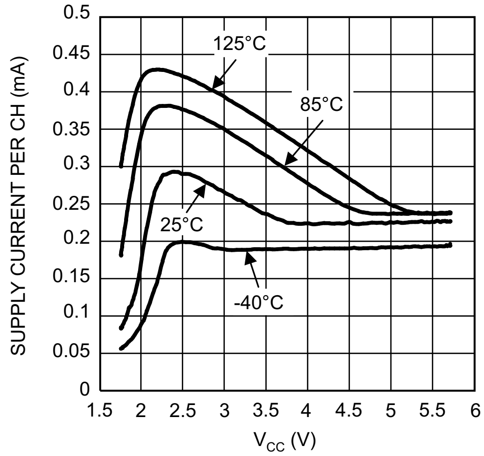
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PD}	Propagation delay R_L = 5.1 kΩ C_L = 50 pF	Overdrive = 5 mV		270		ns
		Overdrive = 10 mV		205		
		Overdrive = 50 mV		120		
t_{SKEW}	Propagation delay skew			5		ns
t_r	Output rise time	10% to 90%		1.7		ns
t_f	Output fall time	90% to 10%		1.8		ns
t_{on}	Turnon time from shutdown			6		μs

6.9 5-V Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

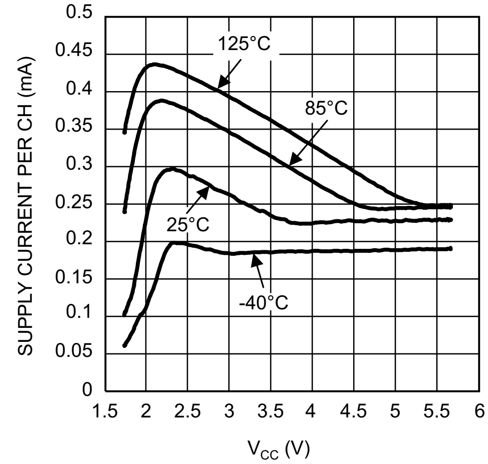
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PD}	Propagation delay R_L = 5.1 kΩ C_L = 50 pF	Overdrive = 5 mV		225		ns
		Overdrive = 10 mV		190		
		Overdrive = 50 mV		120		
t_{SKEW}	Propagation delay skew			5		ns
t_r	Output rise time	10% to 90%		1.7		ns
t_f	Output fall time	90% to 10%		1.5		ns
t_{on}	Turnon time from shutdown			4		μs

6.10 Typical Characteristics



V_O = High

Figure 1. PSI vs V_{CC}



V_O = Low

Figure 2. PSI vs V_{CC}

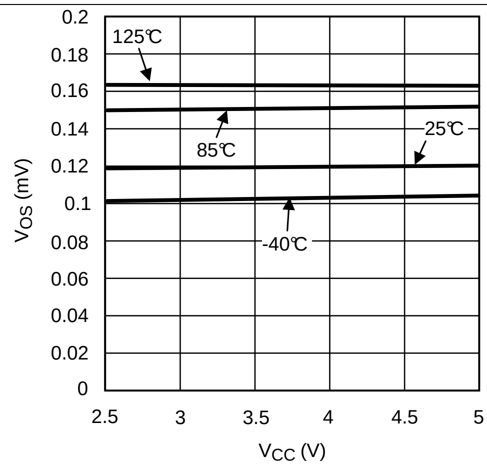


Figure 3. V_{OS} vs V_{CC}

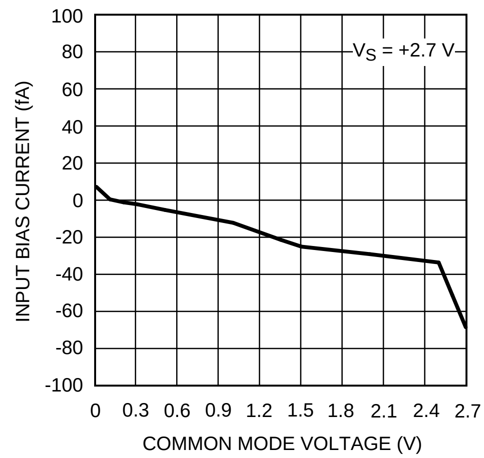


Figure 4. Input Bias vs Common Mode at 25°C

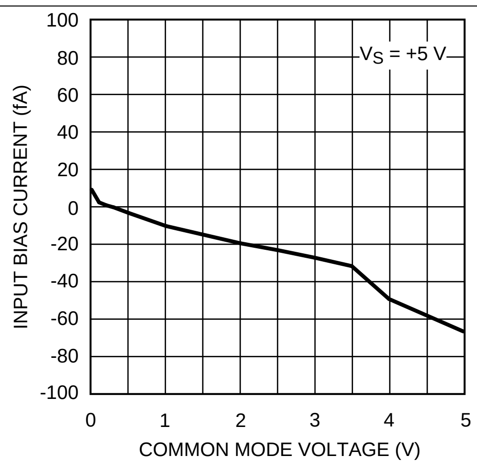


Figure 5. Input Bias vs Common Mode at 25°C

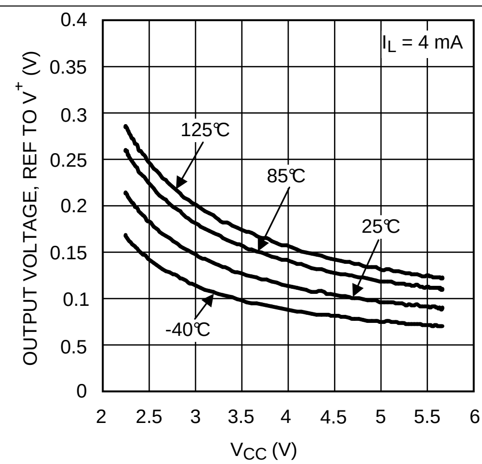


Figure 6. Output Voltage vs Supply Voltage

Typical Characteristics (continued)

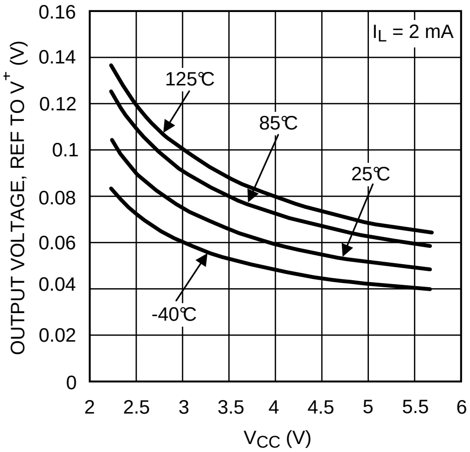


Figure 7. Output Voltage vs Supply Voltage

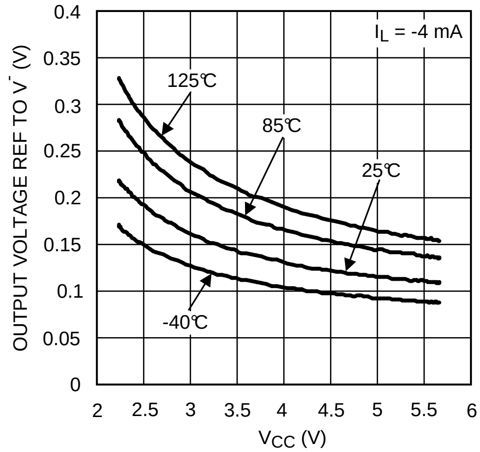


Figure 8. Output Voltage vs Supply Voltage

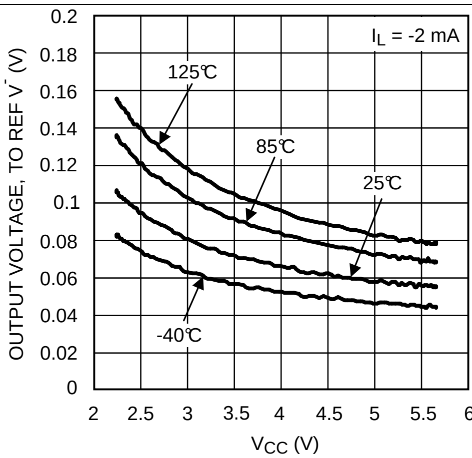


Figure 9. Output Voltage vs Supply Voltage

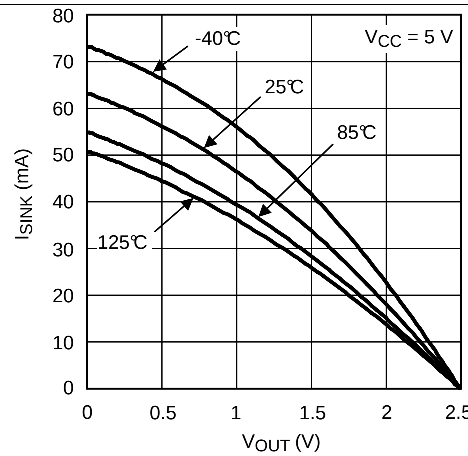


Figure 10. I_{SOURCE} vs V_{OUT}

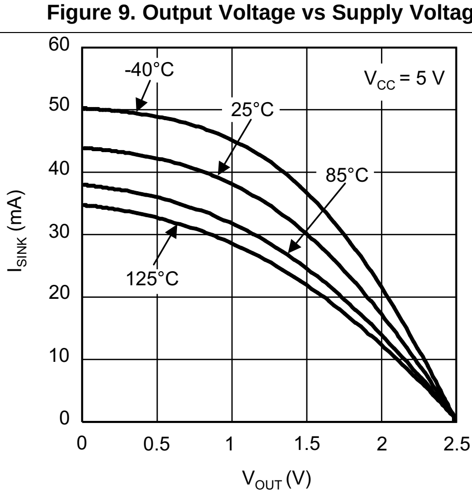


Figure 11. I_{SINK} vs V_{OUT}

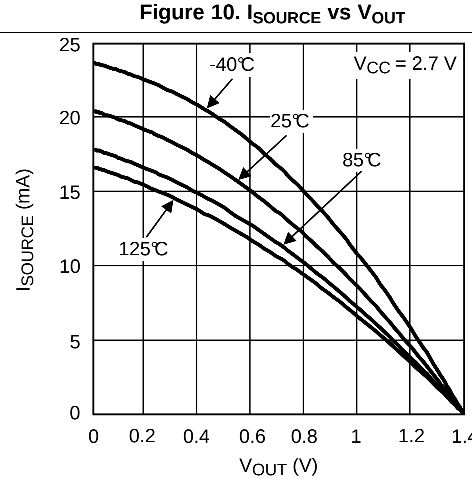


Figure 12. I_{SOURCE} vs V_{OUT}

Typical Characteristics (continued)

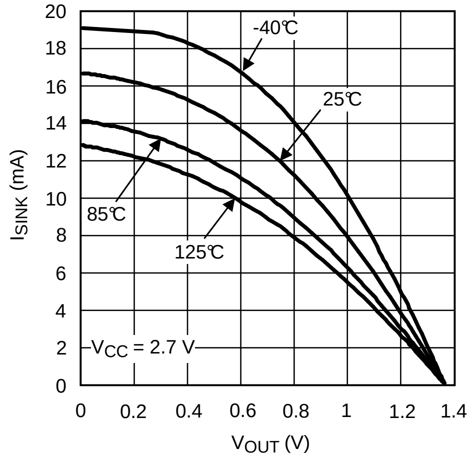


Figure 13. I_{SINK} vs V_{OUT}

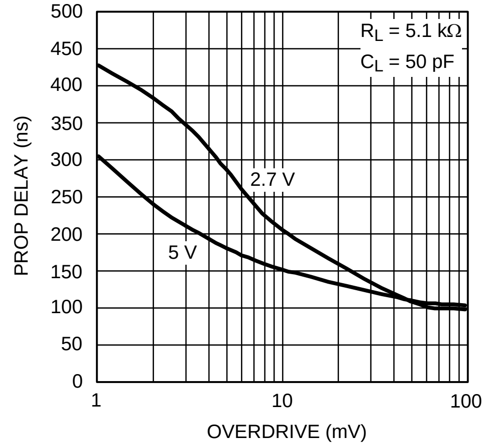


Figure 14. Prop Delay vs Overdrive

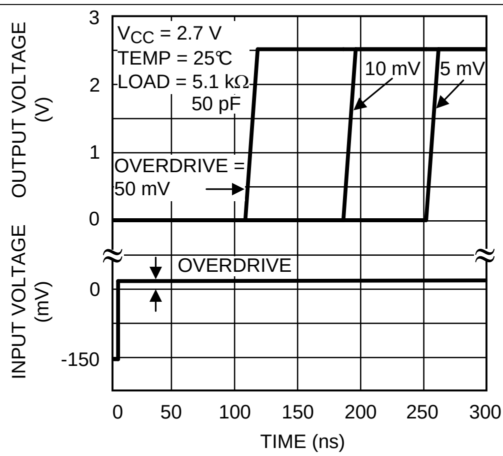


Figure 15. Response Time vs Input Overdrives Positive Transition

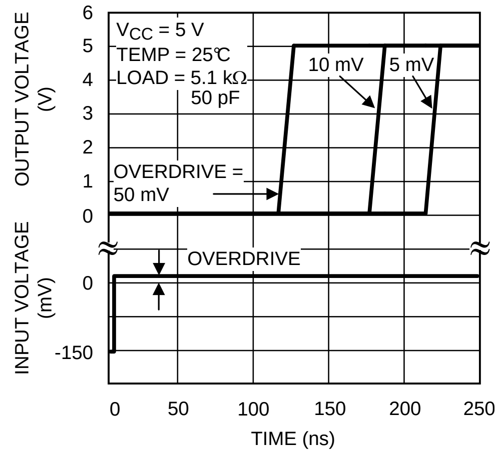


Figure 16. Response Time vs Input Overdrives Positive Transition

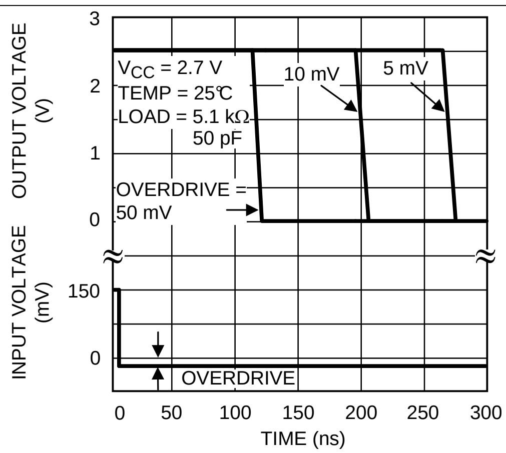


Figure 17. Response Time vs Input Overdrives Negative Transition

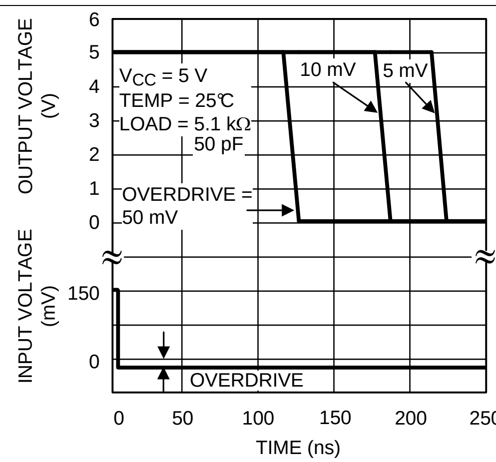


Figure 18. Response Time vs Input Overdrives Negative Transition

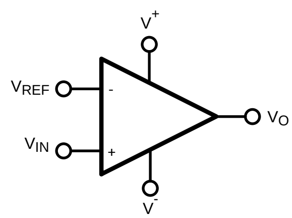
7 Detailed Description

7.1 Overview

The LMV76x family of precision comparators is available in a variety of packages and is ideal for portable and battery-operated electronics.

To minimize external components, the LMV76x family features a push-pull output stage where the output levels are power-supply determined. In addition, the LMV761 (single) features an active-low shutdown pin that can be used to disable the device and reduce the supply current.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Basic Comparator

A basic comparator circuit is used to convert analog input signals to digital output signals. The comparator compares an input voltage (V_{IN}) at the noninverting input to the reference voltage (V_{REF}) at the inverting pin. If V_{IN} is less than V_{REF} the output (V_O) is low (V_{OL}). However, if V_{IN} is greater than V_{REF}, the output voltage (V_O) is high (V_{OH}).

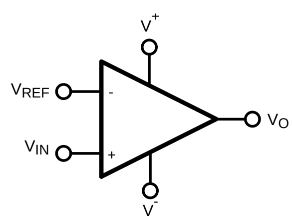


Figure 19. Basic Comparator Without Hysteresis

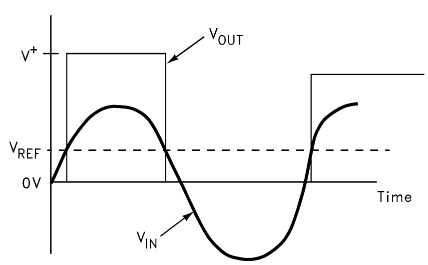


Figure 20. Basic Comparator

7.3.2 Hysteresis

The basic comparator configuration may oscillate or produce a noisy output if the applied differential input is near the input offset voltage of the comparator, which tends to occur when the voltage on one input is equal or very close to the other input voltage. Adding hysteresis can prevent this problem. Hysteresis creates two switching thresholds (one for the rising input voltage and the other for the falling input voltage). Hysteresis is the voltage difference between the two switching thresholds. When both inputs are nearly equal, hysteresis causes one input to effectively move quickly past the other. Thus, moving the input out of the region in which oscillation may occur.

Feature Description (continued)

Hysteresis can easily be added to a comparator in a noninverting configuration with two resistors and positive feedback Figure 22. The output will switch from low to high when V_{IN} rises up to V_{IN1}, where V_{IN1} is calculated by Equation 1:

$$V_{IN1} = [V_{REF}(R_1 + R_2)] / R_2 \quad (1)$$

The output will switch from high to low when V_{IN} falls to V_{IN2}, where V_{IN2} is calculated by Equation 2:

$$V_{IN2} = [V_{REF}(R_1 + R_2) - (V_{CC}\ R_1)] / R_2 \quad (2)$$

The Hysteresis is the difference between V_{IN1} and V_{IN2}, as calculated by Equation 3:

$$\Delta V_{IN} = V_{IN1} - V_{IN2} = [V_{REF}(R_1 + R_2) / R_2] - [V_{REF}(R_1 + R_2)] - [(V_{CC}\ R_1) / R_2] = V_{CC}\ R_1 / R_2 \quad (3)$$

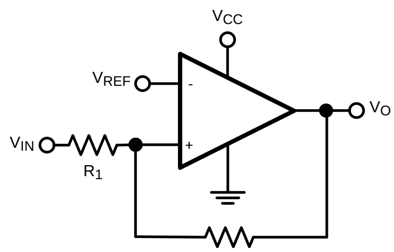


Figure 21. Basic Comparator With Hysteresis

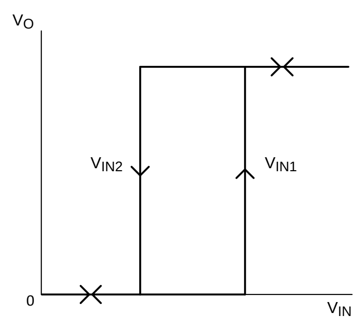


Figure 22. Noninverting Comparator Configuration

7.3.3 Input

The LMV76x devices have near-zero input bias current, which allows very high resistance circuits to be used without any concern for matching input resistances. This near-zero input bias also allows the use of very small capacitors in R-C type timing circuits. This reduces the cost of the capacitors and amount of board space used.

7.4 Device Functional Modes

7.4.1 Shutdown Mode

The LMV761 features a low-power shutdown pin that is activated by driving $\overline{SD}$ low. In shutdown mode, the output is in a high-impedance state, supply current is reduced to 20 nA and the comparator is disabled. Driving $\overline{SD}$ high will turn the comparator on. The $\overline{SD}$ pin must not be left unconnected due to the fact that it is a high-impedance input. When left unconnected, the output will be at an unknown voltage. Do **not** three-state the $\overline{SD}$ pin.

The maximum input voltage for $\overline{SD}$ is 5.5 V referred to ground and is not limited by V_{CC}. This allows the use of 5-V logic to drive $\overline{SD}$ while V_{CC} operates at a lower voltage, such as 3 V. The logic threshold limits for $\overline{SD}$ are proportional to V_{CC}.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LMV76x are single-supply comparators with 120 ns of propagation delay and 300 µA of supply current.

8.2 Typical Application

A typical application for a LMV76x comparator is a programmable square-wave oscillator.

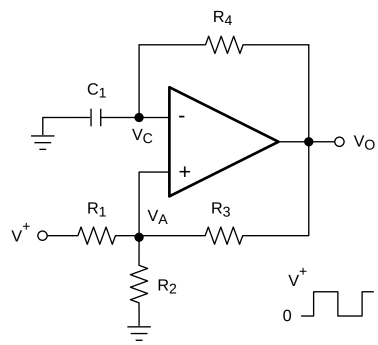


Figure 23. Square-Wave Oscillator

8.2.1 Design Requirements

The circuit in Figure 23 generates a square wave whose period is set by the RC time constant of the capacitor C_1 and resistor R_4. V^+ = 5 V unless otherwise specified.

8.2.2 Detailed Design Procedure

The maximum frequency is limited by the large signal propagation delay of the comparator and by the capacitive loading at the output, which limits the output slew rate.

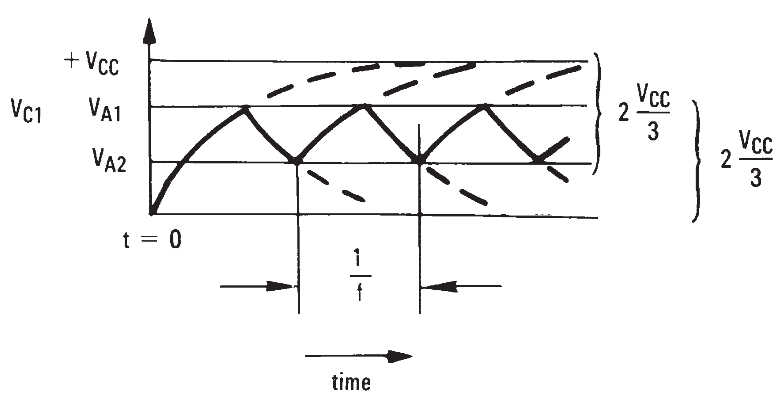


Figure 24. Square-Wave Oscillator Timing Thresholds

Typical Application (continued)

Consider the output of Figure 23 is high to analyze the circuit. That implies that the inverted input (V_C) is lower than the noninverting input (V_A). This causes the C_1 to be charged through R_4, and the voltage V_C increases until it is equal to the noninverting input. The value of V_A at this point is calculated by Equation 4:

$$V_{A1} = \frac{V_{CC} \cdot R_2}{R_2 + R_1 \parallel R_3} \tag{4}$$

If $R_1 = R_2 = R_3$, then $V_{A1} = 2\ V_{CC} / 3$

At this point the comparator switches pulling down the output to the negative rail. The value of V_A at this point is calculated by Equation 5:

$$V_{A2} = \frac{V_{CC}(R_2 \parallel R_3)}{R_1 + (R_2 \parallel R_3)} \tag{5}$$

If $R_1 = R_2 = R_3$, then $V_{A2} = V_{CC} / 3$.

The capacitor C_1 now discharges through R_4, and the voltage V_C decreases until it is equal to V_{A2}, at which point the comparator switches again, bringing it back to the initial stage. The time period is equal to twice the time it takes to discharge C_1 from 2 V_{CC} / 3 to V_{CC} / 3, which is given by $R_4C_1 \times \ln 2$. Hence, the formula for the frequency is calculated by Equation 6:

$$F = 1 / (2 \times R_4 \times C_1 \times \ln 2) \tag{6}$$

8.2.3 Application Curve

Figure Figure 25 shows the simulated results of an oscillator using the following values:

- $R_1 = R_2 = R_3 = R_4 = 100\ k\Omega$
- $C_1 = 100\ pF$, $C_L = 20\ pF$
- V+ = 5 V, V– = GND
- C_{STRAY} (not shown) from V_a to GND = 10 pF

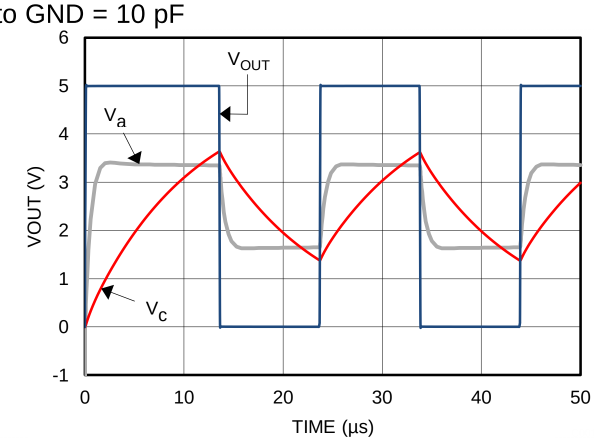


Figure 25. Square-Wave Oscillator Output Waveform

9 Power Supply Recommendations

To minimize supply noise, power supplies must be decoupled by a 0.1-μF ceramic capacitor in parallel with a 10-μF capacitor.

Due to the nanosecond edges on the output transition, peak supply currents will be drawn during output transitions. Peak current depends on the capacitive loading on the output. The output transition can cause transients on poorly bypassed power supplies. These transients can cause a poorly bypassed power supply to *ring* due to trace inductance and low self-resonance frequency of high ESR bypass capacitors.

Treat the LMV6x as a high-speed device. Keep the ground paths short and place small (low-ESR ceramic) bypass capacitors directly between the V^+ and V^- pins.

Output capacitive loading and output toggle rate will cause the average supply current to rise over the quiescent current.

10 Layout

10.1 Layout Guidelines

The LMV76x is designed to be stable and oscillation free, but it is still important to include the proper bypass capacitors and ground pick-ups. Ceramic 0.1-μF capacitors must be placed at both supplies to provide clean switching. Minimize the length of signal traces to reduce stray capacitance.

10.2 Layout Example

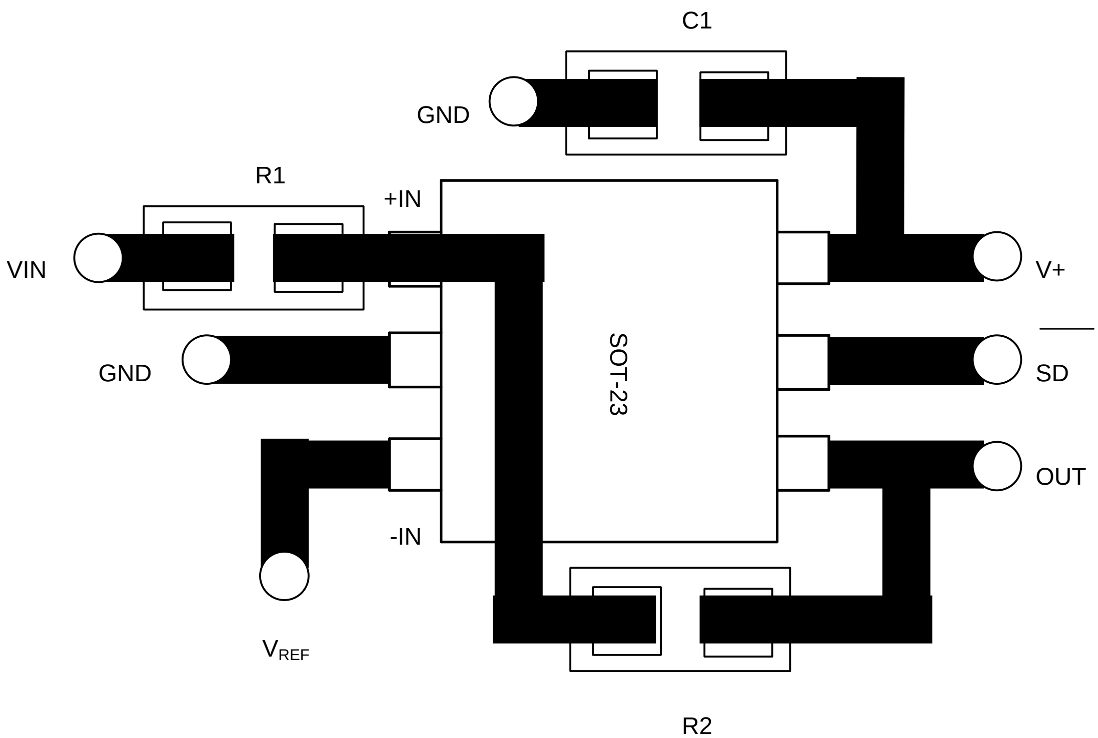


Figure 26. Comparator With Hysteresis

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LMV761	Click here	Click here	Click here	Click here	Click here
LMV762	Click here	Click here	Click here	Click here	Click here
LMV762Q-Q1	Click here	Click here	Click here	Click here	Click here

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

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All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMV761MA	NRND	SOIC	D	8	95	TBD	Call TI	Call TI	-40 to 125	LMV76 1MA	
LMV761MA/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LMV76 1MA	Samples
LMV761MAX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LMV76 1MA	Samples
LMV761MF	NRND	SOT-23	DBV	6	1000	TBD	Call TI	Call TI	-40 to 125	C22A	
LMV761MF/NOPB	ACTIVE	SOT-23	DBV	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	C22A	Samples
LMV761MFX	NRND	SOT-23	DBV	6	3000	TBD	Call TI	Call TI	-40 to 125	C22A	
LMV761MFX/NOPB	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	C22A	Samples
LMV762MA	NRND	SOIC	D	8	95	TBD	Call TI	Call TI	-40 to 125	LMV7 62MA	
LMV762MA/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LMV7 62MA	Samples
LMV762MAX	NRND	SOIC	D	8	2500	TBD	Call TI	Call TI	-40 to 125	LMV7 62MA	
LMV762MAX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LMV7 62MA	Samples
LMV762MM/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	C23A	Samples
LMV762MMX	NRND	VSSOP	DGK	8	3500	TBD	Call TI	Call TI	-40 to 125	C23A	
LMV762MMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	C23A	Samples
LMV762QMA/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LMV76 2QMA	Samples
LMV762QMAX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LMV76 2QMA	Samples
LMV762QMM/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	C32A	Samples
LMV762QMMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	C32A	Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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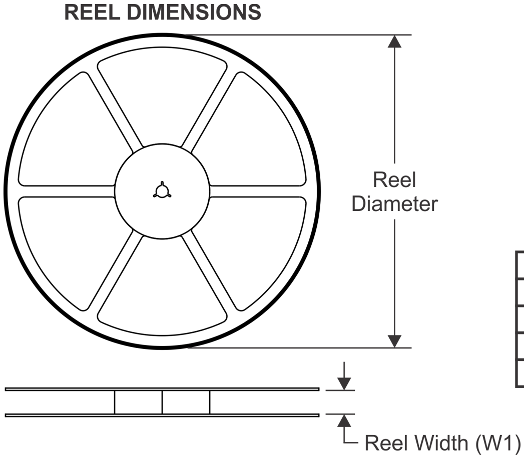
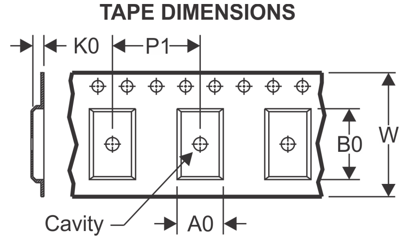
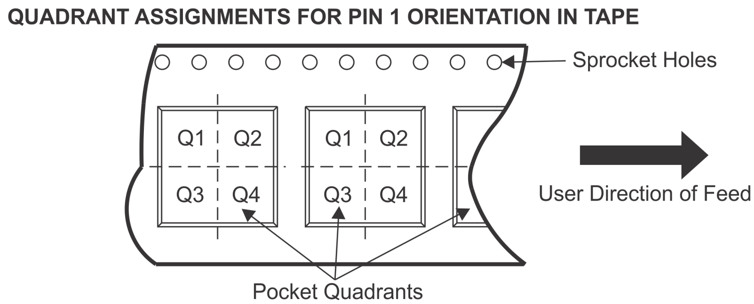
TAPE AND REEL INFORMATION





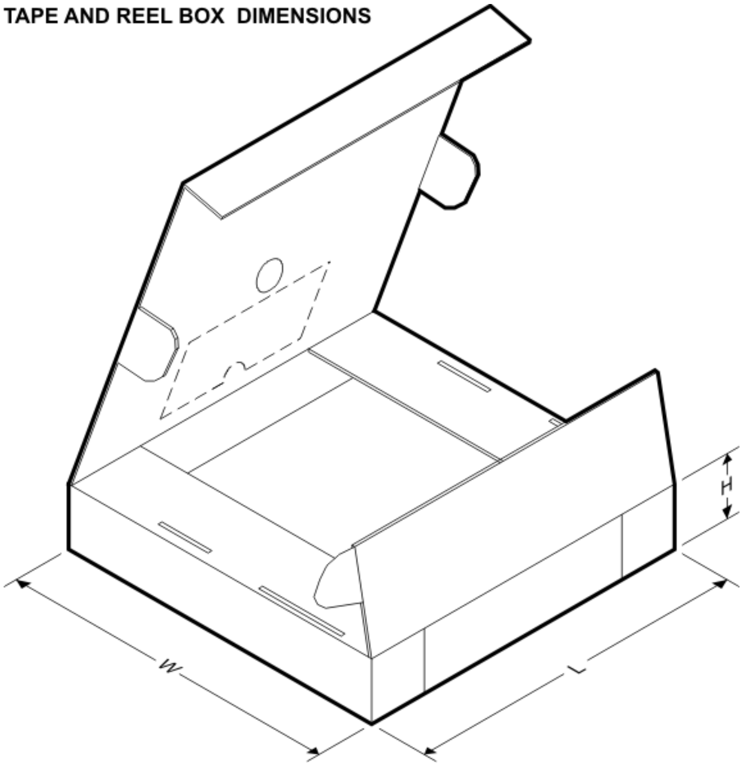
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMV761MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMV761MF	SOT-23	DBV	6	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV761MF/NOPB	SOT-23	DBV	6	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV761MFX	SOT-23	DBV	6	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV761MFX/NOPB	SOT-23	DBV	6	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV762MAX	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMV762MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMV762MM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV762MMX	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV762MMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV762QMAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMV762QMM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV762QMMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

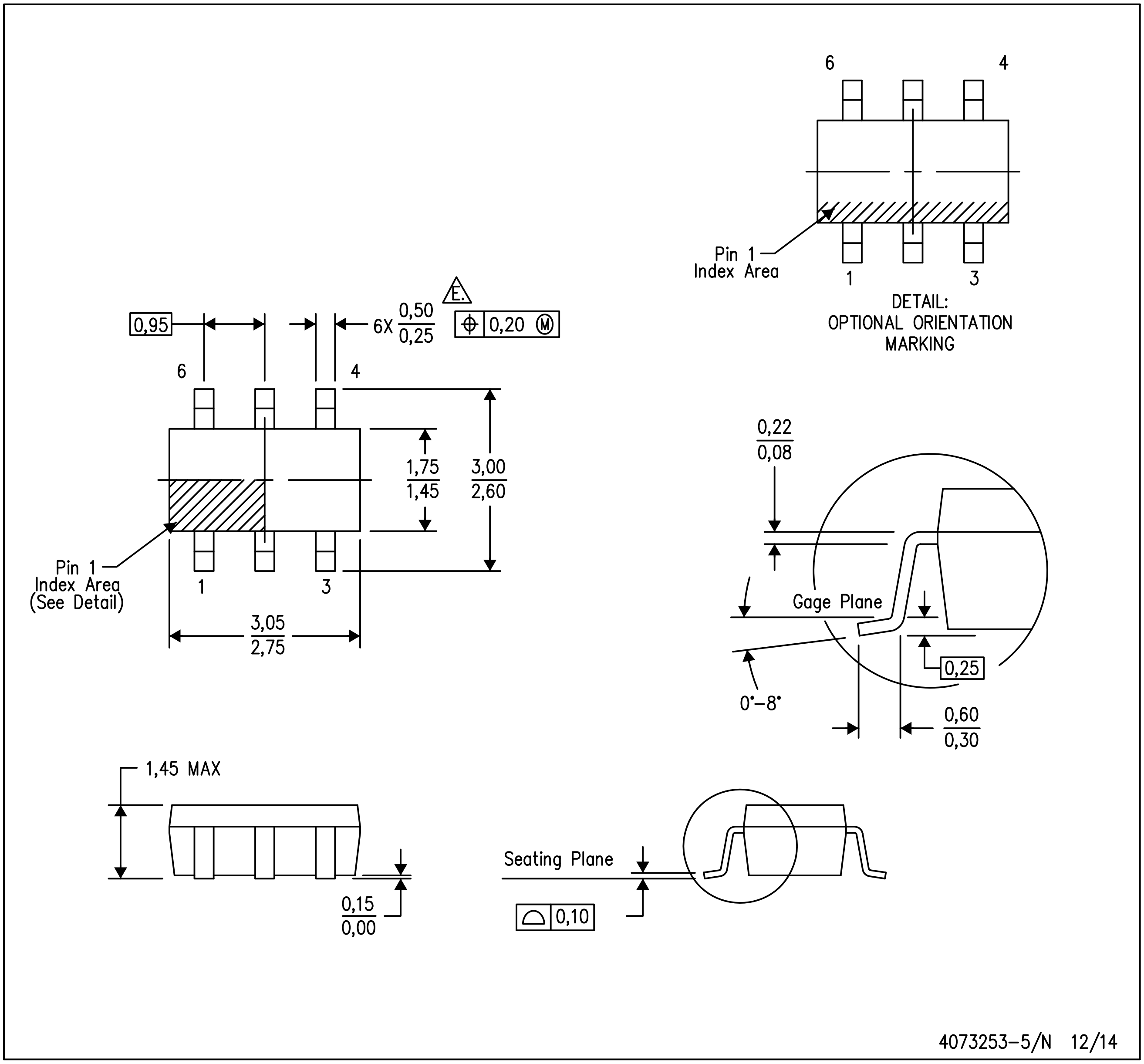
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

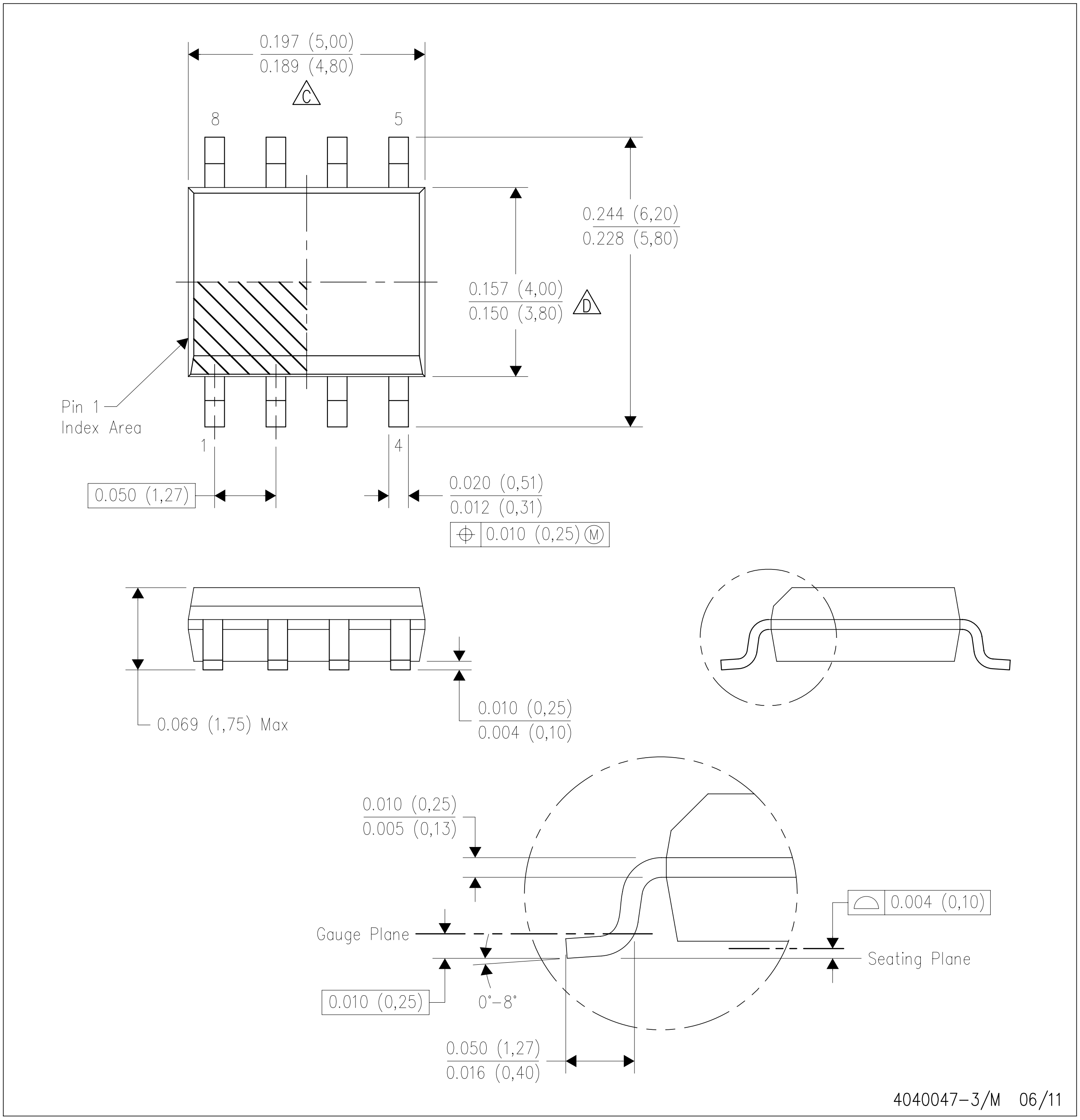
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMV761MAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMV761MF	SOT-23	DBV	6	1000	210.0	185.0	35.0
LMV761MF/NOPB	SOT-23	DBV	6	1000	210.0	185.0	35.0
LMV761MFX	SOT-23	DBV	6	3000	210.0	185.0	35.0
LMV761MFX/NOPB	SOT-23	DBV	6	3000	210.0	185.0	35.0
LMV762MAX	SOIC	D	8	2500	367.0	367.0	35.0
LMV762MAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMV762MM/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LMV762MMX	VSSOP	DGK	8	3500	367.0	367.0	35.0
LMV762MMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LMV762QMAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMV762QMM/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LMV762QMMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0

DBV (R–PDSO–G6) PLASTIC SMALL–OUTLINE PACKAGE



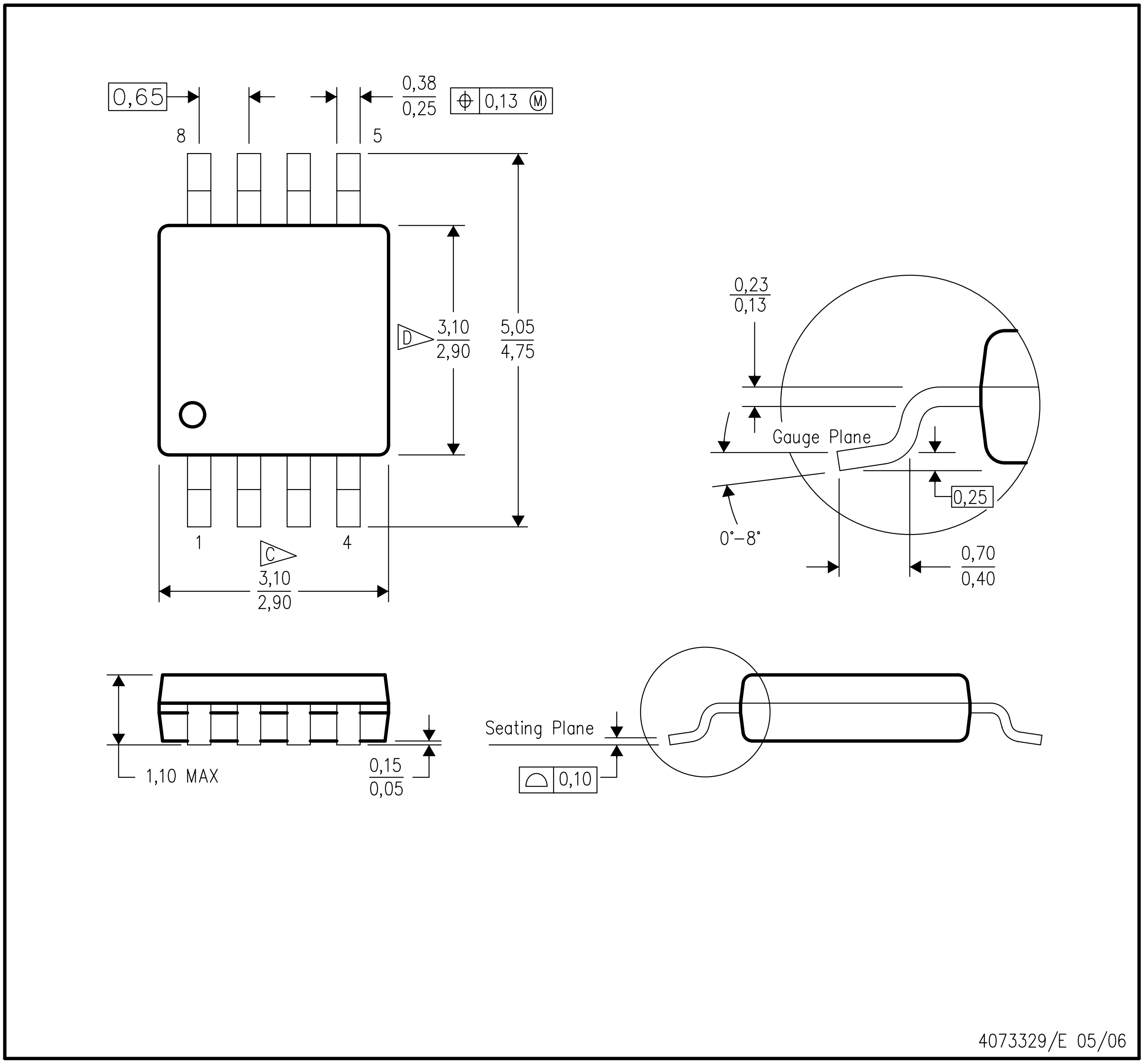
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
- E. Falls within JEDEC MO–178 Variation AB, except minimum lead width.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



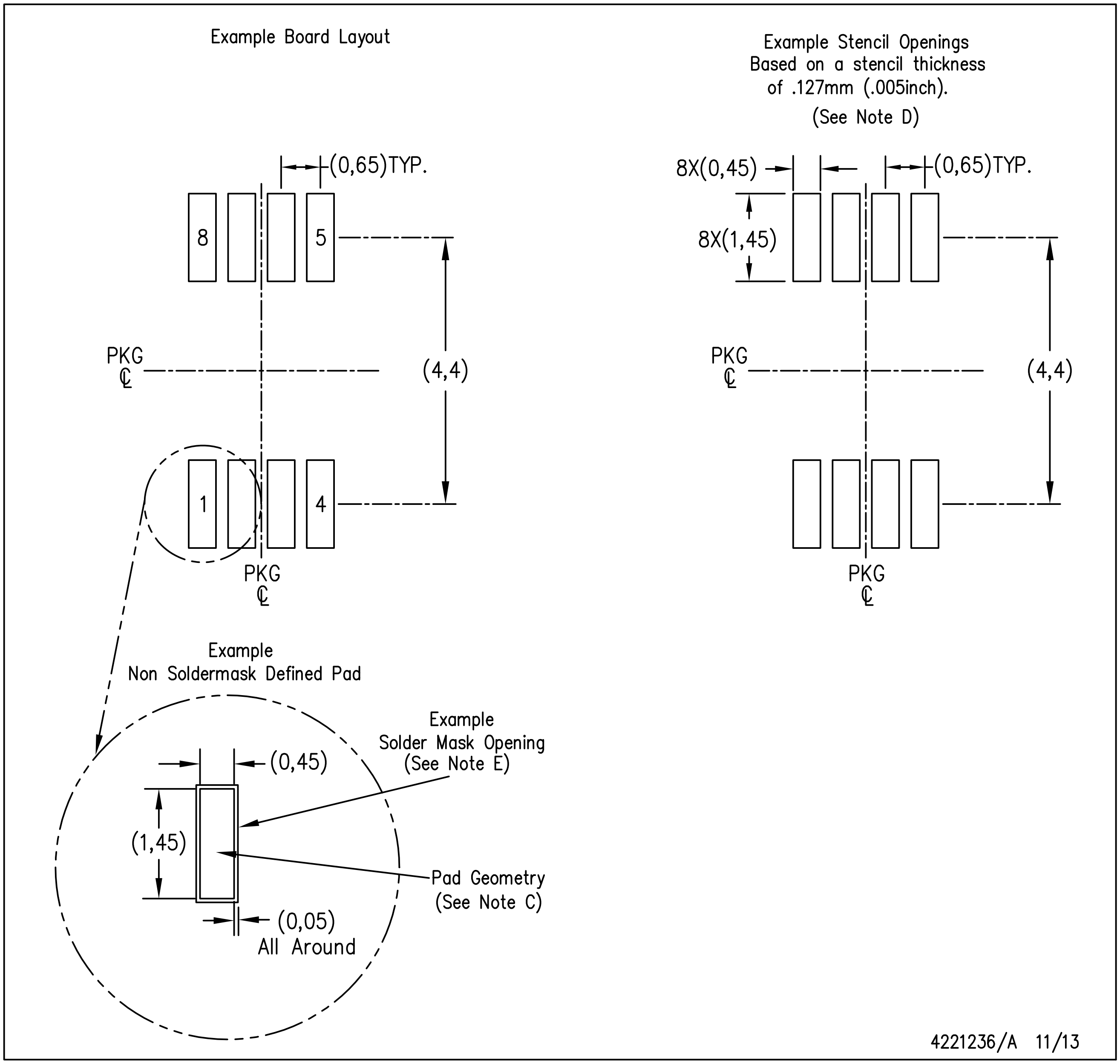
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS-012 variation AA.

DGK (S-PDSO-G8) PLASTIC SMALL-OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO-187 variation AA, except interlead flash.

DGK (S-PDSO-G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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