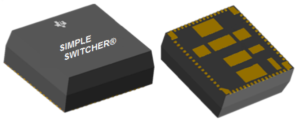


15mm x 16mm x 5.8mm

LMZ31520 20-A SIMPLE SWITCHER® Power Module With 3-V to 14.5-V Input in QFN Package

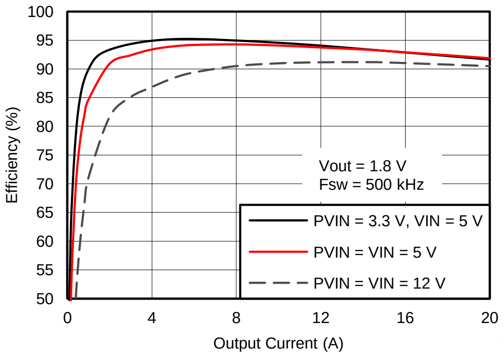
1 Features

- Complete Integrated Power Solution; Smaller than a Discrete Design
- 15 mm × 16 mm × 5.8 mm Package Size - Pin Compatible with LMZ31530
- Ultra-Fast Load Step Response
- Efficiencies Up To 96%
- Wide-Output Voltage Adjust 0.6 V to 3.6 V, with 1% Reference Accuracy
- Optional Split Power Rails Allows Input Voltage Down to 3 V
- Selectable Switching Frequency (300 kHz to 850 kHz)
- Selectable Slow-Start
- Adjustable Overcurrent Limit
- Power Good Output
- Output Voltage Sequencing
- Over Temperature Protection
- Pre-bias Output Start-up
- Operating Temperature Range: –40°C to 85°C
- Enhanced Thermal Performance: 8.6°C/W
- Meets EN55022 Class A Emissions - Integrated Shielded Inductor

2 Applications

- Broadband and Communications Infrastructure
- DSP and FPGA Point of Load Applications
- High Density Power Systems

Efficiency

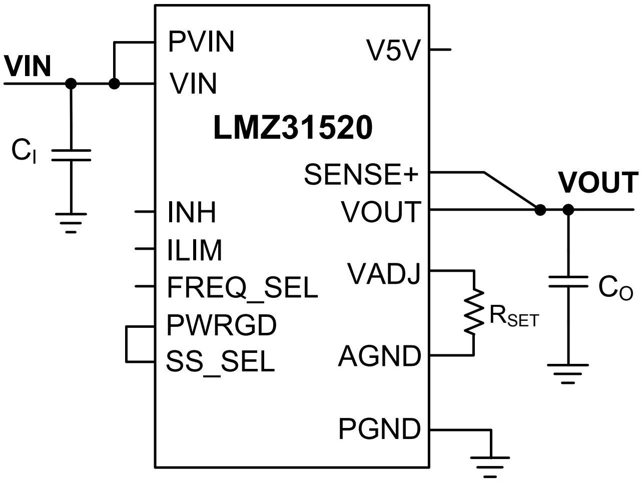


3 Description

The LMZ31520 SIMPLE SWITCHER® power module is an easy-to-use integrated power solution that combines a 20-A DC-DC converter with power MOSFETs, a shielded inductor, and passives into a low profile, QFN package. This total power solution allows as few as three external components and eliminates the loop compensation and magnetics part selection process.

The 15×16×5.8 mm QFN package is easy to solder onto a printed circuit board and allows a compact point-of-load design. Achieves greater than 95% efficiency, has ultra-fast load step response and excellent power dissipation capability with a thermal impedance of 8.6°C/W. The LMZ31520 offers the flexibility and the feature-set of a discrete point-of-load design and is ideal for powering a wide range of ICs and systems. Advanced packaging technology affords a robust and reliable power solution compatible with standard QFN mounting and testing techniques.

Simplified Application



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

3.1 Absolute Maximum Ratings(1)

over operating temperature range (unless otherwise noted)		VALUE		UNIT
		MIN	MAX	
Input Voltage	VIN, PVIN	–0.3	20	V
	INH, VADJ, PWRGD, PWRGD_PU, ILIM, FREQ_SEL, SS_SEL, V5V	–0.3	7	V
Output Voltage	PH	–1	25	V
	PH 10ns Transient	–2	27	
	VOUT	–0.3	6	V
V_{DIFF} (GND to exposed thermal pad)			±200	mV
Operating Junction Temperature		–40	125(2)	°C
Storage Temperature		–55	150	°C
Peak Reflow Case Temperature(3)			240	°C
Maximum Number of Reflows Allowed(3)			1	
Mechanical Shock	Mil-STD-883D, Method 2002.3, 1 msec, 1/2 sine, mounted		250	G
Mechanical Vibration	Mil-STD-883D, Method 2007.2, 20-2000Hz		20	

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) See the temperature derating curves in the Typical Characteristics section for thermal information.
(3) For soldering specifications, refer to the *Soldering Requirements for BQFN Packages* application note.

3.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
PV_{IN}	Input Switching Voltage	3	14.5	V
V_{IN}	Input Bias Voltage	4.5	14.5	V
V_{OUT}	Output Voltage	0.6	3.6	V
f_{SW}	Switching Frequency	300	850	kHz

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3.3 Thermal Information

THERMAL METRIC(1)			LMZ31520 RLG 72 PINS	UNIT
θ_{JA}	Junction-to-ambient thermal resistance(2)	Natural Convection	8.6	°C/W
$\theta_{JA(100LFM)}$	Junction-to-ambient thermal resistance(3)	100 LFM	7.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter(4)		1.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter(5)		4.2	°C/W

(1) For more information about traditional and new thermal metrics, see the*Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance, θ_{JA}, applies to devices soldered directly to a 100 mm x 100 mm, 6-layer PCB with 1 oz. copper and natural convection cooling. Additional airflow reduces θ_{JA}.
(3) The junction-to-ambient thermal resistance, θ_{JA}, applies to devices soldered directly to a 100 mm x 100 mm, 6-layer PCB with 1 oz. copper and 100 LFM forced air cooling. Additional airflow reduces θ_{JA}.
(4) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature, T_J, of a device in a real system, using a procedure described in JESD51-2A (sections 6 and 7). $T_J = \psi_{JT} * Pdis + T_T$; where Pdis is the power dissipated in the device and T_T is the temperature of the top of the device.
(5) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature, T_J, of a device in a real system, using a procedure described in JESD51-2A (sections 6 and 7). $T_J = \psi_{JB} * Pdis + T_B$; where Pdis is the power dissipated in the device and T_B is the temperature of the board 1mm from the device.

3.4 Package Specifications

LMZ31520		UNIT
Weight		4.96 grams
Flammability	Meets UL 94 V-O	
MTBF Calculated reliability	Per Bellcore TR-332, 50% stress, T_A = 40°C, ground benign	26.5 MHrs

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3.5 Electrical Characteristics

T_A = -40°C to 85°C, VIN = 12 V, VOUT = 1.8 V, I_{OUT} = 20A
C_{IN} = 2x 22 µF ceramic & 330 µF bulk, C_{OUT} = 4x 100 µF ceramic (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{OUT}	Output current			0		20	A
V_{IN}	Input bias voltage range	Over I_{OUT} range		4.5		14.5	V
P_{VIN}	Input switching voltage range	Over I_{OUT} range		3.0[1]		14.5	V
UVLO	VIN Undervoltage lockout	V_{IN} Increasing		4.0	4.2	4.33	V
		Hysteresis			0.25		
$V_{OUT(adj)}$	Output voltage adjust range	Over I_{OUT} range		0.6		3.6	V
V_{OUT}	Set-point voltage tolerance	I_{OUT} = 20 A, FCCM mode				±1.0% [2]	
	Temperature variation	-40°C ≤ T_A ≤ +85°C			±0.25%		
	Load regulation	Over I_{OUT} range			+0.3%		
	Total output voltage variation	Includes set-point, load, and temperature variation				±1.8% [2]	
	Line regulation	P_{VIN} ±10%			±0.1%		
		Over P_{VIN} range			±0.5%		
η	Efficiency	P_{VIN} = V_{IN} = 12 V I_O = 15 A	V_{OUT} = 3.3 V, f_{SW} = 500kHz		94		%
			V_{OUT} = 1.8 V, f_{SW} = 500kHz		92		
			V_{OUT} = 1.2 V, f_{SW} = 500kHz		88		
			V_{OUT} = 0.9 V, f_{SW} = 500kHz		86		
			V_{OUT} = 0.6 V, f_{SW} = 500kHz		82		
		P_{VIN} = V_{IN} = 5 V I_O = 15 A	V_{OUT} = 3.3 V, f_{SW} = 500kHz		96		%
			V_{OUT} = 1.8 V, f_{SW} = 500kHz		94		
			V_{OUT} = 1.2 V, f_{SW} = 500kHz		91		
			V_{OUT} = 0.9 V, f_{SW} = 500kHz		88		
			V_{OUT} = 0.6 V, f_{SW} = 500kHz		85		
	Output voltage ripple	20 MHz bandwith			1%		VOUT
I_{LIM}	Current limit threshold				30		A
	Transient response	2.5 A/µs load step from 25 to 75% $IOUT_{(max)}$	Recovery time		25		µs
			VOUT over/undershoot		25		mV
V_{INH}	Inhibit Control	Inhibit High Voltage		1.8		Open[3]	V
		Inhibit Low Voltage		-0.3		0.6	V
$I_{IN(stby)}$	VIN standby current	INH pin to AGND	V_{IN} = 5 V		0.5	0.7	mA
			V_{IN} = 12 V		1.2	1.5	mA
Power Good	PWRGD Thresholds	V_{OUT} rising	Good		95		%
			Fault		115		
		V_{OUT} falling	Fault		90		
			Good		110		
	PWRGD Low Voltage	I(PWRGD) = 2 mA			0.2	0.3	V
f_{SW}	Switching frequency	FREQ_SEL pin OPEN, I_{OUT} = 10 A		470	520	570	kHz
f_{SEL}	Frequency Select[4]	66 kΩ resistor between FREQ_SEL pin and PGND			300		kHz
		FREQ_SEL pin connected to V5V (pin 61)			850		kHz
	Thermal Shutdown	Thermal shutdown			145		°C
		Thermal shutdown hysteresis			10		°C
C_{IN}	External input capacitance	Ceramic		44 [5]	94		µF
		Non-ceramic			330		

(1) The minimum PVIN voltage is 3.0V or (V_{OUT}+ 1.1V), whichever is greater. See VIN and PVIN Input Voltage for more details.
(2) The stated limit of the set-point voltage tolerance includes the tolerance of both the internal voltage reference and the internal adjustment resistor. The overall output voltage tolerance will be affected by the tolerance of the external R_{SET} resistor.
(3) This pin has an internal pull-up to approximately 0.4 x V_{IN}. If this pin is left open circuit, the device operates when a valid input voltage is applied. A small, low-leakage (<300nA) MOSFET is recommended for control.
(4) See the Frequency Select section for more information on selecting the frequency.
(5) A minimum of 44 µF (2x 22 µF) of external ceramic capacitance is required across the input (PVIN/VIN and PGND connected) for proper operation. Locate the capacitor close to the device. See Table 3 for more details. When operating with split VIN and PVIN rails, place 4.7 µF of ceramic capacitance directly at the VIN pin to PGND.

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Electrical Characteristics (continued)

T_A = -40°C to 85°C, VIN = 12 V, VOUT = 1.8 V, I_{OUT} = 20A
C_{IN} = 2x 22 µF ceramic & 330 µF bulk, C_{OUT} = 4x 100 µF ceramic (unless otherwise noted)

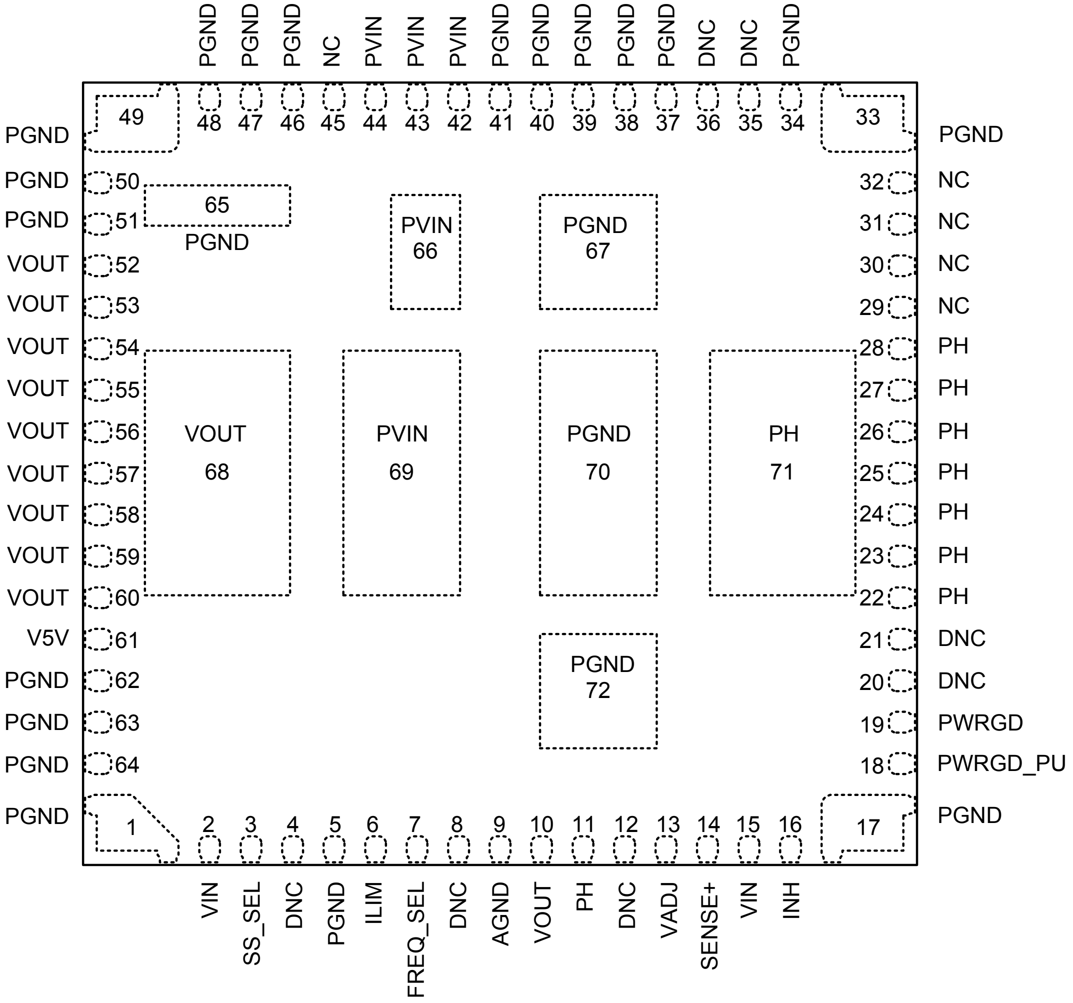
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{OUT}	External output capacitance		100 (6)	400	5000	µF

---

(6) A minimum of 100 µF of ceramic capacitance is required at the output. Locate the capacitance close to the device. Adding additional capacitance close to the load improves the response of the regulator to load transients and reduces ripple. See Table 3 for more details.

4 Device Information

RLG PACKAGE
(TOP VIEW)



Pin Functions

TERMINAL		DESCRIPTION
NAME	NO.	
AGND	9	This pin is connected internally to the power ground of the device. This pin should only be used as the zero volt ground reference for connecting the voltage setting resistor (R_{SET}). Do not connect AGND to PGND. See Layout Recommendations.
DNC	4 8 12 20 21 35 36	Do Not Connect. Do not connect these pins to AGND, to another DNC pin, or to any other voltage. These pins are connected to internal circuitry. Each pin must be soldered to an isolated pad.
FREQ_SEL	7	Frequency Select pin. Leave this pin open (floating) to select 500 kHz (typ) operating frequency. Connect this pin to V5V pin to select 850 kHz (typ) operating frequency. Connect a 66 kΩ resistor between this pin and PGND to select 300 kHz (typ) operating frequency. See Table 2 for more info.
ILIM	6	Current limit setting pin. Connecting a resistor between this pin and PGND sets the current limit. When left open, refer to the Electrical Characterization table for current limit value.
INH	16	Inhibit pin. Use an open drain or open collector logic device to ground this pin to control the INH function.
NC	29 30 31 32 45	Not Connected. These pins are internally isolated from any signal and all other pins. Each pin must be soldered to a pad on the PCB. These pins can be left isolated, connected to one another, or connected to any signal on the PCB.
PGND	1 5 17 33 34 37 38 39 40 41 46 47 48 49 50 51 62 63 64 65 67 70 72	This is the return current path for the power stage of the device. Connect these pins to the load and to the bypass capacitors associated with VIN and VOUT. Pads 65, 67, 70, and 72 should be connected to PCB ground planes using multiple vias for good thermal performance. Not all pins are connected together internally. All pins must be connected together externally with a copper plane or pour directly under the device.

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Pin Functions (continued)

TERMINAL		DESCRIPTION
NAME	**NO.**	
PH	11 22 23 24 25 26 27 28 71	Phase switch node. Do not place any external component on these pins or tie them to a pin of another function. Connect these pins using a copper area beneath pad 71.
PVIN	42 43 44 66 69	Input switching voltage pin. This pin supplies voltage to the power switches of the converter.
PWRGD	19	Power Good flag pin. This open drain output asserts low if the output voltage is more than approximately ±6% out of regulation.
PWRGD_PU	18	Power Good pull-up pin. This pin is connected to a 100kΩ resistor which is tied to the PWRGD pin internally. Connect this pin to V5V or to any voltage between 1.3V and 6.5V.
SENSE+	14	Remote sense connection. Connect this pin to VOUT at the load for improved regulation. This pin must be connected to VOUT at the load, or at the module pins.
SS_SEL	3	Slow-start select pin. Connect a resistor between this pin and PWRGD (or PGND) to select the slow-start time. See the SS_SEL section of the datasheet for slow-start times and corresponding resistor values. Connect the SS_SEL pin to PGND to select Auto-skip Eco-mode or to the PWRGD pin (pin 19) to select FCCM.
V5V	61	5V regulator pin. This regulator supplies the internal circuitry.
VADJ	13	Output voltage adjust pin. Connecting a resistor between this pin and AGND sets the output voltage.
VIN	2 15	Input bias voltage pins. Supplies the control circuitry of the power converter.
VOUT	10 52 53 54 55 56 57 58 59 60 68	Output voltage. These pins are connected to the internal output inductor. Connect these pins to the output load and connect external bypass capacitors between these pins and PGND.

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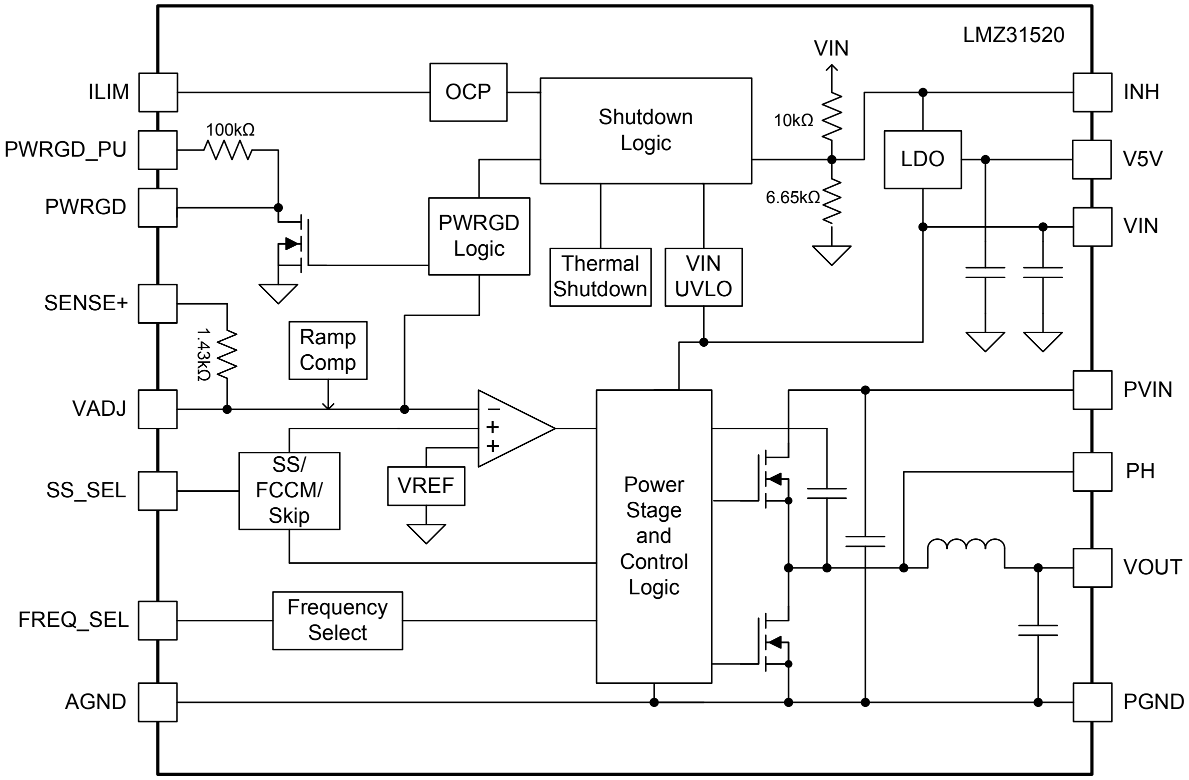
Functional Block Diagram



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5 Typical Characteristics (PVIN = VIN = 12 V) (1) (2)

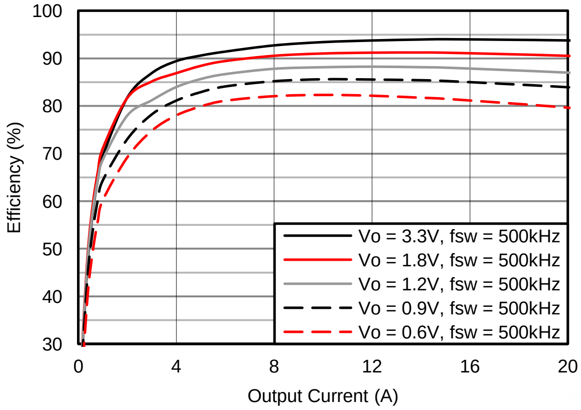

Figure 1. Efficiency vs. Output Current

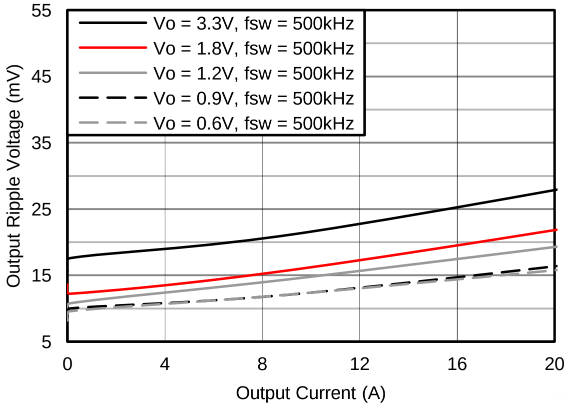

Figure 2. Voltage Ripple vs. Output Current

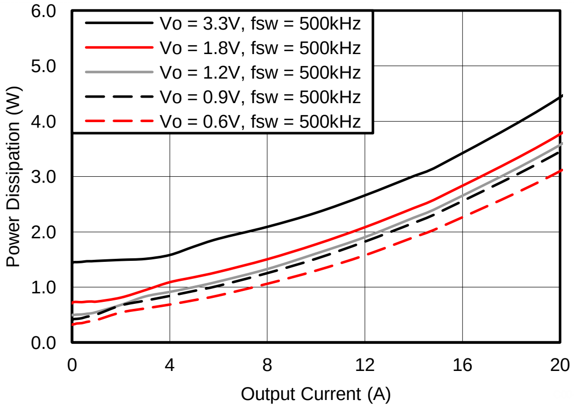

Figure 3. Power Dissipation vs. Output Current

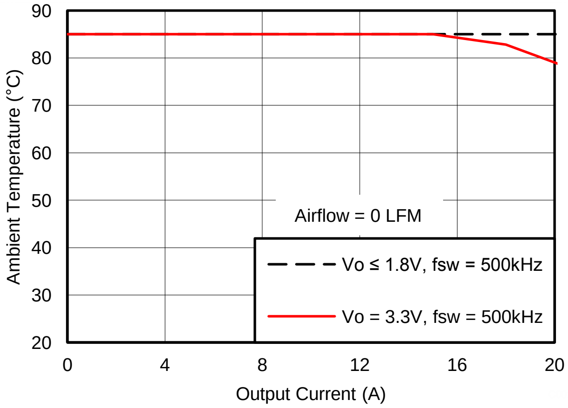

Figure 4. Safe Operating Area (0 LFM)

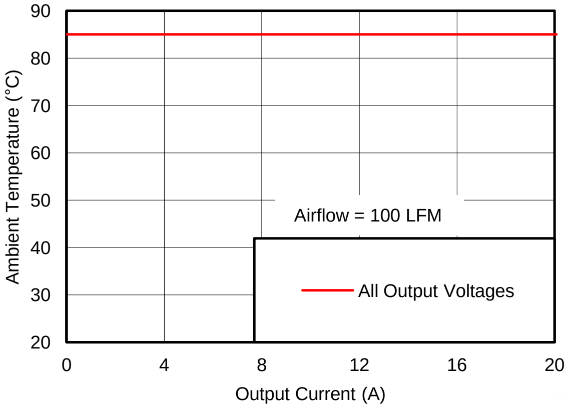

Figure 5. Safe Operating Area (100 LFM)

(1) The electrical characteristic data has been developed from actual products tested at 25°C. This data is considered typical for the converter. Applies to Figure 1, Figure 2, and Figure 3.

(2) The temperature derating curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to devices soldered directly to a 100 mm × 100 mm six-layer PCB with 1 oz. copper. Applies to Figure 4 and Figure 5.

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6 Typical Characteristics (PVIN = VIN = 5 V) (1) (2)

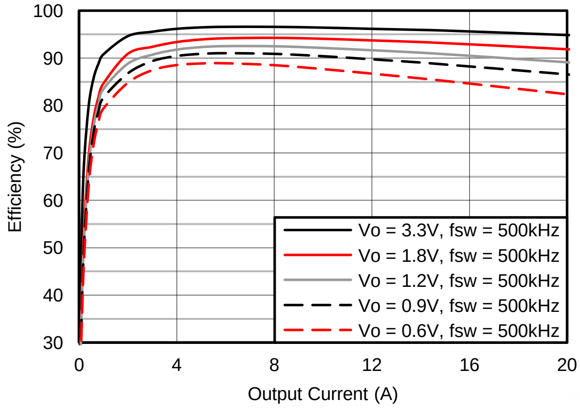

Figure 6. Efficiency vs. Output Current

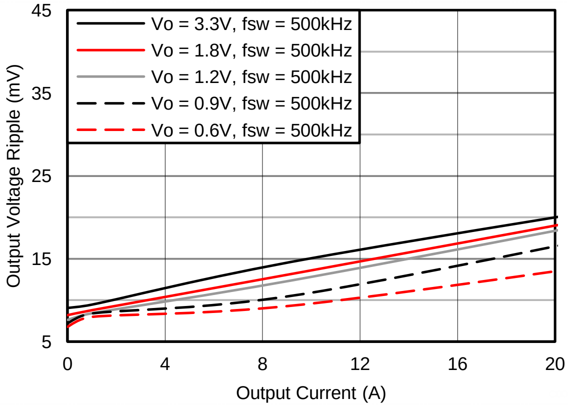

Figure 7. Voltage Ripple vs. Output Current

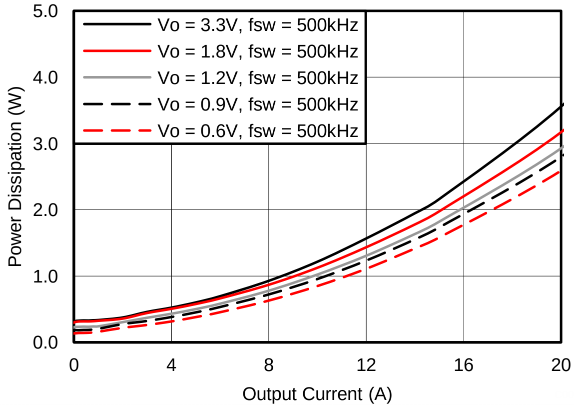

Figure 8. Power Dissipation vs. Output Current

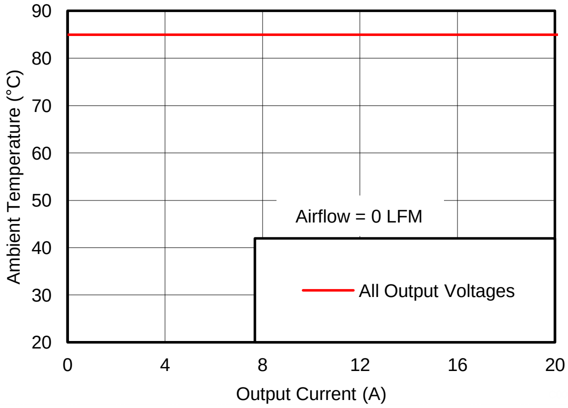

Figure 9. Safe Operating Area (0 LFM)

(1) The electrical characteristic data has been developed from actual products tested at 25°C. This data is considered typical for the converter. Applies to Figure 6, Figure 7, and Figure 8.

(2) The temperature derating curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to devices soldered directly to a 100 mm × 100 mm six-layer PCB with 1 oz. copper. Applies to Figure 9.

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7 Application Information

7.1 Adjusting the Output Voltage

The VADJ control sets the output voltage of the LMZ31520. The output voltage adjustment range is from 0.6V to 3.6V. The adjustment method requires the addition of R_{SET}, which sets the output voltage, and the connection of SENSE+ to VOUT. The R_{SET} resistor must be connected directly between the VADJ (pin 13) and AGND (pin 9). The SENSE+ pin (pin 14) must be connected to VOUT either at the load for improved regulation or at VOUT of the device.

The LMZ31520 relies on a precision trimmed 0.6 V reference for the feedback voltage regulation and operates by regulating the valley of the voltage ripple appearing at the VADJ pin. The voltage ripple is a function of the input voltage and the output voltage, therefore the R_{SET} resistor will change based on the input voltage. Table 1 gives the calculated external R_{SET} resistor for a number of common bus voltages for PVIN of 12 V, 5 V, and 3.3 V. The recommended switching frequency is 500 kHz which can be configured by leaving the FREQ_SEL pin open. To adjust the frequency, see Table 2.

Table 1. R_{SET} Resistor Values

	R_{SET} (Ω)		
V_{OUT} (V)	**PVIN = 12 V**	**PVIN = 5 V**	**PVIN = 3.3 V**
0.60	open	open	open
0.65	18787	18681	18588
0.70	9024	8993	8966
0.75	5939	5923	5908
0.80	4427	4416	4406
0.85	3529	3521	3513
0.90	2934	2927	2921
0.95	2511	2505	2500
1.00	2195	2190	2185
1.05	1950	1945	1941
1.10	1754	1749	1745
1.15	1594	1589	1586
1.20	1460	1456	1453
1.25	1348	1344	1341
1.30	1251	1248	1244
1.35	1168	1164	1161
1.40	1095	1091	1088
1.45	1031	1027	1024
1.50	973	970	968
1.55	922	919	916
1.60	876	873	870
1.65	834	831	828
1.70	797	793	790
1.75	762	759	756
1.80	730	727	724
1.85	701	698	695
1.90	674	671	668
1.95	650	646	643
2.00	626	623	620
2.05	605	602	599
2.10	585	581	578
2.15	566	563	560
2.20	548	545	542
2.25	532	528	525
2.30	516	513	510
2.35	502	498	495
2.40	488	484	481
2.45	475	471	468
2.50	462	459	456
2.55	451	447	444
2.60	439	436	433
2.65	429	425	422
2.70	419	415	412
2.75	409	405	402
2.80	400	396	393
2.85	391	387	384
2.90	382	379	375
2.95	374	370	367
3.00	367	363	359
3.05	359	355	352
3.10	352	348	345
3.15	345	341	338
3.20	339	335	331
3.25	332	328	325
3.30	326	322	318
3.35	320	316	312
3.40	315	310	307
3.45	309	305	301
3.50	304	300	296
3.55	299	294	291
3.60	294	289	286

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7.2 Frequency Select

The LMZ31520 switching frequency can be selected from several values as shown in Table 2. To select a switching frequency, a resistor (R_{FREQ}) must be connected between the FREQ_SEL pin and either PGND or V5V (pin 61) as shown in Table 2. For all output voltages, the recommended switching frequency is 500 kHz which can be configured by leaving the FREQ_SEL pin open. Table 2 also shows the output voltage range for each frequency.

Table 2. Frequency Selection

Frequency Select (kHz)	R_{FREQ} (kΩ)	Connect To	V_{OUT} RANGE (V)	
			MIN	MAX
300	66	PGND	0.6	3.6
400	498	PGND	0.6	3.6
500	open	-	0.6	3.6
650	745	V5V	0.8	3.6
750	188	V5V	1.0	3.6
850	short	V5V	1.2	3.6

7.3 Capacitor Recommendations for the LMZ31520 Power Supply

7.3.1 Capacitor Technologies

7.3.1.1 Electrolytic, Polymer-Electrolytic Capacitors

Aluminum electrolytic capacitors provide adequate decoupling over the frequency range of 2 kHz to 150 kHz. When using electrolytic capacitors, high-quality, polymer-electrolytic capacitors are recommended. Polymer-electrolytic type capacitors are recommended for applications where the ambient operating temperature is less than 0°C. The Panasonic OS-CON capacitor series is suggested due to the lower ESR, higher rated surge, power dissipation, ripple current capability, and small package size.

7.3.1.2 Ceramic Capacitors

The performance of ceramic capacitors is most effective above 150 kHz. Multilayer ceramic capacitors have a low ESR and a resonant frequency higher than the bandwidth of the regulator. They can be used to reduce the reflected ripple current at the input as well as improve the transient response of the output.

7.3.1.3 Tantalum, Polymer-Tantalum Capacitors

Polymer-tantalum type capacitors are recommended for applications where the ambient operating temperature is less than 0°C. The Panasonic POSCAP series and Kemet T530 capacitor series are recommended rather than many other tantalum types due to their lower ESR, higher rated surge, power dissipation, ripple current capability, and small package size. Tantalum capacitors that have no stated ESR or surge current rating are not recommended for power applications.

7.3.1.4 Input Capacitor

The LMZ31520 requires a minimum input capacitance of 44 µF of ceramic type. The voltage rating of input capacitors must be greater than the maximum input voltage. The input RMS ripple current is a function of the output current and the duty cycle for any application. The input capacitor must be rated for the application's RMS ripple current. Table 3 includes a preferred list of capacitors by vendor.

7.3.1.5 Output Capacitor

The required output capacitance of the LMZ31520 can be comprised of either all ceramic capacitors, or a combination of ceramic and bulk capacitors. The required output capacitance must include at least 100 µF of ceramic type. When adding additional non-ceramic bulk capacitors, low-ESR devices like the ones recommended in Table 3 are required. The required capacitance above the minimum is determined by actual transient deviation requirements. See Table 4 for typical transient response values for several output voltage, input voltage and capacitance combinations. Table 3 includes a preferred list of capacitors by vendor.

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Capacitor Recommendations for the LMZ31520 Power Supply (continued)

Table 3. Recommended Input/Output Capacitors(1)

VENDOR	SERIES	PART NUMBER	CAPACITOR CHARACTERISTICS		
			WORKING VOLTAGE (V)	CAPACITANCE (µF)	ESR (2) (mΩ)
Murata	X5R	GRM32ER61E226K	25	22	2
TDK	X5R	C3216X5R1E476M	25	47	2
TDK	X5R	C3216X5R1C476M	16	47	2
Murata	X5R	GRM32ER61C476M	16	47	2
TDK	X5R	C3225X5R0J107M	6.3	100	2
Murata	X5R	GRM32ER60J107M	6.3	100	2
TDK	X5R	C3225X5R0J476K	6.3	47	2
Murata	X5R	GRM32ER60J476M	6.3	47	2
Panasonic	EEH-ZA	EEH-ZA1E101XP	25	100	30
Kemet	T520	T520V107M010ASE025	10	100	25
Panasonic	POSCAP	6TPE100MI	6.3	100	25
Panasonic	POSCAP	2R5TPE220M7	2.5	220	7
Kemet	T530	T530D227M006ATE006	6.3	220	6
Kemet	T530	T530D337M006ATE010	6.3	330	10
Panasonic	POSCAP	2TPF330M6	2.0	330	6
Panasonic	POSCAP	6TPE330MFL	6.3	330	15

(1) **Capacitor Supplier Verification, RoHS, Lead-free and Material Details**
Consult capacitor suppliers regarding availability, material composition, RoHS and lead-free status, and manufacturing process requirements for any capacitors identified in this table.
(2) Maximum ESR @ 100kHz, 25°C.

7.4 Transient Response

The LMZ31520 is designed to have an ultra-fast load step response with minimal output capacitance. Table 4 shows the voltage deviation and recovery time for several different transient conditions. Several transient waveforms are shown in Application Curves (1).

Table 4. Output Voltage Transient Response

C_{IN1} = 3 x 47 µF CERAMIC						
V_{OUT} (V)	V_{IN} (V)	C_{OUT1} Ceramic	C_{OUT2} BULK	VOLTAGE DEVIATION (mV)		RECOVERY TIME (µs)
				5 A LOAD STEP, (1 A/µs)	10 A LOAD STEP, (1 A/µs)	
0.6	5	500 µF	-	8	15	35
	12	500 µF	-	8	15	35
0.9	5	500 µF	-	8	15	40
		500 µF	470 µF	6	12	40
	12	500 µF	-	8	20	40
		500 µF	470 µF	7	16	40
1.2	5	500 µF	-	10	20	40
		500 µF	330 µF	8	15	40
	12	500 µF	-	10	20	40
		500 µF	330 µF	8	16	40
1.8	5	500 µF	-	10	20	40
		500 µF	330 µF	8	16	40
	12	500 µF	-	10	20	40
		500 µF	330 µF	8	16	45
3.3	5	500 µF	-	12	25	50
	12	500 µF	-	12	25	50

(1) Device configured for FCCM mode of operation, (pin 3 connected to pin 19).

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7.5 Application Curves (1)

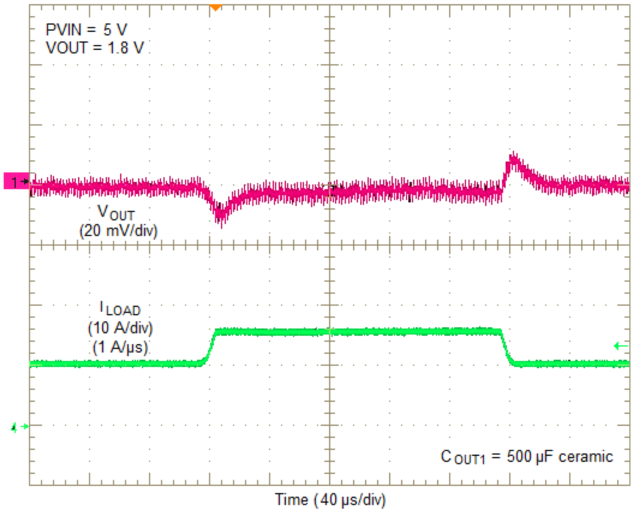

Figure 10. PVIN = 5V, VOUT = 1.8V, 5A Load Step

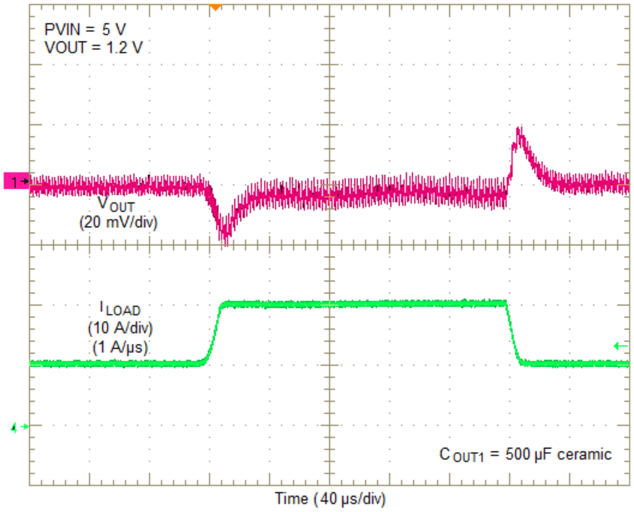

Figure 11. PVIN = 5V, VOUT = 1.2V, 10A Load Step

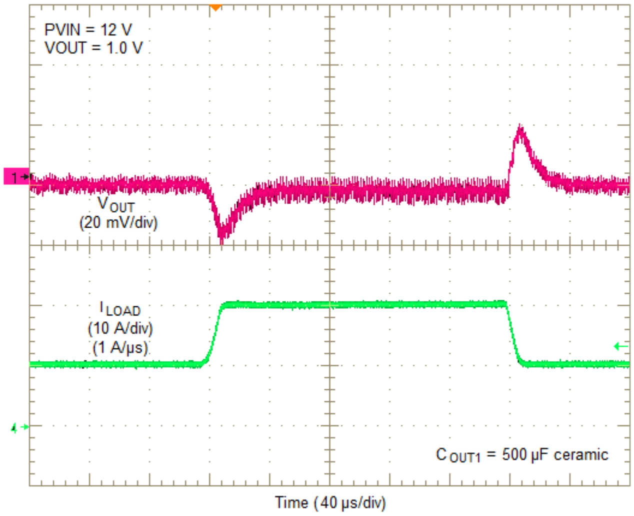

Figure 12. PVIN = 12V, VOUT = 1.0V, 10A Load Step

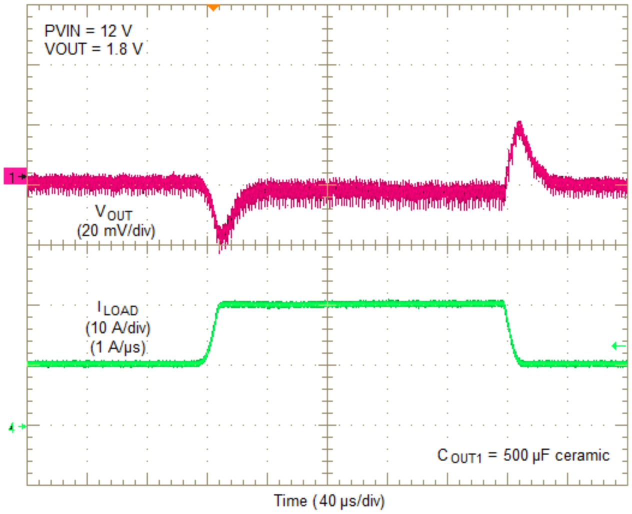

Figure 13. PVIN = 12V, VOUT = 1.8V, 10A Load Step

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(1) Device configured for FCCM mode of operation, (pin 3 connected to pin 19).

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7.6 Application Schematics

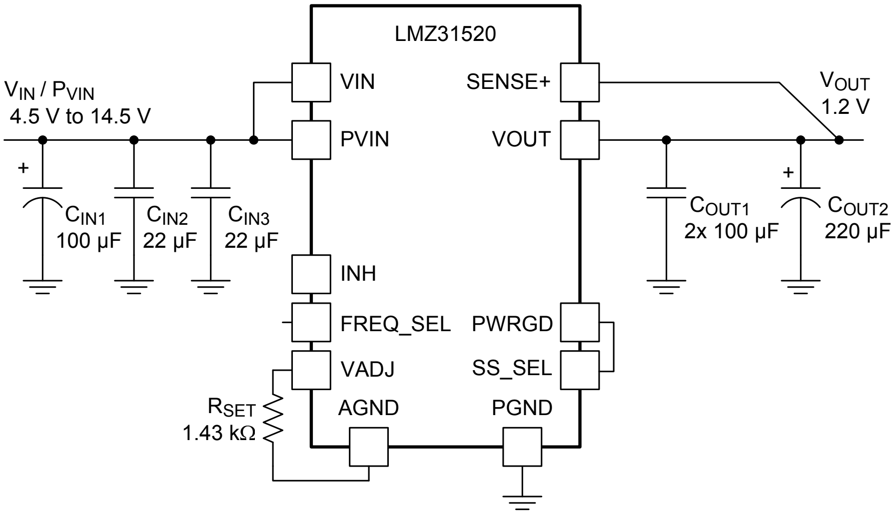

Figure 14. Typical Schematic
PVIN = VIN = 4.5 V to 14.5 V, VOUT = 1.2 V

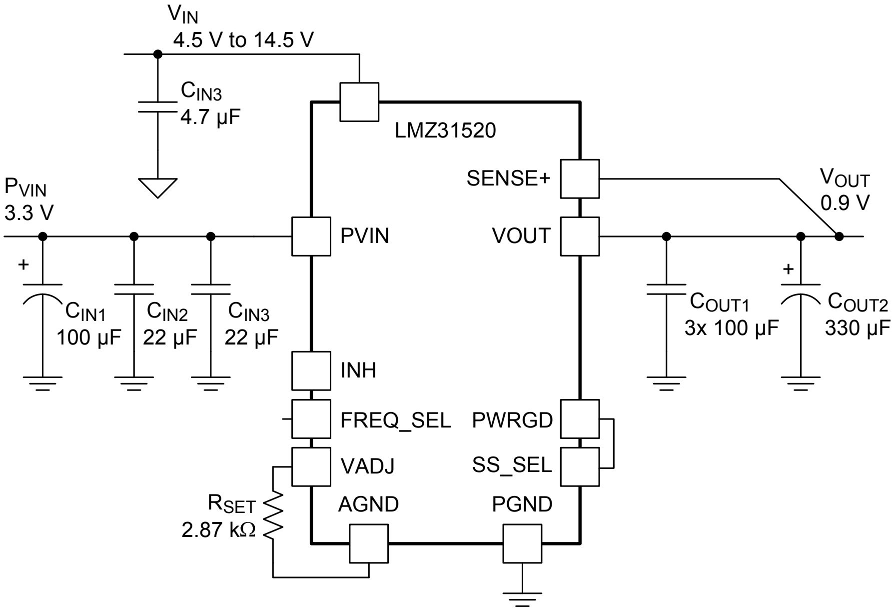

Figure 15. Typical Schematic
PVIN = 3.3 V, VIN = 4.5 V to 14.5 V, VOUT = 0.9 V

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7.7 VIN and PVIN Input Voltage

The LMZ31520 allows for a variety of applications by using the VIN and PVIN pins together or separately. The VIN voltage supplies the internal control circuits of the device. The PVIN voltage provides the input voltage to the power converter system.

If tied together, the input voltage for the VIN pin and the PVIN pin can range from 4.5 V to 14.5 V. If using the VIN pin separately from the PVIN pin, the VIN pin must be greater than 4.5 V, and the PVIN pin can range from as low as 3.0 V to 14.5 V. When operating from a split rail, it is recommended to supply VIN from 5 V to 12 V, for best performance.

7.8 3.3 V PVIN Operation

Applications operating from a PVIN of 3.3 V must provide at least 4.5 V for VIN. It is recommended to supply VIN from 5 V to 12 V, for best performance. See application note, SNVA692 for help creating 5 V from 3.3 V using a small, simple charge pump device.

7.9 Power Good (PWRGD)

The PWRGD pin is an open drain output. Once the voltage on the SENSE+ pin is between 90% and 115% of the set voltage, the PWRGD pin pull-down is released and the pin floats. The recommended pull-up resistor value is between 10 kΩ and 100 kΩ to a voltage source that is less than 7 V. An internal 100 kΩ pull-up resistor is provided internal to the device between the PWRGD pin (pin 19) and PWRGD_PU pin (pin 18). The PWRGD_PU pin can be connected to a voltage source less than 7 V or connected directly to V5V (pin 61), which is an internal 5V regulator. The PWRGD pin is in a defined state once VIN is greater than 1.0 V. The PWRGD pin is pulled low when the voltage on SENSE+ is lower than 90% or greater than 115% of the nominal set voltage. Also, the PWRGD pin is pulled low if the input UVLO or thermal shutdown is asserted or the INH pin is pulled low.

7.10 Slow Start (SS_SEL)

Connecting the SS_SEL pin to PWRGD or PGND sets the slow start interval of approximately 0.7 ms. The connection to either PWRGD or PGND determines the mode of the LMZ31520 as decribed in Auto-Skip Eco-Mode™ / Forced Continuous Conduction Mode. Adding a resistor between SS_SEL pin and PWRGD or PGND increases the slow start time. Increasing the slow start time will reduce inrush current.Table 5 shows a resistor connected between SS_SEL pin and PWRGD to select FCCM and Figure 17 shows a resistor between SS_SEL pin and PGND to select Auto-skip mode. See Table 5 below for SS resistor values and timing interval.

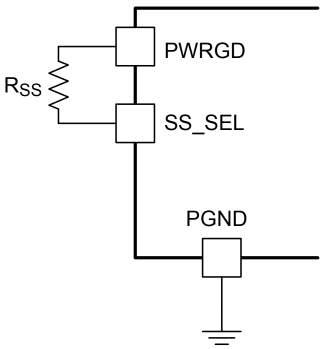

Figure 16. Slow-Start Resistor (R_{SS}) in FCCM

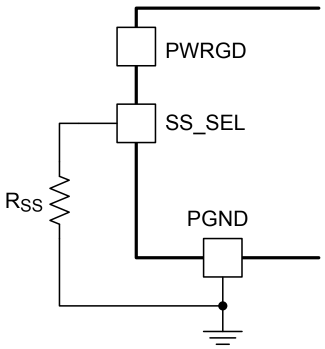

Figure 17. Slow-Start Resistor (R_{SS}) in Auto-skip Mode

Table 5. Slow-Start Resistor Values and Slow-Start Time

R_{SS} (kΩ)	short	61.9	161	436
SS Time (msec)	0.7	1.4	2.8	5.6

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7.11 Auto-Skip Eco-Mode™ / Forced Continuous Conduction Mode

Auto-skip Eco-mode or Forced Continuous Conduction Mode (FCCM) can be selected using the SS_SEL pin (pin 3). Connect the SS_SEL pin to PGND to select Auto-skip Eco-mode or to the PWRGD pin to select FCCM.

In Auto-skip Eco-mode, the LMZ31520 automatically reduces the switching frequency at light load conditions to maintain high efficiency. In FCCM, the controller keeps continuous conduction mode in light load condition and the switching frequency is kept almost constant over the entire load range. Transient performance is best in FCCM.

7.12 Power-Up Characteristics

When configured as shown in the front page schematic, the LMZ31520 produces a regulated output voltage following the application of a valid input voltage. During the power-up, internal soft-start circuitry slows the rate that the output voltage rises, thereby limiting the amount of in-rush current that can be drawn from the input source. Figure 18 shows the start-up waveforms for a LMZ31520, operating from a 5-V input (PVIN=VIN) and with the output voltage adjusted to 1.8 V. Figure 19 shows the start-up waveforms for a LMZ31520 starting up into a pre-biased output voltage. The waveforms were measured with a 15-A constant current load.

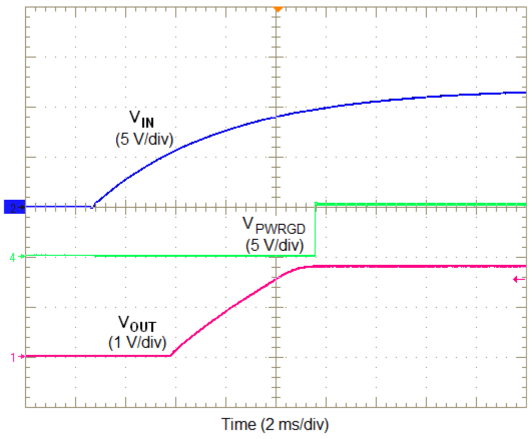

Figure 18. Start-Up Waveforms

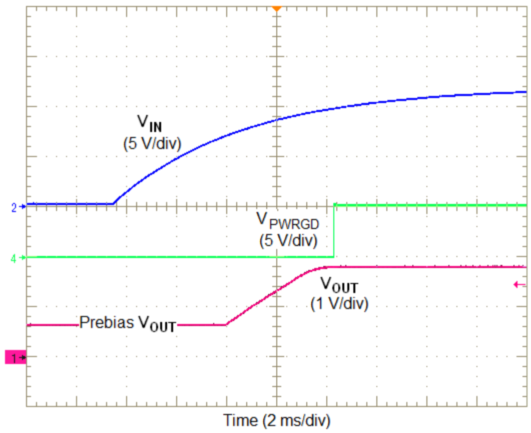

Figure 19. Start-up into Pre-bias

7.13 Pre-Biased Start-Up

The LMZ31520 has been designed to prevent the low-side MOSFET from discharging a pre-biased output. During pre-biased startup, the low-side MOSFET does not turn on until the high-side MOSFET has started switching. The high-side MOSFET does not start switching until the slow start voltage exceeds the voltage on the VADJ pin. Refer to Figure 19.

7.14 Remote Sense

The SENSE+ pin must be connected to V_{OUT} at the load, or at the device pins.

Connecting the SENSE+ pin to V_{OUT} at the load improves the load regulation performance of the device by allowing it to compensate for any I-R voltage drop between its output pins and the load. An I-R drop is caused by the high output current flowing through the small amount of pin and trace resistance. This should be limited to a maximum of 300 mV.

NOTE

The remote sense feature is not designed to compensate for the forward drop of nonlinear or frequency dependent components that may be placed in series with the converter output. Examples include OR-ing diodes, filter inductors, ferrite beads, and fuses. When these components are enclosed by the SENSE+ connection, they are effectively placed inside the regulation control loop, which can adversely affect the stability of the regulator.

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7.15 Output On/Off Inhibit (INH)

The INH pin provides electrical on/off control of the device. Once the INH pin voltage exceeds the threshold voltage, the device starts operation. If the INH pin voltage is pulled below the threshold voltage, the regulator stops switching and enters low quiescent current state.

The INH pin has an internal pull-up current source, allowing the user to float the INH pin for enabling the device. If an application requires controlling the INH pin, use an open drain/collector device, or a suitable logic gate to interface with the pin.

Figure 20 shows the typical application of the inhibit function. The Inhibit control has its own internal pull-up to VIN potential. An open-collector or open-drain device is recommended to control this input.

Turning Q1 on applies a low voltage to the inhibit control (INH) pin and disables the output of the supply, shown in Figure 21. If Q1 is turned off, the supply executes a soft-start power-up sequence, as shown in Figure 22. A regulated output voltage is produced within 2 ms. The waveforms were measured with a 5-A constant current load.

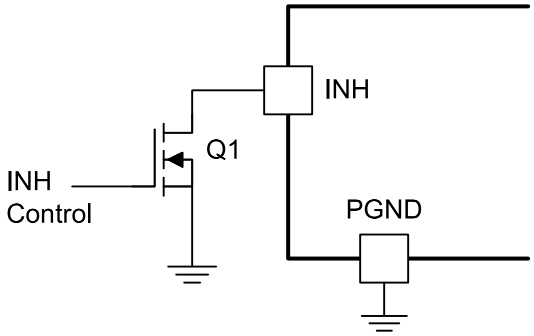

Figure 20. Typical Inhibit Control

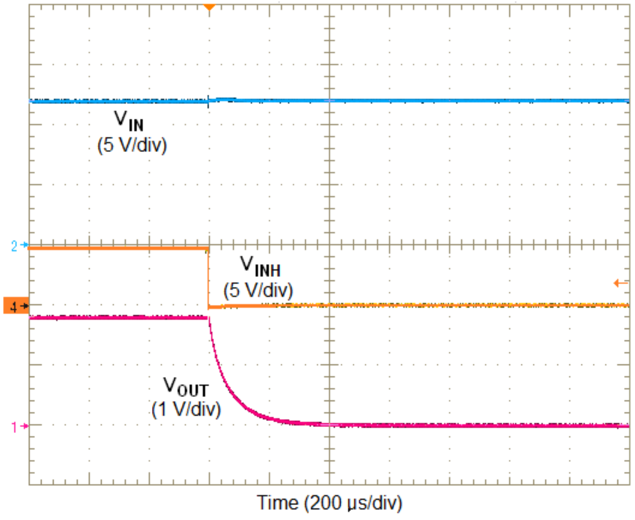

Figure 21. Inhibit Turn-Off

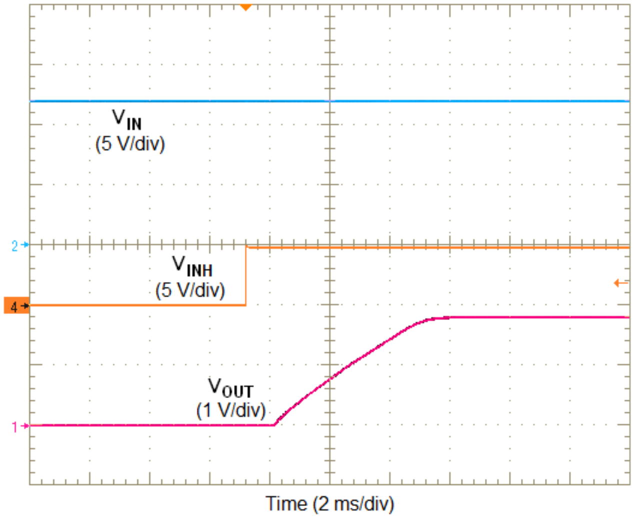

Figure 22. Inhibit Turn-On

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7.16 Overcurrent Protection

For protection against load faults, the LMZ31520 incorporates cycle-by-cycle overcurrent limiting control. The inductor current is monitored during the OFF state and the controller maintains the OFF state during the period in that the inductor current is larger than the overcurrent trip level. In cycle-by-cycle mode, applying a load that exceeds the regulator's overcurrent threshold limits the output current and reduces the output voltage as shown in Figure 23. If the overcurrent condition remains and the output voltage drops below 70% of the set-point, the LMZ31520 shuts down. Following shutdown, the module periodically attempts to recover by initiating a soft-start power-up as shown in Figure 23. This is described as a hiccup mode of operation, whereby the module continues in a cycle of successive shutdown and power up until the load fault is removed. During this period, the average current flowing into the fault is significantly reduced which reduces power dissipation. Once the fault is removed, the module automatically recovers and returns to normal operation as shown in Figure 24.

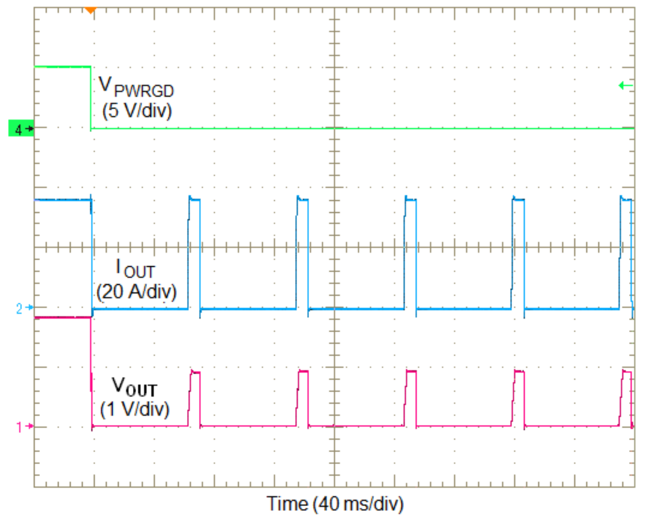

Figure 23. Typical Overcurrent Limiting

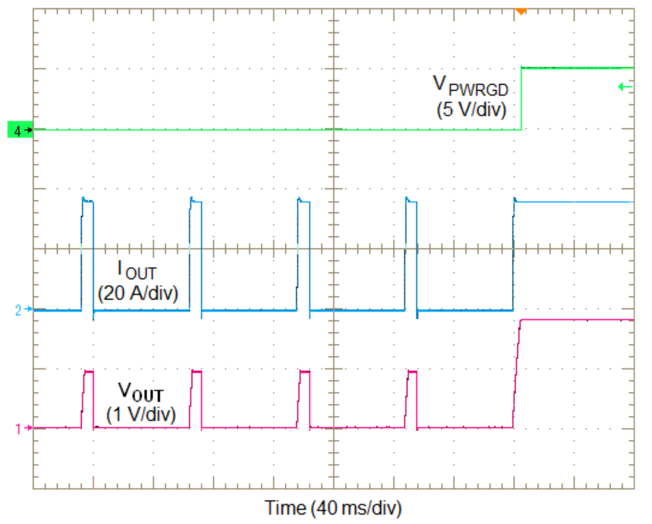

Figure 24. Typical Removal of Overcurrent

7.17 Current Limit (ILIM) Adjust

The current limit of this device can be adjusted lower by connecting a resistor, R_{ILIM}, between the ILIM pin (pin 6) and PGND. To adjust the typical current limit threshold, as listed in the electrical characteristics table, refer to Table 6.

Table 6. Current Limit Adjust Resistor

Current Limit Reduction	R_{ILIM} (kΩ)
10 %	715
20 %	383
30 %	243

7.18 Thermal Shutdown

The internal thermal shutdown circuitry forces the device to stop switching if the junction temperature exceeds 145°C typically. The device reinitiates the power up sequence when the junction temperature drops below 135°C typically.

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7.19 Layout Considerations

To achieve optimal electrical and thermal performance, an optimized PCB layout is required. Figure 25 thru Figure 30, shows a typical PCB layout. Some considerations for an optimized layout are:

- Use large copper areas for power planes (PVIN, VOUT, and PGND) to minimize conduction loss and thermal stress.
- Place ceramic input and output capacitors close to the device pins to minimize high frequency noise.
- Locate additional output capacitors between the ceramic capacitor and the load.
- Keep AGND and PGND separate from one another. AGND should only be used as the return for R_{SET}.
- Place R_{SET}, R_{FREQ}, and R_{SS} as close as possible to their respective pins.
- Use multiple vias to connect the power planes to internal layers.

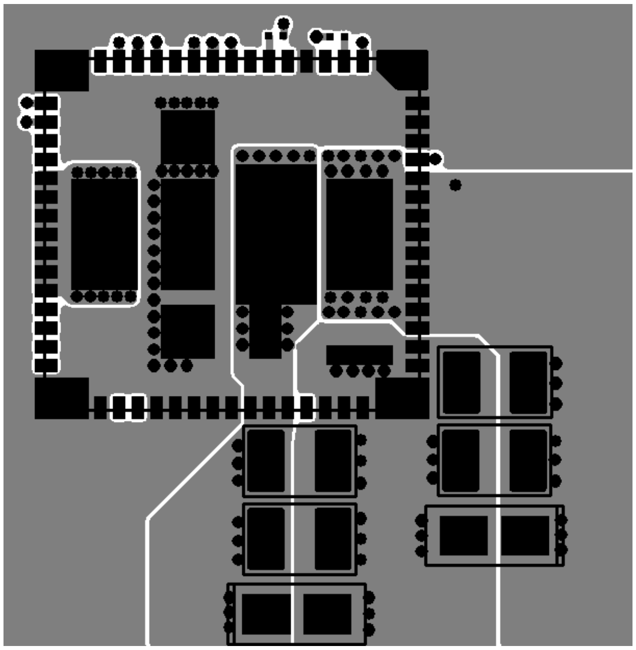

Figure 25. Typical Top Layer Layout

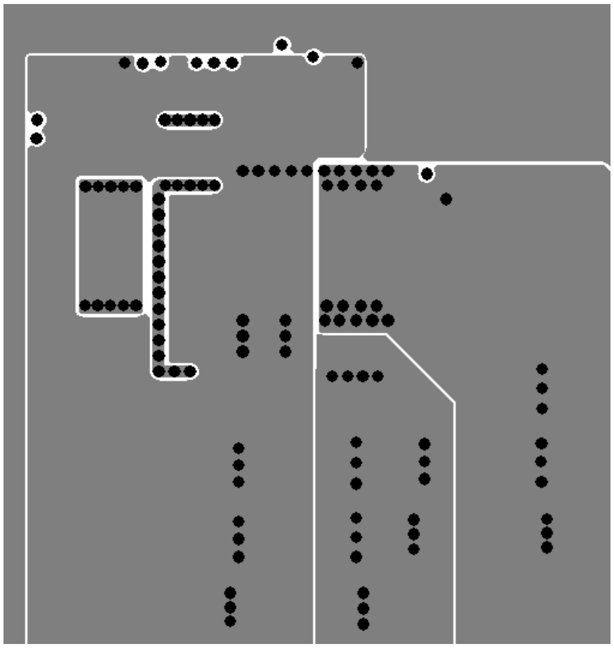

Figure 26. Typical Layer 2 Layout

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Layout Considerations (continued)

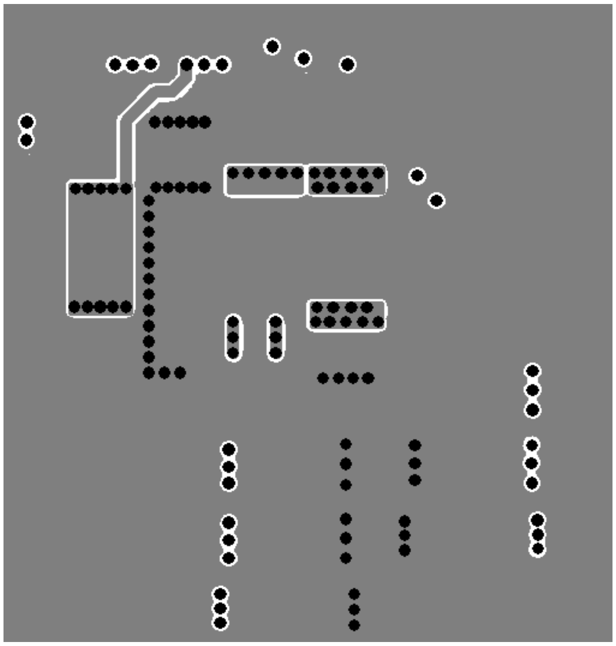

Figure 27. Typical Layer 3 Layout

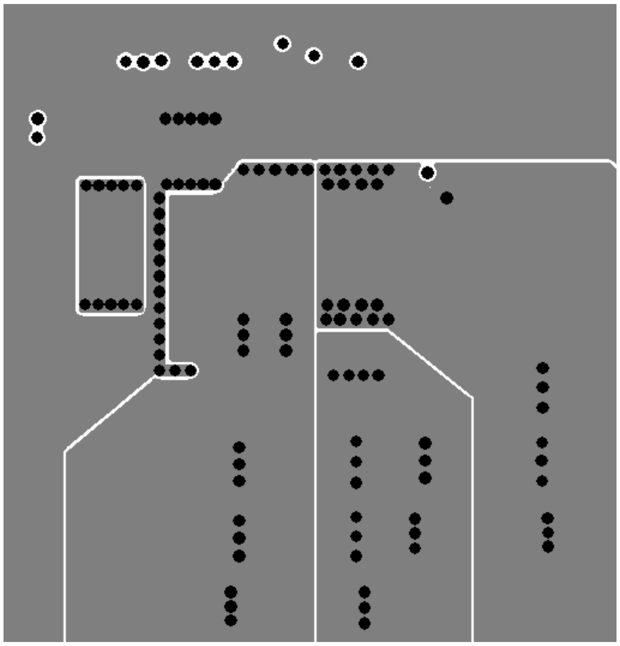

Figure 28. Typical Layer 4 Layout

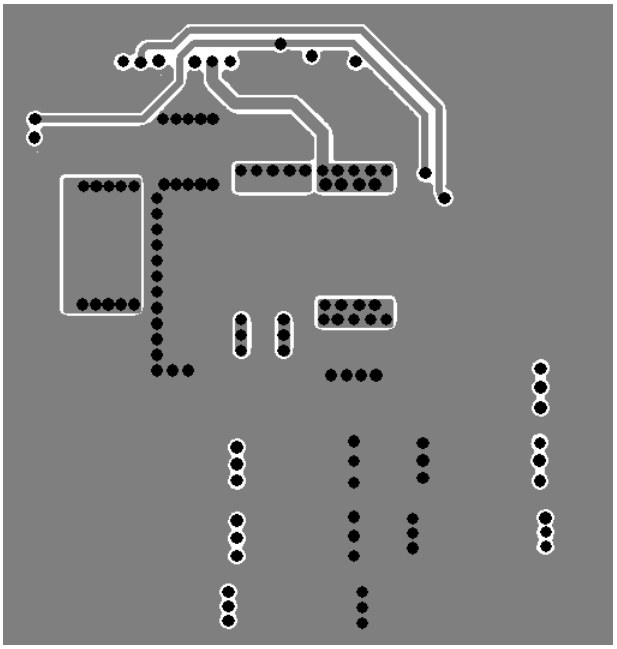

Figure 29. Typical Layer 5 Layout

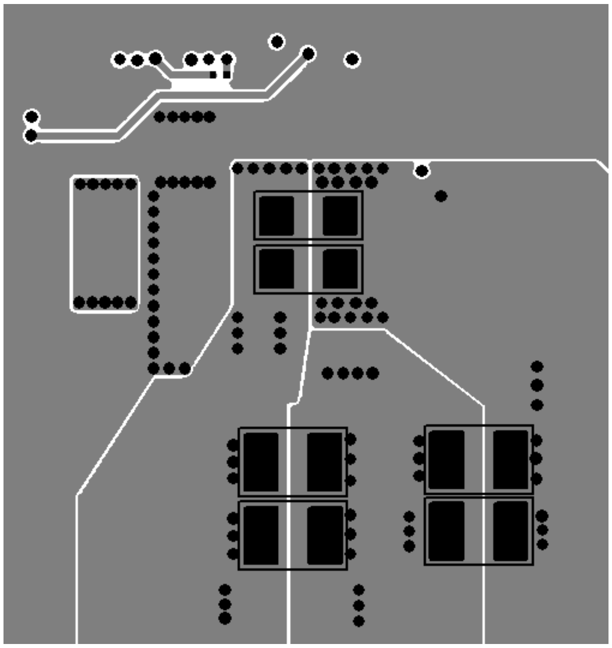

Figure 30. Typical Bottom Layer Layout

7.20 EMI

The LMZ31520 is compliant with EN55022 Class A radiated emissions. Figure 31 and Figure 32 show typical examples of radiated emissions plots for the LMZ31520 operating from 5V and 12V respectively. Both graphs include the plots of the antenna in the horizontal and vertical positions.

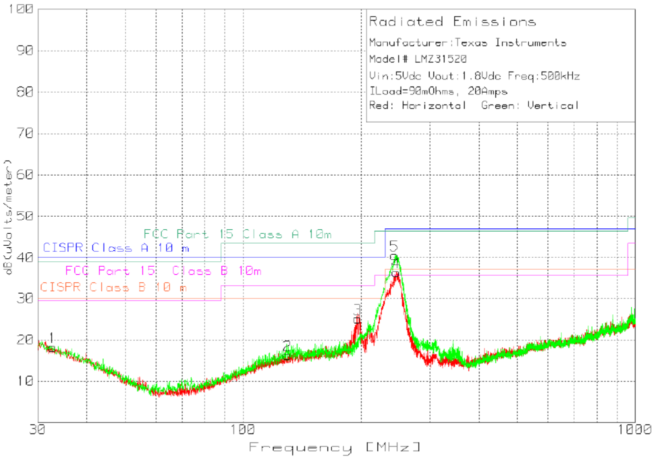

Figure 31. Radiated Emissions 5-V Input, 1.8-V Output, 20-A Load (EN55022 Class A)

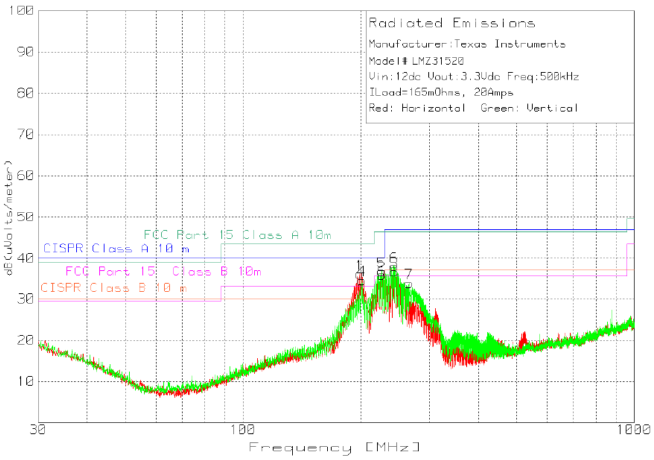

Figure 32. Radiated Emissions 12-V Input, 3.3-V Output, 20-A Load (EN55022 Class A)

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8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (December 2013) to Revision C	Page
• Added peak reflow and maximum number of reflows information	2

Changes from Revision A (December 2013) to Revision B	Page
• Added additional capacitors to the recommended capacitor table	13

Changes from Original (October 2013) to Revision A	Page
• Changed status from Preview to Production	1

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation see the following:

Soldering Requirements for BQFN Packages

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Community Resources

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9.4 Trademarks

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9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

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