LP3991 300-mA LDO for Digital Applications

1 Features

- Input Voltage From 1.65 V to 4 V
- Output Voltage From 0.8 V to 3 V
- 1% Accuracy at Room Temperature
- 125-mV Dropout at 300-mA Load
- 50-µA Quiescent Current at 1-mA Load
- Inrush Current Controlled to 600 mA
- PSRR 65 dB at 1 kHz
- 100-µs Start-Up Time for 1.5-V V_{OUT}
- Stable With Ceramic Capacitors as Small as 0402
- Thermal-Overload and Short-Circuit Protection

2 Applications

- Post DC-DC Regulator
- Battery Operated Devices
- Hand-Held Information Appliances

3 Description

Operating from a minimum input voltage of 1.65 V, the LP3991 LDO has been designed to provide fixed stable output voltages for load currents up to 300 mA. This device is suitable where accurate low voltages are required from low input voltage sources and is therefore suitable for post regulation of switched mode regulators. In such applications, significant improvements in performance and EMI can be realized, with little reduction in overall efficiency. The LP3991 provides fixed outputs as low as 1.2 V from a wide input range from 1.65 V to 4 V Using the enable (EN) pin, the device may be controlled to provide a shutdown state, in which negligible supply current is drawn.

The LP3991 is designed to be stable with space-saving ceramic capacitors as small as 0402 case size.

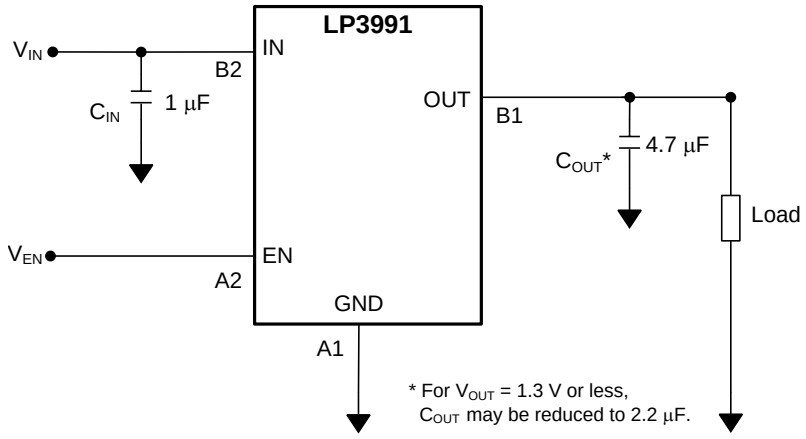
Performance is specified for a –40°C to +125°C junction temperature range. For output voltage options, contact your local Texas Instruments sales office.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LP3991	DSBGA (4)	1.43 mm × 0.96 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Typical Application Circuit



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision I (August 2015) to Revision J — **Page**

- Changed "Linear Voltage Regulator" to "LDO" in title ... 1
- Changed "regulator" to "LDO" in *Description* ... 1
- Changed Body Size dimensions from (MAX) to (NOM) in *Device Information* ... 1
- Added footnote 2 for *Thermal Information* ... 4
- Added *Power Dissipation* and *Estimating Junction Temperature* subsections ... 14
- Added *Receiving Notification of Documentation Updates* ... 18

Changes from Revision H (May 2013) to Revision I — **Page**

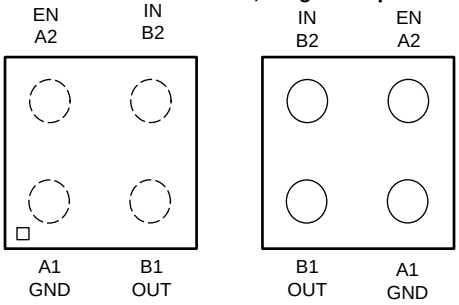
- Added *Device Information* and *Pin Configuration and Functions* sections, ESD Rating table, *Feature Description*, *Device Functional Modes*, *Application and Implementation*, *Power Supply Recommendations*, *Layout*, *Device and Documentation Support* , and *Mechanical, Packaging, and Orderable Information* sections ... 1
- Changed pin names to TI nomenclature; added icon for Reference Design to Top Navigators ... 1
- Changed Output voltage range from "1.2 V to 2.8 V" to "0.8 V to 3 V" due to new options available to buy ... 1
- Deleted Lead temp spec from Abs Max table; this info is in POA ... 4
- Added updated thermal values ... 4
- Changed values in Table 1 based on updated thermal values ... 10

Changes from Revision G (May 2013) to Revision H — **Page**

- Changed layout of National Data Sheet to TI format ... 10

5 Pin Configuration and Functions

YZR Package
4-Pin Thin DSBGA, Large Bump



Pin Functions

PIN		I/O	DESCRIPTION
NUMBER	NAME		
A1	GND	—	Common ground. Connect to pad.
A2	EN	I	Enable Input; enables the regulator when ≥ 0.95 V. Disables the regulator when ≤ 0.4 V. Enable input has an internal 1.2-MΩ pulldown resistor to GND.
B1	OUT	O	Voltage output. A low-ESR ceramic capacitor must be connected from this pin to GND (see *Application and Implementation*). Connect this output to the load circuit.
B2	IN	I	Voltage supply input. A 1-µF capacitor must be connected from this pin to GND.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)(3)

	MIN	MAX	UNIT
IN, OUT pins, voltage to GND	–0.3	6.5	V
EN pin, voltage to GND	–0.3	(V_{IN} + 0.3) < 6.5	V
Junction temperature		150	°C
Continuous power dissipation(4)	Internally Limited		
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to the potential at the GND pin.
(3) If Military/Aerospace specified devices are required, contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(4) Internal thermal shutdown circuitry protects the device from permanent damage.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Input voltage	1.65		4	V
Recommended load current			300	mA
Junction temperature	–40		125	°C
Ambient temperature, T_A(1)	–40		85	°C

(1) The maximum ambient temperature ($T_{A\text{-}MAX}$) is a suggested value dependant on the maximum operating junction temperature ($T_{J\text{-}MAX\text{-}OP}$) = 125°C); the maximum power dissipation of the device in the application ($P_{D\text{-}MAX}$), and the junction-to-ambient thermal resistance of the part / package in the application ($R_{\theta JA}$), as given by the following equation: $T_{A\text{-}MAX} = T_{J\text{-}MAX\text{-}OP} – (R_{\theta JA} \times P_{D\text{-}MAX})$.

6.4 Thermal Information

THERMAL METRIC(1)		LP3991 YZR (DSBGA) 4 PINS	UNIT
$R_{\theta JA}$(2)	Junction-to-ambient thermal resistance, High K	189.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	112.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	8.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	112.8	°C/W

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics*.
(2) Thermal resistance value $R_{\theta JA}$ is based on the EIA/JEDEC High-K printed circuit board defined by: JESD51-7 - *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*.

6.5 Electrical Characteristics

Unless otherwise noted, V_{EN} = 950 mV, V_{IN} = V_{OUT} + 0.5 V, or 1.8 V, whichever is higher, C_{IN} = 1 µF, C_{OUT} = 4.7 µF, I_{OUT} = 1 mA. Typical values and limits apply for T_A = 25°C. Minimum and maximum limits apply over the full junction temperature range for operation, −40°C to +125°C, unless otherwise specified. (1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage	See (2)		1.65		3.6	V
		See (3) (4) (5)				4	
ΔV_{OUT}	Output voltage tolerance	V_{IN} = $V_{IN(NOM)}$ to 3.6 V, I_{LOAD} = 1 to 300 mA	T_J = 25°C		–1%	1%	
					–3%	3%	
			T_J = –25°C to 85°C		–2.5%	2.5%	
	Line regulation error	V_{IN} = $V_{OUT(NOM)}$ 0.5 V to 3.6 V, I_{OUT} = 1 mA, 0.8 V ≤ V_{OUT} ≤ 2.8 V			0.05	1	%/V
	Load regulation error	I_{OUT} = 1 mA to 300 mA			10	60	µV/mA
V_{DO}	Dropout voltage (6)	1.8 V ≤ V_{OUT} ≤ 2.5 V	I_{OUT} = 150 mA		55	90	mV
			I_{OUT} = 300 mA		110	180	
		V_{OUT} > 2.5 V	I_{OUT} = 150 mA		40	80	
			I_{OUT} = 300 mA		75	160	
I_{LOAD}	Minimum load current	See (7)		0			mA
I_Q	Quiescent current	V_{EN} = 950 mV, I_{OUT} = 0 mA			50	100	µA
		V_{EN} = 950 mV, I_{OUT} = 300 mA			120	225	
		V_{EN} = 0.4 V			0.001	1	
I_{SC}	Short-circuit current limit	V_{IN} = 3.6 V (8)			550	900	mA
I_{OUT}	Maximum output current			300			mA
PSRR	Power Supply Rejection Ratio (9)	f = 1kHz, I_{OUT} = 1 mA to 300 mA			65		dB
e_n	Output noise voltage (9)	BW = 10 Hz to 100 kHz, V_{IN} = 4.2 V, C_{OUT} = 4.7 µF			280		μV_{RMS}
$T_{SHUTDOWN}$	Thermal shutdown	Temperature			160		°C
		Hysteresis			20		
ENABLE CONTROL CHARACTERISTICS							
I_{EN} (10)	Maximum input current at V_{EN} input	V_{EN} = 0 V, V_{IN} = 3.6 V			0.001		µA
		V_{EN} = V_{IN} = 3.6 V			3	5.5	
V_{IL}	Low input threshold	V_{IN} = 1.65 V to 3.6 V				0.4	V
V_{IH}	High input threshold	V_{IN} = 1.65 V to 3.6 V		0.95			V

(1) All limits are ensured. All electrical characteristics having room-temperature limits are tested during production at T_J = 25°C or correlated using Statistical Quality Control methods. Operation over the temperature specification is ensured by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(2) All voltages are with respect to the potential at the GND pin.
(3) $V_{IN(MIN)}$ = $V_{OUT(NOM)}$ + 0.5 V or 1.65 V, whichever is greater. (See Figure 19 in *DSBGA Light Sensitivity*.)
(4) The device operates with input voltages up to 4 V. However special care must be taken in relation to thermal dissipation and the need to derate the maximum allowable ambient temperature.
(5) The maximum ambient temperature (T_{A-MAX}) is a suggested value dependant on the maximum operating junction temperature ($T_{J-MAX-OP}$) = 125°C); the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to-ambient thermal resistance of the part / package in the application ($R_{\theta JA}$), as given by the following equation: T_{A-MAX} = $T_{J-MAX-OP}$ – ($R_{\theta JA}$ × P_{D-MAX}).
(6) Dropout voltage is voltage difference between input and output at which the output voltage drops to 100 mV below its nominal value. This parameter is only specified for output voltages above 1.8 V.
(7) The device maintains the regulated output voltage without a load.
(8) Short circuit current is measured with V_{OUT} pulled to 0 V.
(9) This electrical specification is ensured by design.
(10) EN pin has an internal 1.2-MΩ (typical) resistor connected to GND.

Electrical Characteristics (continued)

Unless otherwise noted, V_{EN} = 950 mV, V_{IN} = V_{OUT} + 0.5 V, or 1.8 V, whichever is higher, C_{IN} = 1 µF, C_{OUT} = 4.7 µF, I_{OUT} = 1 mA. Typical values and limits apply for T_A = 25°C. Minimum and maximum limits apply over the full junction temperature range for operation, −40°C to +125°C, unless otherwise specified. (1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
TIMING CHARACTERISTICS							
Transient Response	Line transient response $\|\delta V_{OUT}\|$	T_{rise} = T_{fall} = 30 µs(9) δV_{IN} = 600 mV			6		mV (pk - pk)
	Load transient response $\|\delta V_{OUT}\|$	T_{rise} = T_{fall} = 1 µs(9)	I_{OUT} = 0 mA to 300 mA		140		mV
			I_{OUT} = 1 mA to 300 mA		110		
			I_{OUT} = 300 mA to 1 mA		80		
			I_{OUT} = 0 mA to 200 mA		110		
			I_{OUT} = 1 mA to 200 mA		80		
			I_{OUT} = 200 mA to 1 mA		60		
			I_{OUT} = 0 mA to 150 mA		100		
			I_{OUT} = 1 mA to 150 mA		70		
			I_{OUT} = 150 mA to 1 mA		50		
	Overshoot on start-up				0%	2%	
I_{IR}	In-rush current(9)				600	1000	mA
OUTPUT CAPACITANCE							
C_{OUT}	Output capacitor	Capacitance(11)	V_{OUT} ≥ 1.5 V	2	4.7		µF
			V_{OUT} < 1.5 V(12)	1.6	2.2		
		ESR		5		500	mΩ

(11) The capacitor tolerance must be 30% or better over temperature. The full operating conditions for the application must be considered when selecting a suitable capacitor to ensure that the minimum value of capacitance is always met. Recommended capacitor type is X7R or X5R. (See *External Capacitors* in *Detailed Design Procedure*.)

(12) On lower voltage options, 2.2-µF output capacitor may be used but some degradation in load transient (10 -15%) can be expected, compared to a 4.7-µF capacitor.

6.6 Timing Requirements

		MIN	NOM	MAX	UNIT
t_{ON}	Turnon time(1) To 95% Level $V_{IN(MIN)}$ to 3.6 V, V_{OUT} ≤ 2 V		100		µs
	Turnon time(1) To 95% Level $V_{IN(MIN)}$ to 3.6 V, V_{OUT} ≥ 2 V		140		

(1) This electrical specification is ensured by design.

6.7 Typical Characteristics

Unless otherwise specified, C_{IN} = 1 µF ceramic, C_{OUT} = 4.7 µF ceramic, V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 1.8 V, whichever is greater, T_A = 25°C, $V_{OUT(NOM)}$ = 1.5 V, EN pin is tied to V_{IN}.

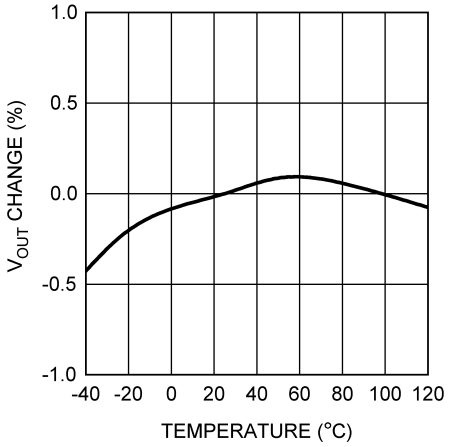


Figure 1. Output Voltage Change vs Temperature

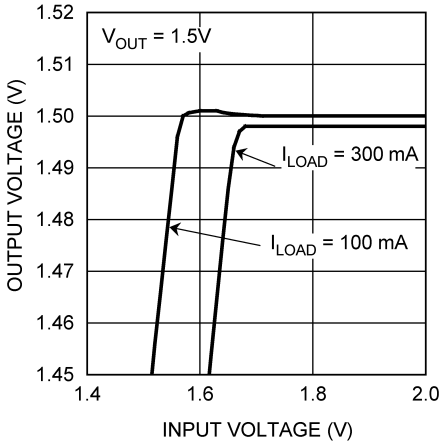


Figure 2. Output Voltage vs Minimum Input Voltage

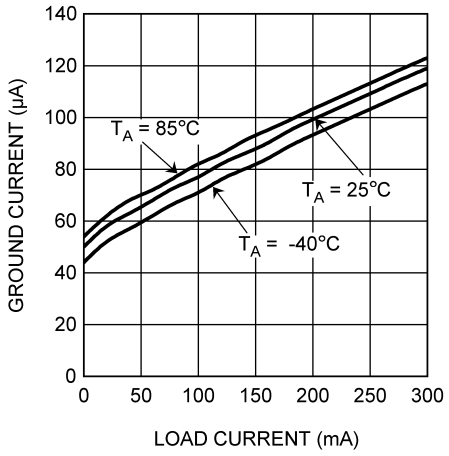


Figure 3. Ground Current vs Load Current

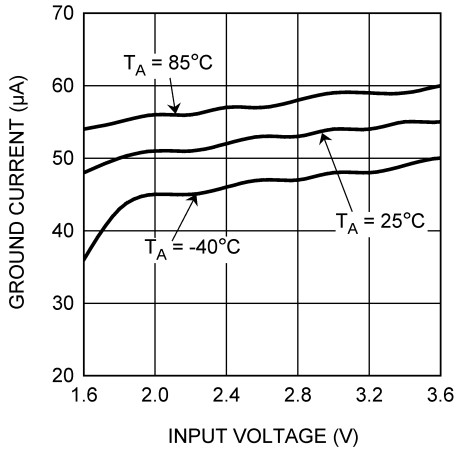


Figure 4. Ground Current vs V_{IN}. I_{LOAD} = 1mA

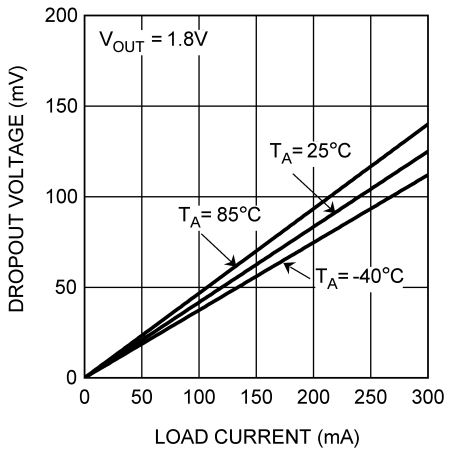


Figure 5. Dropout Voltage

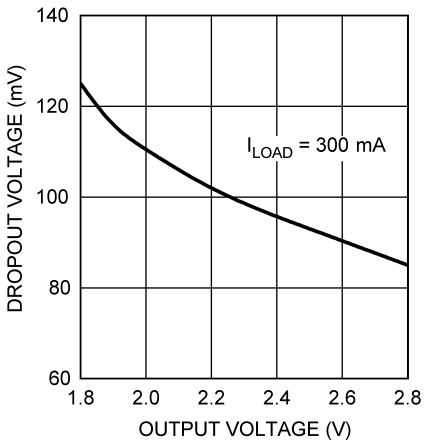


Figure 6. Dropout Voltage vs Output Voltage

Typical Characteristics (continued)

Unless otherwise specified, C_{IN} = 1 µF ceramic, C_{OUT} = 4.7 µF ceramic, V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 1.8 V, whichever is greater, T_A = 25°C, $V_{OUT(NOM)}$ = 1.5 V, EN pin is tied to V_{IN}.

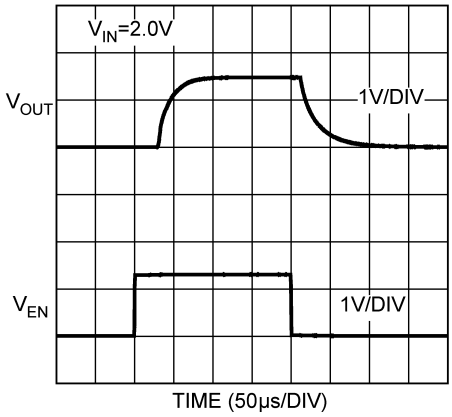


Figure 7. Enable Characteristics

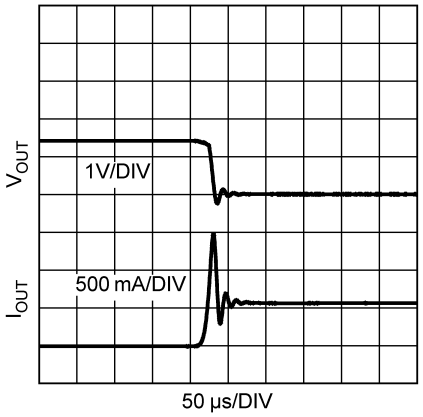


Figure 8. Short Circuit Current

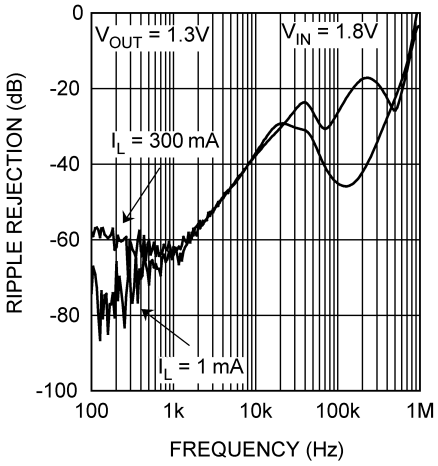


Figure 9. Power Supply Rejection Ratio

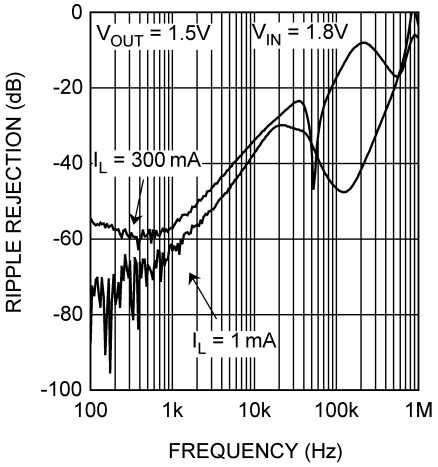


Figure 10. Power Supply Rejection Ratio

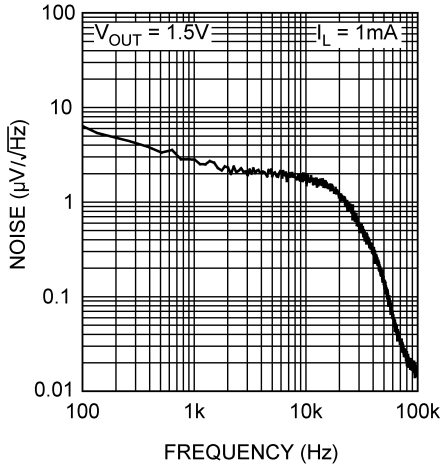


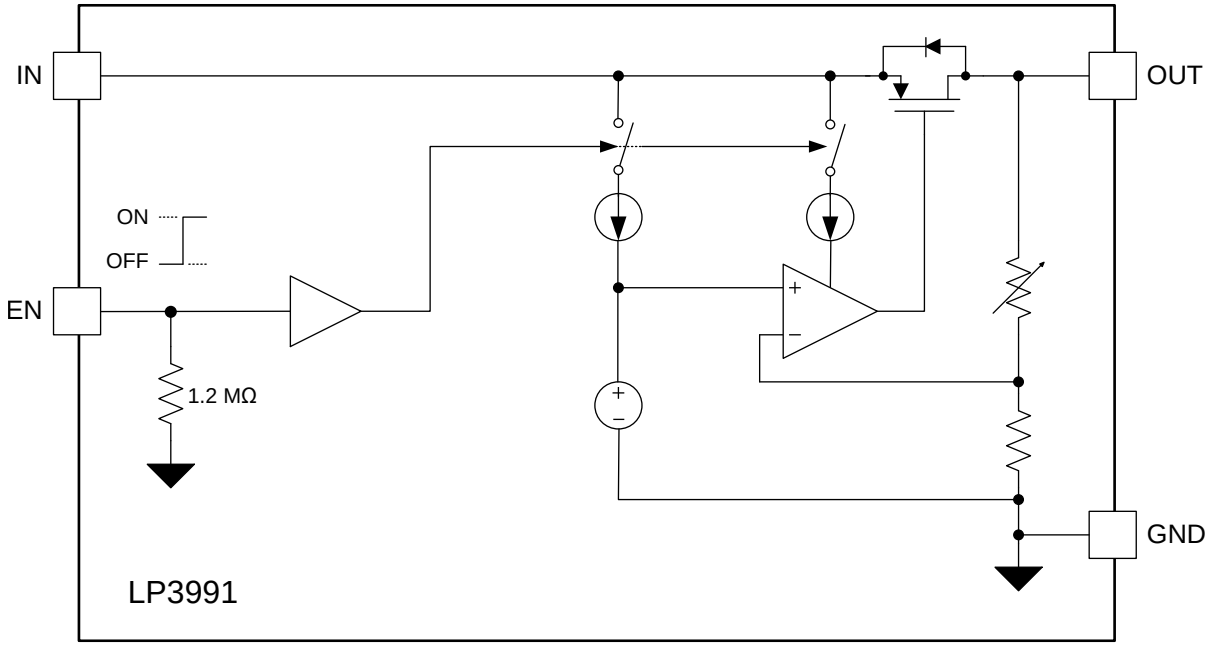
Figure 11. Noise Density

7 Detailed Description

7.1 Overview

The LP3991 device is a monolithic integrated low-dropout voltage regulator with a low input operating voltage tolerance. Key protection circuits, including output current limitation and thermal shutdown, are integrated in the device. Using the EN pin, the device may be controlled to provide a shutdown state, in which negligible supply current is drawn. The LP3991 is designed to be stable with space-saving ceramic capacitors as small as 0402 case size.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Post-Buck Regulator

Linear post-regulation can be an effective way to reduce ripple and switching noise from DC-DC convertors while still maintaining a reasonably high overall efficiency.

The LP3991 is particularly suitable for this role due to its low input voltage requirements. In addition, there is often no need for a separate input capacitor for the LP3991 as it can share the output cap of the DC-DC convertor.

Care of PCB layouts involving switching regulators is paramount. In particular, the ground paths for the LDO must be routed separately from the switcher ground and star connected close to the battery. Routing of the switch pin of the DC-DC convertor must be kept short to minimize radiated EMI. A low pass filter such as a ferrite bead or common mode choke on the battery input leads can further reduce radiated EMI.

Figure 19 shows a typical example using an LM3673, 350-mA DC-DC buck regulator with a nominal output of 1.8 V and a 1.5-V LP3991 device. The overall efficiency is greater than 70% over the full Li-Ion battery voltage range. Maximum efficiency is achieved by minimizing the difference between V_{IN} and V_{OUT} of the LP3991 device. The LP3991-1.5 remains in regulation down to an input voltage of 1.65 V; thus, in this case, a 1.8-V buck with 5% tolerance is adequate for all conditions of temperature and load.

Feature Description (continued)

7.3.2 Maximum Supply Voltage and Thermal Considerations

Maximum recommended input voltage is 3.6 V. The device may be operated at 4-V V_{IN} if proper care is given to the board design in regard to thermal dissipation. As a guide, refer to Table 1 for ambient temperature at two input voltages and two load currents for the example board types.

Table 1. Example Board Ambient Temperatures

$R_{\theta JA}$	V_{IN}	V_{OUT}	I_{OUT}	P_D	AMBIENT TEMPERATURE
189ºC/W	3.6 V	2.8 V	160 mA	0.13 W	100ºC
			250 mA	0.20 W	87ºC
	4 V	2.8 V	160 mA	0.19 W	89ºC
			250 mA	0.30 W	68ºC
160ºC/W	3.6 V	2.8 V	160 mA	0.13 W	104ºC
			250 mA	0.20 W	93ºC
	4 V	2.8 V	160 mA	0.19 W	94ºC
			250 mA	0.30 W	77ºC

7.4 Device Functional Modes

7.4.1 Enable Control

The LP3991 features an active high enable (EN) pin, which turns the device on when pulled high. When not enabled the regulator output is off and the device typically consumes 2 nA.

If the application does not require the enable switching feature, the EN pin must be tied to V_{IN} to keep the regulator output permanently on.

To ensure proper operation, the signal source used to drive the EN input must be able to swing above and below the specified turnon/off voltage thresholds listed in *Typical Characteristics* under V_{IL} and V_{IH}.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LP3991 can provide 300-mA output current with 1.65-V to 4-V input. It is stable with a 2.2-µF or 4.7-µF ceramic output capacitor. An optional external bypass capacitor reduces the output noise without slowing down the load transient response. Typical output noise is 280 μV_{RMS} at frequencies from 10 Hz to 100 kHz. Typical power supply rejection is 65 dB at 1 kHz.

8.2 Typical Application

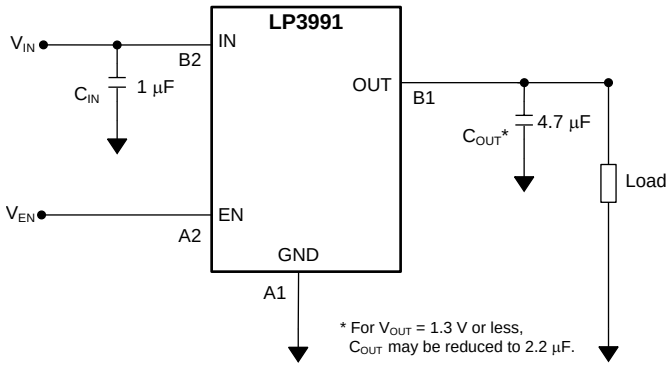


Figure 12. LP3991 Typical Application

8.2.1 Design Requirements

For typical linear voltage regulator applications, use the parameters listed in Table 2.

Table 2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	1.65 V to 4 V
Output voltage	1.2 V to 2.8 V
Output current	300 mA (maximum)
RMS noise, 10 Hz to100 kHz	280 μV_{RMS}
PSRR at 1 kHz	65 dB

8.2.2 Detailed Design Procedure

8.2.2.1 External Capacitors

In common with most regulators, the LP3991 requires external capacitors for regulator stability. The LP3991 is specifically designed for portable applications requiring minimum board space and smallest components. These capacitors must be correctly selected for good performance.

8.2.2.2 Input Capacitor

An input capacitor is required for stability. It is recommended that a 1-µF capacitor be connected between the LP3991 IN pin and ground (this capacitance value may be increased without limit).

This capacitor must be located a distance of not more than 1 cm from the IN pin and returned to a clean analog ground. Any good-quality ceramic, tantalum, or film capacitor may be used at the input.

NOTE

Tantalum capacitors can suffer catastrophic failures due to surge current when connected to a low-impedance source of power (like a battery or a very large capacitor). If a tantalum capacitor is used at the input, a surge current rating sufficient for the application must be ensured by the manufacturer.

There are no requirements for the equivalent series resistance (ESR) on the input capacitor, but tolerance, temperature, and voltage coefficients must be considered when selecting the capacitor to ensure the capacitance remains ≅ 1 µF over the entire operating temperature range.

8.2.2.3 Output Capacitor

Correct selection of the output capacitor is critical to ensure stable operation in the intended application.

The output capacitor must meet all the requirements specified in the recommended capacitor table over all conditions in the application. these conditions include DC bias, frequency and temperature. Unstable operation results if the capacitance drops below the minimum specified value.

The LP3991 is designed specifically to work with very small ceramic output capacitors. For voltage options of 1.5 V and higher, A 4.7-µF ceramic capacitor (dielectric type X7R or X5R) with an ESR between 5 mΩ to 500 mΩ, is suitable in the LP3991 application circuit. However, on lower V_{OUT} options a 2.2-µF may be employed with only a small increase in load transient.

Other ceramic types such as Y5V and Z5U are less suitable owing to their inferior temperature characteristics. (See *Capacitor Characteristics*.)

It is also recommended that the output capacitor is placed within 1 cm of the OUT pin and returned to a clean, low impedance, ground connection.

It is possible to use tantalum or film capacitors at the device output, V_{OUT}, but these are not as attractive for reasons of size and cost. (See *Capacitor Characteristics*.)

8.2.2.4 No-Load Stability

The LP3991 remains stable and in regulation with no external load. This is an important consideration in some circuits, for example CMOS RAM keep-alive applications.

8.2.2.5 Capacitor Characteristics

The LP3991 is designed to work with ceramic capacitors on the input and output to take advantage of the benefits they offer. For capacitance values around 4.7 µF, ceramic capacitors give the circuit designer the best design options in terms of low cost and minimal area.

For both input and output capacitors, careful interpretation of the capacitor specification is required to ensure correct device operation. The capacitor value can change greatly dependant on the conditions of operation and capacitor type.

In particular, to ensure stability, the output capacitor selection must take account of all the capacitor parameters, to ensure that the specification is met within the application. Capacitance value can vary with DC bias conditions as well as temperature and frequency of operation. Capacitor values also show some decrease over time due to aging. The capacitor parameters are also dependant on the particular case size with smaller sizes giving poorer performance figures in general.

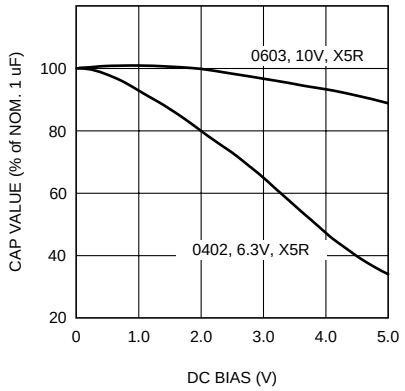


Figure 13. Effect of DC Bias on Capacitance Value

As an example Figure 13 shows a typical graph showing a comparison of capacitor case sizes in a capacitance vs. DC Bias plot. As shown in Figure 13, as a result of the DC Bias condition, the capacitance value may drop below the minimum capacitance value given in the recommended capacitor table. Note that Figure 13 shows the capacitance out of spec for the 0402 case size capacitor at higher bias voltages. TI therefore recommends that the capacitor manufacturers' specifications for the nominal value capacitor are consulted for all conditions as some capacitor sizes (for example, 0402) may not be suitable in the actual application. Ceramic capacitors have the lowest ESR values, thus making them best for eliminating high frequency noise. The ESR of a typical 4.7-µF ceramic capacitor is in the range of 20 mΩ to 40 mΩ, which easily meets the ESR requirement for stability for the LP3991. The temperature performance of ceramic capacitors varies by type. Capacitor type X7R is specified with a tolerance of ±15% over the temperature range –55°C to +125°C. The X5R has a similar tolerance over the reduced temperature range of –55°C to +85°C. Some large value ceramic capacitors (4.7 µF) are manufactured with Z5U or Y5V temperature characteristics, which can result in the capacitance dropping by more than 50% as the temperature varies from 25°C to +85°C. Therefore, X7R or X5R types are recommended in applications where the temperature changes significantly above or below 25°C.

Tantalum capacitors are less desirable than ceramic for use as output capacitors because they are more expensive when comparing equivalent capacitance and voltage ratings in the 1-µF to 4.7-µF range. Another important consideration is that tantalum capacitors have higher ESR values than equivalent size ceramics. This means that while it may be possible to find a tantalum capacitor with an ESR value within the stable range, it would have to be larger in capacitance (which means bigger and more costly) than a ceramic capacitor with the same ESR value. The ESR of a typical tantalum increases about 2:1 as the temperature goes from 25°C down to –40°C, so some guard band must be allowed.

8.2.2.6 Power Dissipation

Knowing the device power dissipation and proper sizing of the thermal plane connected to the tab or pad is critical to ensuring reliable operation. Device power dissipation depends on input voltage, output voltage, and load conditions and can be calculated with Equation 1.

$$P_{D(MAX)} = (V_{IN(MAX)} - V_{OUT}) \times I_{OUT} \quad (1)$$

Power dissipation can be minimized, and greater efficiency can be achieved, by using the lowest available voltage drop option that would still be greater than the dropout voltage (V_{DO}). However, keep in mind that higher voltage drops result in better dynamic (that is, PSRR and transient) performance.

On the LP3991 DSBGA (YZR) package, the primary conduction path for heat is through the four bumps to the PCB. The maximum allowable junction temperature ($T_{J(MAX)}$) determines maximum power dissipation allowed ($P_{D(MAX)}$) for the device package.

Power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance ($R_{\theta JA}$) of the combined PCB and device package and the temperature of the ambient air (T_A), according to Equation 2 or Equation 3:

$$T_{J(MAX)} = T_{A(MAX)} + (R_{\theta JA} \times P_{D(MAX)}) \quad (2)$$

$$P_{D(MAX)} = (T_{J(MAX)} - T_{A(MAX)}) / R_{\theta JA} \quad (3)$$

Unfortunately, this $R_{\theta JA}$ is highly dependent on the heat-spreading capability of the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The $R_{\theta JA}$ recorded in *Thermal Information* is determined by the specific EIA/JEDEC JESD51-7 standard for PCB and copper-spreading area, and is to be used only as a relative measure of package thermal performance. For a well-designed thermal layout, $R_{\theta JA}$ is actually the sum of the package junction-to-board thermal resistance ($R_{\theta JB}$) plus the thermal resistance contribution by the PCB copper area acting as a heat sink.

8.2.2.7 Estimating Junction Temperature

The EIA/JEDEC standard recommends the use of psi (Ψ) thermal characteristics to estimate the junction temperatures of surface mount devices on a typical PCB board application. These characteristics are not true thermal resistance values, but rather package specific thermal characteristics that offer practical and relative means of estimating junction temperatures. These psi metrics are determined to be significantly independent of copper-spreading area. The key thermal characteristics (Ψ_{JT} and Ψ_{JB}) are given in *Thermal Information* and are used in accordance with Equation 4 or Equation 5.

$$T_{J(MAX)} = T_{TOP} + (\Psi_{JT} \times P_{D(MAX)}) \quad (4)$$

where

- $P_{D(MAX)}$ is explained in Equation 1
- T_{TOP} is the temperature measured at the center-top of the device package.

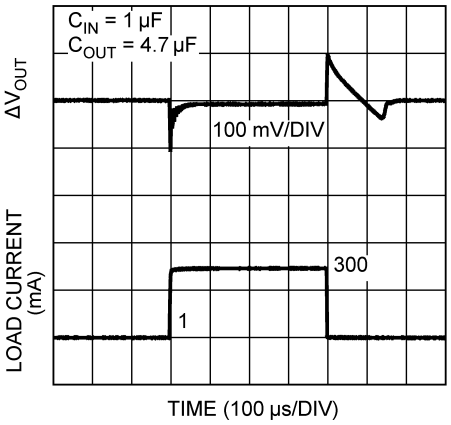
$$T_{J(MAX)} = T_{BOARD} + (\Psi_{JB} \times P_{D(MAX)}) \quad (5)$$

where

- $P_{D(MAX)}$ is explained in Equation 1
- T_{BOARD} is the PCB surface temperature measured 1 mm from the device package and centered on the package edge.

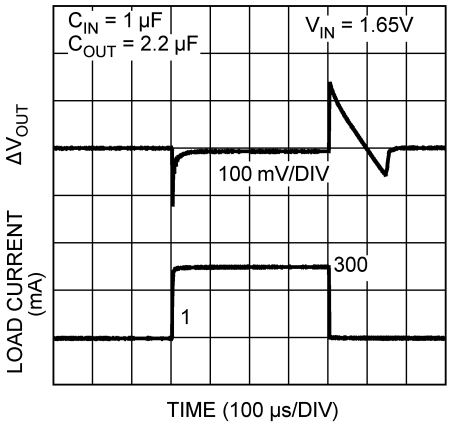
For more information about the thermal characteristics Ψ_{JT} and Ψ_{JB}, see *Semiconductor and IC Package Thermal Metrics* (SPRA953); for more information about measuring T_{TOP} and T_{BOARD}, see *Using New Thermal Metrics* (SBVA025); and for more information about the EIA/JEDEC JESD51 PCB used for validating $R_{\theta JA}$, see the *Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs* (SZZA017). These application notes are available at www.ti.com.

8.2.3 Application Curves



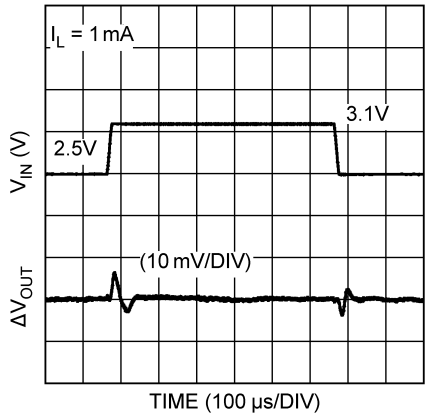
V_{OUT} = 1.5 V

Figure 14. Load Transient



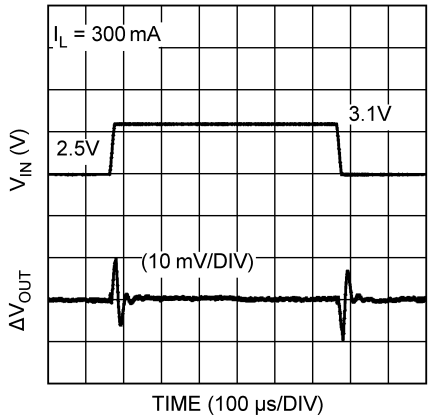
V_{OUT} = 1.2 V

Figure 15. Load Transient



I_{LOAD} = 1 mA

Figure 16. Line Transient



I_{LOAD} = 300 mA

Figure 17. Line Transient

9 Power Supply Recommendations

The LP3991 is designed to operate from an input voltage supply range from 1.65 V to 4 V.

10 Layout

10.1 Layout Guidelines

The dynamic performance of the LP3991 is dependant on the layout of the PCB. PCB layout practices that are adequate for typical LDOs may degrade the PSRR or transient performance of the LP3991.

Best performance is achieved by placing all of the components on the same side of the PCB as the LP3991, as close as is practical to the LP3991 package. All component ground connections must be back to the LP3991 analog ground connection using as wide and as short of a copper trace as is practical.

Connections using long trace lengths, narrow trace widths, and connections through vias must be avoided. These add parasitic inductances and resistance that results in inferior performance especially during transient conditions.

A ground plane, either on the opposite side of a two-layer PCB, or embedded in a multi-layer PCB, is strongly recommended. This ground plane serves two purposes:

1. Provides a circuit reference plane to assure accuracy, and
2. Provides a thermal plane to remove heat from the LP3991 through thermal vias under the package DAP.

10.2 Layout Example

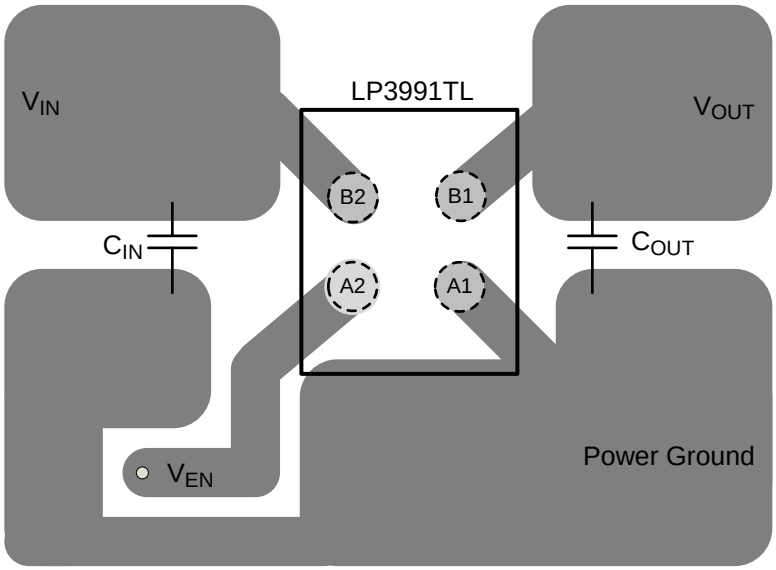


Figure 18. LP3991 Example Layout

10.3 DSBGA Mounting

The DSBGA package requires specific mounting techniques which are detailed in *AN-1112 DSBGA Wafer Level Chip Scale Package*. Referring to the section *Surface Mount Technology (SMT) Assembly Considerations*, the pad style that must be used with the 4-pin package is a NSMD (non-solder mask defined) type.

For best results during assembly, alignment ordinals on the PCB may be used to facilitate placement of the DSBGA device.

10.4 DSBGA Light Sensitivity

Exposing the DSBGA device to direct sunlight may cause mis-operation of the device. Light sources such as halogen lamps can affect the electrical performance if brought near to the device.

The wavelengths that have the most detrimental effect are reds and infra-reds, which means that the fluorescent lighting used inside most buildings has little effect on performance.

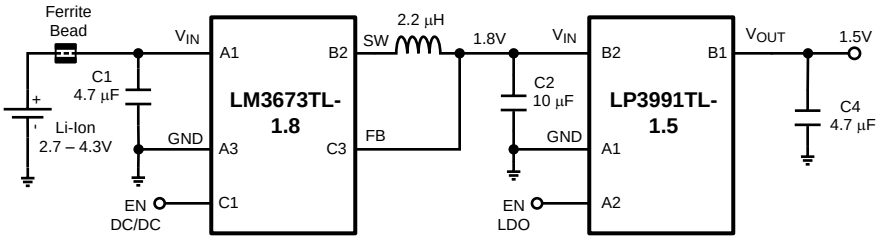


Figure 19. LP3991 Used as a Post DC-DC Regulator

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For additional information, see the following:

- *AN-1112 DSBGA Wafer Level Chip Scale Package* (SNVA009)
- *Semiconductor and IC Package Thermal Metrics* (SPRA953)
- *Using New Thermal Metrics* (SBVA025)
- *Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs* (SZZA017)

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP3991TL-1.2/NOPB	ACTIVE	DSBGA	YZR	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples
LP3991TL-1.3/NOPB	ACTIVE	DSBGA	YZR	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples
LP3991TL-1.5/NOPB	ACTIVE	DSBGA	YZR	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples
LP3991TL-1.55/NOPB	ACTIVE	DSBGA	YZR	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM			Samples
LP3991TL-1.7/NOPB	ACTIVE	DSBGA	YZR	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM			Samples
LP3991TL-1.8/NOPB	ACTIVE	DSBGA	YZR	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM			Samples
LP3991TL-2.0/NOPB	ACTIVE	DSBGA	YZR	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM			Samples
LP3991TL-2.5/NOPB	ACTIVE	DSBGA	YZR	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM			Samples
LP3991TL-2.8/NOPB	ACTIVE	DSBGA	YZR	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples
LP3991TL-3.0/NOPB	ACTIVE	DSBGA	YZR	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM			Samples
LP3991TLX-0.8/NOPB	ACTIVE	DSBGA	YZR	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM			Samples
LP3991TLX-1.2/NOPB	ACTIVE	DSBGA	YZR	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples
LP3991TLX-1.3/NOPB	ACTIVE	DSBGA	YZR	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples
LP3991TLX-1.5/NOPB	ACTIVE	DSBGA	YZR	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples
LP3991TLX-1.55/NOPB	ACTIVE	DSBGA	YZR	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM			Samples
LP3991TLX-1.7/NOPB	ACTIVE	DSBGA	YZR	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM			Samples
LP3991TLX-1.8/NOPB	ACTIVE	DSBGA	YZR	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM			Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP3991TLX-2.0/NOPB	ACTIVE	DSBGA	YZR	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM			Samples
LP3991TLX-2.5/NOPB	ACTIVE	DSBGA	YZR	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM			Samples
LP3991TLX-2.8/NOPB	ACTIVE	DSBGA	YZR	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples
LP3991TLX-3.0/NOPB	ACTIVE	DSBGA	YZR	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM			Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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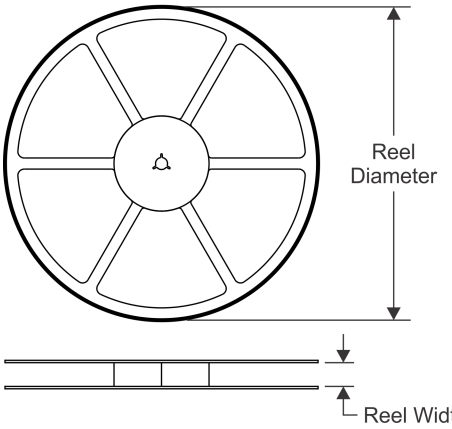
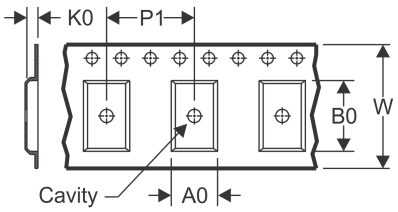
TAPE AND REEL INFORMATION

REEL DIMENSIONS

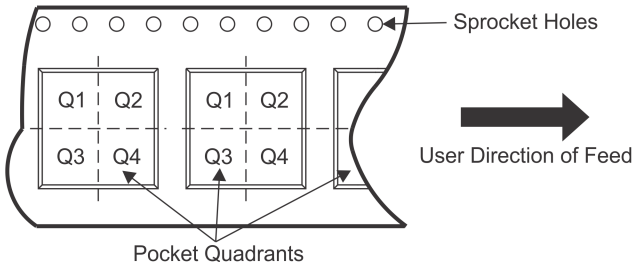


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

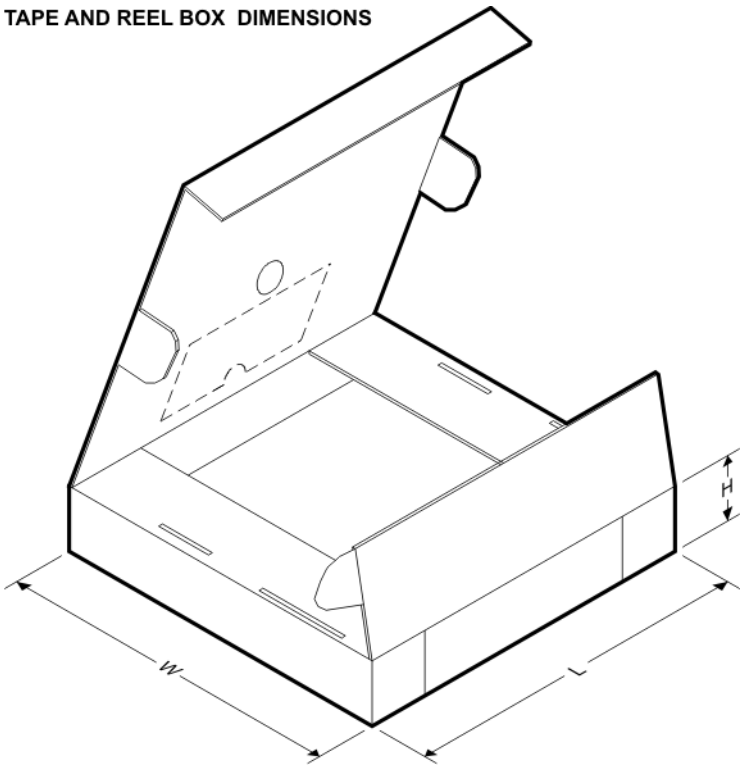


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP3991TL-1.2/NOPB	DSBGA	YZR	4	250	178.0	8.4	1.04	1.55	0.76	4.0	8.0	Q1
LP3991TL-1.3/NOPB	DSBGA	YZR	4	250	178.0	8.4	1.04	1.55	0.76	4.0	8.0	Q1
LP3991TL-1.5/NOPB	DSBGA	YZR	4	250	178.0	8.4	1.04	1.55	0.76	4.0	8.0	Q1
LP3991TL-1.55/NOPB	DSBGA	YZR	4	250	178.0	8.4	1.04	1.55	0.76	4.0	8.0	Q1
LP3991TL-1.7/NOPB	DSBGA	YZR	4	250	178.0	8.4	1.04	1.55	0.76	4.0	8.0	Q1
LP3991TL-1.8/NOPB	DSBGA	YZR	4	250	178.0	8.4	1.04	1.55	0.76	4.0	8.0	Q1
LP3991TL-2.0/NOPB	DSBGA	YZR	4	250	178.0	8.4	1.04	1.55	0.76	4.0	8.0	Q1
LP3991TL-2.5/NOPB	DSBGA	YZR	4	250	178.0	8.4	1.04	1.55	0.76	4.0	8.0	Q1
LP3991TL-2.8/NOPB	DSBGA	YZR	4	250	178.0	8.4	1.04	1.55	0.76	4.0	8.0	Q1
LP3991TL-3.0/NOPB	DSBGA	YZR	4	250	178.0	8.4	1.04	1.55	0.76	4.0	8.0	Q1
LP3991TLX-0.8/NOPB	DSBGA	YZR	4	3000	178.0	8.4	1.04	1.55	0.76	4.0	8.0	Q1
LP3991TLX-1.2/NOPB	DSBGA	YZR	4	3000	178.0	8.4	1.04	1.55	0.76	4.0	8.0	Q1
LP3991TLX-1.3/NOPB	DSBGA	YZR	4	3000	178.0	8.4	1.04	1.55	0.76	4.0	8.0	Q1
LP3991TLX-1.5/NOPB	DSBGA	YZR	4	3000	178.0	8.4	1.04	1.55	0.76	4.0	8.0	Q1
LP3991TLX-1.55/NOPB	DSBGA	YZR	4	3000	178.0	8.4	1.04	1.55	0.76	4.0	8.0	Q1
LP3991TLX-1.7/NOPB	DSBGA	YZR	4	3000	178.0	8.4	1.04	1.55	0.76	4.0	8.0	Q1
LP3991TLX-1.8/NOPB	DSBGA	YZR	4	3000	178.0	8.4	1.04	1.55	0.76	4.0	8.0	Q1
LP3991TLX-2.0/NOPB	DSBGA	YZR	4	3000	178.0	8.4	1.04	1.55	0.76	4.0	8.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP3991TLX-2.5/NOPB	DSBGA	YZR	4	3000	178.0	8.4	1.04	1.55	0.76	4.0	8.0	Q1
LP3991TLX-2.8/NOPB	DSBGA	YZR	4	3000	178.0	8.4	1.04	1.55	0.76	4.0	8.0	Q1
LP3991TLX-3.0/NOPB	DSBGA	YZR	4	3000	178.0	8.4	1.04	1.55	0.76	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS

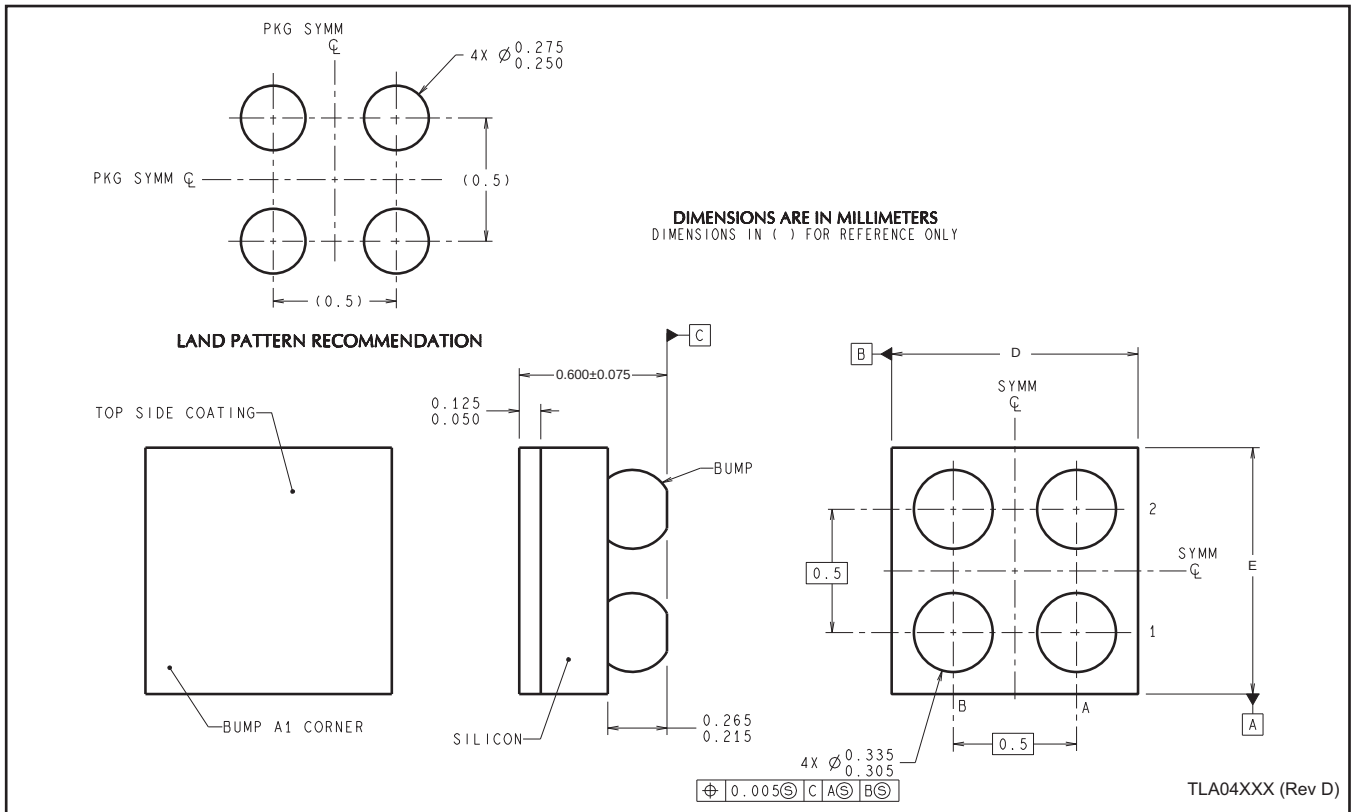


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP3991TL-1.2/NOPB	DSBGA	YZR	4	250	210.0	185.0	35.0
LP3991TL-1.3/NOPB	DSBGA	YZR	4	250	210.0	185.0	35.0
LP3991TL-1.5/NOPB	DSBGA	YZR	4	250	210.0	185.0	35.0
LP3991TL-1.55/NOPB	DSBGA	YZR	4	250	210.0	185.0	35.0
LP3991TL-1.7/NOPB	DSBGA	YZR	4	250	210.0	185.0	35.0
LP3991TL-1.8/NOPB	DSBGA	YZR	4	250	210.0	185.0	35.0
LP3991TL-2.0/NOPB	DSBGA	YZR	4	250	210.0	185.0	35.0
LP3991TL-2.5/NOPB	DSBGA	YZR	4	250	210.0	185.0	35.0
LP3991TL-2.8/NOPB	DSBGA	YZR	4	250	210.0	185.0	35.0
LP3991TL-3.0/NOPB	DSBGA	YZR	4	250	210.0	185.0	35.0
LP3991TLX-0.8/NOPB	DSBGA	YZR	4	3000	210.0	185.0	35.0
LP3991TLX-1.2/NOPB	DSBGA	YZR	4	3000	210.0	185.0	35.0
LP3991TLX-1.3/NOPB	DSBGA	YZR	4	3000	210.0	185.0	35.0
LP3991TLX-1.5/NOPB	DSBGA	YZR	4	3000	210.0	185.0	35.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP3991TLX-1.55/NOPB	DSBGA	YZR	4	3000	210.0	185.0	35.0
LP3991TLX-1.7/NOPB	DSBGA	YZR	4	3000	210.0	185.0	35.0
LP3991TLX-1.8/NOPB	DSBGA	YZR	4	3000	210.0	185.0	35.0
LP3991TLX-2.0/NOPB	DSBGA	YZR	4	3000	210.0	185.0	35.0
LP3991TLX-2.5/NOPB	DSBGA	YZR	4	3000	210.0	185.0	35.0
LP3991TLX-2.8/NOPB	DSBGA	YZR	4	3000	210.0	185.0	35.0
LP3991TLX-3.0/NOPB	DSBGA	YZR	4	3000	210.0	185.0	35.0

YZR0004



D: Max = 1.46 mm, Min = 1.4 mm

E: Max = 0.99 mm, Min = 0.93 mm

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NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

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