TEXAS INSTRUMENTS

**OPA548**

SBOS070C −OCTOBER 1997−REVISED JUNE 2015

# OPA548 High-Voltage, High-Current Operational Amplifier

## 1 Features

- Wide Supply Range
  - Single Supply: 8 V to 60 V
  - Dual Supply: ±4 V to ±30 V
- High-Output Current:
  - 3-A Continuous
  - 5-A Peak
- Wide Output Voltage Swing
- Fully Protected:
  - Thermal Shutdown
  - Adjustable Current Limit
- Output Disable Control˘
- Thermal Shutdown Indicator
- High Slew Rate: 10 V
- Low Quiescent Current
- Packages:
  - 7-Lead TO-220, Zip and Straight Leads
  - 7-Lead DDPAK Surface-Mount

## 2 Applications

- Valve, Actuator Drivers
- SYNCHRO, SERVO Drivers
- Power Supplies
- Test Equipment
- Transducer Excitation
- Audio Amplifiers

## 3 Description

The OPA548 device is a low-cost, high-voltage and high-current operational amplifier that's ideal for driving a wide variety of loads. A laser-trimmed monolithic integrated circuit provides excellent low-level signal accuracy and high-output voltage and current.

The OPA548 device operates from either single or dual supplies for design flexibility. In single-supply operation, the input common-mode range extends below ground.

The OPA548 device is internally protected against over-temperature conditions and current overloads. In addition, the OPA548 device was designed to provide an accurate, user-selected current limit. Unlike other designs, which use a *power* resistor in series with the output current path, the OPA548 device senses the load indirectly. This allows the current limit to be adjusted from 0 A to 5 A with a resistor and potentiometer or controlled digitally with a voltage-out or current-out DAC.

### Device Information[1]

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| OPA548 | TO-220 (7) | 10.17 mm × 8.38 mm |
|  | TO-263 (7) | 10.10 mm × 8.89 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.
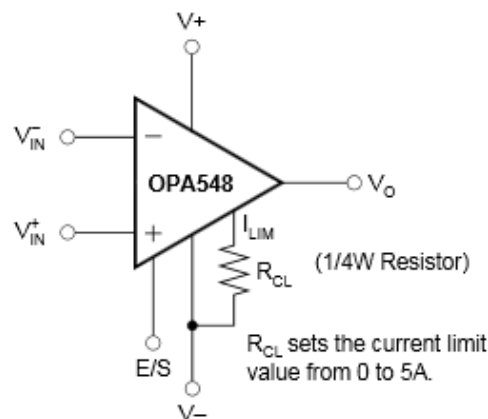
**Simplified Schematic**

## Table of Contents

## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| **Changes from Revision B (October 2003) to Revision C** | **Page** |
|---|---|
| • Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section | 1 |

## 5 Description (continued)

The Enable/Status (E/S) pin provides two functions. An input on the pin not only disables the output stage to effectively disconnect the load, but also reduces the quiescent current to conserve power. The E/S pin output can be monitored to determine if the OPA548 is in thermal shutdown.
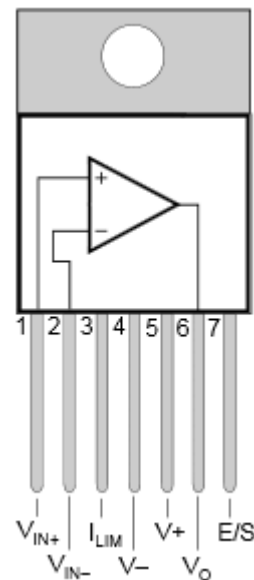
The OPA548 device is available in an industry-standard 7-lead staggered and straight lead TO-220 package, and a 7-lead DDPAK surface-mount plastic power package. The copper tab allows easy mounting to a heat sink or circuit board for excellent thermal performance. The device is specified for operation over the extended industrial temperature range, –40°C to 85°C. A SPICE macromodel is available for design analysis.

## 6 Pin Configuration and Functions

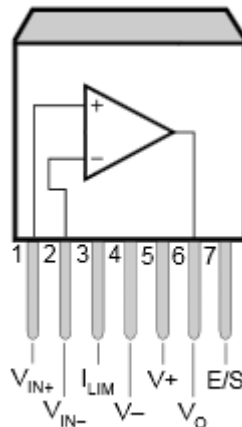**KVT and KC Packages Stagger-Formed
7-Pin TO-220
Top View**
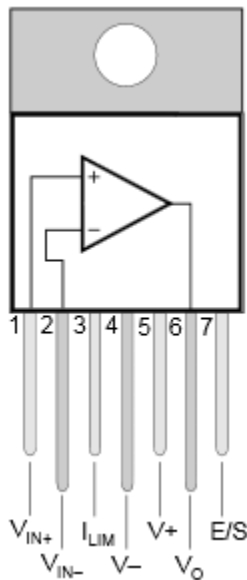


**KVT and KC Packages Straight-Formed
7-Pin TO-220
Top View**



**KTW Package Surface-Mount
7-Pin TO-263
Top View**

*Submit Documentation Feedback*   3

Product Folder Links: *OPA548*

## Pin Functions

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| $V_{IN+}$ | 1 | I | Noninverting input |
| $V_{IN-}$ | 2 | I | Inverting input |
| $I_{LIM}$ | 3 | I | Current limit set |
| V- | 4 | I | Negative power supply |
| V+ | 5 | I | Positive power supply |
| $V_O$ | 6 | O | Output |
| E/S | 7 | I/O | Enable/disable control input, thermal shutdown status output |

Product Folder Links: *OPA548*

# 7 Specifications

## 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) [1]

|  |  | MIN | MAX | UNIT |
|---|---|---|---|---|
|  | Output current | See Figure 40 | | |
|  | Supply voltage, V+ to V− | | 60 | V |
|  | Input voltage | (V−) −0.5V | (V+) + 0.5 | V |
|  | Input shutdown voltage | | | V+ |
|  | Operating temperature | −40 | 125 | °C |
|  | Junction temperature | | 150 | °C |
| $T_{stg}$ | Storage temperature | −55 | 125 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## 7.2 ESD Ratings

|  |  | VALUE | UNIT |
|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1] | ±2000 | V |
| | | Machine model | ±200 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

## 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

|  | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|
| Supply Voltage (V+-V-) | 8(+/-4) | | 60(±30) | V |
| Specified temperature | −40 | | 125 | °C |

## 7.4 Thermal Information

| THERMAL METRIC[1] | | OPA548 | | UNIT |
|---|---|---|---|---|
| | | KVT and KC (TO-220) | KTW (DDPAK) | |
| | | 7 PINS | 7 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 30.2 | 30.2 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 37.4 | 37.4 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 14.4 | 14.4 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 5.1 | 5.1 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 14.3 | 14.3 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | 0.2 | 0.2 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

## 7.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **OFFSET VOLTAGE** | | | | | | |
| Input Offset Voltage | | $V_{CM}$ = 0, $I_O$ = 0 | | ±2 | ±10 | mV |
| vs Temperature | | $T_A$ = −40°C to 85°C | | ±30 | | µV/°C |
| vs Power supply | | $V_{CM}$ = 0 V | | 30 | 100 | µV/V |
| **INPUT BIAS CURRENT**[1] | | | | | | |
| Input Bias Current[2] | | $V_{CM}$ = 0 V | −100 | −500 | | nA |
| vs Temperature | | $T_A$ = −40°C to 85°C | ±0.5 | | | nA/°C |
| Input Offset Current | | $V_{CM}$ = 0 V | ±5 | ±50 | | nA |
| **NOISE** | | | | | | |
| Input Voltage Noise Density, f = 1 kHz | | | | 90 | | nV/√Hz |
| Current Noise Density, f = 1 kHz | | | | 200 | | fA/√Hz |
| **INPUT VOLTAGE RANGE** | | | | | | |
| Common-Mode Voltage Range: | Positive | Linear Operation | (V+) − 3 | (V+) − 2.3 | | V |
| | Negative | Linear Operation | (V−) − 0.1 | (V−) − 0.2 | | V |
| Common-Mode Rejection | | $V_{CM}$ = (V−) −0.1V to (V+) −3 V | 80 | 95 | | dB |
| **INPUT IMPEDANCE** | | | | | | |
| Differential | | | | $10^7$ ‖ 6 | | Ω ‖ pF |
| Common-Mode | | | | $10^9$ ‖ 4 | | Ω ‖ pF |
| **OPEN-LOOP GAIN** | | | | | | |
| Open-Loop Voltage Gain | | $V_O$ = ±25 V, $R_L$ = 1 kΩ | 90 | 98 | | dB |
| | | $V_O$ = ±25 V, $R_L$ = 8 Ω | | 90 | | dB |
| **FREQUENCY RESPONSE** | | | | | | |
| Gain-Bandwidth Product | | $R_L$ = 8 Ω | | 1 | | MHz |
| Slew Rate | | G = 1, 50Vp-p, $R_L$ = 8 Ω | | 10 | | V/µs |
| Full-Power Bandwidth | | | See *Typical Characteristics* | | | kHz |
| Settling Time: ±0.1% | | G = −10, 50-V Step | | 15 | | µs |
| Total Harmonic Distortion + Noise, f = 1 kHz | | $R_L$ = 8 Ω, G = 3, Power = 10 W | | 0.02%[3] | | |
| **OUTPUT** | | | | | | |
| Voltage Output | Positive | $I_O$ = 3 A | (V+) − 4.1 | (V+) − 3.7 | | V |
| | Negative | $I_O$ = −3 A | (V−) + 3.7 | (V−) + 3.3 V | | |
| | Positive | $I_O$ = 0.6 A | (V+) − 2.4 | (V+) − 2.1 V | | |
| | Negative | $I_O$ = −0.6 A | (V−) + 1.3 | (V−) + 1 V | | |
| Maximum continuous current output: | DC<br>AC | ±3<br>3 | A<br>Arms | | | A<br>Arms |
| Leakage Current, Output Disabled, DC | | | See *Typical Characteristics* | | | |
| Output Current Limit | | | | | | |
| Current Limit Range | | | | 0 to ±5 | | A |
| Current Limit Equation | | | $I_{LIM}$ = (15000)(4.75)/(13750 W + $R_{CL}$) | | | A |
| Current Limit Tolerance[1] | | $R_{CL}$ = 14.8 kW ($I_{LIM}$ = ±2.5 A), $R_L$ = 8 Ω | | ±100 | ±250 | mA |
| Capacitive Load Drive | | | See Figure 19 | | | |
| **OUTPUT ENABLE /STATUS (E/S) PIN** | | | | | | |
| Shutdown Input Mode | | | | | | |
| $V_{E/S}$ HIGH (output enabled) | | E/S Pin Open or Forced High | (V−) + 2.4 | | | V |

(1) High-speed test at $T_J$ = 25°C.
(2) Positive conventional current flows into the input terminals.
(3) See Figure 12 for additional power levels.

Product Folder Links: *OPA548*

## Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

| | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| | $V_{E/S}$ LOW (output disabled) | E/S Pin Forced Low | | | (V−) + 0.8 | V |
| | $I_{E/S}$ HIGH (output enabled) | E/S Pin High | | −65 | | µA |
| | $I_{E/S}$ LOW (output disabled) | E/S Pin Low | | −70 | | µA |
| Output Disable Time | | | | 1 | | µs |
| Output Enable Time | | | | 3 | | µs |
| Thermal Shutdown Status Output | | | | | | |
| | Normal Operation | Sourcing 20 µA | (V−) + 2.4 | (V−) + 3.5 | | V |
| | Thermally Shutdown | Sinking 5 µA, $T_J$ > 160°C | | (V−) + 0.35 | (V−) + 0.8 | V |
| Junction Temperature | Shutdown | | | 160 | | °C |
| | Reset from Shutdown | | | 140 | | °C |
| **POWER SUPPLY** | | | | | | |
| Specified Voltage | | | | ±30 | | V |
| Operating Voltage Range | | | ±4 | | ±30 | V |
| Quiescent Current | | $I_{LIM}$ Connected to V−, $I_O$ = 0 | | ±17 | ±20 | mA |
| Quiescent Current, Shutdown Mode | | $I_{LIM}$ Connected to V−, $I_O$ = 0 | | ±6 | | nA |
| **TEMPERATURE RANGE** | | | | | | |
| Specified Range | | | −40 | | 85 | °C |
| Operating Range | | | −40 | | 125 | °C |
| Storage Range | | | −55 | | 125 | °C |
| Thermal Resistance, $R_{\theta JC}$ | | | | | | |
| | 7-Lead DDPAK, 7-Lead TO-220 | f > 50 Hz | | 2 | | °C/W |
| | 7-Lead DDPAK, 7-Lead TO-220 | DC | | 2.5 | | °C/W |
| Thermal Resistance, $R_{\theta JA}$ | | | | | | |
| | 7-Lead DDPAK, 7-Lead TO-220 | No Heat Sink | | 65 | | °C/W |

## 7.6 Typical Characteristics

At $T_{CASE}$ = 25°C, $V_S$ = ±30V and E/S pin open, unless otherwise noted.
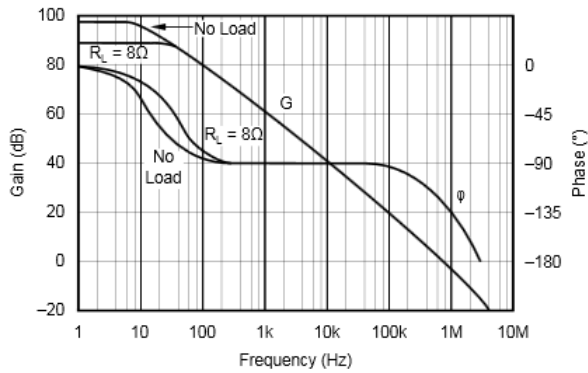


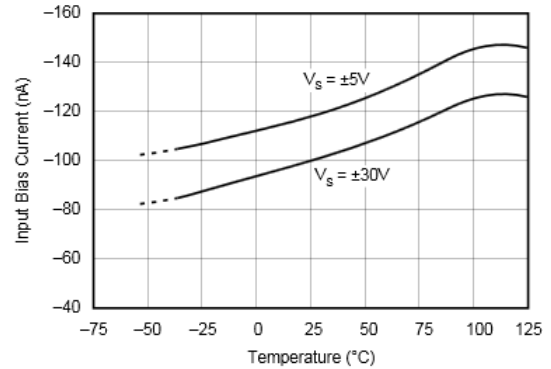Figure 1. Open-Loop Gain and Phase vs Frequency



Figure 2. Input Bias Current vs Temperature
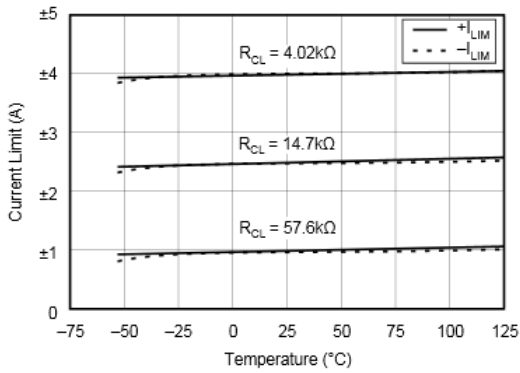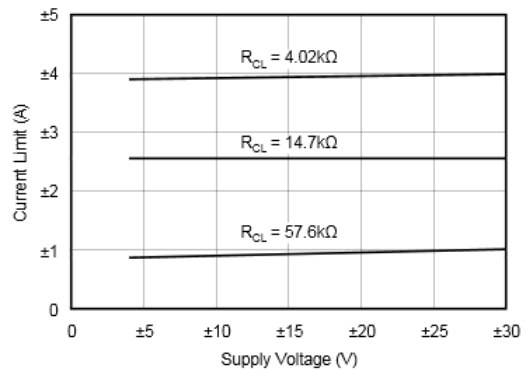


Figure 3. Current Limit vs Temperature



Figure 4. Current Limit vs Supply Voltage



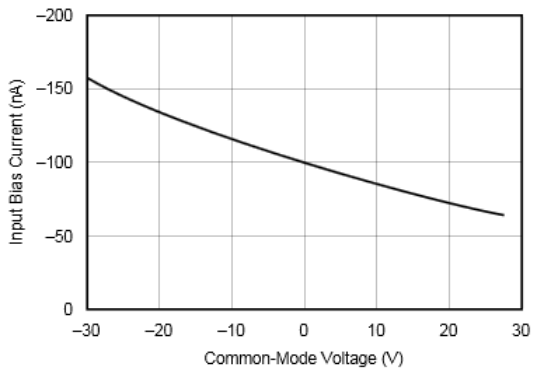Figure 5. Input Bias Current vs Common-Mode Voltage



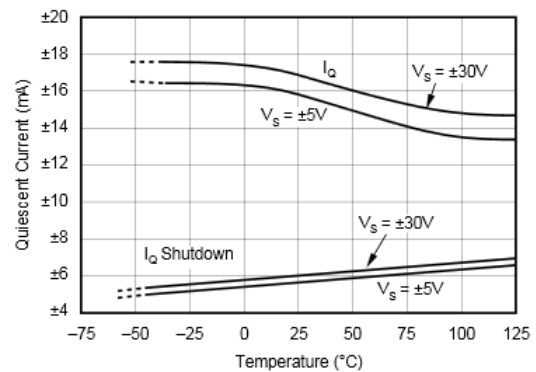Figure 6. Quiescent Current vs Temperature

Product Folder Links: *OPA548*

## Typical Characteristics (continued)

At $T_{CASE}$ = 25°C, $V_S$ = ±30V and E/S pin open, unless otherwise noted.
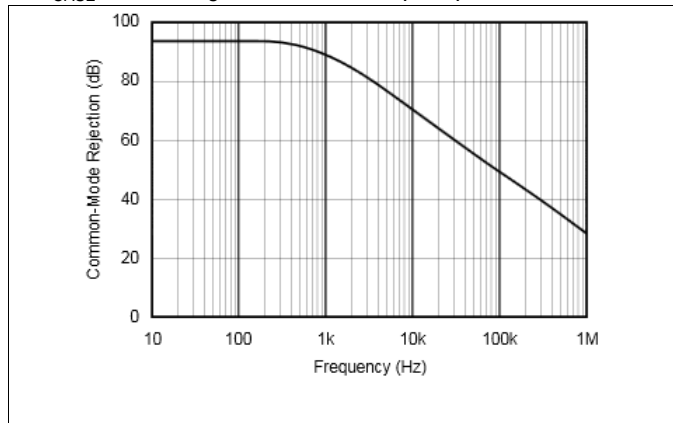


Figure 7. Common-Mode Rejection vs Frequency
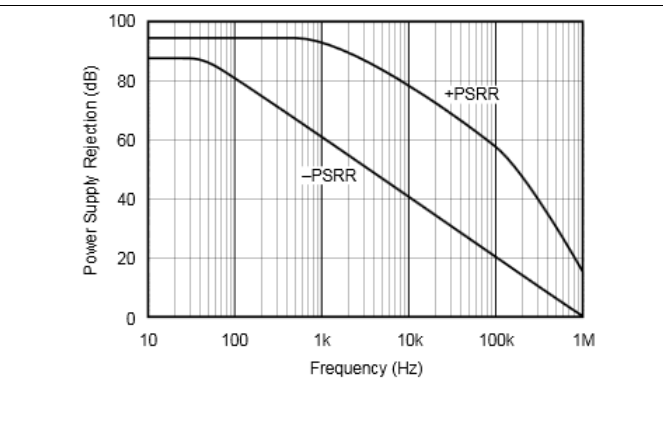


Figure 8. Power-Supply Rejection vs Frequency
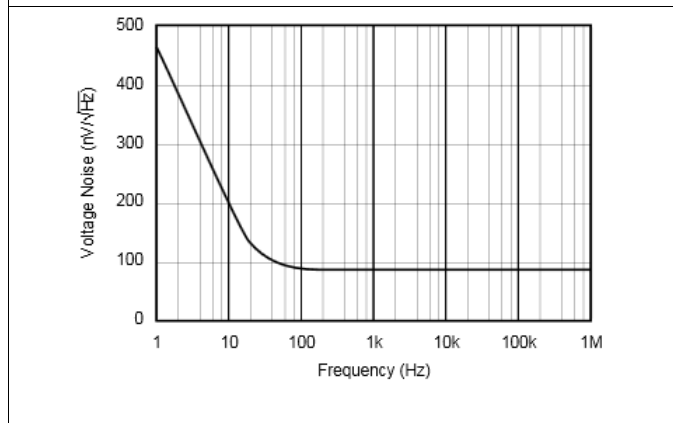


Figure 9. Voltage Noise Density vs Frequency
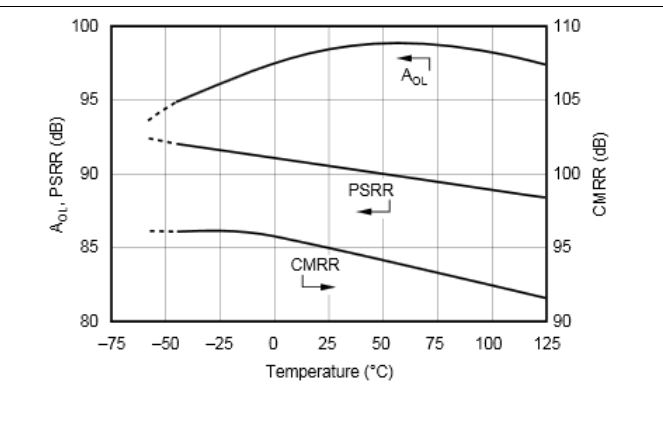


Figure 10. Open-loop Gain, Common-Mode Rejection, and Power-Supply Rejection vs Temperature
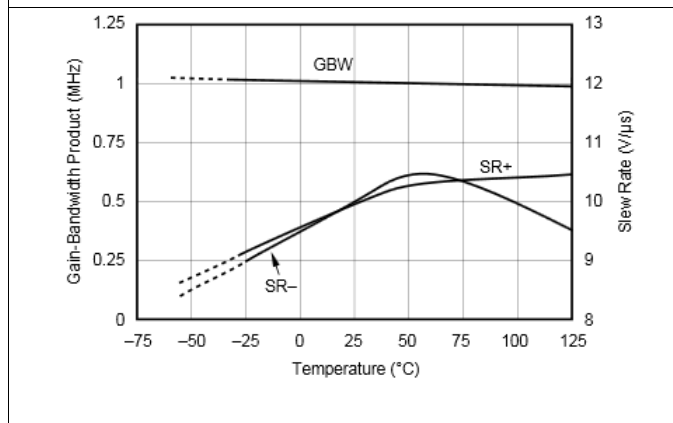


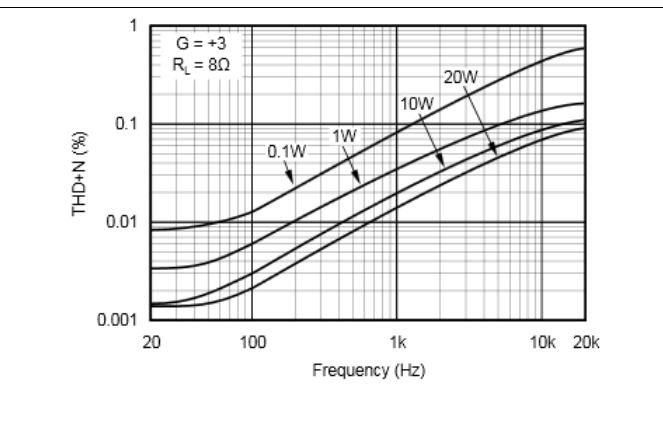Figure 11. Gain-Bandwidth Product and Slew Rate vs Temperature



Figure 12. Total Harmonic Distortion+Noise vs Frequency

## Typical Characteristics (continued)

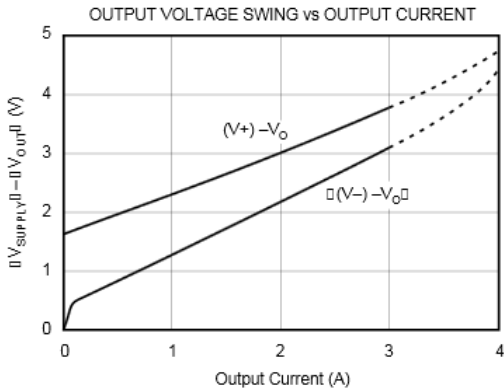At $T_{CASE}$ = 25°C, $V_S$ = ±30V and E/S pin open, unless otherwise noted.



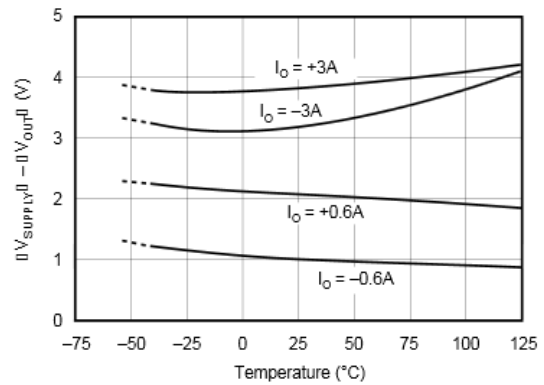Figure 13. Output Voltage Swing vs Output Current

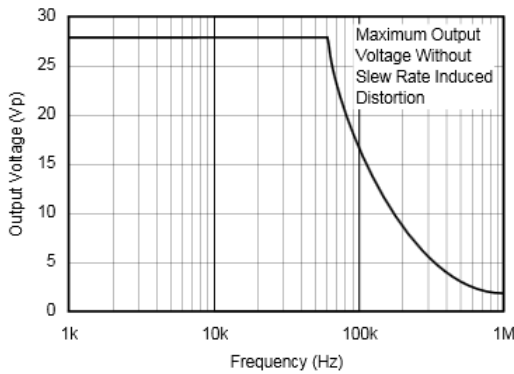

Figure 14. Output Voltage Swing vs Temperature



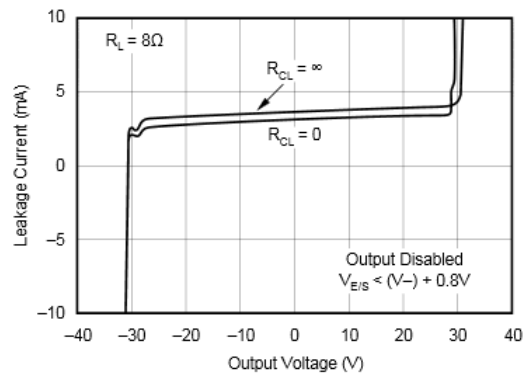Figure 15. Maximum Output Voltage Swing vs Frequency



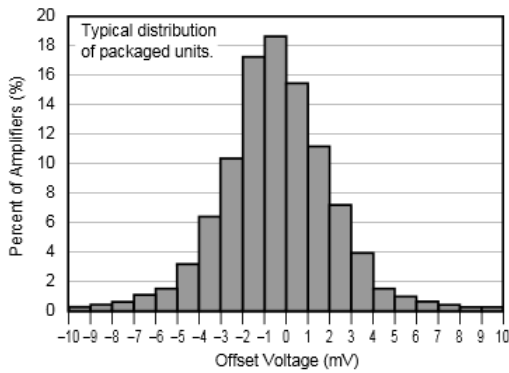Figure 16. Output Leakage Current vs Applied Output Voltage



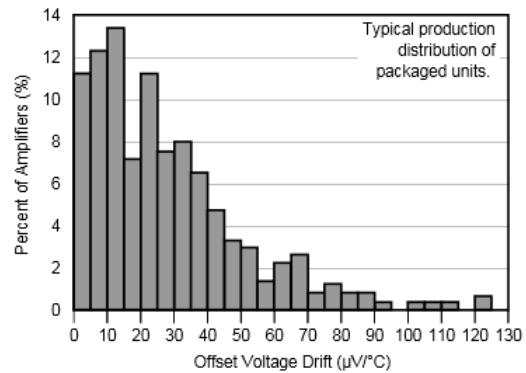Figure 17. Offset Voltage Production Distribution



Figure 18. Offset Voltage Drift Production Distribution

Product Folder Links: *OPA548*

## Typical Characteristics (continued)

At $T_{CASE}$ = 25°C, $V_S$ = ±30V and E/S pin open, unless otherwise noted.
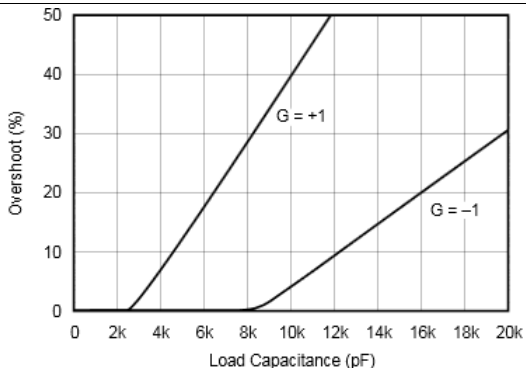


**Figure 19. Small-Signal Overshoot vs Load Capacitance**
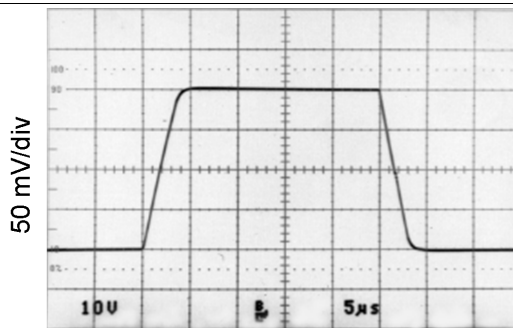


G = 3          $C_L$ = 1000 pF,          $R_L$ = 8 Ω

**Figure 20. Large-Signal Step Response**



G = 1          $C_L$ = 1000 pF

**Figure 21. Small-Signal Step Response**
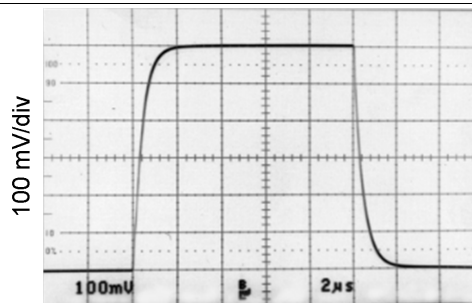


G = 3          $C_L$ = 1000 pF

**Figure 22. Small-Signal Step Response**

Product Folder Links: *OPA548*

# 8 Detailed Description

## 8.1 Overview

The OPA548 device uses a PNP input stage (resulting in negative bias currents at each input) without input bias current compensation so matched resistances on the inputs will reduce errors. After the main voltage gain stage is the high current output stage with temperature compensated class A/B biasing to reduce crossover distortion. Local feedback in the output stage may require additional compensation for highly reactive loads (see *Output Stage Compensation*).

## 8.2 Functional Block Diagram
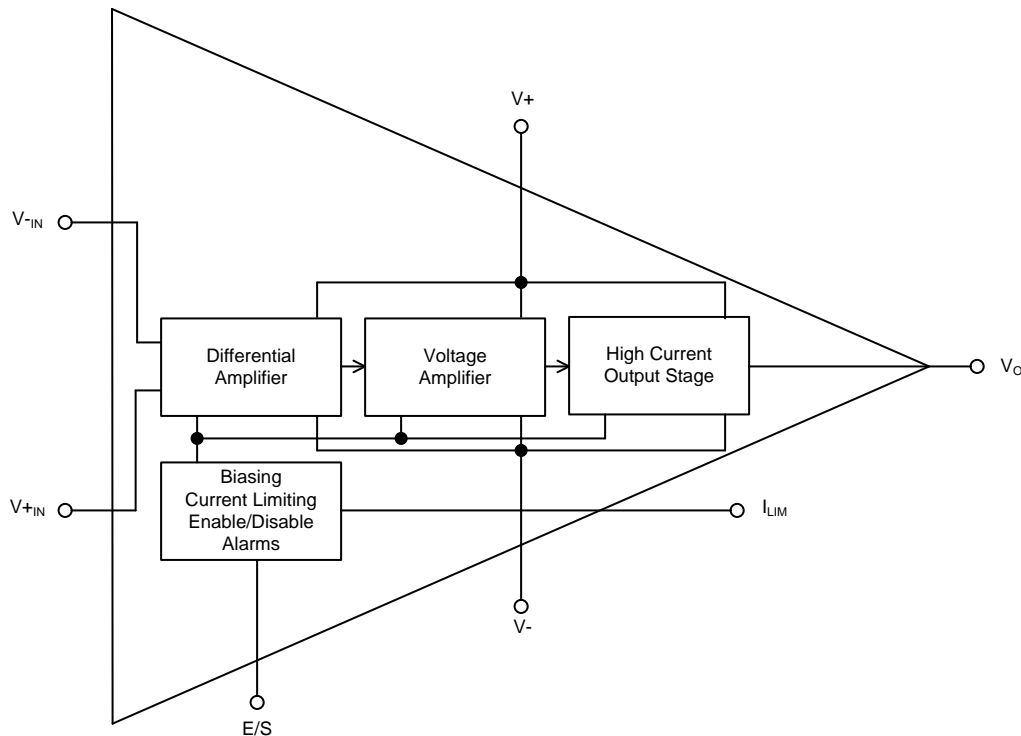


## 8.3 Feature Description

### 8.3.1 Adjustable Current Limit

The OPA548 features an accurate, user-selected current limit. The current limit is set from 0 A to 5 A by controlling the input to the $I_{LIM}$ pin. Unlike other designs, which use a power resistor in series with the output current path, the OPA548 senses the load indirectly. This allows the current limit to be set with a 0-µA to 330-µA control signal. In contrast, other designs require a limiting resistor to handle the full output current (5 A in this case).

With the OPA548, the simplest method for adjusting the current limit uses a resistor or potentiometer connected between the $I_{LIM}$ pin and V– according to the Equation 1:

$$R_{CL} = \frac{(15000)(4.75)}{I_{LIM}} - 13750 \ \Omega$$

(1)

The low-level control signal (0 µA to 330 µA) also allows the current limit to be digitally controlled.

See Figure 41 for a simplified schematic of the internal circuitry used to set the current limit. Leaving the $I_{LIM}$ pin open programs the output current to zero, while connecting $_{ILIM}$ directly to V– programs the maximum output current limit, typically 5 A.

## Feature Description (continued)

### 8.3.2  Enable/Status (E/S) Pin

The Enable/Status pin provides two functions: forcing this pin LOW disables the output stage, or E/S can be monitored to determine if the OPA548 is in thermal shutdown. One or both of these functions can be used on the same device using single or dual supplies. For normal operation (output enabled), the E/S pin can be left open or pulled HIGH (at least 2.4 V more than the negative rail). A small value capacitor connected between the E/S pin and V− may be required for noisy applications.

### 8.3.3  Thermal Shutdown Status

Internal thermal shutdown circuitry shuts down the output when the die temperature reaches approximately 160°C, resetting when the die has cooled to 140°C. The E/S pin can be monitored to determine if shutdown has occurred. During normal operation the voltage on the E/S pin is typically 3.5 V more than the negative rail. Once shutdown has occurred, this voltage drops to approximately 350 mV more than the negative rail.

## 8.4  Device Functional Modes

### 8.4.1  Output Disable

A unique feature of the OPA548 is its output disable capability. This function not only conserves power during idle periods (quiescent current drops to approximately 6 mA), but also allows multiplexing in low frequency (f < 20 kHz), multichannel applications. Signals greater than 20 kHz may cause leakage current to increase in devices that are shutdown. Figure 33 shows the two OPA548s in a switched amplifier configuration. The ON/OFF state of the two amplifiers is controlled by the voltage on the E/S pin.

To disable the output, the E/S pin is pulled LOW, no greater than 0.8 V more than the negative rail. Typically the output is shutdown in 1 μs. Figure 23 provides an example of how to implement this function using a single supply. Figure 24 gives a circuit for dual-supply applications. To return the output to an enabled state, the E/S pin should be disconnected (open) or pulled to at least (V−) + 2.4 V. It should be noted that pulling the E/S pin HIGH (output enabled) does not disable internal thermal shutdown.
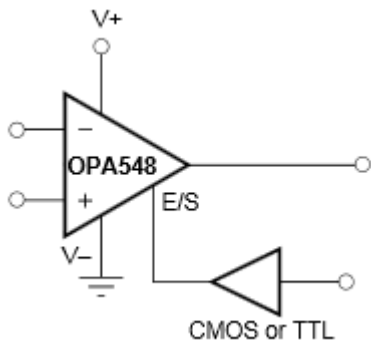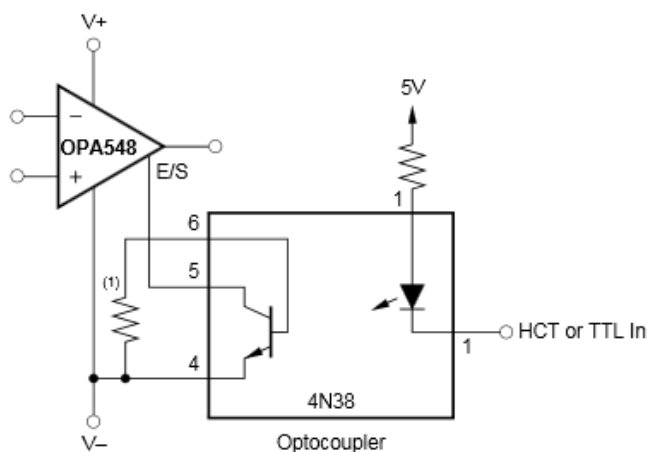


**Figure 23. Output Disable With a Single Supply**



NOTE: (1) Optional—may be required to limit leakage current of optocoupler at high temperatures.

**Figure 24. Output Disable With Dual Supplies**

# 9 Application and Implementation

> **NOTE**
>
> Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 9.1 Application Information

The OPA548 is specified for operation from 8 V to 60 V (±4 V to ±30 V). Specifications apply over the –40°C to 85°C temperature range while the device operates from –40°C to 125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in *Typical Characteristics*.

## 9.2 Typical Applications

### 9.2.1 Basic Circuit Connections

Figure 25 shows the OPA548 connected as a basic noninverting amplifier. The OPA548 can be used in virtually any operational amplifier configuration.

Power-supply terminals should be bypassed with low series impedance capacitors. The technique shown in Figure 45, using a ceramic and tantalum type in parallel is recommended. In addition, we recommend a 0.01-μF capacitor between V+ and V– as close to the OPA548 as possible. Power-supply wiring should have low series impedance.
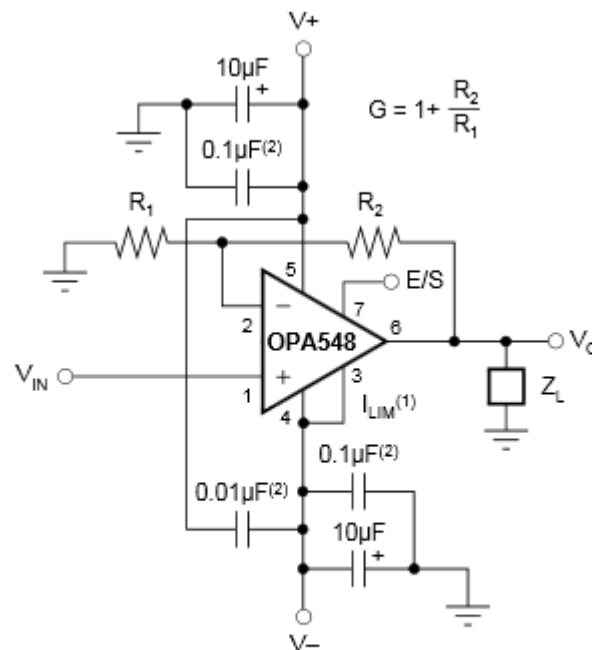


NOTES: (1) $I_{LIM}$ connected to V– gives the maximum current limit, 5A (peak). (2) Connect capacitors directly to package power-supply pins.

**Figure 25.  Basic Circuit Connections Example**

Product Folder Links: *OPA548*

## Typical Applications (continued)

### 9.2.1.1 Design Requirements

To design an example of a noninverting circuit, the following requirements are spelled out:
*   Gain: 1
*   Output voltage swing: ±10 V
*   Maximum Output Current: ±2.5 A
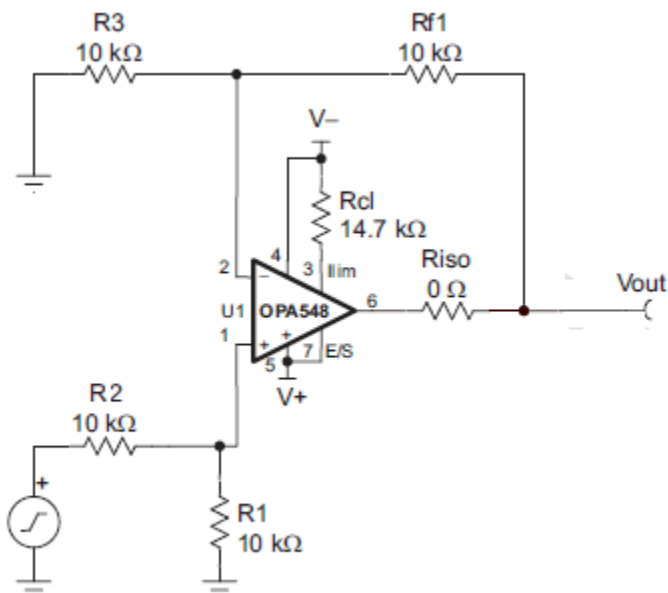*   Load: 4-Ω resistive
*   Ambient Temperature: Up to 40°C



**Figure 26. Noninverting Amplifier Configuration Schematic**

### 9.2.1.2 Detailed Design Procedure

#### 9.2.1.2.1 Power Supply Requirements

Select the power supply based on the requirement to achieve a ±10-V output with up to a 2.5-A load. The maximum value for output voltage swing at 3-A is approximately within 4 V of either rail, standard 15-V power supplies rated at >2.5 A each will suffice.

#### 9.2.1.2.2 Gain Setting and Input Configuration

A unity gain noninverting application could be provided by simply connecting the output of an operational amplifier back to its input, with the signal applied to the noninverting input. Power operational amplifiers are frequently subject to unpredictable load impedances that can cause instability. Increasing gain can enhance stability. Furthermore, the feedback network provides locations for further opportunities for stability enhancing components if necessary.

In this application two 10-kΩ resistors are used for the input and feedback resistance, which would normally result in a noninverting gain of 2. Adding a voltage divider consisting of R1 and R2 reduces the input signal by half before it is applied to the operational amplifier. In this case the solution just happens to restore us back to the desired overall gain of 1. This solution using an identical pair of resistors before the noninverting input between the signal and ground creates what is known as a difference amplifier.

Product Folder Links: *OPA548*

## Typical Applications (continued)

### 9.2.1.2.3  Current Limit

The OPA548 provides means to limit the maximum output current delivered by the amplifier. A resistor between the negative supply and the amplifier`s Ilim pin, or a DAC can be used to set the current limit. For this circuit a 14.7-kΩ resistor (Rcl) limits the output current to approximately 2.5 A.

### 9.2.1.2.4  Safe-Operating-Area

Plotting the load on the Safe-Operating-Area (SOA) curve allows the safety of the application to be assessed. Figure 40 depicts the 4-Ω load on the curve. With a resistive load, maximum dissipation occurs at an output voltage one-half of the supply voltage, in this case 7.5 V and 1.875 A for 22.5 W.

Consideration should be given to the condition of a shorted output. In this application this is a stress of 15 V at 2.5 A on the output stage, or 37.5 W which is just within the 50-W SOA of the OPA548. How long the circuit can withstand a short to ground will be determined by the size of the heatsink. Ultimately the thermal shutdown will activate providing short circuit protection, although even this is not recommended as a continuous condition.

### 9.2.1.2.5  Heat Sinking

From Safe-Operating-Area we know we will must support 22.5 W of dissipation up to the 40°C ambient requirements of the application. This indicates the need for a heatsink with a $R_{\theta HA}$ < 2.5°C/W, such as an Aavid Thermalloy 530002B02500G.

### 9.2.1.3  Application Curve

Figure 27 shows the expected results for the Noninverting Operation of the OPA548. The left picture shows the Noninverting Operation in dual supply mode and the right picture shows the Noninverting Operation in single supply mode. The input signal is a zero-centered sine wave with an amplitude of 10 V p-p and a frequency of 1 kHz. In this trace the OPA548 is delivering a peak current of 1.25 A to the 4-Ω load.
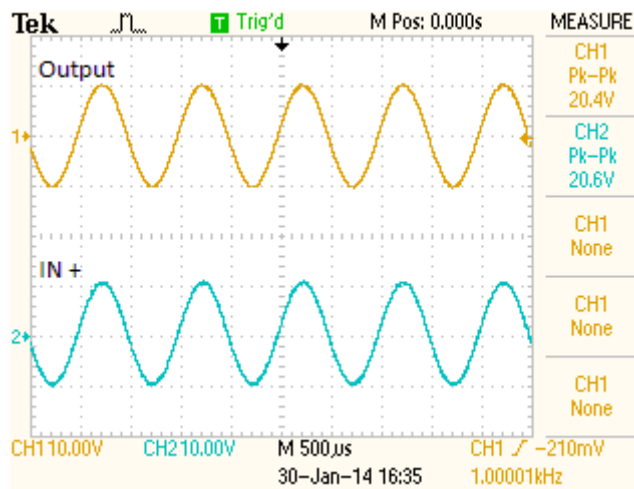


**Figure 27. Noninverting Operation, Dual-Supply Waveforms**

Product Folder Links: *OPA548*

## Typical Applications (continued)

### 9.2.2 Monitoring Single- and Dual-Supplies

Figure 28 gives an example of monitoring shutdown in a single-supply application. Figure 29 provides a circuit for dual supplies. External logic circuitry or an LED could be used to indicate if the output has been thermally shutdown, see Figure 31.
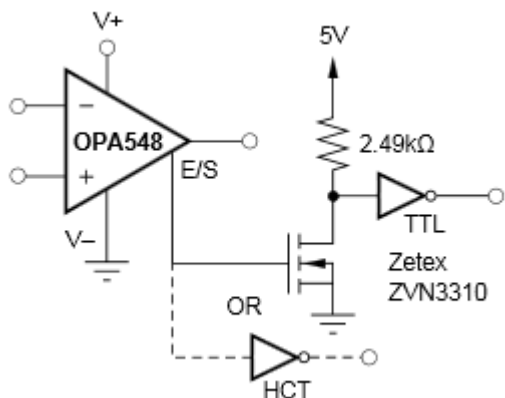


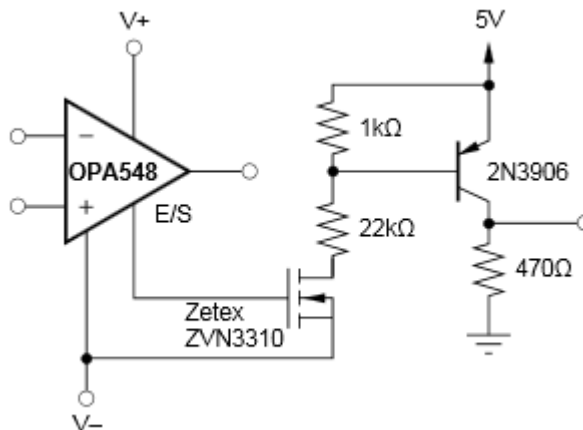**Figure 28. Thermal Shutdown Status With a Single-Supply**



**Figure 29. Thermal Shutdown Status With Dual-Supplies**

#### 9.2.2.1 Design Requirements

See the previous *Design Requirements*.

#### 9.2.2.2 Detailed Design Procedure

##### 9.2.2.2.1 Output Disable and Thermal Shutdown Status

As mentioned earlier, the OPA548's output can be disabled and the disable status can be monitored simultaneously. Figure 28 and Figure 29 provide examples interfacing to the E/S pin while using a single supply and dual supplies, respectively.

## Typical Applications (continued)

### 9.2.3 Programmable Power Supply

A programmable source or sink power supply can easily be built using the OPA548. Both the output voltage and output current are user-controlled. See Figure 30 for a circuit using potentiometers to adjust the output voltage and current while Figure 31 uses DACs. An LED tied to the E/S pin through a logic gate indicates if the OPA548 is in thermal shutdown.

Figure 30 illustrates how to use the OPA548 to provide an accurate voltage source with only three external resistors. First, the current limit resistor, $R_{CL}$, is chosen according to the desired output current. The resulting voltage at the $I_{LIM}$ pin is constant and stable over temperature. This voltage, $V_{CL}$, is connected to the noninverting input of the operational amplifier and used as a voltage reference, thus eliminating the need for an external reference. The feedback resistors are selected to gain $V_{CL}$ to the desired output voltage level.
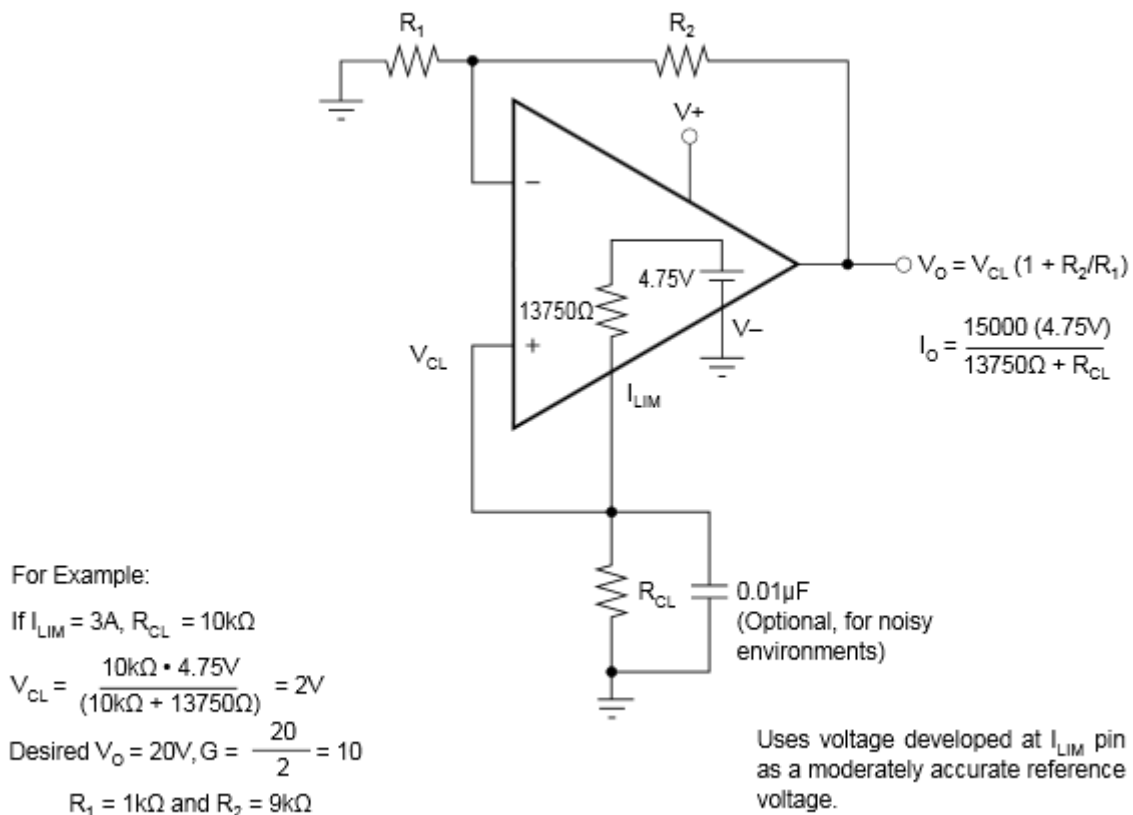


For Example:

If $I_{LIM}$ = 3A, $R_{CL}$ = 10kΩ

$$V_{CL} = \frac{10k\Omega \cdot 4.75V}{(10k\Omega + 13750\Omega)} = 2V$$

Desired $V_O$ = 20V, G = $\dfrac{20}{2}$ = 10

$R_1$ = 1kΩ and $R_2$ = 9kΩ

$$V_O = V_{CL} (1 + R_2/R_1)$$

$$I_O = \frac{15000 \,(4.75V)}{13750\Omega + R_{CL}}$$

0.01μF
(Optional, for noisy environments)

Uses voltage developed at $I_{LIM}$ pin as a moderately accurate reference voltage.

**Figure 30. Voltage Source Schematic**

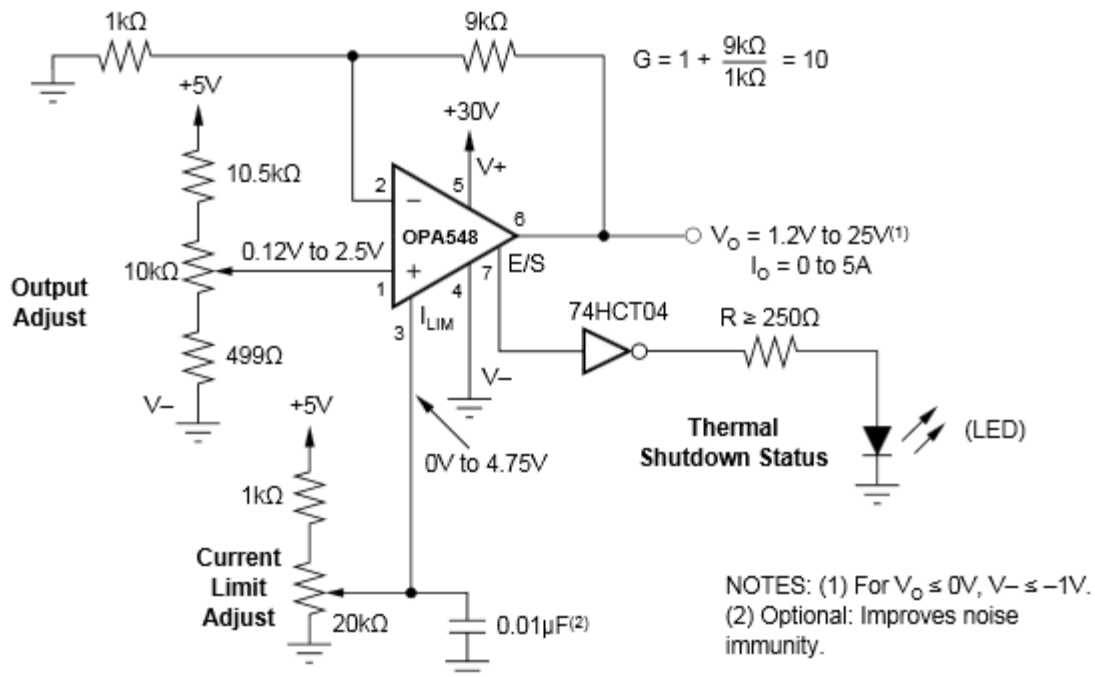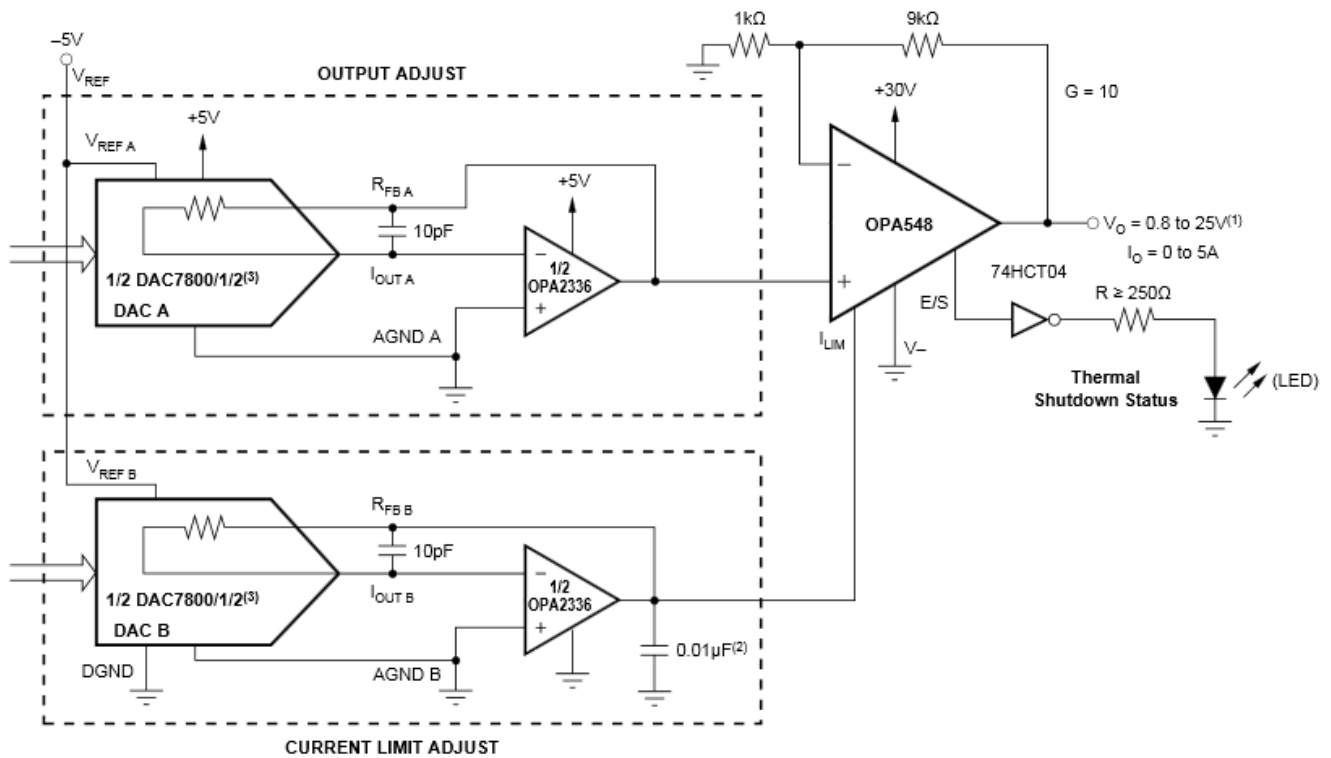## Typical Applications (continued)



**Figure 31. Resistor-Controlled Programmable Power Supply Schematic**

## Typical Applications (continued)



NOTES: (1) For $V_O \leq 0V$, $V- \leq -1V$. (2) Optional, improves noise immunity. (3) Chose DAC780X based on digital interface: DAC7800—12-bit interface, DAC7801—8-bit interface + 4 bits, DAC7802—serial interface.

**Figure 32.  Digitally-Controlled Programmable Power Supply Schematic**

Product Folder Links: *OPA548*
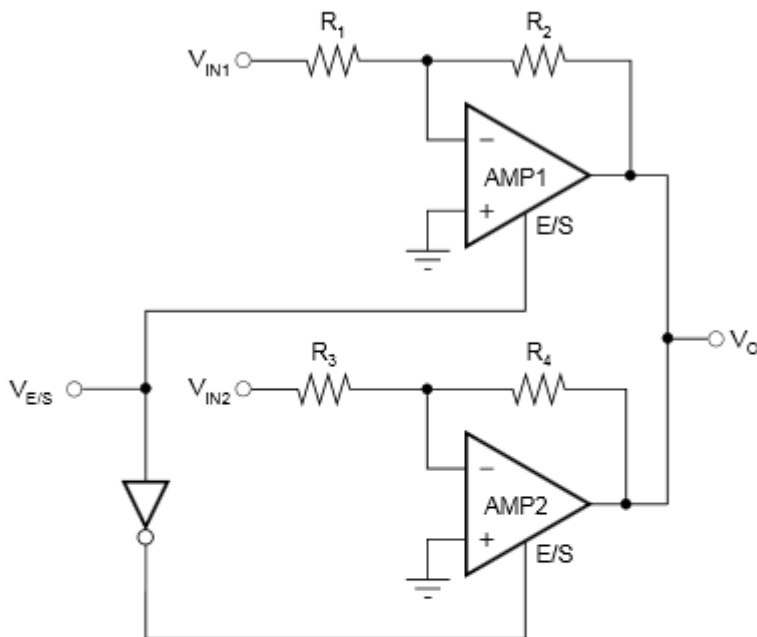
## 9.3  System Examples



$V_{E/S} > (V-) +2.4V$: Amp 1 is on, Amp 2 if off

$$\longrightarrow V_O = -V_{IN1}\left(\frac{R_2}{R_1}\right)$$

$V_{E/S} < (V-) +2.4V$: Amp 2 is on, Amp 1 if off

$$\longrightarrow V_O = -V_{IN2}\left(\frac{R_4}{R_3}\right)$$

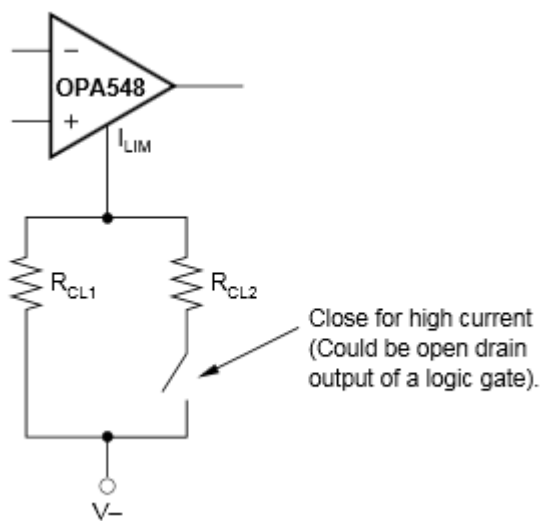**Figure 33.  Switched Amplifier Schematic**



**Figure 34.  Multiple Current Limit Values Schematic**
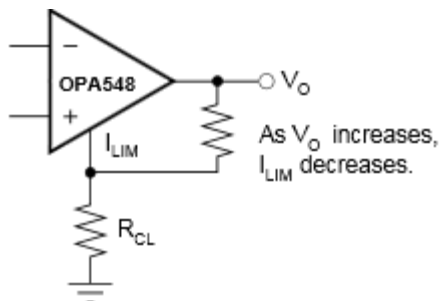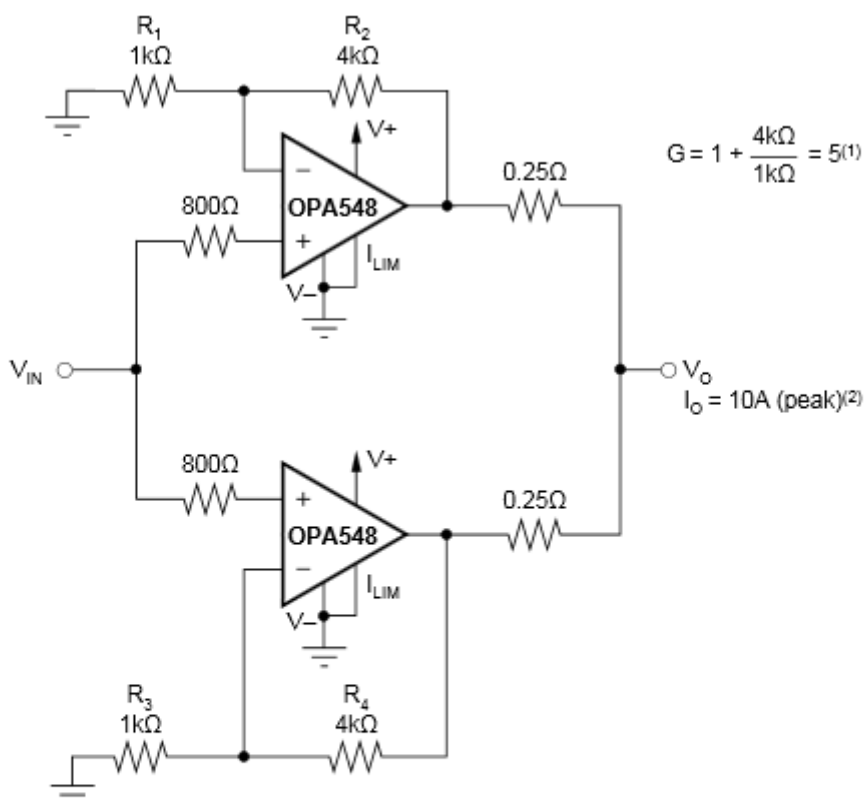
## System Examples (continued)



**Figure 35. Single Quadrant V × I Limiting**



$$G = 1 + \frac{4k\Omega}{1k\Omega} = 5^{(1)}$$

$I_O = 10A \text{ (peak)}^{(2)}$

NOTES: (1) Works well for G < 10. Input offset causes output current to flow between amplifiers with G > 10. Gains (resistor ratios) of the two amplifiers should be carefully matched to ensure equal current sharing. (2) As configured ($I_{LIM}$ connected to V−) output current limit is set to 10A (peak). Each amplifier is limited to 5A (peak). Other current limit values may be obtained, see Figure 3, "Adjustable Current Limit".

**Figure 36. Parallel Output for Increased Output Current Schematic**

Product Folder Links: *OPA548*

# 10  Power Supply Recommendations

The OPA548 operates from single (8 V to 60 V) or dual (±4 V to ±30 V) supplies with excellent performance. Most behavior remains unchanged throughout the full operating voltage range. Parameters which vary significantly with operating voltage are shown Typical Characteristics.

Some applications do not require equal positive and negative output voltage swing. Power-supply voltages do not must be equal. The OPA548 can operate with as little as 8 V between the supplies and with up to 60 V between the supplies. For example, the positive supply could be set to 55 V with the negative supply at –5 V, or vice-versa.

## 10.1  Output Stage Compensation

The complex load impedances common in power operational amplifier applications can cause output stage instability. For normal operation output compensation circuitry is typically not required. However, if the OPA548 is intended to be driven into current limit, an R/C network may be required. See Figure 38 for an output series R/C compensation (snubber) network which generally provides excellent stability.

A snubber circuit may also enhance stability when driving large capacitive loads (> 1000 pF) or inductive loads (motors, loads separated from the amplifier by long cables). Typically 3 Ω to 10 Ω in series with 0.01 µF to 0.1 µF is adequate. Some variations in circuit value may be required with certain loads.

## 10.2  Output Protection

Reactive and EMF-generating loads can return load current to the amplifier, causing the output voltage to exceed the power-supply voltage. This damaging condition can be avoided with clamp diodes from the output terminal to the power supplies, as shown in Figure 38. Schottky rectifier diodes with a 5 A or greater continuous rating are recommended.
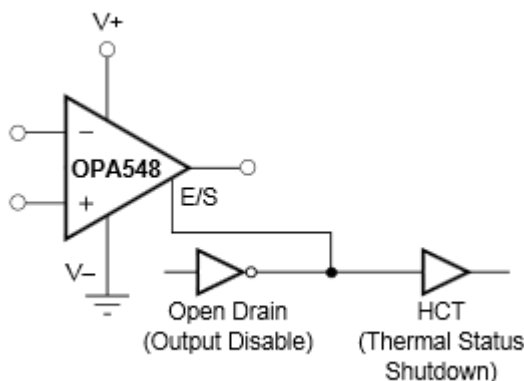


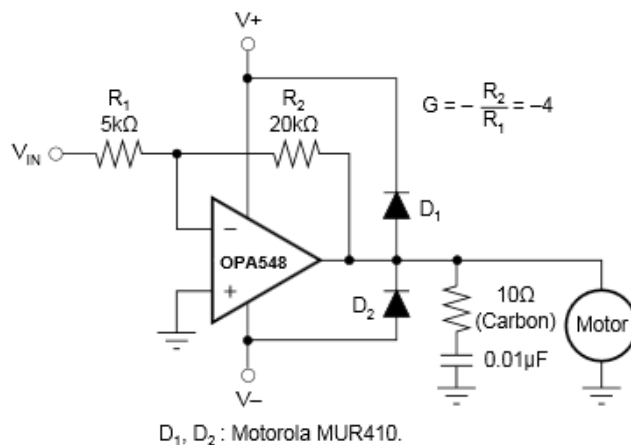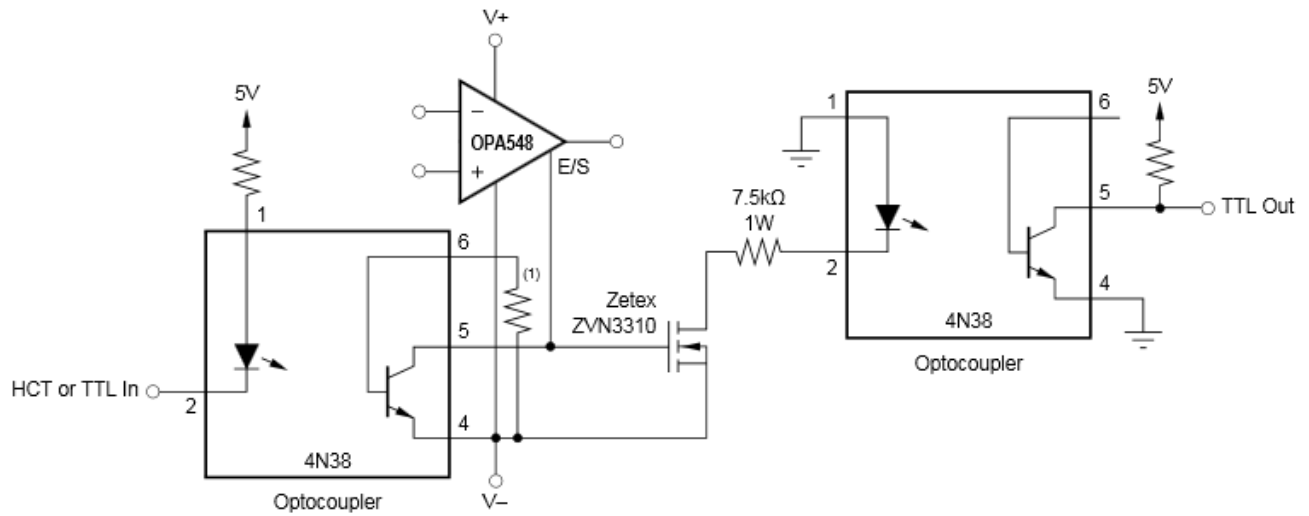**Figure 37. Output Disable and Thermal Shutdown Status With a Single Supply**

**Figure 38. Motor Drive Circuit**

## Output Protection (continued)



NOTE: (1) Optional—may be required to limit leakage
current of optocoupler at high temperatures.

**Figure 39.  Output Disable and Thermal Shutdown Status With Dual Supplies**

# 11  Layout

## 11.1  Layout Guidelines

### 11.1.1  Safe Operating Area

Stress on the output transistors is determined both by the output current and by the output voltage across the conducting output transistor, $V_S - V_O$. The power dissipated by the output transistor is equal to the product of the output current and the voltage across the conducting transistor, $V_S - V_O$. The Safe Operating Area (SOA curve, Figure 40) shows the permissible range of voltage and current.
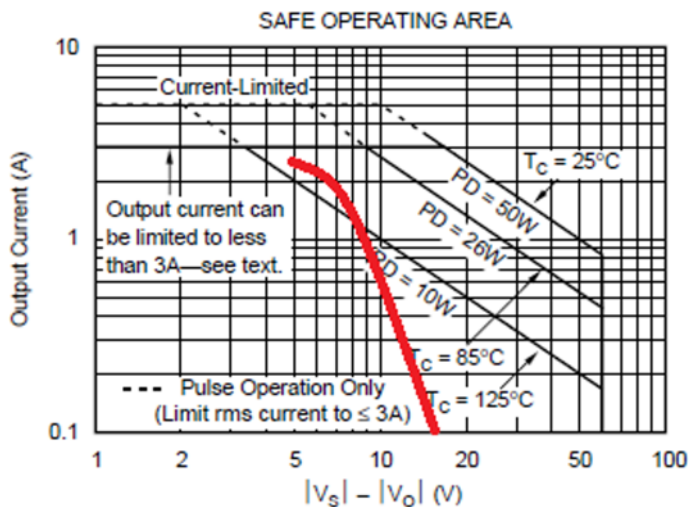


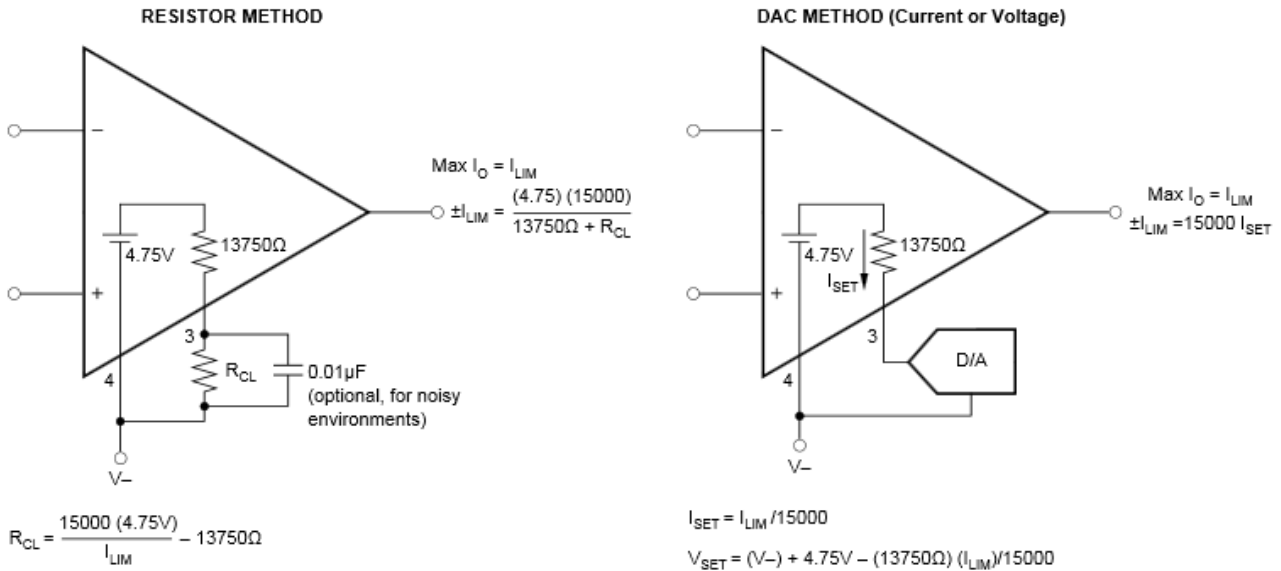**Figure 40.  4-Ω Load Plotted on OPA548 SOA for this Application**

The safe output current decreases as $V_S - V_O$ increases. Output short circuits are a very demanding case for SOA. A short-circuit to ground forces the full power-supply voltage (V+ or V−) across the conducting transistor. Increasing the case temperature reduces the safe output current that can be tolerated without activating the thermal shutdown circuit of the OPA548. For further insight on SOA, consult Application Bulletin SBOA022.

### 11.1.2  Amplifier Mounting

Figure 46 provides recommended solder footprints for both the TO-220 and DDPAK power packages. The tab of both packages is electrically connected to the negative supply, V−. It may be desirable to isolate the tab of the TO-220 package from its mounting surface with a mica (or other film) insulator (see Figure 43). For lowest overall thermal resistance it is best to isolate the entire heat sink/OPA548 structure from the mounting surface rather than to use an insulator between the semiconductor and heat sink.

For best thermal performance, the tab of the DDPAK surface-mount version should be soldered directly to a circuit board copper area. Increasing the copper area improves heat dissipation. See Figure 44 for typical thermal resistance from junction-to-ambient as a function of the copper area.

## Layout Guidelines (continued)



**RESISTOR METHOD**

Max $I_O = I_{LIM}$

$$\pm I_{LIM} = \frac{(4.75)(15000)}{13750\Omega + R_{CL}}$$

4.75V   13750Ω

$R_{CL}$   0.01µF
(optional, for noisy environments)

$$R_{CL} = \frac{15000\,(4.75V)}{I_{LIM}} - 13750\Omega$$

**DAC METHOD (Current or Voltage)**

Max $I_O = I_{LIM}$

$\pm I_{LIM} = 15000\,I_{SET}$

4.75V   13750Ω
$I_{SET}$

D/A

$I_{SET} = I_{LIM}/15000$

$V_{SET} = (V-) + 4.75V - (13750\Omega)\,(I_{LIM})/15000$

**OPA547 CURRENT LIMIT: 0 to 5A**

| DESIRED CURRENT LIMIT | RESISTOR[1] ($R_{CL}$) | CURRENT ($I_{SET}$) | VOLTAGE ($V_{SET}$) |
|---|---|---|---|
| 0A | $I_{LIM}$ Open | 0µA | (V−) + 4.75V |
| 1A | 57.6kΩ | 67µA | (V−) + 3.8V |
| 2.5A | 14.7kΩ | 167µA | (V−) + 2.5V |
| 3A | 10kΩ | 200µA | (V−) + 2V |
| 4A | 4.02kΩ | 267µA | (V−) + 1.1V |
| 5A | $I_{LIM}$ Connected to V− | 333µA | (V−) |

NOTE: (1) Resistors are nearest standard 1% values.

**Figure 41. Adjustable Current Limit**

## 11.2 Layout Example
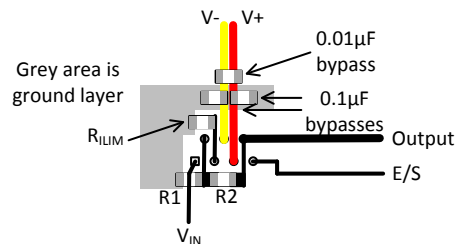


**Figure 42. Recommended Layout Example**

## 11.3 Power Dissipation

Power dissipation depends on power supply, signal, and load conditions. For DC signals, power dissipation is equal to the product of output current times the voltage across the conducting output transistor. Power dissipation can be minimized by using the lowest possible power-supply voltage necessary to assure the required output voltage swing.

For resistive loads, the maximum power dissipation occurs at a DC output voltage of one-half the power-supply voltage. Dissipation with AC signals is lower. Application Bulletin SBOA022 explains how to calculate or measure power dissipation with unusual signals and loads.
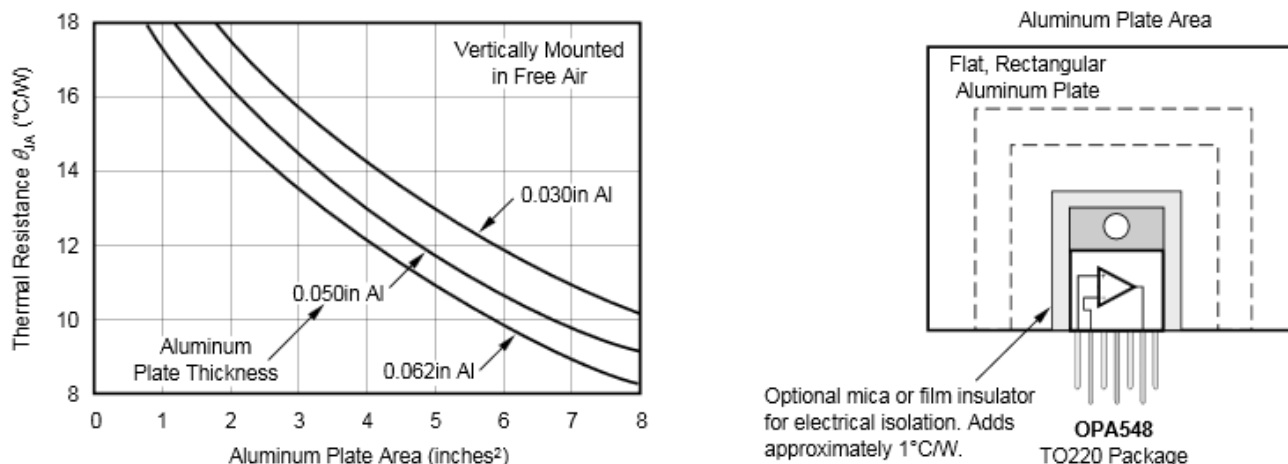
## Power Dissipation (continued)



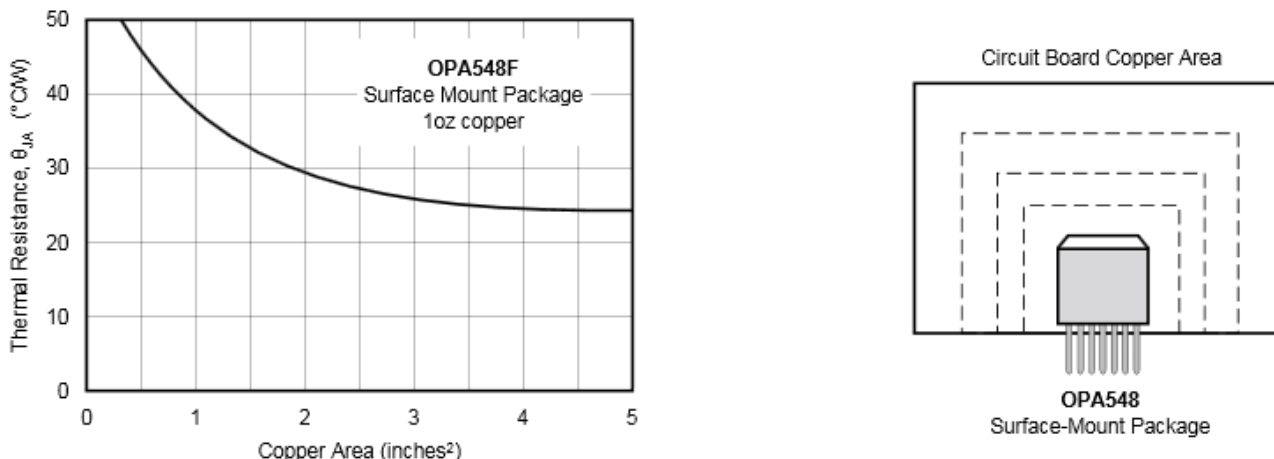**Figure 43.  TO-220 Thermal Resistance vs Aluminum Plate Area**



**Figure 44.  DDPAK Thermal Resistance vs Circuit Board Copper Area**

## 11.4  Thermal Considerations

Power dissipated in the OPA548 will cause the junction temperature to rise. The OPA548 has thermal shutdown circuitry that protects the amplifier from damage. The thermal protection circuitry disables the output when the junction temperature reaches approximately 160°C, allowing the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry is again enabled. Depending on load and signal conditions, the thermal protection circuit may cycle on and off. This limits the dissipation of the amplifier but may have an undesirable effect on the load.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heat sink. For reliable operation, junction temperature should be limited to 125°C, maximum. To estimate the margin of safety in a complete design (including heat sink) increase the ambient temperature until the thermal protection is triggered. Use worst-case load and signal conditions. For good reliability, thermal protection should trigger more than 35°C more than the maximum expected ambient condition of your application. This produces a junction temperature of 125°C at the maximum expected ambient condition.

The internal protection circuitry of the OPA548 was designed to protect against overload conditions. It was not intended to replace proper heat sinking. Continuously running the OPA548 into thermal shutdown will degrade reliability.

## 11.5 Heat Sinking

Most applications require a heat sink to assure that the maximum operating junction temperature (125°C) is not exceeded. In addition, the junction temperature should be kept as low as possible for increased reliability. Junction temperature can be determined according to the equation:

$T_J = T_A + P_D R_{\theta JA}$

where

- $R_{\theta JA} = R_{\theta JC} + R_{\theta CH} + R_{\theta HA}$
- $T_J$ = Junction Temperature (°C)
- $T_A$ = Ambient Temperature (°C)
- $P_D$ = Power Dissipated (W)
- $R_{\theta JC}$ = Junction-to-Case Thermal Resistance (°C/W)
- $R_{\theta CH}$ = Case-to-Heat Sink Thermal Resistance (°C/W)
- $R_{\theta HA}$ = Heat Sink-to-Ambient Thermal Resistance (°C/W)
- $R_{\theta JA}$ = Junction-to-Air Thermal Resistance (°C/W) (2)

Figure 45 shows maximum power dissipation versus ambient temperature with and without the use of a heat sink. Using a heat sink significantly increases the maximum power dissipation at a given ambient temperature as shown.

The difficulty in selecting the heat sink required lies in determining the power dissipated by the OPA548. For DC output into a purely resistive load, power dissipation is simply the load current times the voltage developed across the conducting output transistor, $P_D = I_L(V_S-V_O)$. Other loads are not as simple. Consult Application Bulletin SBOA022 for further insight on calculating power dissipation. Once power dissipation for an application is known, the proper heat sink can be selected.
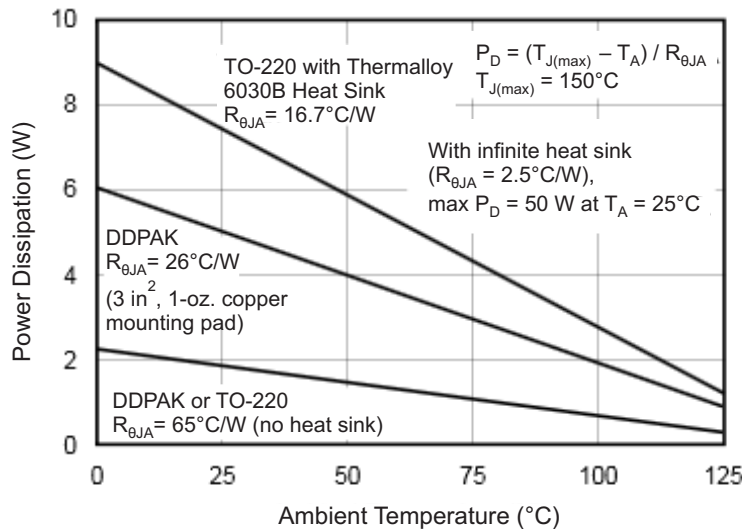


**Figure 45. Maximum Power Dissipation vs Ambient Temperature**

### 11.5.1 Heat Sink Selection Example

A TO-220 package is dissipating 5 W. The maximum expected ambient temperature is 40°C. Find the proper heat sink to keep the junction temperature less than 125°C (150°C minus 25°C safety margin).

Combining Equation 2 and Equation 3 gives:

$T_J = T_A + P_D(R_{\theta JC} + R_{\theta CH} + R_{\theta HA})$ (3)

$T_J$, $T_A$, and $P_D$ are given. $R_{\theta JC}$ is provided in the specification table, 2.5°C/W (DC). $R_{\theta CH}$ can be obtained from the heat sink manufacturer. Its value depends on heat sink size, area, and material used. Semiconductor package type, mounting screw torque, insulating material used (if any), and thermal joint compound used (if any) also affect $R_{\theta CH}$. A typical $R_{\theta CH}$ for a TO-220 mounted package is 1°C/W. Now we can solve for $R_{\theta HA}$:

## Heat Sinking (continued)

$$\theta_{HA} = \frac{T_J - T_A}{P_D} - \left(\theta_{JC} + \theta_{CH}\right)$$

$$\theta_{HA} = \frac{125°C - 40°C}{5W} - \left(2.5°C\,/\,W + 1°C\,/\,W\right) = 13.5°C\,/\,W$$

(4)

To maintain junction temperature less than 125°C, the heat sink selected must have a $R_{\theta HA}$ less than 14°C/W. In other words, the heat sink temperature rise above ambient must be less than 67.5°C (13.5°C/W × 5 W). For example, at 5-W Thermalloy model number 6030B has a heat sink temperature rise of 66°C more than ambient ($R_{\theta HA}$ = 66°C / 5 W = 13.2°C / W), which is less than the 67.5°C required in this example. Figure 45 shows power dissipation versus ambient temperature for a TO-220 package with a 6030B heat sink.

Another variable to consider is natural convection versus forced convection air flow. Forced-air cooling by a small fan can lower $R_{\theta JCA}$ ($R_{\theta CH}$ + $R_{\theta HA}$) dramatically. Heat sink manufactures provide thermal data for both of these cases. For additional information on determining heat sink requirements, consult Application Bulletin SBOA021.

As mentioned earlier, once a heat sink has been selected, the complete design should be tested under worst-case load and signal conditions to ensure proper thermal protection.

## 12 Device and Documentation Support

### 12.1 Device Support

#### 12.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

### 12.2 Documentation Support

#### 12.2.1 Related Documentation

*Heat Sinking — TO-3 Thermal Model*, SBOA021

### 12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 12.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

### 12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 13  Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
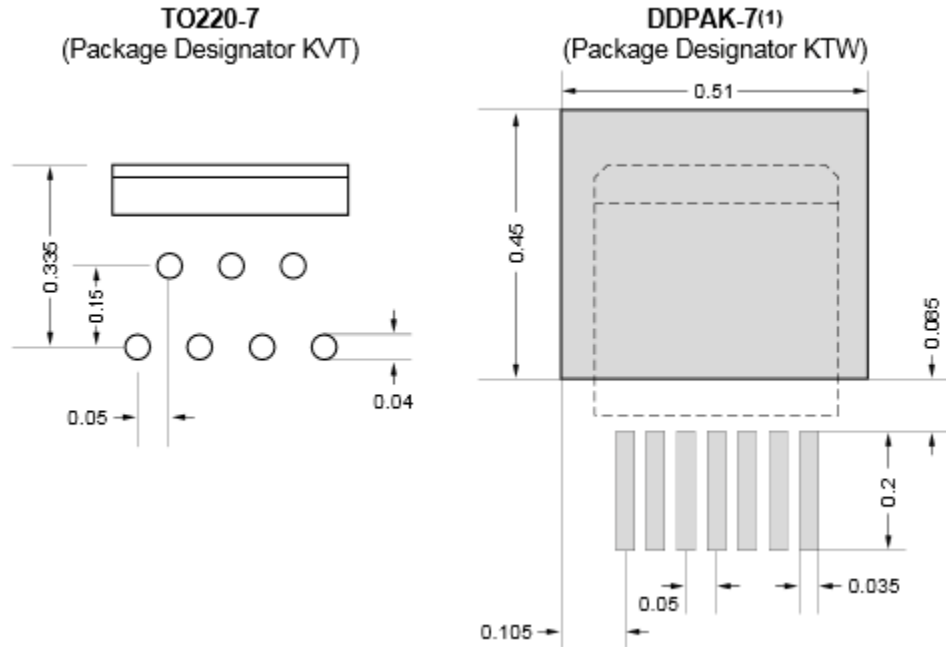


(1) For improved thermal performance, increase footprint area. See Figure 44.

(2) Mean dimensions in inches. Refer to the mechanical drawings or www.ti.com for tolerances and detailed package drawings.

**Figure 46.  TO-220 and DDPAK Solder Footprints**

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| OPA548F/500 | ACTIVE | DDPAK/ TO-263 | KTW | 7 | 500 | Green (RoHS & no Sb/Br) | CU SN | Level-2-260C-1 YEAR | -40 to 85 | OPA548F | Samples |
| OPA548F/500G3 | ACTIVE | DDPAK/ TO-263 | KTW | 7 | 500 | Green (RoHS & no Sb/Br) | CU SN | Level-2-260C-1 YEAR | -40 to 85 | OPA548F | Samples |
| OPA548FKTWT | ACTIVE | DDPAK/ TO-263 | KTW | 7 | 250 | Green (RoHS & no Sb/Br) | CU SN | Level-2-260C-1 YEAR | -40 to 85 | OPA548F | Samples |
| OPA548FKTWTG3 | ACTIVE | DDPAK/ TO-263 | KTW | 7 | 250 | Green (RoHS & no Sb/Br) | CU SN | Level-2-260C-1 YEAR | -40 to 85 | OPA548F | Samples |
| OPA548T | ACTIVE | TO-220 | KVT | 7 | 50 | Green (RoHS & no Sb/Br) | CU SN | N / A for Pkg Type | -40 to 85 | OPA548T | Samples |
| OPA548T-1 | ACTIVE | TO-220 | KC | 7 | 50 | Green (RoHS & no Sb/Br) | CU SN | N / A for Pkg Type | -40 to 85 | OPA548T | Samples |
| OPA548T-1G3 | ACTIVE | TO-220 | KC | 7 | 50 | Green (RoHS & no Sb/Br) | CU SN | N / A for Pkg Type | -40 to 85 | OPA548T | Samples |
| OPA548TG3 | ACTIVE | TO-220 | KVT | 7 | 50 | Green (RoHS & no Sb/Br) | CU SN | N / A for Pkg Type | -40 to 85 | OPA548T | Samples |

**(1)** The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

**(2)** Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

**(3)** MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**(4)** There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

**(6)** Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

# PACKAGE MATERIALS INFORMATION

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

**TAPE DIMENSIONS**

| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

User Direction of Feed

Pocket Quadrants

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| OPA548F/500 | DDPAK/ TO-263 | KTW | 7 | 500 | 330.0 | 24.4 | 10.95 | 16.5 | 5.15 | 16.0 | 24.0 | Q2 |
| OPA548FKTWT | DDPAK/ TO-263 | KTW | 7 | 250 | 330.0 | 24.4 | 10.6 | 15.6 | 4.9 | 16.0 | 24.0 | Q2 |

**TAPE AND REEL BOX  DIMENSIONS**



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------|--------------|-----------------|------|-----|-------------|------------|-------------|
| OPA548F/500 | DDPAK/TO-263 | KTW | 7 | 500 | 346.0 | 346.0 | 41.0 |
| OPA548FKTWT | DDPAK/TO-263 | KTW | 7 | 250 | 367.0 | 367.0 | 45.0 |

**KTW (R-PSFM-G7)**                                                                                   **PLASTIC FLANGE-MOUNT**



0.410 (10,41)
0.385 (9,78)          −A−

0.303 (7,70)
0.297 (7,54)

0.0625 (1,587)  H
0.0585 (1,485)

0.370 (9,40)
0.330 (8,38)

H
0.605 (15,37)
0.595 (15,11)

A

C

0.050 (1,27)

C  F  0.034 (0,86)
0.022 (0,57)

⊕ 0.010 (0,25) M  B  A M  C M

0.183 (4,65)
0.170 (4,32)

0.055 (1,40)
0.045 (1,14)

☐ 0.006
−B−

0.012 (0,305)
0.000 (0,00)

0.019 (0,48)
0.017 (0,43)

0.104 (2,64)
0.096 (2,44)  H

C  0.026 (0,66)
0.014 (0,36)

0°~3°

0.304 (7,72)
0.296 (7,52)

0.300 (7,62)
0.252 (6,40)

0.064 (1,63)
0.056 (1,42)

0.187 (4,75)
0.179 (4,55)
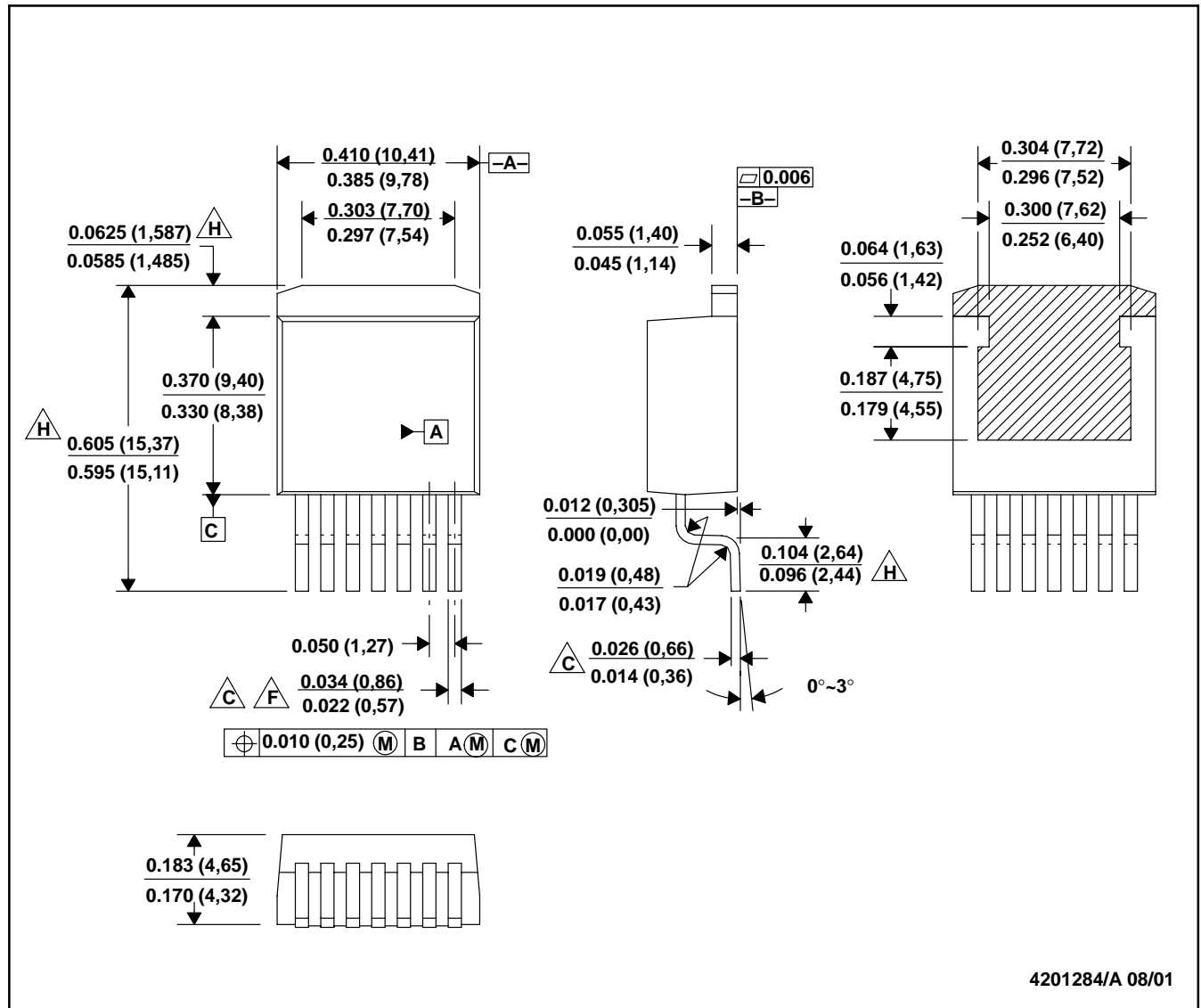
4201284/A 08/01

NOTES:  A.  All linear dimensions are in inches (millimeters).
        B.  This drawing is subject to change without notice.
        C.  Lead width and height dimensions apply to the
            plated lead.
        D.   Leads are not allowed above the Datum B.
        E.  Stand–off height is measured from lead tip
            with reference to Datum B.
        F.  Lead width dimension does not include dambar
            protrusion. Allowable dambar protrusion shall not
            cause the lead width to exceed the maximum
            dimension by more than 0.003".
        G.  Cross–hatch indicates exposed metal surface.
        H.  Falls within JEDEC MO–169 with the exception
            of the dimensions indicated.

0.410 (10,41)
0.390 (9,91)

0.185 (4,70)
0.169 (4,29)

0.055 (1,40)
0.045 (1,14)

0.113 (2,87)
0.103 (2,62)

0.258 (6,55)
0.235 (5,97)

Ø  0.155 (3,94)
   0.147 (3,73)

0.590 (14,99)
0.560 (14,22)

0.453 (11,51)
0.395 (10,03)

0.571 (14,50)
0.503 (12,78)

0.024 (0,61)
0.014 (0,36)

0.251 (6,38)
0.243 (6,17)

0.022 (0,56)
0.016 (0,41)

0.165 (4,19)
0.135 (3,43)

0.195 (4,95)
0.155 (3,94)

0.036 (0,91)
0.026 (0,66)

0.055 (1,40)
0.045 (1,14)

4204912/A 01/03

NOTES:    A.   All linear dimensions are in inches (millimeters).
          B.   This drawing is subject to change without notice.

**KC (R-PSFM-T7)**                    **PLASTIC FLANGE-MOUNT PACKAGE**
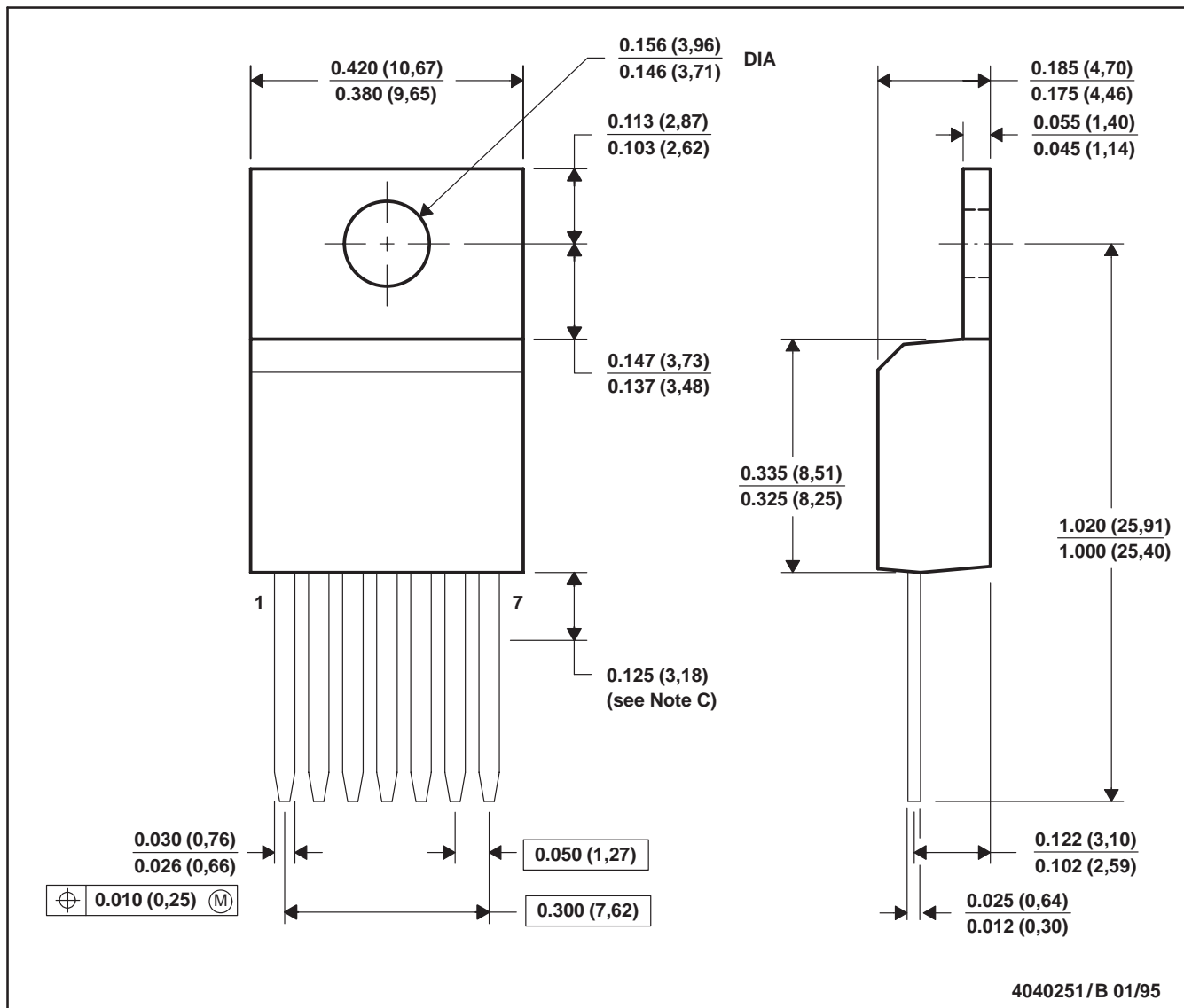
0.420 (10,67) / 0.380 (9,65)

0.156 (3,96) / 0.146 (3,71) DIA

0.113 (2,87) / 0.103 (2,62)

0.147 (3,73) / 0.137 (3,48)

0.185 (4,70) / 0.175 (4,46)

0.055 (1,40) / 0.045 (1,14)

0.335 (8,51) / 0.325 (8,25)

1.020 (25,91) / 1.000 (25,40)

1      7

0.125 (3,18) (see Note C)

0.030 (0,76) / 0.026 (0,66)

0.050 (1,27)

⊕ 0.010 (0,25) Ⓜ

0.300 (7,62)

0.122 (3,10) / 0.102 (2,59)

0.025 (0,64) / 0.012 (0,30)

4040251 / B 01/95

NOTES:  A.  All linear dimensions are in inches (millimeters).
        B.  This drawing is subject to change without notice.
        C.  Lead dimensions are not controlled within this area.
        D.  All lead dimensions apply before solder dip.
        E.  The center lead is in electrical contact with the mounting tab.

1

# IMPORTANT NOTICE