

## REF20xx Low-Drift, Low-Power, Dual-Output, $V_{REF}$ and $V_{REF} / 2$ Voltage References

### 1 Features

- Two Outputs,  $V_{REF}$  and  $V_{REF} / 2$ , for Convenient Use in Single-Supply Systems
- Excellent Temperature Drift Performance:
  - 8 ppm/°C (max) from –40°C to 125°C
- High Initial Accuracy:  $\pm 0.05\%$  (max)
- $V_{REF}$  and  $V_{BIAS}$  Tracking over Temperature:
  - 6 ppm/°C (max) from –40°C to 85°C
  - 7 ppm/°C (max) from –40°C to 125°C
- Microsize Package: SOT23-5
- Low Dropout Voltage: 10 mV
- High Output Current:  $\pm 20$  mA
- Low Quiescent Current: 360  $\mu$ A
- Line Regulation: 3 ppm/V
- Load Regulation: 8 ppm/mA

### 2 Applications

- Digital Signal Processing:
  - Power Inverters
  - Motor Controls
- Current Sensing
- Industrial Process Controls
- Medical Equipment
- Data Acquisition Systems
- Single-Supply Systems

### 3 Description

Applications with only a positive supply voltage often require additional stable voltage in the middle of the analog-to-digital converter (ADC) input range to bias input bipolar signals. The REF20xx provides a reference voltage ( $V_{REF}$ ) for the ADC and a second highly-accurate voltage ( $V_{BIAS}$ ) that can be used to bias the input bipolar signals.

The REF20xx offers excellent temperature drift (8 ppm/°C, max) and initial accuracy (0.05%) on both the  $V_{REF}$  and  $V_{BIAS}$  outputs while operating at a quiescent current less than 430  $\mu$ A. In addition, the  $V_{REF}$  and  $V_{BIAS}$  outputs track each other with a precision of 6 ppm/°C (max) across the temperature range of –40°C to 85°C. All these features increase the precision of the signal chain and decrease board space, while reducing the cost of the system as compared to a discrete solution. Extremely low dropout voltage of only 10 mV allows operation from very low input voltages, which can be very useful in battery-operated systems.

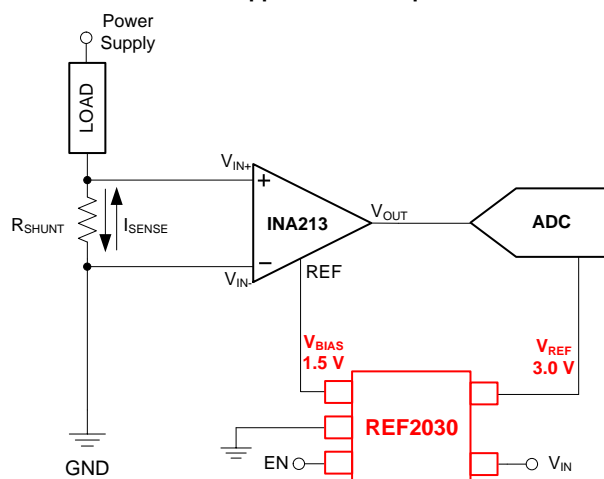
Both the  $V_{REF}$  and  $V_{BIAS}$  voltages have the same excellent specifications and can sink and source current equally well. Very good long-term stability and low noise levels make these devices ideally-suited for high-precision industrial applications.

#### Device Information<sup>(1)</sup>

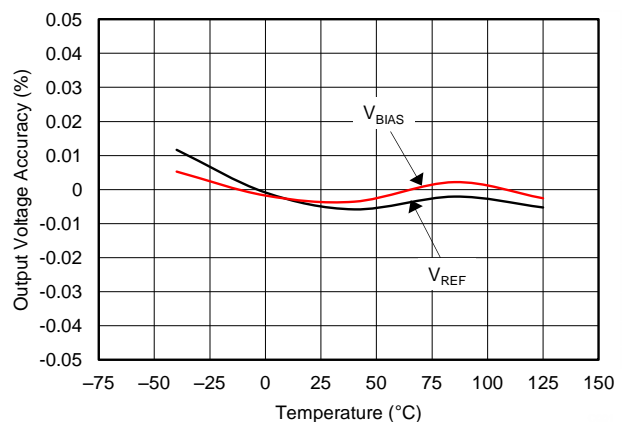
| PART NAME | PACKAGE | BODY SIZE (NOM)   |
|-----------|---------|-------------------|
| REF20xx   | SOT (5) | 2.90 mm x 1.60 mm |

(1) For all available packages, see the orderable addendum at the end of the datasheet.

#### Application Example



#### $V_{REF}$ and $V_{BIAS}$ vs Temperature



## Table of Contents

|  |  |
|--|--|
| <b>1 Features</b> ..... 1<br><b>2 Applications</b> ..... 1<br><b>3 Description</b> ..... 1<br><b>4 Revision History</b> ..... 2<br><b>5 Device Comparison Table</b> ..... 3<br><b>6 Pin Configuration and Functions</b> ..... 3<br><b>7 Specifications</b> ..... 4<br>7.1 Absolute Maximum Ratings ..... 4<br>7.2 ESD Ratings..... 4<br>7.3 Recommended Operating Conditions ..... 4<br>7.4 Thermal Information ..... 4<br>7.5 Electrical Characteristics..... 5<br>7.6 Typical Characteristics ..... 6<br><b>8 Parameter Measurement Information</b> ..... 13<br>8.1 Solder Heat Shift ..... 13<br>8.2 Thermal Hysteresis ..... 14<br>8.3 Noise Performance ..... 15<br><b>9 Detailed Description</b> ..... 16<br>9.1 Overview ..... 16 | 9.2 Functional Block Diagram ..... 16<br>9.3 Feature Description..... 16<br>9.4 Device Functional Modes..... 17<br><b>10 Applications and Implementation</b> ..... 18<br>10.1 Application Information..... 18<br>10.2 Typical Application ..... 18<br><b>11 Power-Supply Recommendations</b> ..... 23<br><b>12 Layout</b> ..... 24<br>12.1 Layout Guidelines ..... 24<br>12.2 Layout Example ..... 24<br><b>13 Device and Documentation Support</b> ..... 25<br>13.1 Documentation Support ..... 25<br>13.2 Related Links ..... 25<br>13.3 Receiving Notification of Documentation Updates 25<br>13.4 Community Resources..... 25<br>13.5 Trademarks ..... 25<br>13.6 Electrostatic Discharge Caution..... 25<br>13.7 Glossary ..... 25<br><b>14 Mechanical, Packaging, and Orderable Information</b> ..... 26 |
|--|--|

## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision B (July 2014) to Revision C  | Page |
|--|------|
| • Added I/O column to <i>Pin Functions</i> table ..... 3   | 3    |
| • Added <i>Storage temperature</i> parameter to <i>Absolute Maximum Ratings</i> table (moved from <i>ESD Ratings</i> table)..... 4 | 4    |
| • Changed <i>ESD Rating</i> table: changed title, updated table format ..... 4   | 4    |

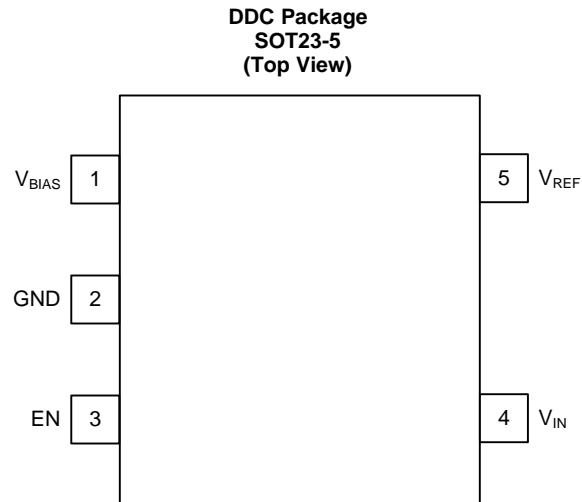
| Changes from Revision A (June 2014) to Revision B                    | Page |
|--|------|
| • Changed device status to Production Data from Mixed Status ..... 1 | 1    |
| • Deleted footnote 2 from Device Information table ..... 1           | 1    |
| • Deleted footnote from Device Comparison Table ..... 3              | 3    |
| • Added Thermal Information table ..... 4                            | 4    |

| Changes from Original (May 2014) to Revision A      | Page |
|---|------|
| • Made changes to product preview data sheet..... 1 | 1    |

## 5 Device Comparison Table

| PRODUCT | $V_{REF}$ | $V_{BIAS}$ |
|---------|-----------|------------|
| REF2025 | 2.5 V     | 1.25 V     |
| REF2030 | 3.0 V     | 1.5 V      |
| REF2033 | 3.3 V     | 1.65 V     |
| REF2041 | 4.096 V   | 2.048 V    |

## 6 Pin Configuration and Functions



### Pin Functions

| PIN |            | I/O    | DESCRIPTION  |
|-----|------------|--------|--|
| NO. | NAME       |        |  |
| 1   | $V_{BIAS}$ | Output | Bias voltage output ( $V_{REF} / 2$ )                      |
| 2   | GND        | —      | Ground   |
| 3   | EN         | Input  | Enable ( $EN \geq V_{IN} - 0.7\text{ V}$ , device enabled) |
| 4   | $V_{IN}$   | Input  | Input supply voltage                                       |
| 5   | $V_{REF}$  | Output | Reference voltage output ( $V_{REF}$ )                     |

## 7 Specifications

### 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|               |                           | MIN  | MAX                   | UNIT |
|---------------|---------------------------|------|-----------------------|------|
| Input voltage | V <sub>IN</sub>           | -0.3 | 6                     | V    |
|               | EN                        | -0.3 | V <sub>IN</sub> + 0.3 |      |
| Temperature   | Operating                 | -55  | 150                   | °C   |
|               | Junction, T <sub>j</sub>  |      | 150                   |      |
|               | Storage, T <sub>stg</sub> | -65  | 170                   |      |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 7.2 ESD Ratings

|  |  | VALUE | UNIT |
|--|--|-------|------|
| V <sub>(ESD)</sub> Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>              | ±4000 | V    |
|  | Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup> | ±1500 |      |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

|                 |   | MIN                                    | NOM | MAX | UNIT |
|-----------------|---|--|-----|-----|------|
| V <sub>IN</sub> | Supply input voltage range (I <sub>L</sub> = 0 mA, T <sub>A</sub> = 25°C) | V <sub>REF</sub> + 0.02 <sup>(1)</sup> |     | 5.5 | V    |

(1) See [Figure 28](#) in [Typical Characteristics](#) for minimum input voltage at different load currents and temperature

### 7.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |  | REF20xx     | UNIT |
|-------------------------------|--|-------------|------|
|                               |  | DDC (SOT23) |      |
|                               |  | 5 PINS      |      |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance       | 193.6       | °C/W |
| R <sub>θJC(top)</sub>         | Junction-to-case (top) thermal resistance    | 40.2        | °C/W |
| R <sub>θJB</sub>              | Junction-to-board thermal resistance         | 34.5        | °C/W |
| ψ <sub>JT</sub>               | Junction-to-top characterization parameter   | 0.9         | °C/W |
| ψ <sub>JB</sub>               | Junction-to-board characterization parameter | 34.3        | °C/W |
| R <sub>θJC(bot)</sub>         | Junction-to-case (bottom) thermal resistance | N/A         | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 7.5 Electrical Characteristics

At  $T_A = 25^\circ\text{C}$ ,  $I_L = 0\text{ mA}$ , and  $V_{IN} = 5\text{ V}$ , unless otherwise noted. Both  $V_{REF}$  and  $V_{BIAS}$  have the same specifications.

| PARAMETER  |                       | TEST CONDITIONS   | MIN            | TYP       | MAX      | UNIT                    |
|--|-----------------------|---|----------------|-----------|----------|-------------------------|
| <b>ACCURACY AND DRIFT</b>  |                       |   |                |           |          |                         |
| Output voltage accuracy  |                       |   | -0.05%         |           | 0.05%    |                         |
| Output voltage temperature coefficient <sup>(1)</sup>                |                       | $-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$   |                | $\pm 3$   | $\pm 8$  | ppm/ $^\circ\text{C}$   |
| $V_{REF}$ and $V_{BIAS}$ tracking over temperature <sup>(2)</sup>    |                       | $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$  |                | $\pm 1.5$ | $\pm 6$  | ppm/ $^\circ\text{C}$   |
|  |                       | $-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$   |                | $\pm 2$   | $\pm 7$  |                         |
| <b>LINE AND LOAD REGULATION</b>                                      |                       |   |                |           |          |                         |
| $\Delta V_{O(\Delta V_I)}$   | Line regulation       | $V_{REF} + 0.02\text{ V} \leq V_{IN} \leq 5.5\text{ V}$   |                | 3         | 35       | ppm/V                   |
| $\Delta V_{O(\Delta I_L)}$   | Load regulation       | Sourcing<br>$0\text{ mA} \leq I_L \leq 20\text{ mA}$ ,<br>$V_{REF} + 0.6\text{ V} \leq V_{IN} \leq 5.5\text{ V}$  |                | 8         | 20       | ppm/mA                  |
|  |                       | Sinking<br>$0\text{ mA} \leq I_L \leq -20\text{ mA}$ ,<br>$V_{REF} + 0.02\text{ V} \leq V_{IN} \leq 5.5\text{ V}$ |                | 8         | 20       |                         |
| <b>POWER SUPPLY</b>  |                       |   |                |           |          |                         |
| $I_{CC}$   | Supply current        | Active mode<br>$-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$  |                | 360       | 430      | $\mu\text{A}$           |
|  |                       |   |                |           | 460      |                         |
| Shutdown mode<br>$-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$ |                       | 3.3   | 5              |           |          |                         |
|  |                       |   | 9              |           |          |                         |
| Enable voltage   |                       | Device in shutdown mode ( $EN = 0$ )  | 0              |           | 0.7      | V                       |
|  |                       | Device in active mode ( $EN = 1$ )  | $V_{IN} - 0.7$ |           | $V_{IN}$ |                         |
| Dropout voltage  |                       | $I_L = 20\text{ mA}$  |                | 10        | 20       | mV                      |
|  |                       |   |                |           |          |                         |
| $I_{SC}$   | Short-circuit current |   |                | 50        |          | mA                      |
| $t_{on}$   | Turn-on time          | 0.1% settling, $C_L = 1\text{ }\mu\text{F}$   |                | 500       |          | $\mu\text{s}$           |
| <b>NOISE</b>   |                       |   |                |           |          |                         |
| Low-frequency noise <sup>(3)</sup>                                   |                       | $0.1\text{ Hz} \leq f \leq 10\text{ Hz}$  |                | 12        |          | ppm <sub>PP</sub>       |
| Output voltage noise density   |                       | $f = 100\text{ Hz}$   |                | 0.25      |          | ppm/ $\sqrt{\text{Hz}}$ |
| <b>CAPACITIVE LOAD</b>   |                       |   |                |           |          |                         |
| Stable output capacitor range  |                       |   | 0              |           | 10       | $\mu\text{F}$           |
| <b>HYSTERESIS AND LONG TERM STABILITY</b>                            |                       |   |                |           |          |                         |
| Long-term stability  |                       | 0 to 1000 hours   |                | 60        |          | ppm                     |
| Output voltage hysteresis <sup>(4)</sup>                             |                       | $25^\circ\text{C}$ , $-40^\circ\text{C}$ , $125^\circ\text{C}$ , $25^\circ\text{C}$                               | Cycle 1        | 60        |          | ppm                     |
|  |                       |   | Cycle 2        | 35        |          |                         |

(1) Temperature drift is specified according to the box method. See the [Feature Description](#) section for more details.

(2) The  $V_{REF}$  and  $V_{BIAS}$  tracking over temperature specification is explained in more detail in the [Feature Description](#) section.

(3) The peak-to-peak noise measurement procedure is explained in more detail in the [Noise Performance](#) section.

(4) The thermal hysteresis measurement procedure is explained in more detail in the [Thermal Hysteresis](#) section.

## 7.6 Typical Characteristics

At  $T_A = 25^\circ\text{C}$ ,  $I_L = 0\text{ mA}$ ,  $V_{IN} = 5\text{-V}$  power supply,  $C_L = 0\text{ }\mu\text{F}$ , and 2.5-V output, unless otherwise noted.

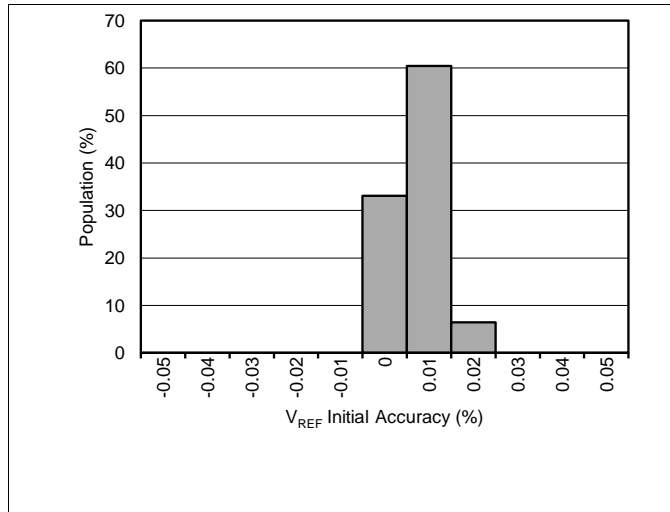


Figure 1. Initial Accuracy Distribution ( $V_{REF}$ )

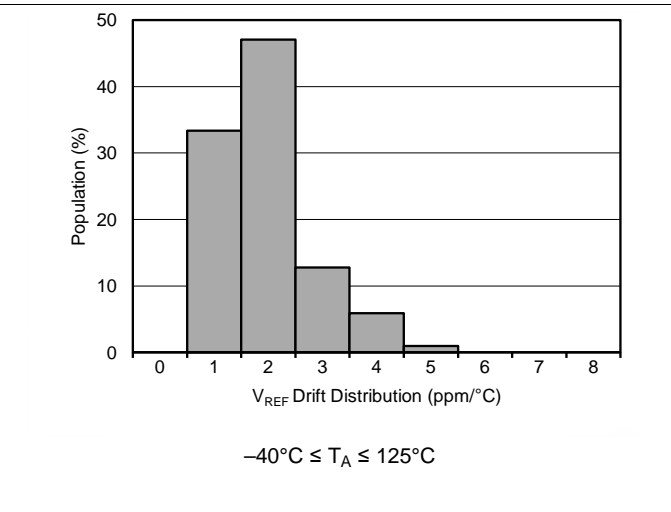


Figure 2. Drift Distribution ( $V_{REF}$ )

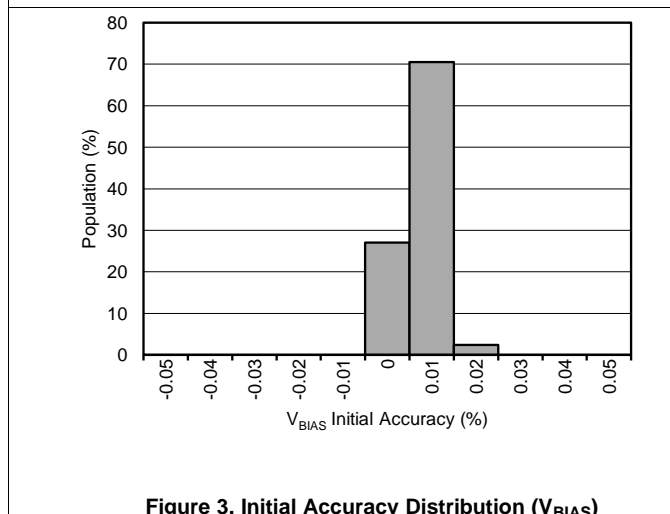


Figure 3. Initial Accuracy Distribution ( $V_{BIAS}$ )

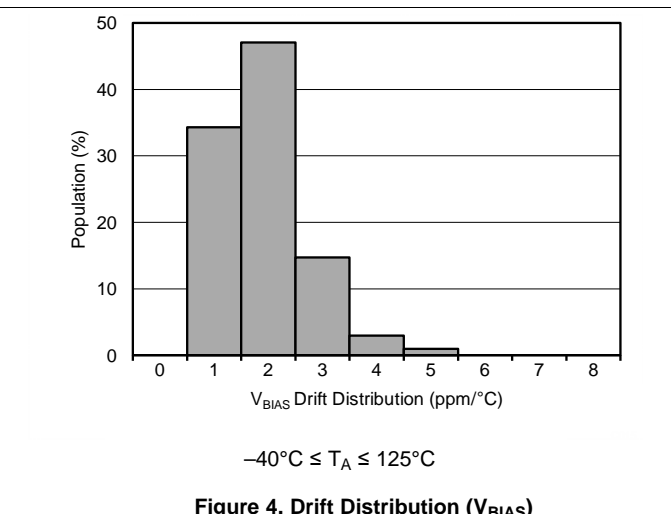


Figure 4. Drift Distribution ( $V_{BIAS}$ )

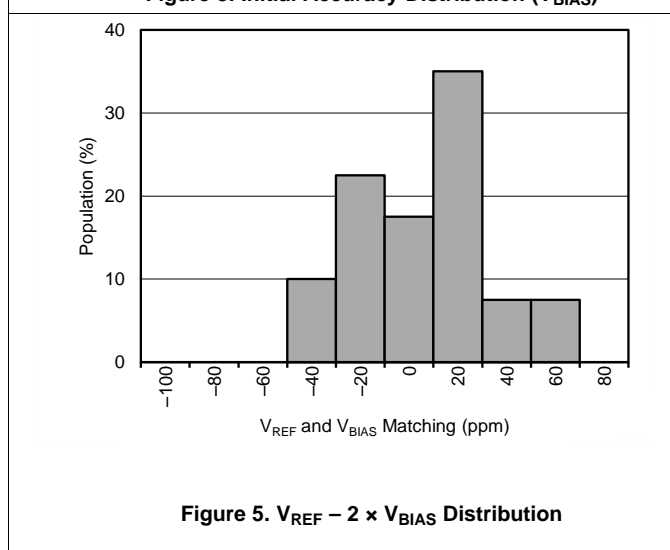


Figure 5.  $V_{REF} - 2 \times V_{BIAS}$  Distribution

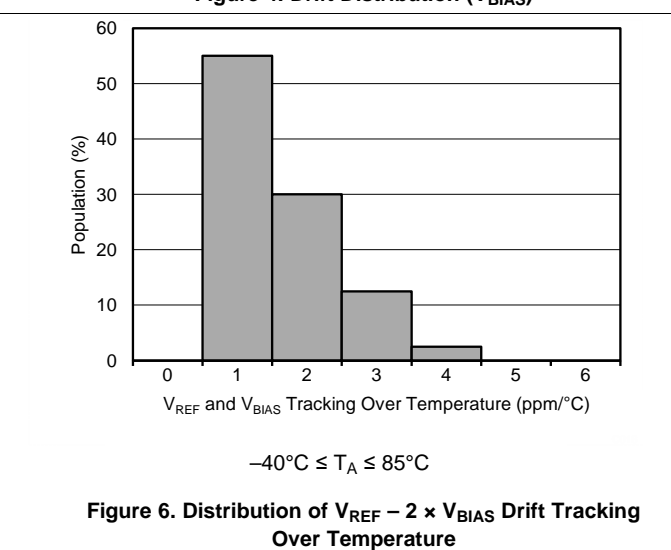
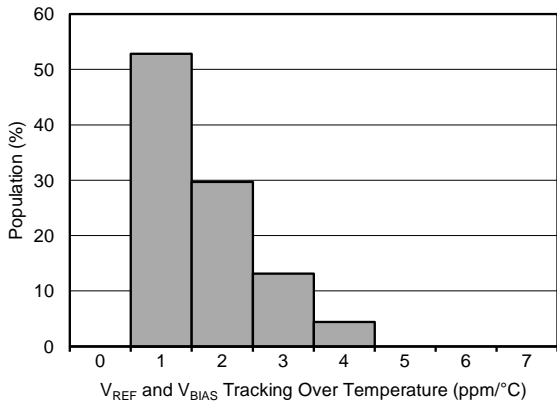


Figure 6. Distribution of  $V_{REF} - 2 \times V_{BIAS}$  Drift Tracking Over Temperature

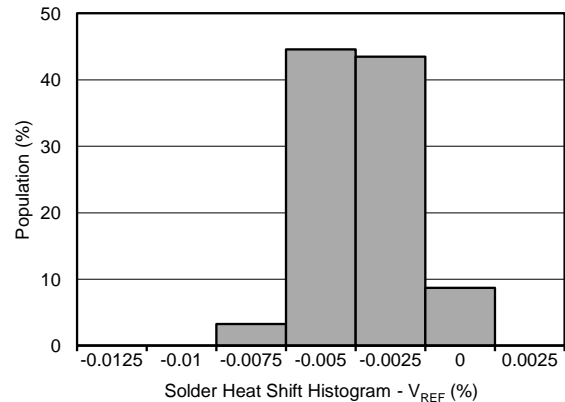
**Typical Characteristics (continued)**

At  $T_A = 25^\circ\text{C}$ ,  $I_L = 0\text{ mA}$ ,  $V_{IN} = 5\text{-V power supply}$ ,  $C_L = 0\text{ }\mu\text{F}$ , and  $2.5\text{-V output}$ , unless otherwise noted.



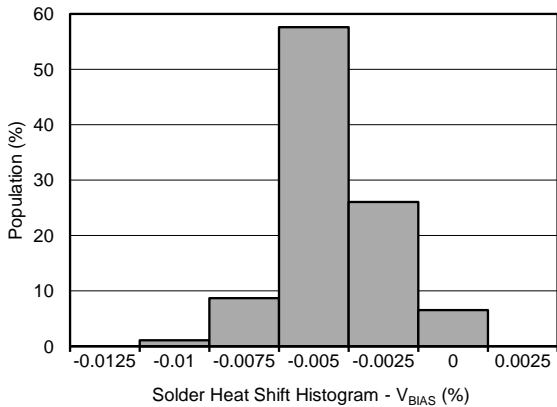
$-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$

**Figure 7. Distribution of  $V_{REF} - 2 \times V_{BIAS}$  Drift Tracking Over Temperature**



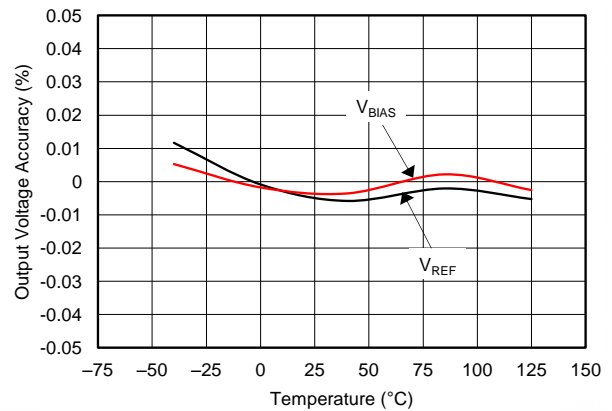
Refer to the [Solder Heat Shift](#) section for more information.

**Figure 8. Solder Heat Shift Distribution ( $V_{REF}$ )**

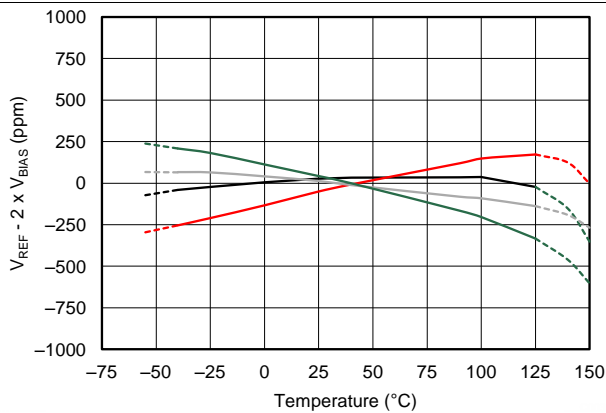


Refer to the [Solder Heat Shift](#) section for more information.

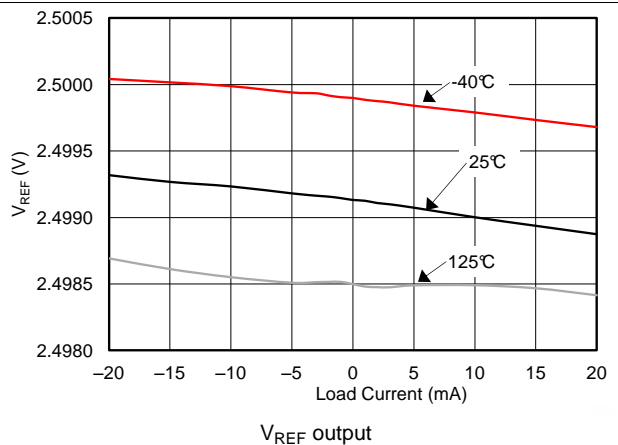
**Figure 9. Solder Heat Shift Distribution ( $V_{BIAS}$ )**



**Figure 10. Output Voltage Accuracy ( $V_{REF}$ ) vs Temperature**



**Figure 11.  $V_{REF} - 2 \times V_{BIAS}$  Tracking vs Temperature**



**Figure 12. Output Voltage Change vs Load Current ( $V_{REF}$ )**

### Typical Characteristics (continued)

At  $T_A = 25^\circ\text{C}$ ,  $I_L = 0\text{ mA}$ ,  $V_{IN} = 5\text{-V}$  power supply,  $C_L = 0\text{ }\mu\text{F}$ , and 2.5-V output, unless otherwise noted.

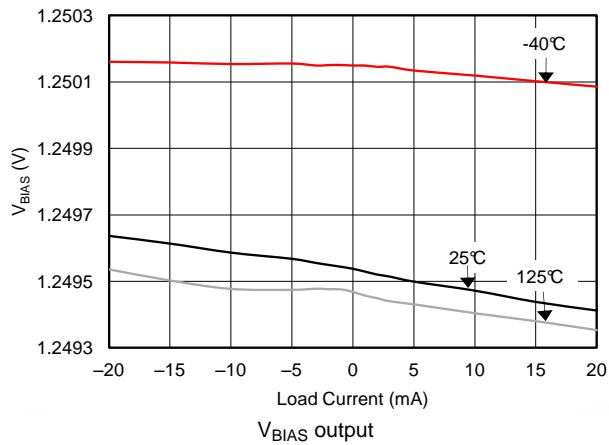


Figure 13. Output Voltage Change vs Load Current ( $V_{BIAS}$ )

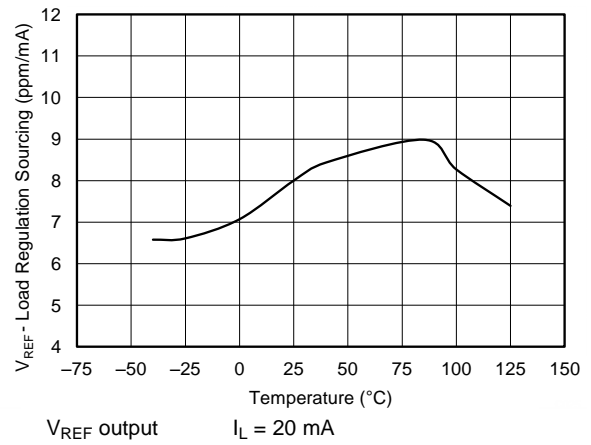


Figure 14. Load Regulation Sourcing vs Temperature ( $V_{REF}$ )

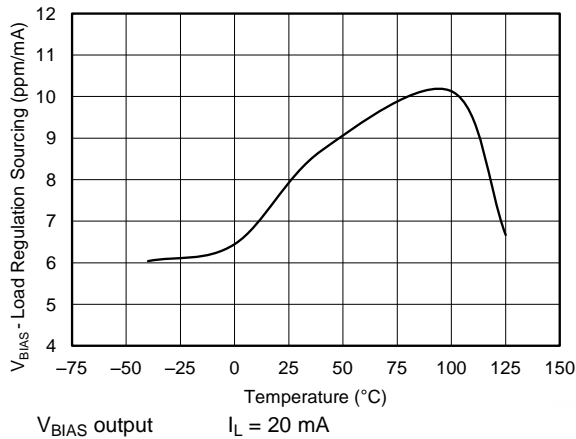


Figure 15. Load Regulation Sourcing vs Temperature ( $V_{BIAS}$ )

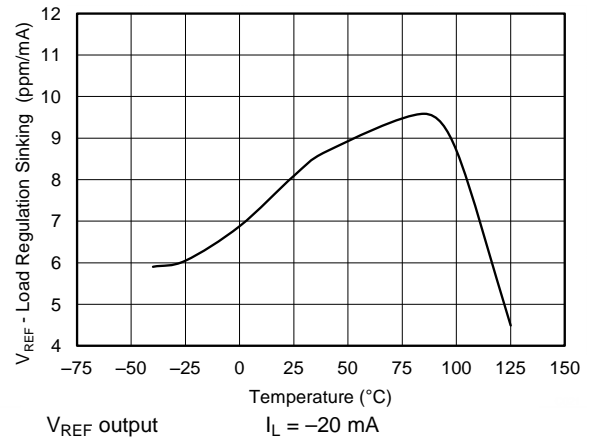


Figure 16. Load Regulation Sinking vs Temperature ( $V_{REF}$ )

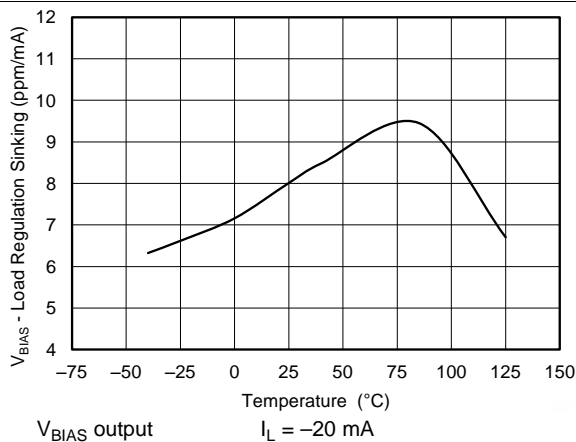


Figure 17. Load Regulation Sinking vs Temperature ( $V_{BIAS}$ )

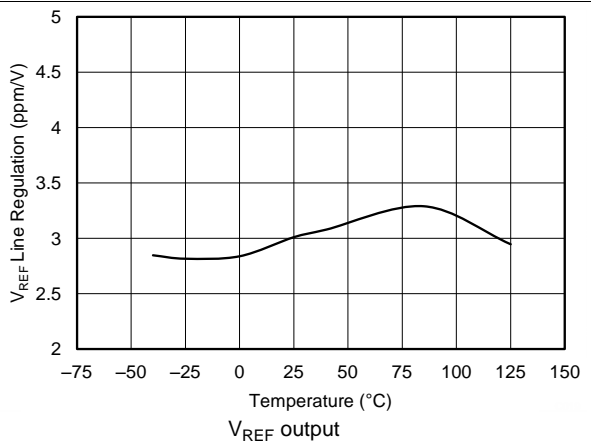


Figure 18. Line Regulation vs Temperature ( $V_{REF}$ )



Typical Characteristics (continued)

At  $T_A = 25^\circ\text{C}$ ,  $I_L = 0\text{ mA}$ ,  $V_{IN} = 5\text{-V power supply}$ ,  $C_L = 0\text{ }\mu\text{F}$ , and  $2.5\text{-V output}$ , unless otherwise noted.

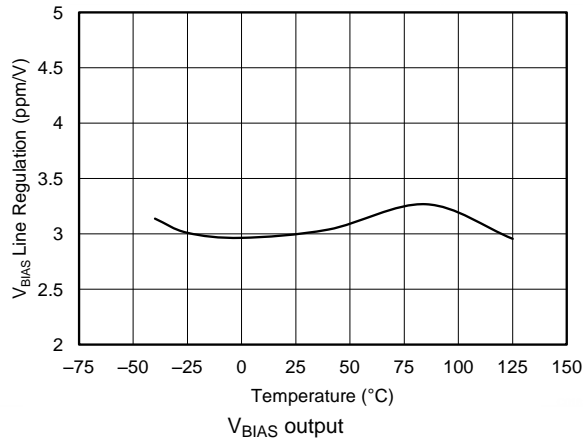


Figure 19. Line Regulation vs Temperature ( $V_{BIAS}$ )

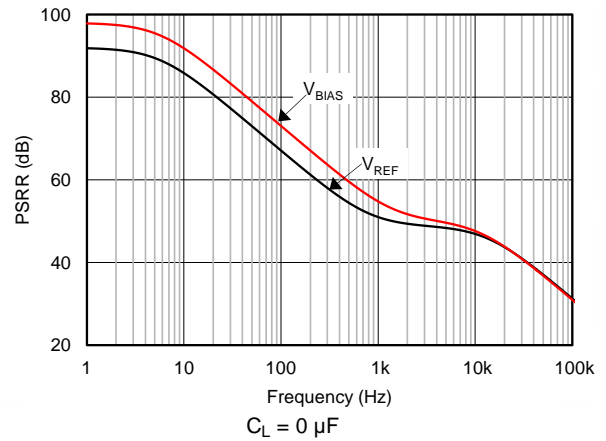


Figure 20. Power-Supply Rejection Ratio vs Frequency

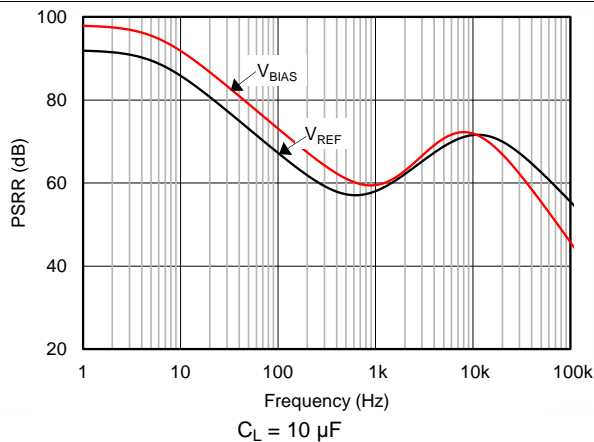


Figure 21. Power-Supply Rejection Ratio vs Frequency

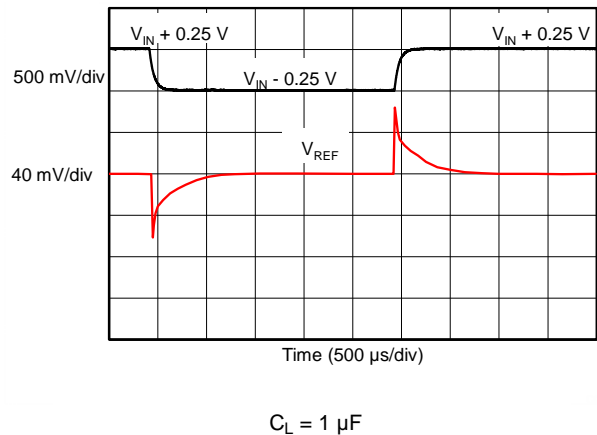


Figure 22. Line Transient Response

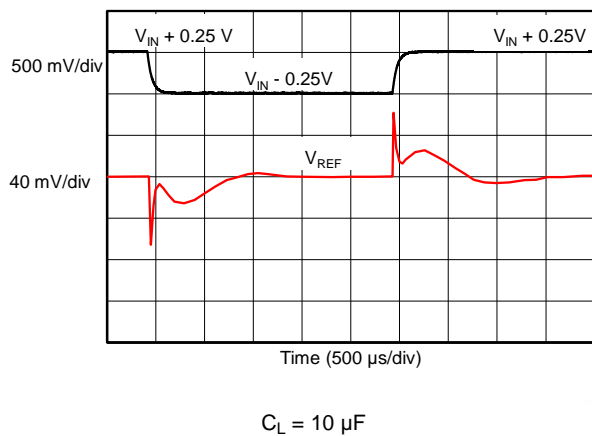


Figure 23. Line Transient Response

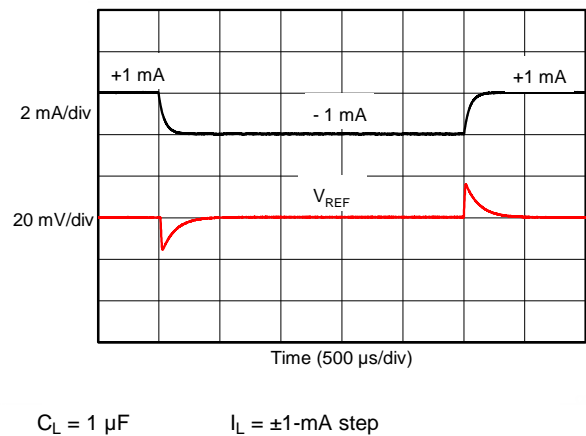
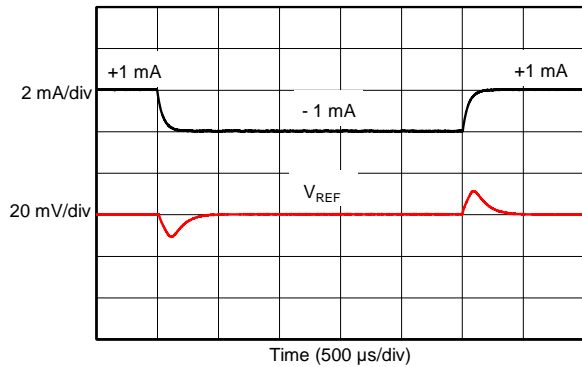


Figure 24. Load Transient Response

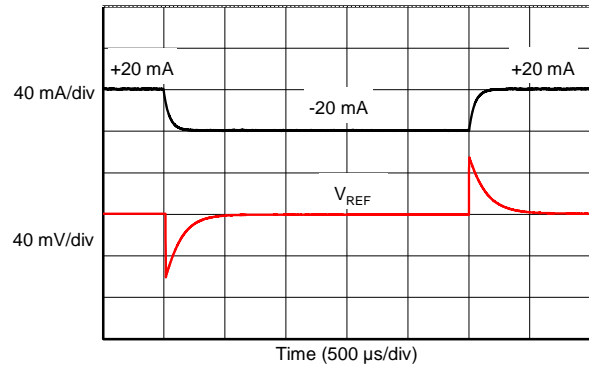
### Typical Characteristics (continued)

At  $T_A = 25^\circ\text{C}$ ,  $I_L = 0\text{ mA}$ ,  $V_{IN} = 5\text{-V}$  power supply,  $C_L = 0\text{ }\mu\text{F}$ , and 2.5-V output, unless otherwise noted.



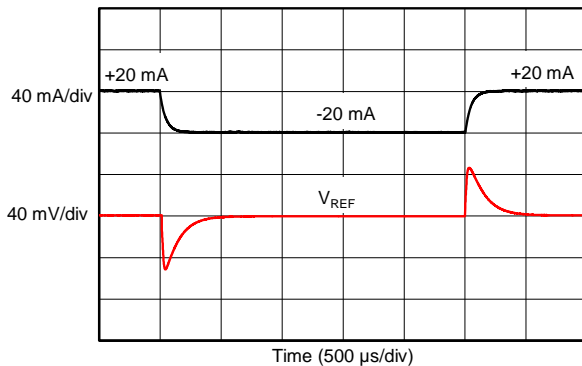
$C_L = 10\text{ }\mu\text{F}$       $I_L = \pm 1\text{-mA}$  step

**Figure 25. Load Transient Response**



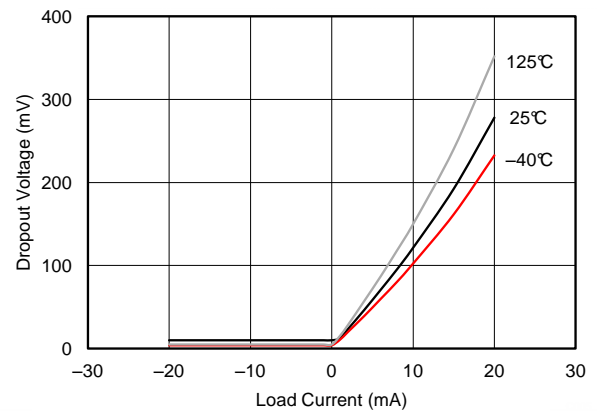
$C_L = 1\text{ }\mu\text{F}$       $I_L = \pm 20\text{-mA}$  step

**Figure 26. Load Transient Response**

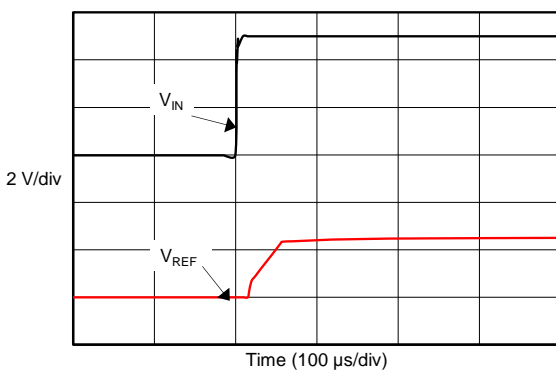


$C_L = 10\text{ }\mu\text{F}$       $I_L = \pm 20\text{-mA}$  step

**Figure 27. Load Transient Response**

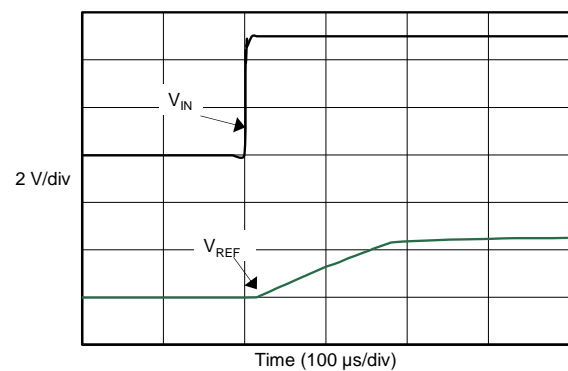


**Figure 28. Minimum Dropout Voltage vs Load Current**



$C_L = 1\text{ }\mu\text{F}$

**Figure 29. Turn-On Settling Time**

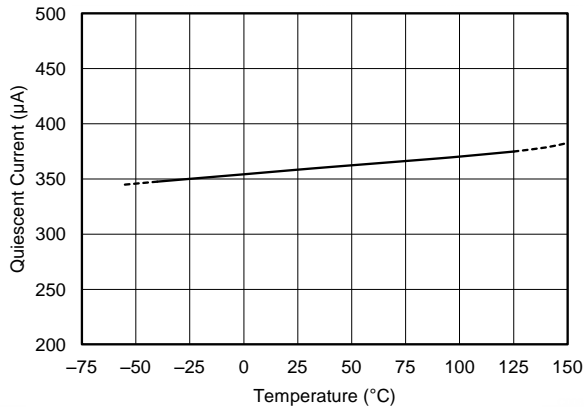


$C_L = 10\text{ }\mu\text{F}$

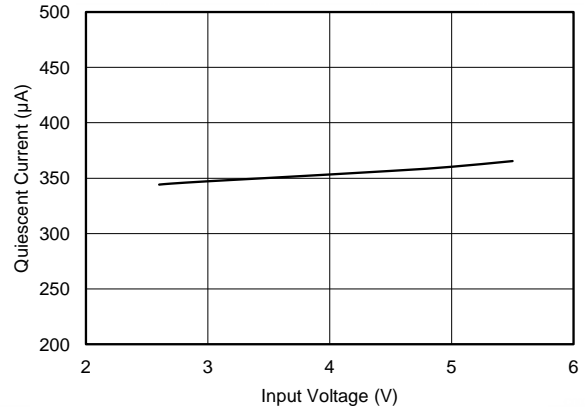
**Figure 30. Turn-On Settling Time**

**Typical Characteristics (continued)**

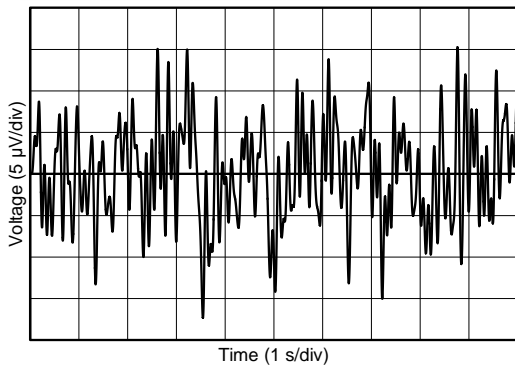
At  $T_A = 25^\circ\text{C}$ ,  $I_L = 0\text{ mA}$ ,  $V_{IN} = 5\text{-V}$  power supply,  $C_L = 0\ \mu\text{F}$ , and 2.5-V output, unless otherwise noted.



**Figure 31. Quiescent Current vs Temperature**

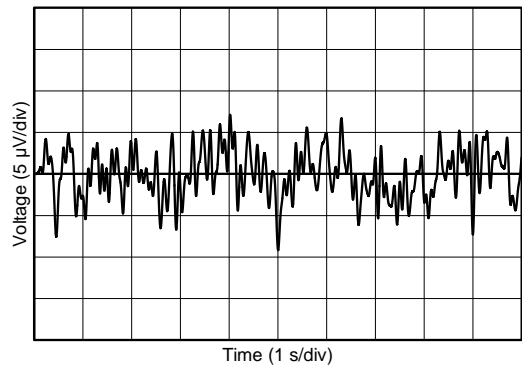


**Figure 32. Quiescent Current vs Input Voltage**



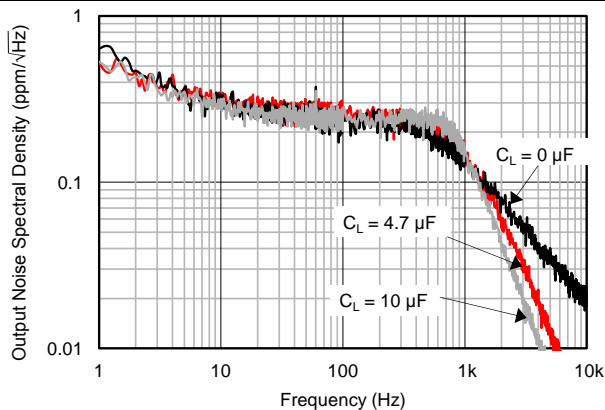
$V_{REF}$  output

**Figure 33. 0.1-Hz to 10-Hz Noise ( $V_{REF}$ )**

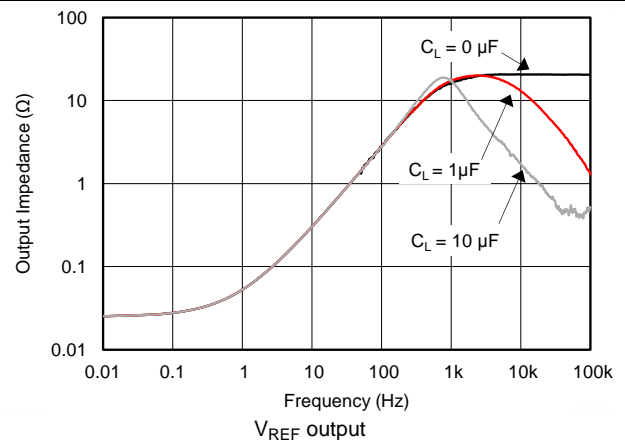


$V_{BIAS}$  output

**Figure 34. 0.1-Hz to 10-Hz Noise ( $V_{BIAS}$ )**



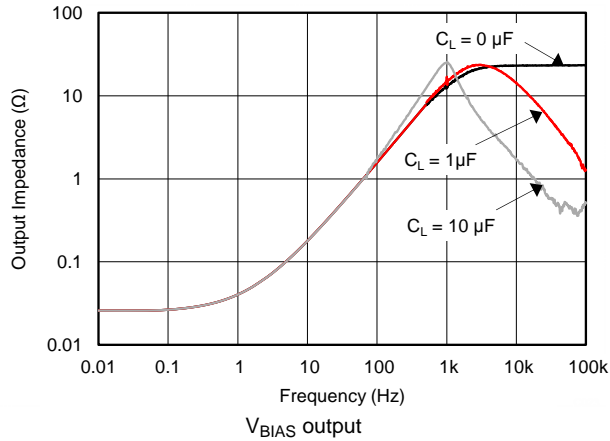
**Figure 35. Output Voltage Noise Spectrum**



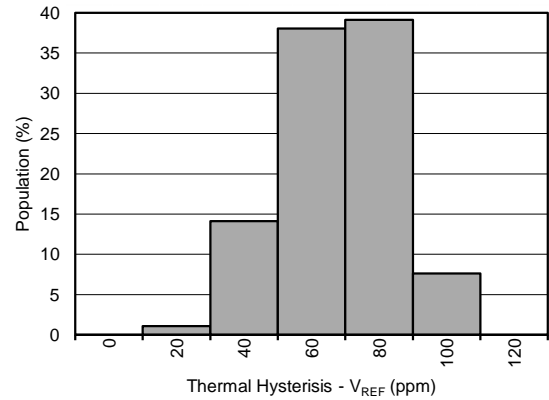
**Figure 36. Output Impedance vs Frequency ( $V_{REF}$ )**

**Typical Characteristics (continued)**

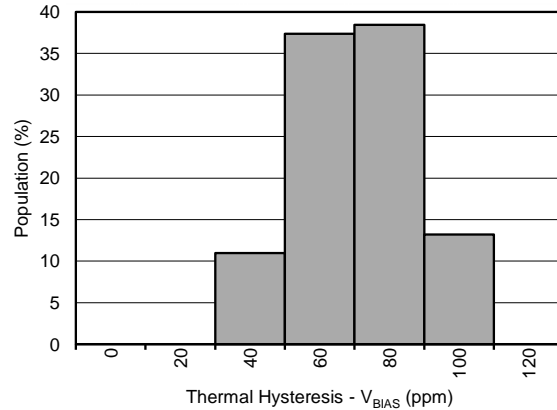
At  $T_A = 25^\circ\text{C}$ ,  $I_L = 0\text{ mA}$ ,  $V_{IN} = 5\text{-V}$  power supply,  $C_L = 0\ \mu\text{F}$ , and 2.5-V output, unless otherwise noted.



**Figure 37. Output Impedance vs Frequency ( $V_{BIAS}$ )**



**Figure 38. Thermal Hysteresis Distribution ( $V_{REF}$ )**



**Figure 39. Thermal Hysteresis Distribution ( $V_{BIAS}$ )**

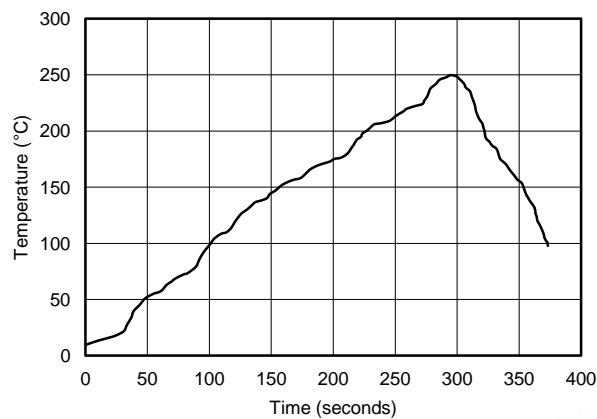
## 8 Parameter Measurement Information

### 8.1 Solder Heat Shift

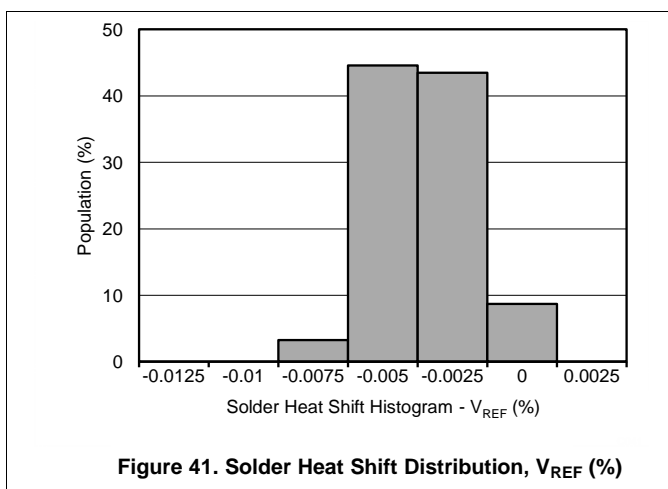
The materials used in the manufacture of the REF20xx have differing coefficients of thermal expansion, resulting in stress on the device die when the part is heated. Mechanical and thermal stress on the device die can cause the output voltages to shift, degrading the initial accuracy specifications of the product. Reflow soldering is a common cause of this error.

In order to illustrate this effect, a total of 92 devices were soldered on four printed circuit boards [23 devices on each printed circuit board (PCB)] using lead-free solder paste and the paste manufacturer suggested reflow profile. The reflow profile is as shown in Figure 40. The printed circuit board is comprised of FR4 material. The board thickness is 1.57 mm and the area is 171.54 mm × 165.1 mm.

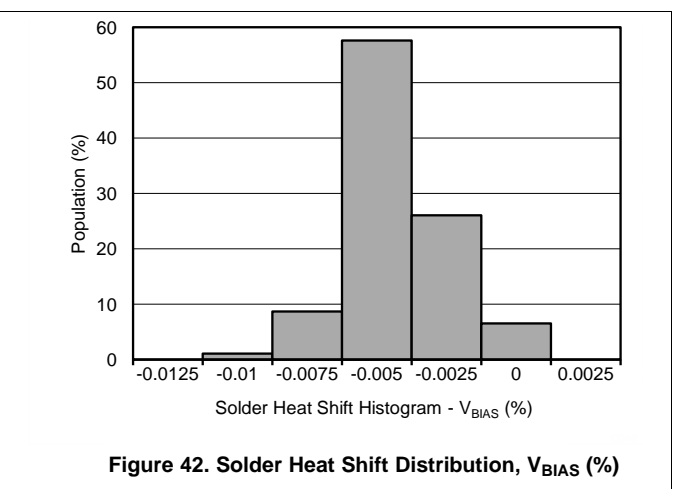
The reference and bias output voltages are measured before and after the reflow process; the typical shift is displayed in Figure 41 and Figure 42. Although all tested units exhibit very low shifts (< 0.01%), higher shifts are also possible depending on the size, thickness, and material of the printed circuit board. An important note is that the histograms display the typical shift for exposure to a single reflow profile. Exposure to multiple reflows, as is common on PCBs with surface-mount components on both sides, causes additional shifts in the output bias voltage. If the PCB is exposed to multiple reflows, the device should be soldered in the second pass to minimize its exposure to thermal stress.



**Figure 40. Reflow Profile**



**Figure 41. Solder Heat Shift Distribution, V<sub>REF</sub> (%)**



**Figure 42. Solder Heat Shift Distribution, V<sub>BIAS</sub> (%)**

## 8.2 Thermal Hysteresis

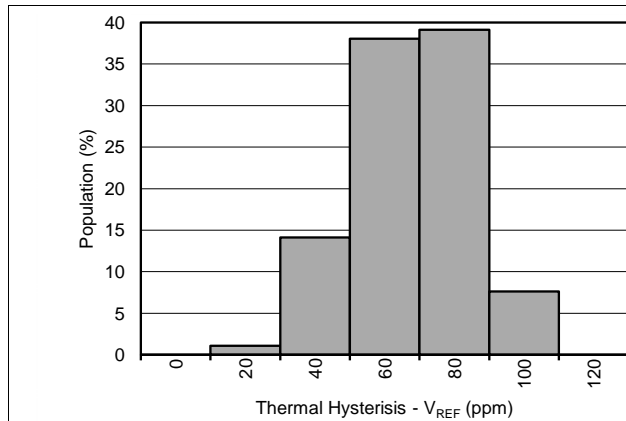
Thermal hysteresis is measured with the REF20xx soldered to a PCB, similar to a real-world application. Thermal hysteresis for the device is defined as the change in output voltage after operating the device at 25°C, cycling the device through the specified temperature range, and returning to 25°C. Hysteresis can be expressed by Equation 1:

$$V_{\text{HYST}} = \left( \frac{|V_{\text{PRE}} - V_{\text{POST}}|}{V_{\text{NOM}}} \right) \cdot 10^6 \text{ (ppm)}$$

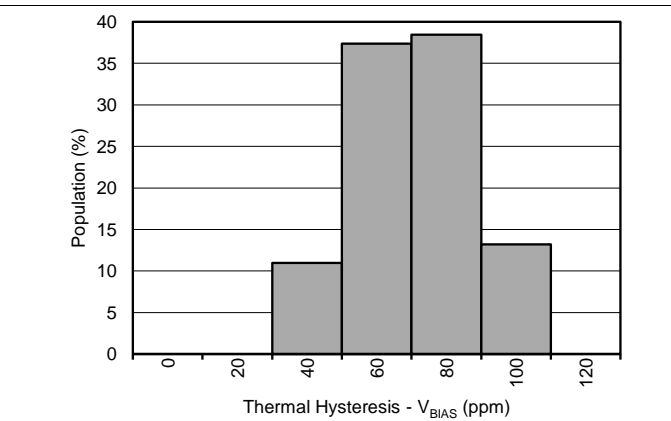
where

- $V_{\text{HYST}}$  = thermal hysteresis (in units of ppm),
  - $V_{\text{NOM}}$  = the specified output voltage,
  - $V_{\text{PRE}}$  = output voltage measured at 25°C pre-temperature cycling, and
  - $V_{\text{POST}}$  = output voltage measured after the device has cycled from 25°C through the specified temperature range of –40°C to 125°C and returns to 25°C.
- (1)

Typical thermal hysteresis distribution is as shown in Figure 43 and Figure 44.



**Figure 43. Thermal Hysteresis Distribution (V<sub>REF</sub>)**



**Figure 44. Thermal Hysteresis Distribution (V<sub>BIAS</sub>)**

### 8.3 Noise Performance

Typical 0.1-Hz to 10-Hz voltage noise can be seen in [Figure 45](#) and [Figure 46](#). Device noise increases with output voltage and operating temperature. Additional filtering can be used to improve output noise levels, although care should be taken to ensure the output impedance does not degrade ac performance. Peak-to-peak noise measurement setup is shown in [Figure 47](#).

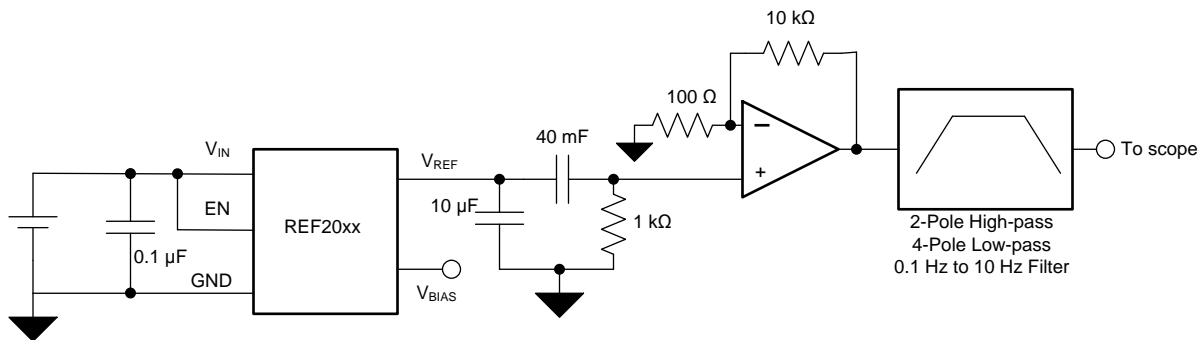
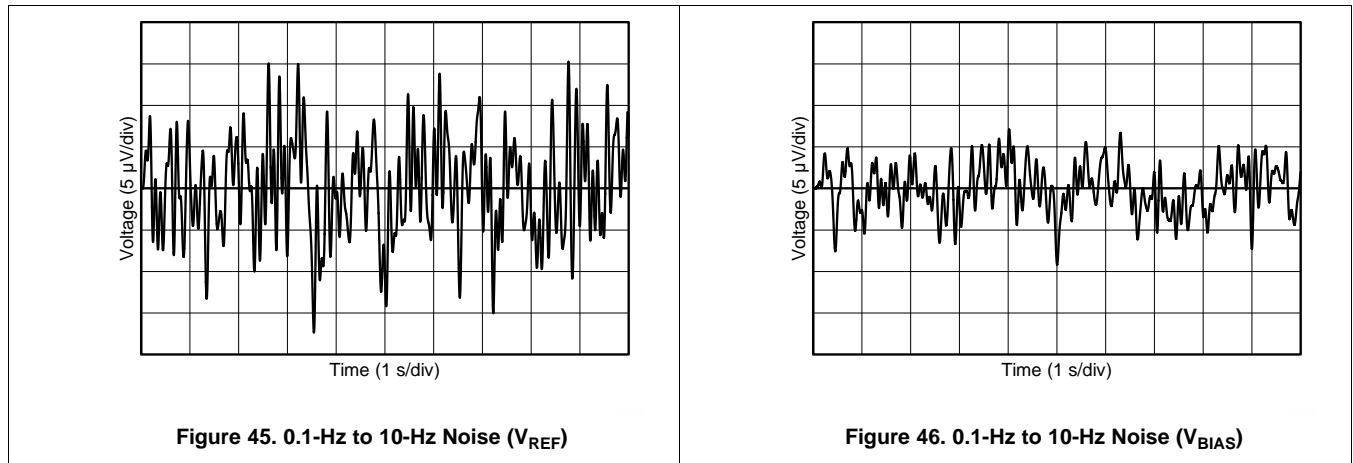


Figure 47. 0.1-Hz to 10-Hz Noise Measurement Setup

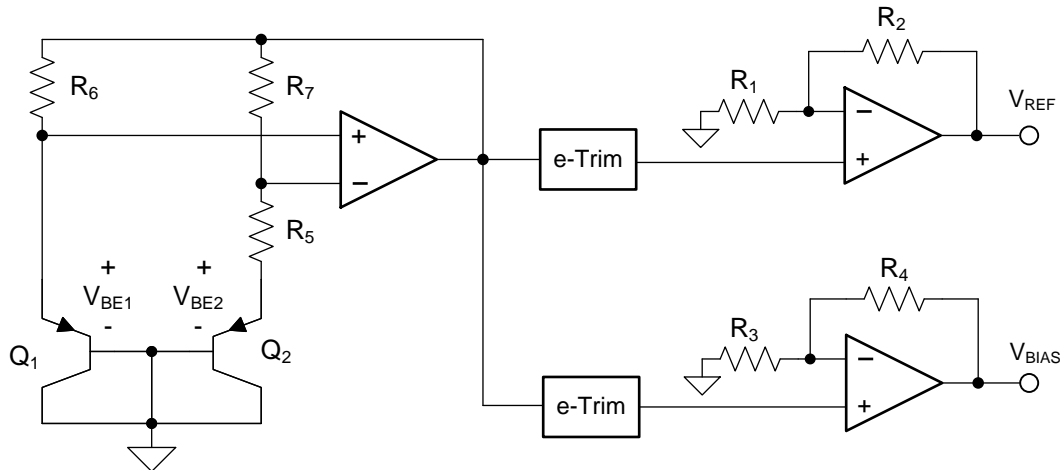
## 9 Detailed Description

### 9.1 Overview

The REF20xx are a family of dual-output,  $V_{REF}$  and  $V_{BIAS}$  ( $V_{REF} / 2$ ) band-gap voltage references. The [Functional Block Diagram](#) section provides a block diagram of the basic band-gap topology and the two buffers used to derive the  $V_{REF}$  and  $V_{BIAS}$  outputs. Transistors  $Q_1$  and  $Q_2$  are biased such that the current density of  $Q_1$  is greater than that of  $Q_2$ . The difference of the two base emitter voltages ( $V_{BE1} - V_{BE2}$ ) has a positive temperature coefficient and is forced across resistor  $R_5$ . The voltage is amplified and added to the base emitter voltage of  $Q_2$ , which has a negative temperature coefficient. The resulting band-gap output voltage is almost independent of temperature. Two independent buffers are used to generate  $V_{REF}$  and  $V_{BIAS}$  from the band-gap voltage. The resistors  $R_1$ ,  $R_2$  and  $R_3$ ,  $R_4$  are sized such that  $V_{BIAS} = V_{REF} / 2$ .

e-Trim™ is a method of package-level trim for the initial accuracy and temperature coefficient of  $V_{REF}$  and  $V_{BIAS}$ , implemented during the final steps of manufacturing after the plastic molding process. This method minimizes the influence of inherent transistor mismatch, as well as errors induced during package molding. e-Trim is implemented in the REF20xx to minimize the temperature drift and maximize the initial accuracy of both the  $V_{REF}$  and  $V_{BIAS}$  outputs.

### 9.2 Functional Block Diagram



### 9.3 Feature Description

#### 9.3.1 $V_{REF}$ and $V_{BIAS}$ Tracking

Most single-supply systems require an additional stable voltage in the middle of the analog-to-digital converter (ADC) input range to bias input bipolar signals. The  $V_{REF}$  and  $V_{BIAS}$  outputs of the REF20xx are generated from the same band-gap voltage as shown in the [Functional Block Diagram](#) section. Hence, both outputs track each other over the full temperature range of  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$  with an accuracy of 7 ppm/ $^{\circ}\text{C}$  (max). The tracking accuracy increases to 6 ppm/ $^{\circ}\text{C}$  (max) when the temperature range is limited to  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ . The tracking error is calculated using the box method, as described by [Equation 2](#):

$$\text{Tracking Error} = \left( \frac{V_{\text{DIFF(MAX)}} - V_{\text{DIFF(MIN)}}}{V_{\text{REF}} \cdot \text{Temperature Range}} \right) \cdot 10^6 \quad (\text{ppm})$$

where

$$\bullet \quad V_{\text{DIFF}} = V_{\text{REF}} - 2 \cdot V_{\text{BIAS}} \quad (2)$$



## Feature Description (continued)

The tracking accuracy is as shown in Figure 48.

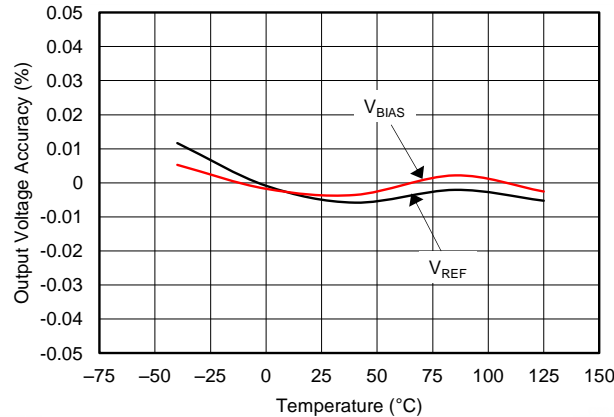


Figure 48.  $V_{REF}$  and  $V_{BIAS}$  Tracking vs Temperature

### 9.3.2 Low Temperature Drift

The REF20xx is designed for minimal drift error, which is defined as the change in output voltage over temperature. The drift is calculated using the box method, as described by Equation 3:

$$\text{Drift} = \left( \frac{V_{REF(MAX)} - V_{REF(MIN)}}{V_{REF} \cdot \text{Temperature Range}} \right) \cdot 10^6 \quad (\text{ppm}) \quad (3)$$

### 9.3.3 Load Current

The REF20xx family is specified to deliver a current load of  $\pm 20$  mA per output. Both the  $V_{REF}$  and  $V_{BIAS}$  outputs of the device are protected from short circuits by limiting the output short-circuit current to 50 mA. The device temperature increases according to Equation 4:

$$T_J = T_A + P_D \cdot R_{\theta JA}$$

where

- $T_J$  = junction temperature ( $^{\circ}\text{C}$ ),
  - $T_A$  = ambient temperature ( $^{\circ}\text{C}$ ),
  - $P_D$  = power dissipated (W), and
  - $R_{\theta JA}$  = junction-to-ambient thermal resistance ( $^{\circ}\text{C}/\text{W}$ )
- (4)

The REF20xx maximum junction temperature must not exceed the absolute maximum rating of  $150^{\circ}\text{C}$ .

## 9.4 Device Functional Modes

When the EN pin of the REF20xx is pulled high, the device is in active mode. The device should be in active mode for normal operation. The REF20xx can be placed in a low-power mode by pulling the ENABLE pin low. When in shutdown mode, the output of the device becomes high impedance and the quiescent current of the device reduces to  $5 \mu\text{A}$  in shutdown mode. See the [Electrical Characteristics](#) for logic high and logic low voltage levels.

## 10 Applications and Implementation

### NOTE

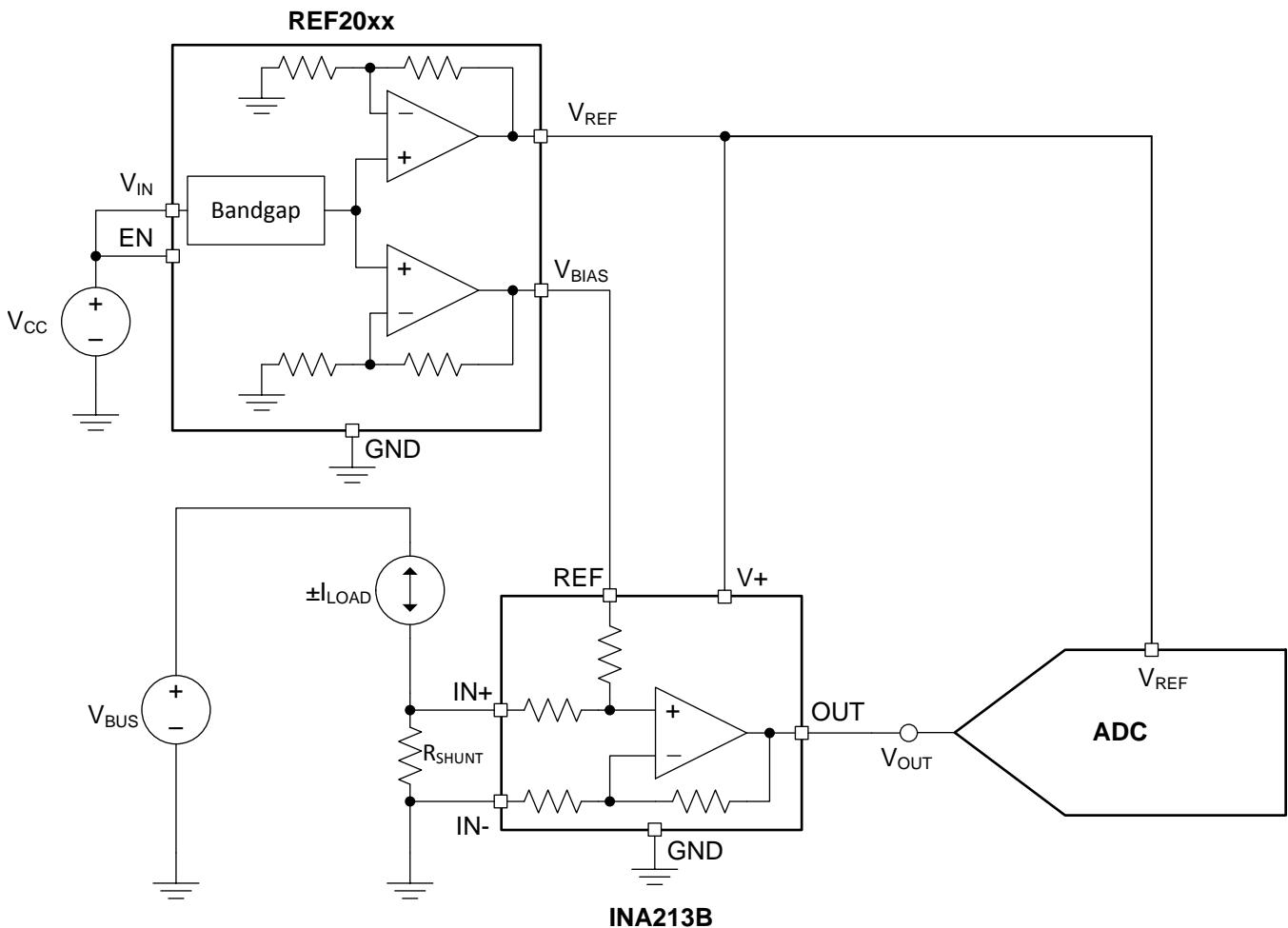
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 10.1 Application Information

The low-drift, bidirectional, single-supply, low-side, current-sensing solution, described in this section, can accurately detect load currents from  $-2.5\text{ A}$  to  $2.5\text{ A}$ . The linear range of the output is from  $250\text{ mV}$  to  $2.75\text{ V}$ . Positive current is represented by output voltages from  $1.5\text{ V}$  to  $2.75\text{ V}$ , whereas negative current is represented by output voltages from  $250\text{ mV}$  to  $1.5\text{ V}$ . The difference amplifier is the [INA213](#) current-shunt monitor, whose supply and reference voltages are supplied by the low-drift REF2030.

### 10.2 Typical Application

#### 10.2.1 Low-Side, Current-Sensing Application



**Figure 49. Low-Side, Current-Sensing Application**

## Typical Application (continued)

### 10.2.1.1 Design Requirements

The design requirements are as follows:

1. Supply voltage: 5.0 V
2. Load current:  $\pm 2.5$  A
3. Output: 250 mV to 2.75 V
4. Maximum shunt voltage:  $\pm 25$  mV

### 10.2.1.2 Detailed Design Procedure

Low-side current sensing is desirable because the common-mode voltage is near ground. Therefore, the current-sensing solution is independent of the bus voltage,  $V_{BUS}$ . When sensing bidirectional currents, use a differential amplifier with a reference pin. This procedure allows for the differentiation between positive and negative currents by biasing the output stage such that it can respond to negative input voltages. There are a variety of methods for supplying power ( $V+$ ) and the reference voltage ( $V_{REF}$ , or  $V_{BIAS}$ ) to the differential amplifier. For a low-drift solution, use a monolithic reference that supplies both power and the reference voltage. Figure 50 shows the general circuit topology for a low-drift, low-side, bidirectional, current-sensing solution. This topology is particularly useful when interfacing with an ADC; see Figure 49. Not only do  $V_{REF}$  and  $V_{BIAS}$  track over temperature, but their matching is much better than alternate topologies. For a more detailed version of the design procedure, refer to TIDU357.

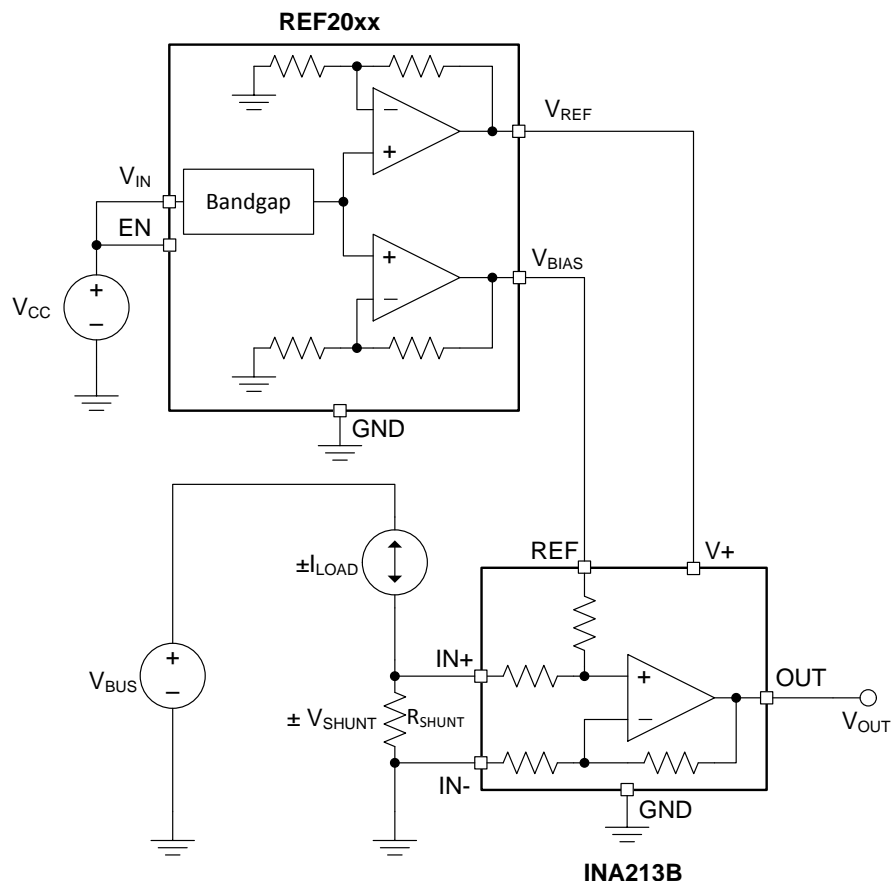


Figure 50. Low-Drift, Low-side, Bidirectional, Current-Sensing Circuit Topology

The transfer function for the circuit given in Figure 50 is as shown in Equation 5:

$$\begin{aligned}
 V_{OUT} &= G \cdot (\pm V_{SHUNT}) + V_{BIAS} \\
 &= G \cdot (\pm I_{LOAD} \cdot R_{SHUNT}) + V_{BIAS}
 \end{aligned}
 \tag{5}$$

## Typical Application (continued)

### 10.2.1.2.1 Shunt Resistor

As illustrated in [Figure 50](#), the value of  $V_{SHUNT}$  is the ground potential for the system load. If the value of  $V_{SHUNT}$  is too large, issues may arise when interfacing with systems whose ground potential is actually 0 V. Also, a value of  $V_{SHUNT}$  that is too negative may violate the input common-mode voltage of the differential amplifier in addition to potential interfacing issues. Therefore, limiting the voltage across the shunt resistor is important. [Equation 6](#) can be used to calculate the maximum value of  $R_{SHUNT}$ .

$$R_{SHUNT(max)} = \frac{V_{SHUNT(max)}}{I_{LOAD(max)}} \quad (6)$$

Given that the maximum shunt voltage is  $\pm 25$  mV and the load current range is  $\pm 2.5$  A, the maximum shunt resistance is calculated as shown in [Equation 7](#).

$$R_{SHUNT(max)} = \frac{V_{SHUNT(max)}}{I_{LOAD(max)}} = \frac{25mV}{2.5A} = 10m\Omega \quad (7)$$

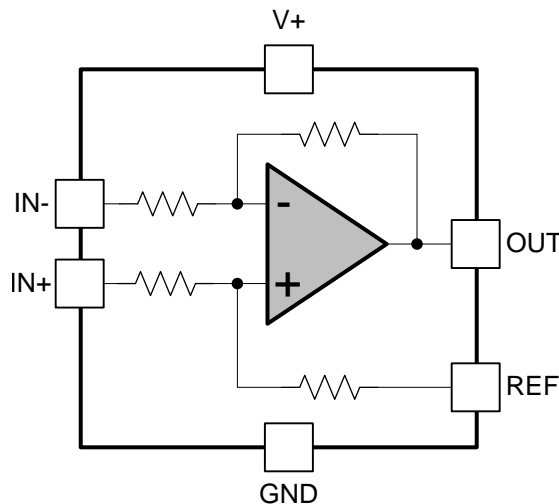
To minimize errors over temperature, select a low-drift shunt resistor. To minimize offset error, select a shunt resistor with the lowest tolerance. For this design, the Y14870R01000B9W resistor is used.

### 10.2.1.2.2 Differential Amplifier

The differential amplifier used for this design should have the following features:

1. Single-supply (3 V),
2. Reference voltage input,
3. Low initial input offset voltage ( $V_{OS}$ ),
4. Low-drift,
5. Fixed gain, and
6. Low-side sensing (input common-mode range below ground).

For this design, a current-shunt monitor (INA213) is used. The INA21x family topology is shown in [Figure 51](#). The INA213B specifications can be found in the [INA213 product data sheet](#).



**Figure 51. INA21x Current-Shunt Monitor Topology**

The INA213B is an excellent choice for this application because all the required features are included. In general, instrumentation amplifiers (INAs) do not have the input common-mode swing to ground that is essential for this application. In addition, INAs require external resistors to set their gain, which is not desirable for low-drift applications. Difference amplifiers typically have larger input bias currents, which reduce solution accuracy at small load currents. Difference amplifiers typically have a gain of 1 V/V. When the gain is adjustable, these amplifiers use external resistors that are not conducive to low-drift applications.

## Typical Application (continued)

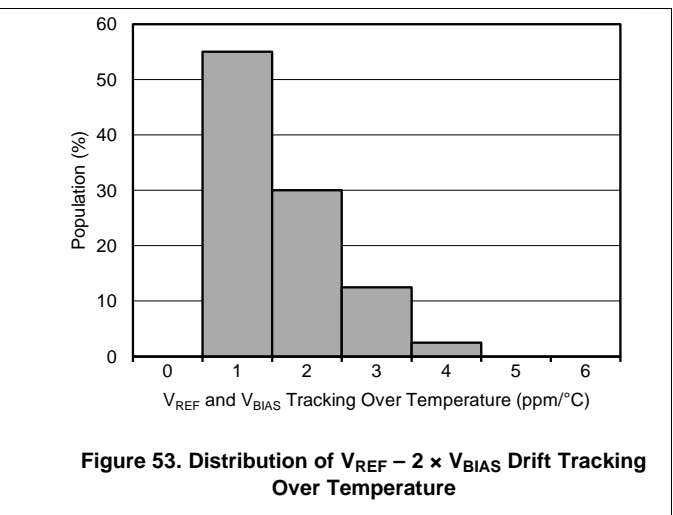
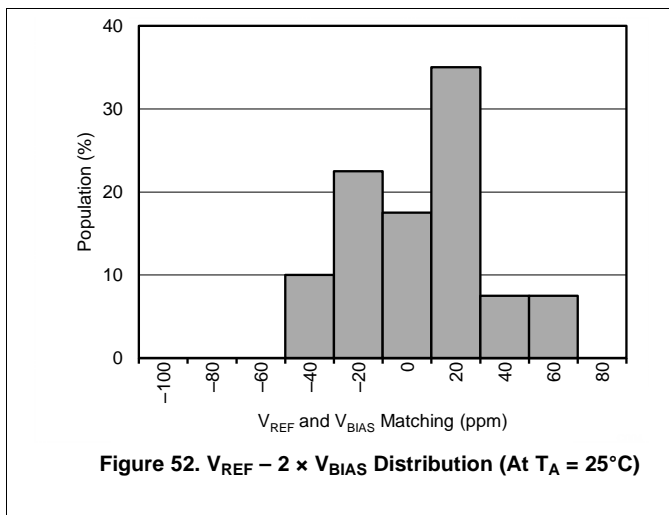
### 10.2.1.2.3 Voltage Reference

The voltage reference for this application should have the following features:

1. Dual output (3.0 V and 1.5 V),
2. Low drift, and
3. Low tracking errors between the two outputs.

For this design, the REF2030 is used. The REF20xx topology is as shown in the [Functional Block Diagram](#) section.

The REF2030 is an excellent choice for this application because of its dual output. The temperature drift of 8 ppm/°C and initial accuracy of 0.05% make the errors resulting from the voltage reference minimal in this application. In addition, there is minimal mismatch between the two outputs and both outputs track very well across temperature, as shown in [Figure 52](#) and [Figure 53](#).



### 10.2.1.2.4 Results

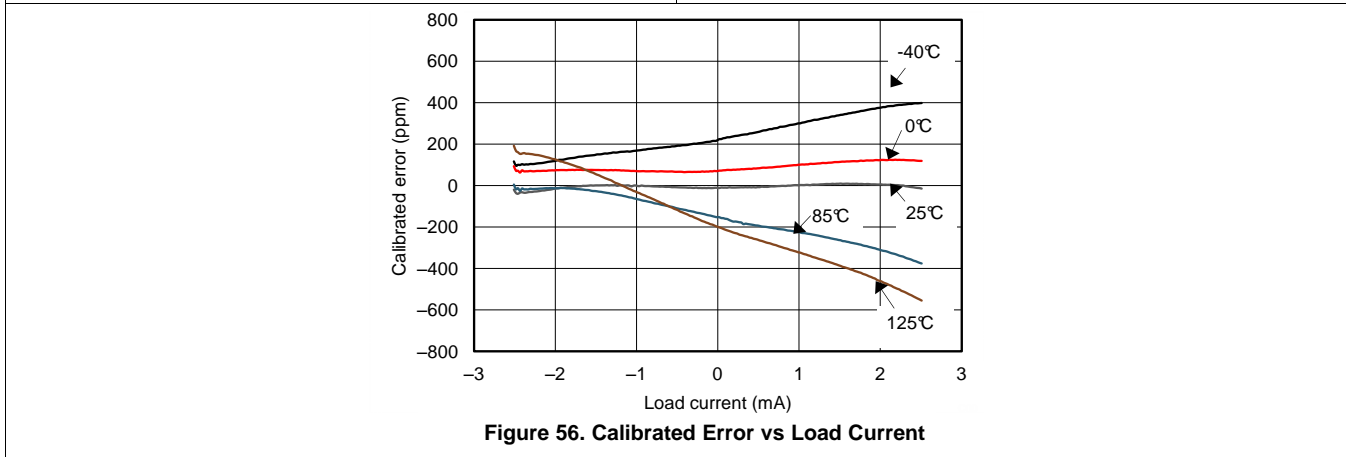
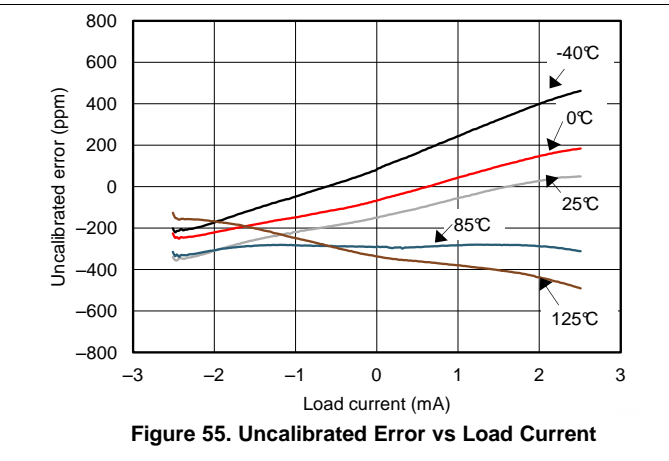
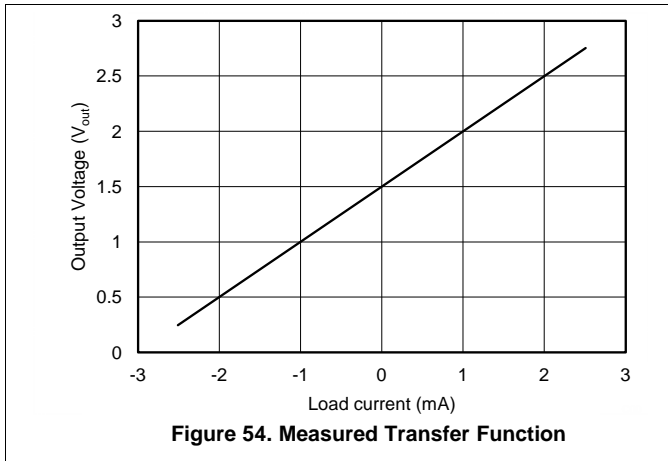
[Table 1](#) summarizes the measured results.

**Table 1. Measured Results**

| ERROR   | UNCALIBRATED (%) | CALIBRATED (%) |
|---|------------------|----------------|
| Error across the full load current range (25°C)           | ±0.0355          | ±0.004         |
| Error across the full load current range (-40°C to 125°C) | ±0.0522          | ±0.0606        |

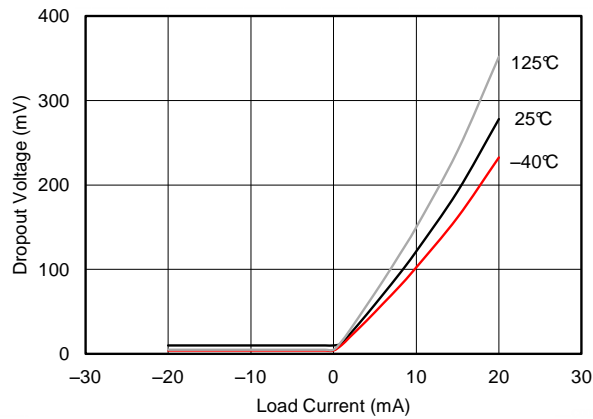
### 10.2.1.3 Application Curves

Performing a two-point calibration at 25°C removes the errors associated with offset voltage, gain error, and so forth. Figure 54 to Figure 56 show the measured error at different conditions. For a more detailed description on measurement procedure, calibration, and calculations, please refer to TIDU357.



## 11 Power-Supply Recommendations

The REF20xx family of references feature an extremely low-dropout voltage. These references can be operated with a supply of only 20 mV above the output voltage. For loaded reference conditions, a typical dropout voltage versus load is shown in [Figure 57](#). A supply bypass capacitor ranging between 0.1  $\mu\text{F}$  to 10  $\mu\text{F}$  is recommended.



**Figure 57. Dropout Voltage vs Load Current**

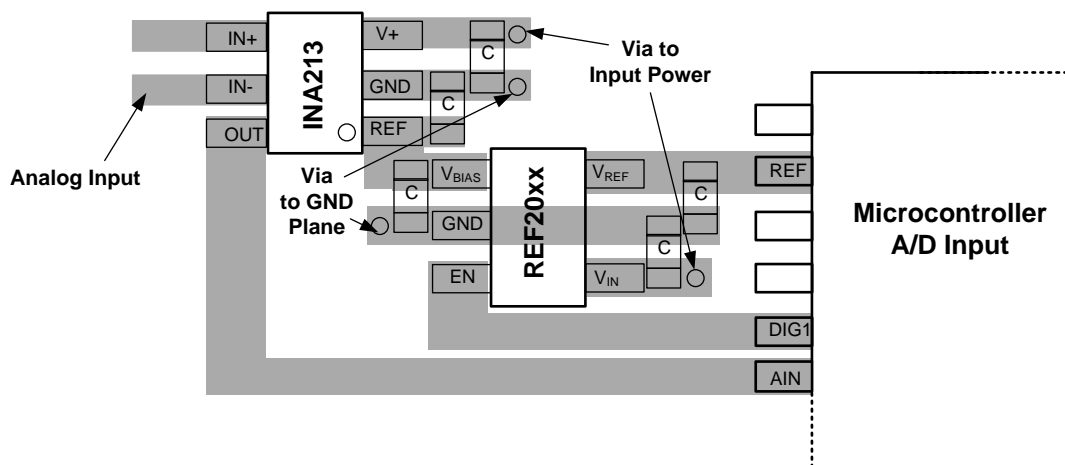
## 12 Layout

### 12.1 Layout Guidelines

Figure 58 shows an example of a PCB layout for a data acquisition system using the REF2030. Some key considerations are:

- Connect low-ESR, 0.1- $\mu$ F ceramic bypass capacitors at  $V_{IN}$ ,  $V_{REF}$ , and  $V_{BIAS}$  of the REF2030.
- Decouple other active devices in the system per the device specifications.
- Using a solid ground plane helps distribute heat and reduces electromagnetic interference (EMI) noise pickup.
- Place the external components as close to the device as possible. This configuration prevents parasitic errors (such as the Seebeck effect) from occurring.
- Minimize trace length between the reference and bias connections to the INA and ADC to reduce noise pickup.
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when absolutely necessary.

### 12.2 Layout Example



**Figure 58. Layout Example**



## 13 Device and Documentation Support

### 13.1 Documentation Support

#### 13.1.1 Related Documentation

For related documentation see the following:

- [INA21x Voltage Output, Low- or High-Side Measurement, Bidirectional, Zero-Drift Series, Current-Shunt Monitors](#) (SBOS437)
- [Low-Drift Bidirectional Single-Supply Low-Side Current Sensing Reference Design](#) (TIDU357)

### 13.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 2. Related Links**

| PARTS   | PRODUCT FOLDER             | SAMPLE & BUY               | TECHNICAL DOCUMENTS        | TOOLS & SOFTWARE           | SUPPORT & COMMUNITY        |
|---------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| REF2025 | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |
| REF2030 | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |
| REF2033 | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |
| REF2041 | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |

### 13.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 13.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 13.5 Trademarks

E2E is a trademark of Texas Instruments.

e-Trim is a trademark of Texas Instruments, Inc.

All other trademarks are the property of their respective owners.

### 13.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 13.7 Glossary

**SLYZ022** — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2)         | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| REF2025AIDDCR    | ACTIVE        | SOT-23-THIN  | DDC             | 5    | 3000        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-2-260C-1 YEAR  | -40 to 125   | GACM                    | <a href="#">Samples</a> |
| REF2025AIDDCT    | ACTIVE        | SOT-23-THIN  | DDC             | 5    | 250         | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-2-260C-1 YEAR  | -40 to 125   | GACM                    | <a href="#">Samples</a> |
| REF2030AIDDCR    | ACTIVE        | SOT-23-THIN  | DDC             | 5    | 3000        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-2-260C-1 YEAR  | -40 to 125   | GADM                    | <a href="#">Samples</a> |
| REF2030AIDDCT    | ACTIVE        | SOT-23-THIN  | DDC             | 5    | 250         | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-2-260C-1 YEAR  | -40 to 125   | GADM                    | <a href="#">Samples</a> |
| REF2033AIDDCR    | ACTIVE        | SOT-23-THIN  | DDC             | 5    | 3000        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-2-260C-1 YEAR  | -40 to 125   | GAEM                    | <a href="#">Samples</a> |
| REF2033AIDDCT    | ACTIVE        | SOT-23-THIN  | DDC             | 5    | 250         | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-2-260C-1 YEAR  | -40 to 125   | GAEM                    | <a href="#">Samples</a> |
| REF2041AIDDCR    | ACTIVE        | SOT-23-THIN  | DDC             | 5    | 3000        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-2-260C-1 YEAR  | -40 to 125   | GAFM                    | <a href="#">Samples</a> |
| REF2041AIDDCT    | ACTIVE        | SOT-23-THIN  | DDC             | 5    | 250         | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-2-260C-1 YEAR  | -40 to 125   | GAFM                    | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| REF2025AIDDCR | SOT-23-THIN  | DDC             | 5    | 3000 | 179.0              | 8.4                | 3.2     | 3.2     | 1.4     | 4.0     | 8.0    | Q3            |
| REF2025AIDDCT | SOT-23-THIN  | DDC             | 5    | 250  | 179.0              | 8.4                | 3.2     | 3.2     | 1.4     | 4.0     | 8.0    | Q3            |
| REF2030AIDDCR | SOT-23-THIN  | DDC             | 5    | 3000 | 179.0              | 8.4                | 3.2     | 3.2     | 1.4     | 4.0     | 8.0    | Q3            |
| REF2030AIDDCT | SOT-23-THIN  | DDC             | 5    | 250  | 179.0              | 8.4                | 3.2     | 3.2     | 1.4     | 4.0     | 8.0    | Q3            |
| REF2033AIDDCR | SOT-23-THIN  | DDC             | 5    | 3000 | 179.0              | 8.4                | 3.2     | 3.2     | 1.4     | 4.0     | 8.0    | Q3            |
| REF2033AIDDCT | SOT-23-THIN  | DDC             | 5    | 250  | 179.0              | 8.4                | 3.2     | 3.2     | 1.4     | 4.0     | 8.0    | Q3            |
| REF2041AIDDCR | SOT-23-THIN  | DDC             | 5    | 3000 | 179.0              | 8.4                | 3.2     | 3.2     | 1.4     | 4.0     | 8.0    | Q3            |
| REF2041AIDDCT | SOT-23-THIN  | DDC             | 5    | 250  | 179.0              | 8.4                | 3.2     | 3.2     | 1.4     | 4.0     | 8.0    | Q3            |

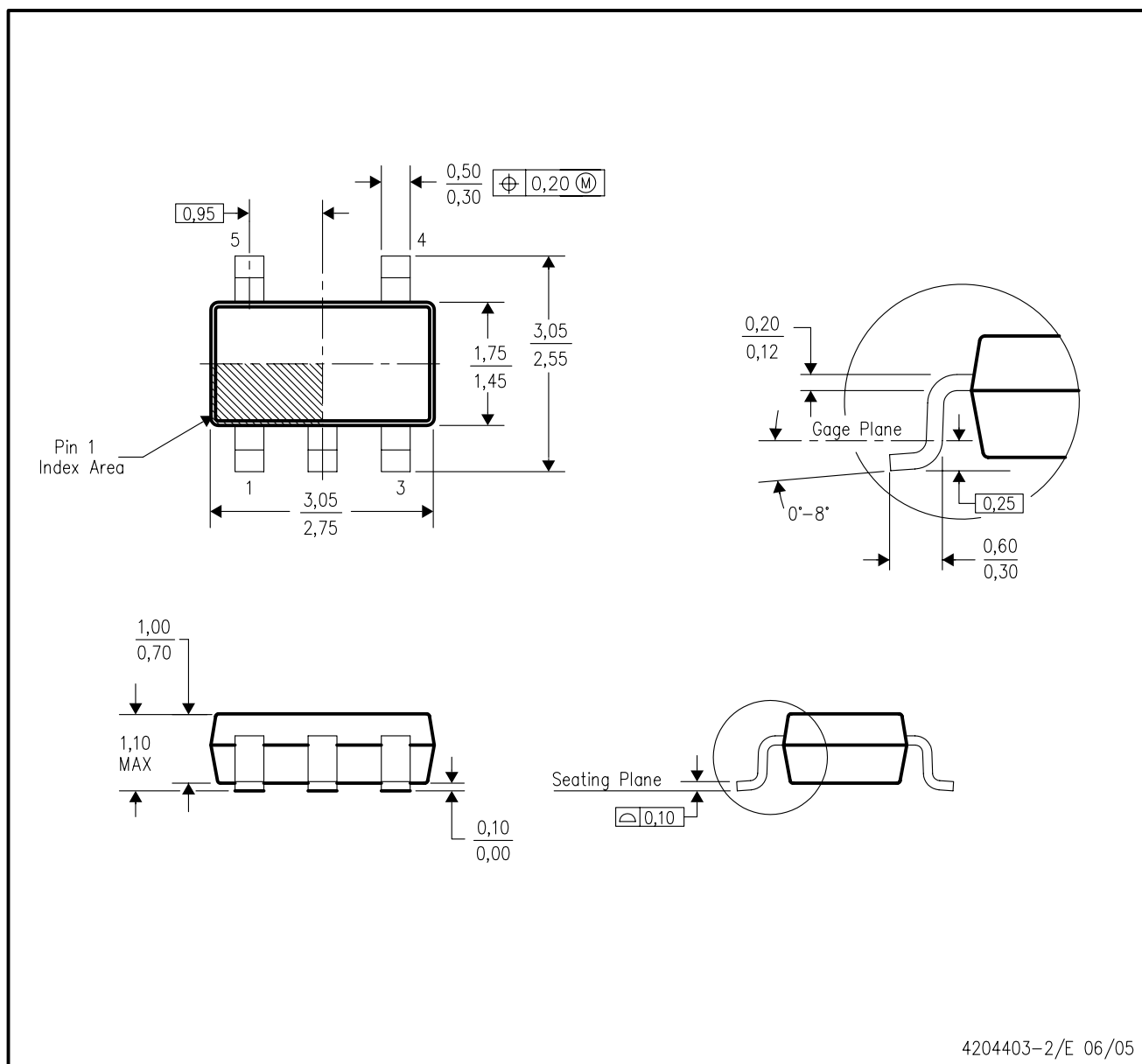
**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| REF2025AIDDCR | SOT-23-THIN  | DDC             | 5    | 3000 | 195.0       | 200.0      | 45.0        |
| REF2025AIDDC  | SOT-23-THIN  | DDC             | 5    | 250  | 195.0       | 200.0      | 45.0        |
| REF2030AIDDCR | SOT-23-THIN  | DDC             | 5    | 3000 | 195.0       | 200.0      | 45.0        |
| REF2030AIDDC  | SOT-23-THIN  | DDC             | 5    | 250  | 195.0       | 200.0      | 45.0        |
| REF2033AIDDCR | SOT-23-THIN  | DDC             | 5    | 3000 | 195.0       | 200.0      | 45.0        |
| REF2033AIDDC  | SOT-23-THIN  | DDC             | 5    | 250  | 195.0       | 200.0      | 45.0        |
| REF2041AIDDCR | SOT-23-THIN  | DDC             | 5    | 3000 | 195.0       | 200.0      | 45.0        |
| REF2041AIDDC  | SOT-23-THIN  | DDC             | 5    | 250  | 195.0       | 200.0      | 45.0        |

DDC (R-PDSO-G5)

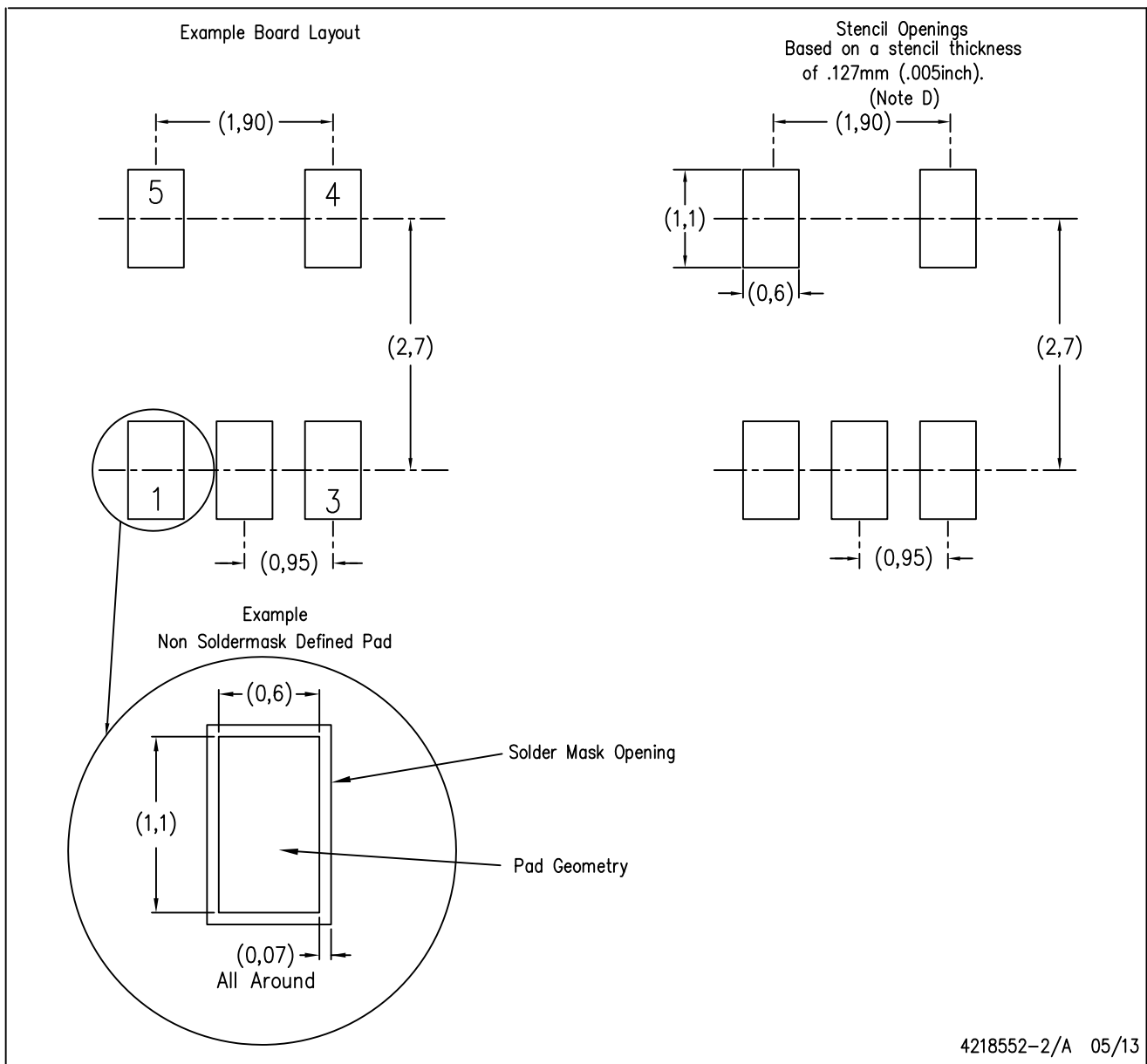
PLASTIC SMALL-OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion.
  - Falls within JEDEC MO-193 variation AB (5 pin).

DDC (R-PDSO-G5)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.



## IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.