SN65HVD63 AISG® On and Off Keying Coax Modem Transceiver

1 Features

- 3-V to 5.5-V Supply Range
- 1.6-V to 5.5-V Independent Logic Supply
- –15-dBm to +5-dBm Wide-Input Dynamic Range for Receiver
- 0-dBm to 6-dBm Adjustable Power Delivered by the Driver to the Coax
- AISG® V2.0-Compliant Output Emission Profile Also Conforms to Proposed AISG V3.0 Specifications
- Low-Power Standby Mode
- Direction Control Output for RS-485 Bus Arbitration
- Up to 115 kbps of Signaling Support
- 2.176-MHz Center Frequency for Integrated Active Bandpass Filter
- 3-mm × 3-mm 16-Pin VQFN Package

2 Applications

- AISG – Interface for Antenna Line Devices
- Tower-Mounted Amplifiers (TMA)
- General Modem Interfaces

3 Description

The SN65HVD63 transceiver modulates and demodulates signals between a logic (baseband) interface and a frequency suitable for long coaxial media, to facilitate wired data transfer among radio equipment.

The SN65HVD63 device is an integrated AISG transceiver designed to meet the requirements of the upcoming Antenna Interface Standards Group v3.0 specification.

The SN65HVD63 receiver integrates an active bandpass filter to enable demodulation of signals even in the presence of spurious frequency components. The filter has a 2.176-MHz center frequency.

The transmitter supports adjustable output power levels from 0 dBm to 6 dBm delivered to the 50-Ω coax cable. The SN65HVD63 transmitter is compliant with the spectrum emission requirement provided by the AISG standard.

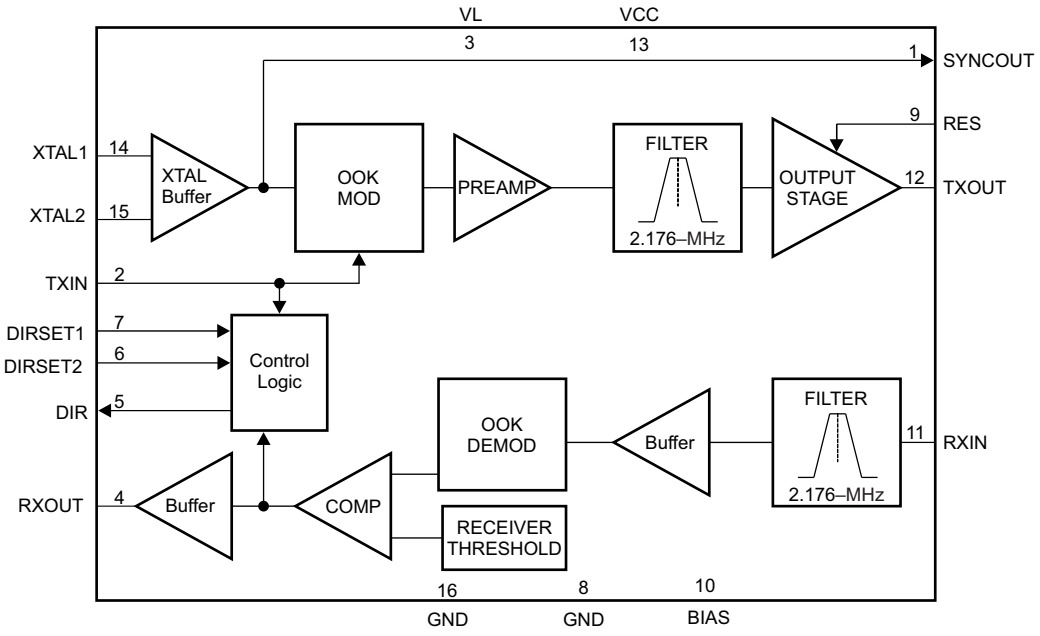
A direction control output facilitates bus arbitration for an RS-485 interface. This device integrates an oscillator input for a crystal, and also accepts standard clock inputs to the oscillator.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN65HVD63	VQFN (16)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Block Diagram



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4 Revision History

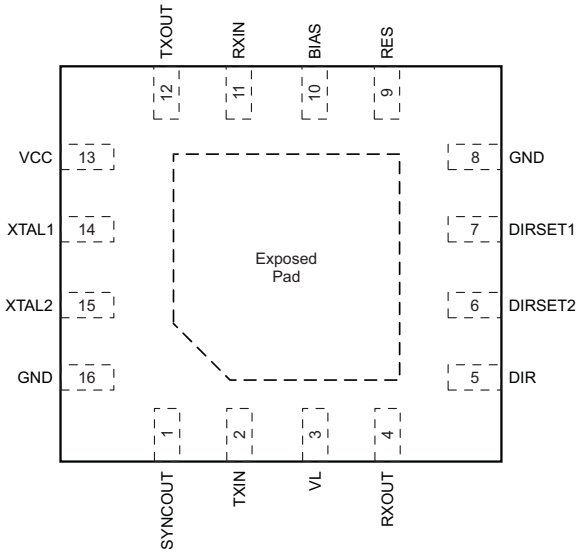
DATE	REVISION	NOTES
July 2015	*	Initial release.

5 Device Comparison Table

PART NUMBER	STANDARD SUPPORTED	SPURIOUS FREQUENCY RANGE	MAXIMUM LEVEL
SN65HVD62	AISG 2.0	≤ 1.1 MHz	2 dBm (793 mV_{PP})
		≤ 4.17 MHz	2 dBm (793 mV_{PP})
SN65HVD63	AISG 3.0	≤ 1.35 MHz	–13 dBm (142 mV_{PP})
		≤ 3.5 MHz	–13 dBm (142 mV_{PP})

6 Pin Configuration and Functions

RGT Package
16-Pin VQFN With Exposed Thermal Pad
Top View



Pin Functions

PIN			DESCRIPTION
NAME	NO.	TYPE	
BIAS	10	O	Bias voltage output for setting driver output power by external resistors
DIR	5	O	Direction control output signal for bus arbitration
DIRSET1	7	—	DIRSET1 and DIRSET2: Bits to set the duration of DIR DIRSET[2:1]: [L:L] = 9.6 kbps; [L:H] = 38.4 kbps; [H:L] = 115 kbps; [H:H] = standby mode
DIRSET2	6	—	
GND	8	—	Ground
	16		
RES	9	P	Input voltage to adjust driver output power that is set by external resistors from BIAS pin to GND
RXIN	11	I	Modulated input signal to the receiver
RXOUT	4	O	Digital data bit stream from receiver
SYNCOUT	1	O	Open-drain output to synchronize other devices to the 4x-carrier oscillator at XTAL1 and XTAL2
TXIN	2	I	Digital data bit stream to driver
TXOUT	12	O	Modulated output signal from the driver
V_{CC}	13	P	Analog supply voltage for the device
VL	3	P	Logic supply voltage for the device
XTAL1	14	I/O	I/O pins of the crystal oscillator. Connect a 4 × f_C crystal between these pins or connect XTAL1 to an 8.704-MHz clock and connect XTAL2 to GND.
XTAL2	15		
EP	—	—	Exposed pad. Connection to ground plane is recommended for best thermal conduction.

7 Specifications

7.1 Absolute Maximum Ratings(1)

	MIN	MAX	UNIT
Supply voltage, V_{CC} and VL	–0.5	6	V
Voltage at coax pins	–0.5	6	V
Voltage at logic pins	–0.3	V_{VL} + 0.3	V
Logic output current	–20	20	mA
TXOUT output current	Internally limited		
SYNCOUT output current	Internally limited		
Junction temperature, T_J		170	°C
Continuous total power dissipation	See the *Thermal Information*		°C
Storage temperature, T_{stg}(2)	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Applicable before the device is installed in the final product.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Analog supply voltage		3		5.5	V
V_L	Logic supply voltage		1.6		5.5	V
$V_{I(pp)}$	Input signal amplitude at RXIN				1.12	Vpp
V_{IH}	High-level input voltage	TXIN, DIRSET1, DIRSET2	70%V_L		V_L	V
		XTAL1, XTAL2	70%V_{CC}		V_{CC}	
V_{IL}	Low-level input voltage	TXIN, DIRSET1, DIRSET2	0		30%V_L	V
		XTAL1, XTAL2	0		30%V_{CC}	
$1/t_{UI}$	Data signaling rate		9.6		115	kbps
F_{OSC}	Oscillator frequency		–30 ppm	8.704	30 ppm	MHz
Z_{LOAD}	Load impedance between TXOUT to RXIN			50		Ω
	Load impedance between RXIN and GND at f_C (channel)			50		Ω
R1	Bias resistor between BIAS and RES			4.1		kΩ
R2	Bias resistor between RES and GND			10		kΩ
R_{SYNC}	Pullup resistor between SYNCOUT and V_{CC}			1		kΩ
V_{RES}	Voltage at RES pin		0.7		1.5	V
C_C	Coupling capacitance between RXIN and coax (channel)			220		nF
C_{BIAS}	Capacitance between BIAS and GND			1		µF
T_A	Operating free-air temperature		–40		105	°C
T_J	Junction temperature		–40		125	°C

7.4 Thermal Information

THERMAL METRIC(1)		VQFN RGT16 Pins	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	49.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

Thermal Information (continued)

THERMAL METRIC[1]		VQFN RGT16 Pins	UNIT
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	64.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	22.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	22.9	°C/W
$R_{\theta JCbot}$	Junction-to-case (bottom) thermal resistance	25	°C/W

7.5 Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
POWER SUPPLY							
I_{CC}	Supply current	DIRSET1 = L, DIRSET2 = H	TXIN = L (active)		28	33	mA
			TXIN = H (quiescent)		25	31	
			TXIN = 115 kbps, 50% duty cycle		27	33	
		DIRSET1 = H, DIRSET2 = H (standby)			12	17	
I_{VL}	Logic supply current	TXIN = H, RXIN = DC input				50	µA
PSRR	Receiver power supply rejection ratio	$V_{TXIN} = V_L$		45	60		dB
LOGIC PINS							
V_{OH}	High-level logic output voltage (RXOUT, DIR)	I_{OH} = –4 mA for V_L > 2.4 V, I_{OH} = –2 mA for V_L < 2.4 V		90%V_{VL}			V
V_{OL}	Low-level logic output voltage (RXOUT, DIR)	I_{OL} = 4 mA for V_L > 2.4 V, I_{OL} = 2 mA for V_L < 2.4 V				10%V_{VL}	V
COAX DRIVER							
$V_{O(PP)}$	Peak-to-peak output voltage at device pin TXOUT (see Figure 19)	V_{RES} = 1.5 V (Maximum setting)		2.24	2.5		V_{PP}
		V_{RES} = 0.7 V (Minimum setting)			1.17	1.3	
$V_{O(PP)}$	Peak-to-peak voltage at coax out (see Figure 19)	V_{RES} = 1.5 V		5	6		dBm
		V_{RES} = 0.7 V			–0.6	0.3	
$V_{O(OFF)}$	Off-state output voltage	At TXOUT				1	mVpp
		At coax out				–60	dBm
	Output emissions	Coupled to coaxial cable with characteristic impedance of 50 Ω, as shown in Figure 1 (1)(2)					N/A
f_O	Output frequency				2.176		MHz
Δf	Output frequency variation			–100		100	ppm
Z_O	Output impedance	At 100 kHz			0.03		Ω
		At 10 MHz			3.5		
$\lvert I_{OS} \rvert$	Short-circuit output current	TXOUT is also protected by a thermal shutdown circuit during short-circuit faults			300	450	mA
COAX RECEIVER							
V_{IT}	Input threshold	f_{IN} = 2.176 MHz		79	112	158	mVPP
				–18	–15	–12	dBm
Z_{IN}	Input impedance	f = f_O		11	21		kΩ
RECEIVER FILTER							
f_{PB}	Passband	VRXIN = 1.12VP_P		1.1		4.17	MHz
f_{REJ}	Receiver rejection range	2.176-MHz carrier amplitude of 112.4 mV_{PP}, frequency band of spurious components with 800 mVPP allowed.		1.1		4.17	MHz
$t_{noise\ filter}$	Receiver noise filter time (slow bit rate)	DIRSET for 9.6 kbps			4		µs
	Receiver noise filter time (fast bit rate)	DIRSET for > 9.6 kbps			2		µs
XTAL AND SYNC							
I_I	Input leakage current	XTAL1, XTAL2, 0V < V_{IN} < V_{CC}		–15		15	µA
V_{OL}	Output low voltage	SYNCOUT, with 1-kΩ resistor from SYNCOUT to V_{CC}				0.4	V

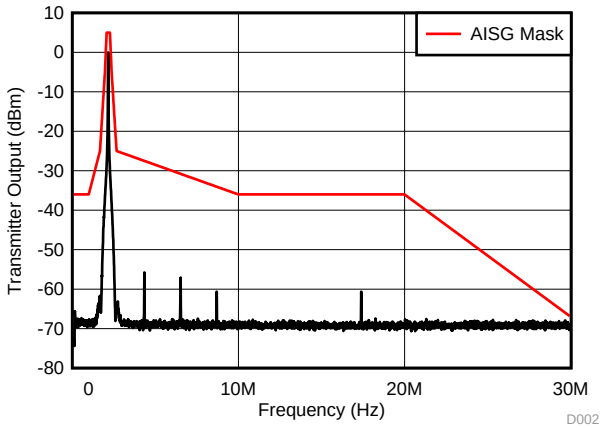
(1) Specified by design with a recommended 470-pF capacitor between RXIN and GND. Measurements above 150 MHz are determined by setup.
(2) Conforms to AISG spectrum emissions mask, 3GPP TS 25.461, see Figure 21.

7.6 Switching Characteristics

over recommended operating conditions (unless otherwise noted)

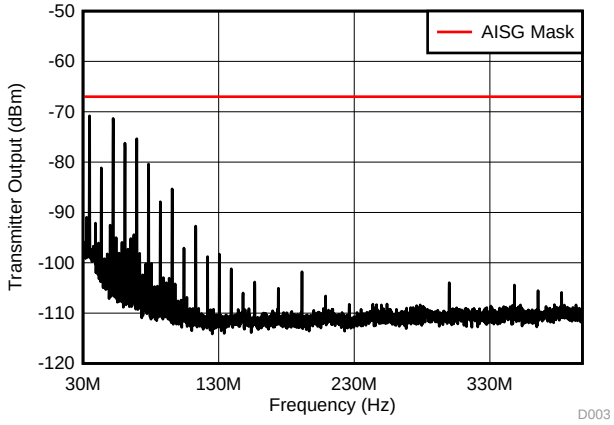
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pAQ}, t_{pQA}	Coax driver propagation delay	See Figure 19			5	µs
t_r, t_f	Coax receiver output rise/fall time	C_L = 15 pF, R_L = 1 kΩ; see Figure 19			20	ns
t_{PHL}, t_{PLH}	Receiver propagation delay	See Figure 20		5.5	11	µs
	Coax receiver output duty cycle	$V_{RXIN(ON)}$ = 630 mVpp, $V_{RXIN(OFF)}$ < 5 mVpp, 50% duty cycle	40%		60%	
		$V_{RXIN(ON)}$ = 200 mVpp, $V_{RXIN(OFF)}$ < 5 mVpp, 50% duty cycle	40%		60%	
t_{DIR}	Direction control active duration	DIRSET2 = GND or OPEN, DIRSET1 = GND or OPEN		1667		µs
		DIRSET2 = GND, DIRSET1 = VL		417		
		DIRSET2 = VL, DIRSET1 = VL		137		
$t_{DIRSKEW}$	Direction control skew (DIR to RXOUT)		270			ns
t_{dis}	Standby disable delay	300 mV_{PP} at 2.176 MHz on RXIN		2		ms
t_{en}	Standby enable delay	300 mV_{PP} at 2.176 MHz on RXIN		2		ms

7.7 Typical Characteristics



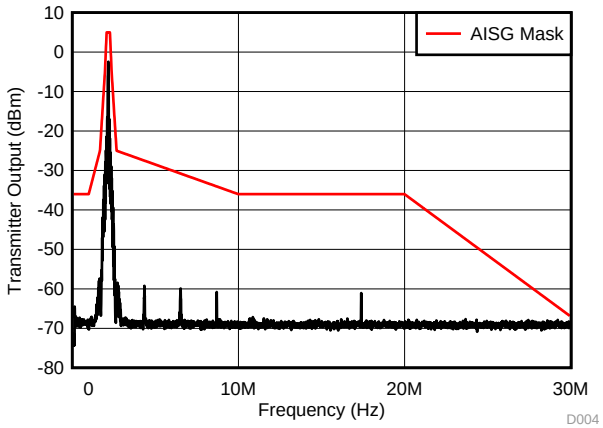
50% Duty Cycle C_F = 470 pF

Figure 1. Low-Frequency Emissions Spectrum With 9.6-kbps Signaling Rate



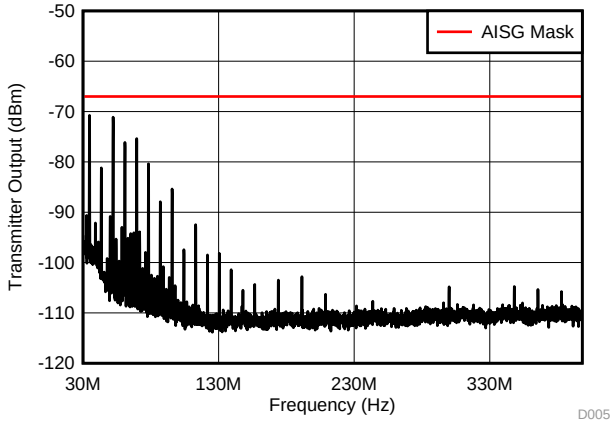
50% Duty Cycle C_F = 470 pF

Figure 2. High-Frequency Emissions Spectrum With 9.6-kbps Signaling Rate



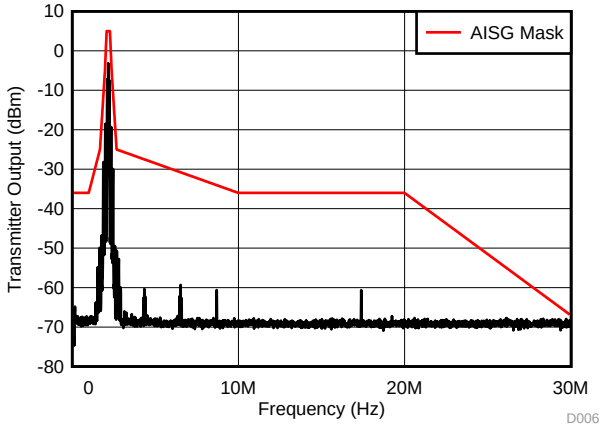
50% Duty Cycle C_F = 470 pF

Figure 3. Low-Frequency Emissions Spectrum With 38.4-kbps Signaling Rate



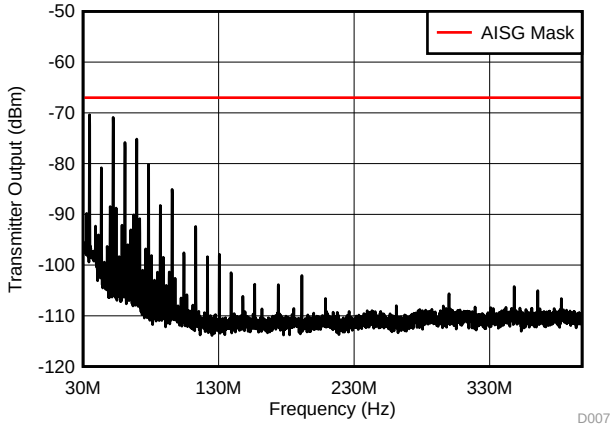
50% Duty Cycle C_F = 470 pF

Figure 4. High-Frequency Emissions Spectrum With 38.4-kbps Signaling Rate



50% Duty Cycle C_F = 470 pF

Figure 5. Low-Frequency Emissions Spectrum With 115.2-kbps Signaling Rate



50% Duty Cycle C_F = 470 pF

Figure 6. High-Frequency Emissions Spectrum With 115.2-kbps Signaling Rate

Typical Characteristics (continued)

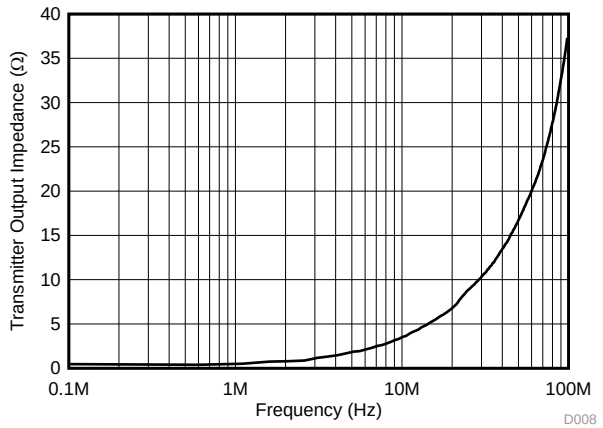


Figure 7. Transmitter Output Impedance

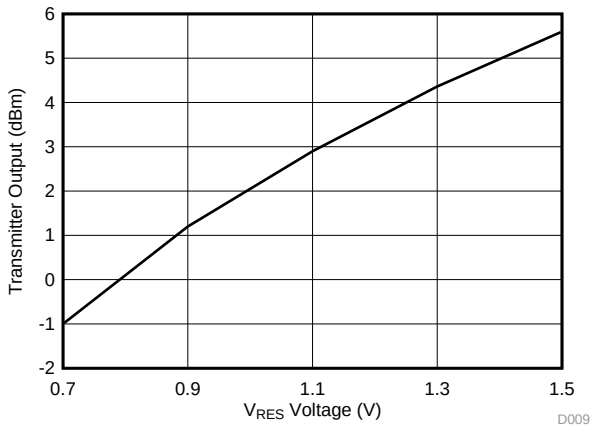


Figure 8. Transmit Power Adjustment

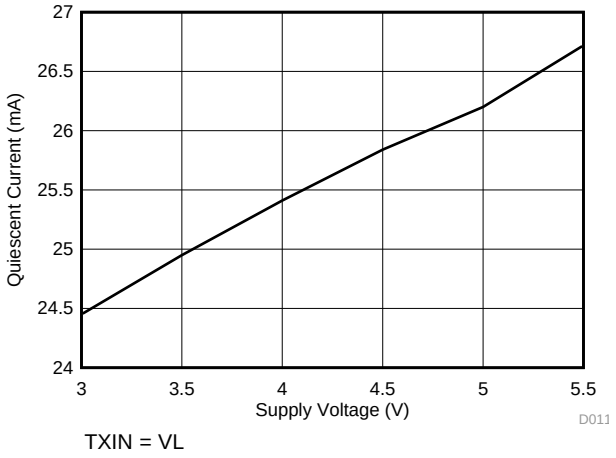


Figure 9. Supply Current vs Supply Voltage While Transmitting

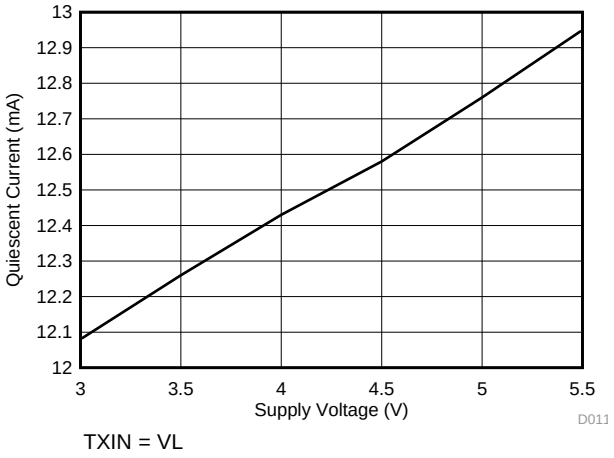


Figure 10. Supply Current vs Supply Voltage in Standby Mode

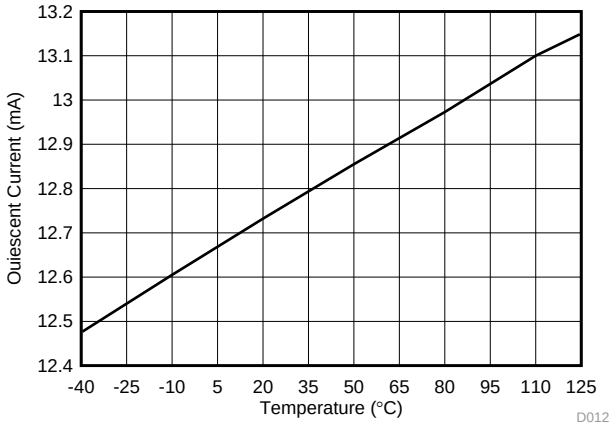


Figure 11. Supply Current vs Temperature in Standby Mode

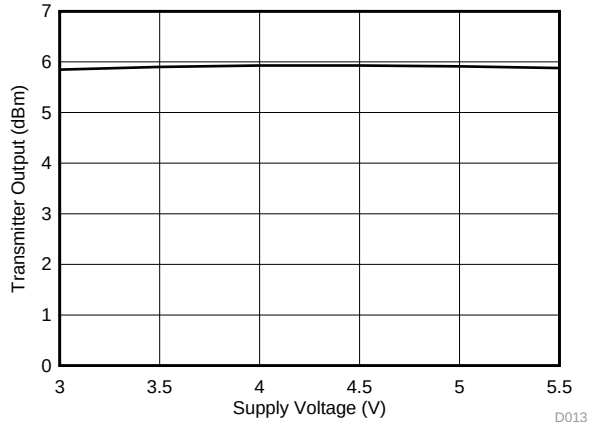


Figure 12. Transmitter Output Power vs Supply Voltage

Typical Characteristics (continued)

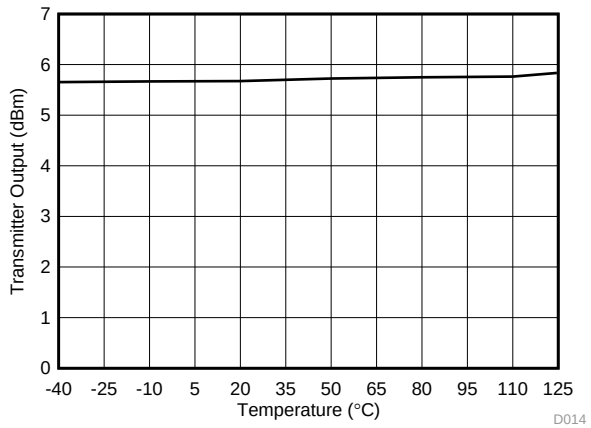


Figure 13. Transmitter Output Power vs Temperature

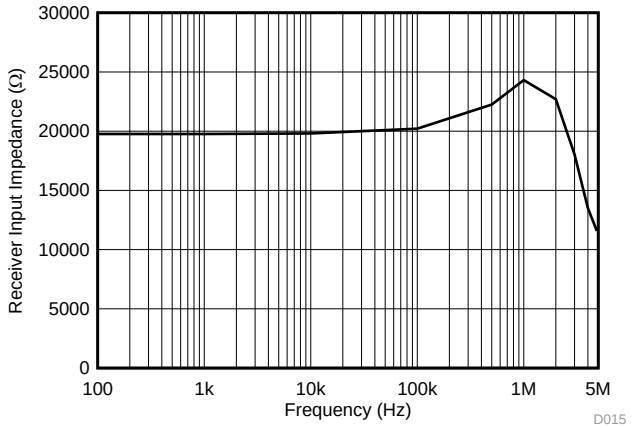


Figure 14. Receiver Input Impedance vs Frequency

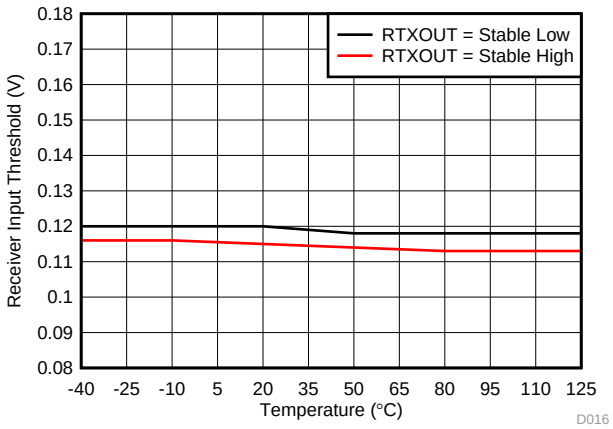


Figure 15. Receiver Input Threshold vs Temperature

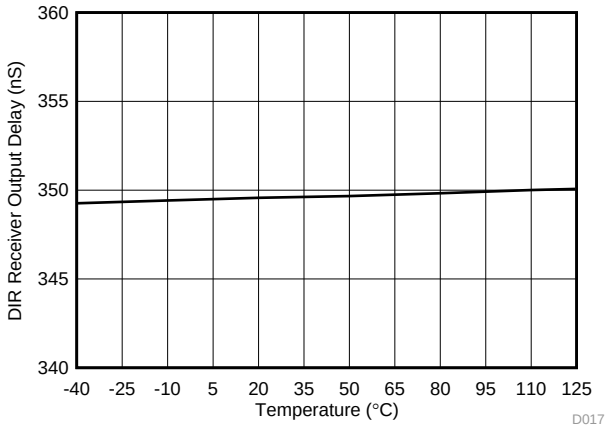


Figure 16. DIR Output Delay vs Temperature

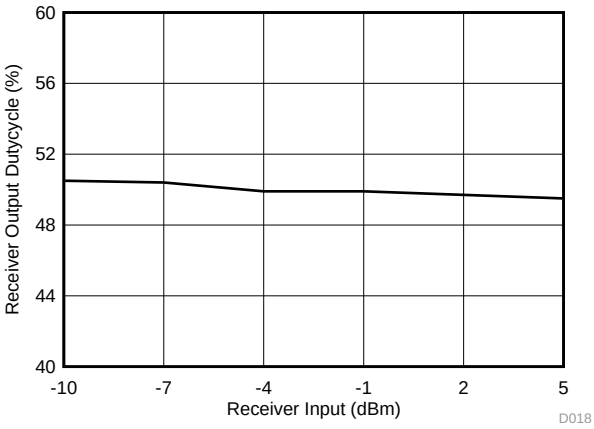


Figure 17. Receiver Duty Cycle With 9.6 kbps Signaling Rate

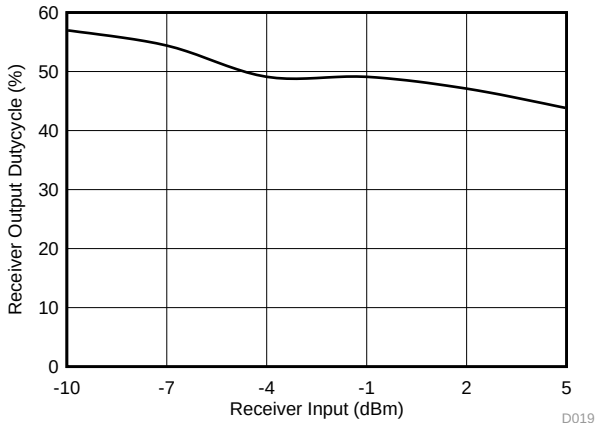


Figure 18. Receiver Duty Cycle With 115.2 kbps Signaling Rate

8 Parameter Measurement Information

Signal generator rate is 115 kbps, 50% duty cycle. Rise and fall times are less than 6 ns, and nominal output levels are 0 V and 3 V. Coupling capacitor, C_C, is 220 nF.

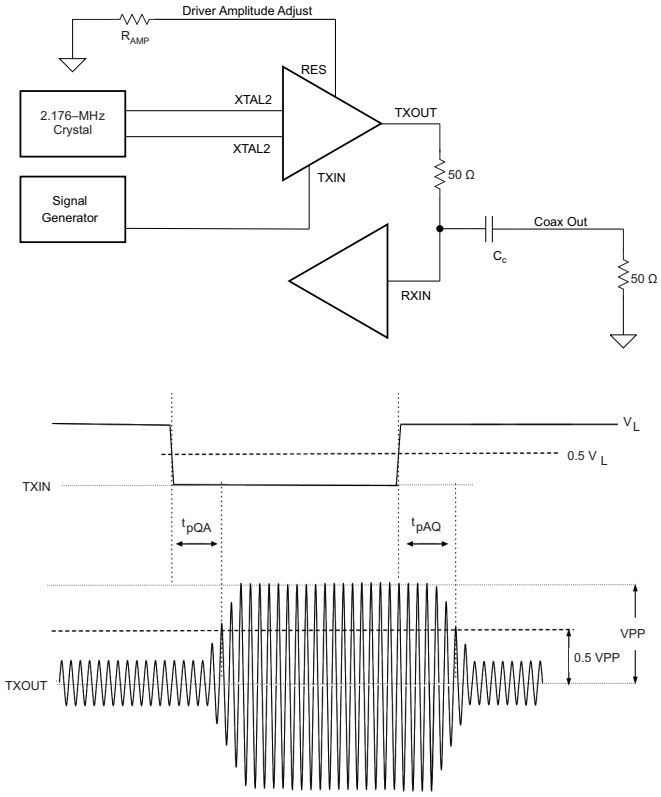


Figure 19. Measurement of Modem Driver Output Voltage With 50-Ω Loads

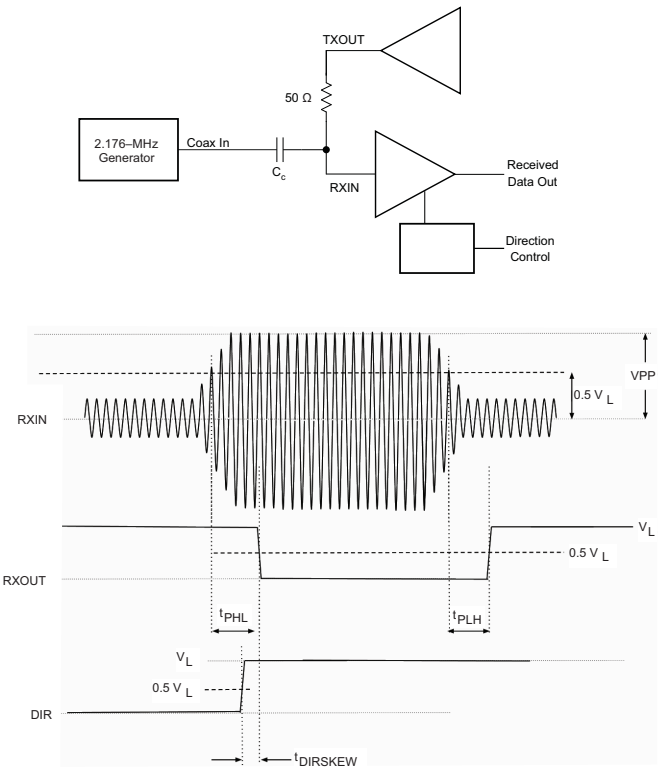


Figure 20. Measurement of Modem Receiver Propagation Delays

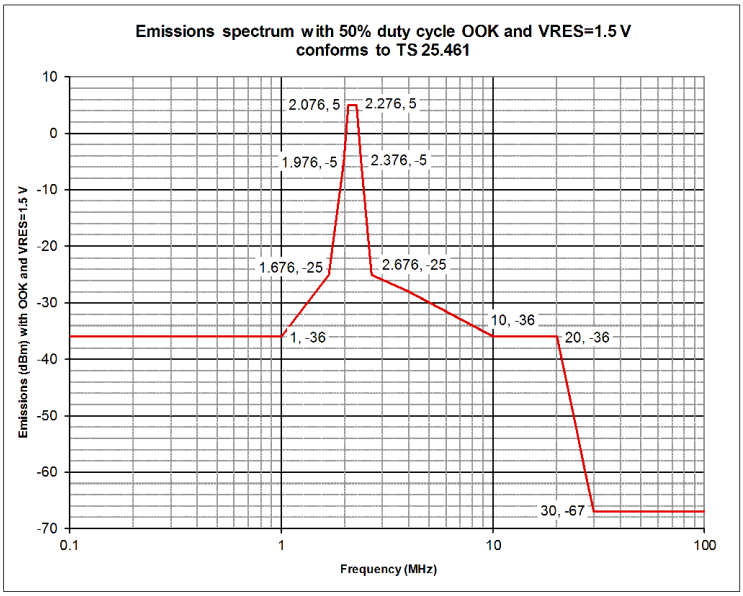


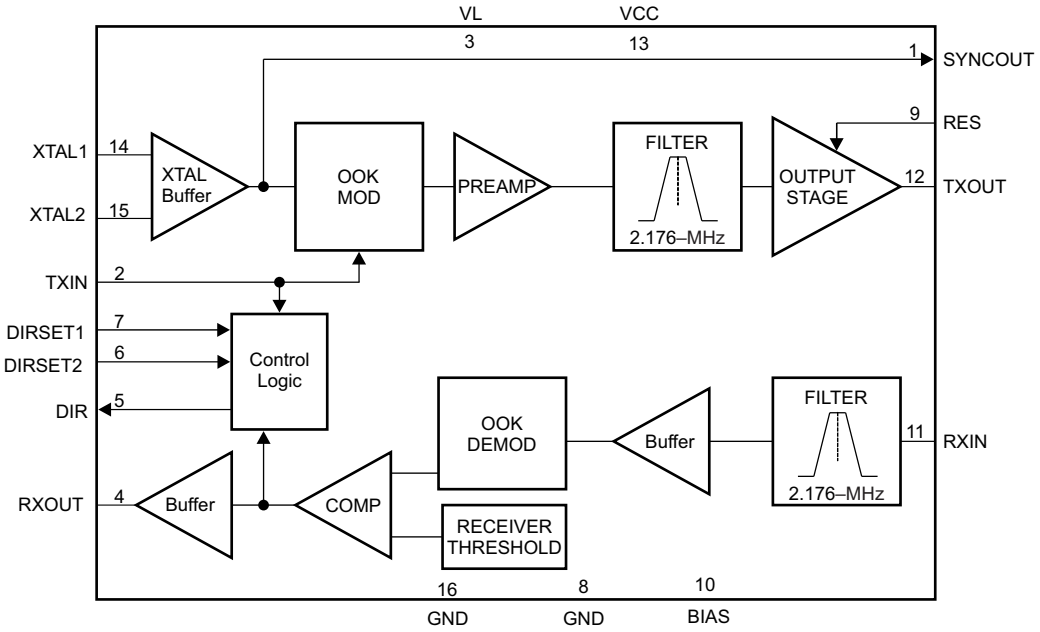
Figure 21. AISG Emissions Template

9 Detailed Description

9.1 Overview

The SN65HVD63 transceiver modulates and demodulates signals between the logic (baseband) and a frequency suitable for long coaxial media. The SN65HVD63 device is an integrated AISG transceiver designed to meet the requirements of the upcoming Antenna Interface Standards Group v3.0 specification. The SN65HVD63 receiver integrates an active bandpass filter to enable demodulation of signals even in the presence of spurious frequency components. The filter has a 2.176-MHz center frequency. The transmitter supports adjustable output power levels from 0 dBm to 6 dBm delivered to the 50-Ω coax cable. The SN65HVD63 transmitter is compliant with the spectrum emission requirement provided by the AISG standard. A direction control output facilitates bus arbitration for an RS-485 interface. This device integrates an oscillator input for a crystal, and also accepts standard clock inputs to the oscillator.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Coaxial Interface

The SN65HVD63 transceiver enables the transfer of data between radio equipment by modulating baseband data to a carrier frequency of 2.176 MHz (per the AISG standard). The transmitter output amplitude can be configured from 0 dBm to 6 dBm in order to communicate over a variety of different links, and the output emissions spectrum is designed to be compliant to AISG limits. The receiver features an active bandpass filter circuit that helps to separate the carrier frequency data from other spurious frequency components.

9.3.2 Reference Input

The 2.176-MHz modulation frequency is derived from an input reference that is nominally 8.704 MHz. The input reference can come either from a crystal or from an oscillator circuit with a tolerance of up to 30 ppm.

9.3.3 RS-485 Direction Control

To facilitate bus arbitration of an RS-485 interface, the SN65HVD63 provides a direction control output that can be used to control the enable/disable controls of an RS-485 transceiver. The direction control output automatically toggles based on activity present on the coaxial input interface, and has an adjustable time constant (controlled by the DIRSET1 and DIRSET2 pins) in order to accommodate various signaling rates.

9.4 Device Functional Modes

If DIRSET1 and DIRSET2 are in a logic high state, the device will be in standby mode. While in standby mode, the receiver functions normally, detecting carrier frequency activity on the RXIN pin and setting the RXOUT state. The transmitter circuits are not active in standby mode, thus the TXOUT pin is idle regardless of the logic state of TXIN. The supply current in standby mode is significantly reduced, allowing power savings when the node is not transmitting.

When not in standby mode, the default power-on state is idle. When in idle mode, RXOUT is high, and TXOUT is quiet. The device transitions to receive mode when a valid modulated signal is detected on the RXIN line or the device transitions to transmit mode when TXIN goes low. The device stays in either receive or transmit mode until DIR time-out (nominal 16 bit times) after the last activity on RXOUT or TXIN.

When in receive mode:

- RXOUT responds to all valid modulated signals on RXIN, whether from the local transmitter, a remote transmitter, or long noise burst.
- TXOUT responds to TXIN, generating 2.176-MHz signals on TXOUT when TXIN is low, and TXOUT is quiet when TXIN is high. (In normal operation, TXIN is expected to remain high when the device is in receive mode.)
- The device stays in receive mode until 16 bit times after the last rising edge on RXOUT, caused by valid modulated signal on the RXIN line.

When in transmit mode:

- RXOUT stays high, regardless of the input signal on RXIN.
- TXOUT responds to TXIN, generating 2.176-MHz signals on TXOUT when TXIN is low, and TXOUT is quiet when TXIN is high.
- The device stays in transmit mode until 16 bit times after TXIN goes high.

Table 1 shows the driver functions. Table 2 shows the receiver functions. Figure 22 shows the transitions between each state.

Table 1. Driver Function Table

TXIN(1)	[DIRSET1, DIRSET2]	TXOUT	COMMENT
H	[L,L], [L,H] or [H,L]	< 1 mV_{PP} at 2.176 MHz	Driver not active
L		V_{OPP} at 2.176 MHz	Driver active
X	[H,H]	< 1 mV_{PP} at 2.176 MHz	Standby mode

(1) H = High, L = Low, X = Indeterminate

Table 2. Receiver and DIR Function Table

RXIN(1)	RXOUT	DIR	COMMENT (see Figure 22)
IDLE mode (not transmitting or receiving)			
< V_{IT} at 2.176 MHz for longer than DIR time-out	H	L	No outgoing or incoming signal
RECEIVE mode (not already transmitting)			
< V_{IT} at 2.176 MHz for less than $t_{DIR\ time\text{-}out}$	H	H	Incoming 1 bit, DIR stays HIGH for DIR time-out
> V_{IT} at 2.176 MHz for longer than $t_{noise\ filter}$	L	H	Incoming 0 bit, DIR output is HIGH
TRANSMIT mode (not already receiving)			
X	H	L	Outgoing message, DIR stays LOW for DIR time-out

(1) H = High, L = Low, X = Indeterminate

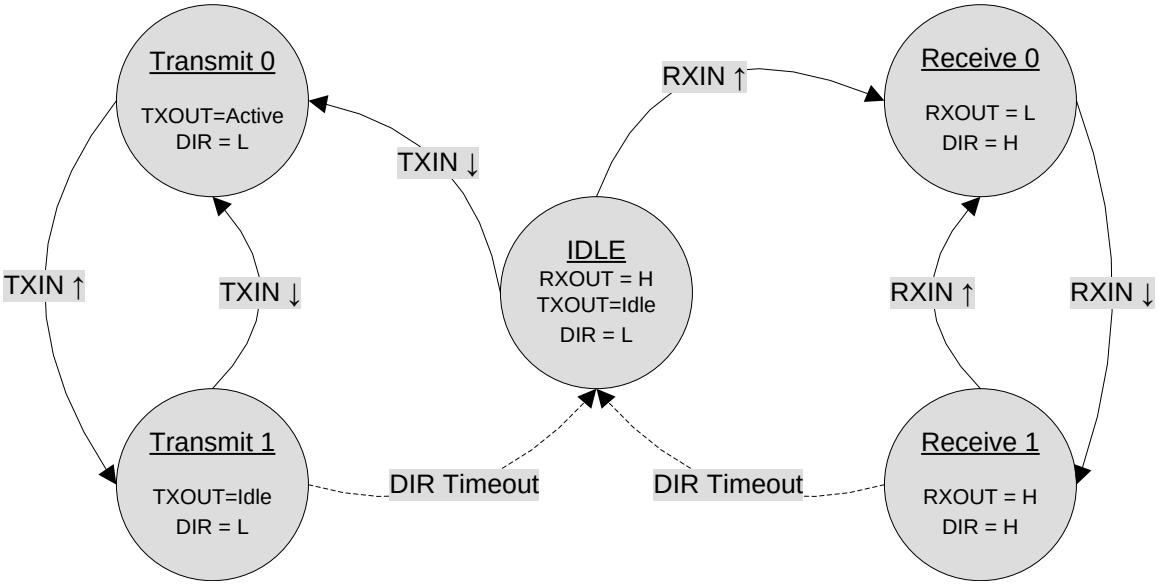


Figure 22. State Transition Diagram

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

10.1.1 Driver Amplitude Adjust

The SN65HVD63 device can provide up to 2.5 V of peak-to-peak output signal at the TXOUT pin to compensate for potential loss within the external filter, cable, connections, and termination. External resistors are used to set the amplitude of the modulated driver output signal. Resistors connected across RES and BIAS set the output amplitude. The maximum peak-to-peak voltage at TXOUT is 2.5 V, corresponding to 6 dBm on the coaxial cable. The TXOUT voltage level can be adjusted by choice of resistors to set the voltage at the RES pin. according to the following equation:

$$VTXOUT\ (V_{PP}) = (2.5\ V_{PP} \times V_{RES}\ (V)) / 1.5\ V\ V_{RES}\ (V) = 1.5\ V \times R2 / (R1 + R2)\ V_{TXOUT}\ (V_{PP}) = 2.5\ V_{PP} \times R2 / (R1 + R2) \quad (1)$$

The voltage at the RES pin should be from 0.7 V to 1.5 V. Connect RES directly to the BIAS (R1 = 0 Ω) for maximum output level of 2.5 VPP. This gives a minimum voltage level at TXOUT of 1.2 VPP, corresponding to about 0 dBm at the coaxial cable. A 1-µF capacitor should be connected between the BIAS pin and GND. To obtain a nominal power level of 3 dBm at the feeder cable as the AISG standard requires, use R1 = 4.1 kΩ and R2 = 10 kΩ that provide 1.78 V_{PP} at TXOUT.

10.1.2 Direction Control

In many applications the mast-top modem that receives data from the base distributes the received data through an RS-485 network to several mast-top devices. When the mast-top modem receives the first logic 0 bit (active modulated signal) it takes control of the mast-top RS-485 network by asserting the direction control signal. The duration of the direction control assertion should be optimized to pass a complete message of length B bits at the known signaling rate ($1/t_{BIT}$) before relinquishing control of the mast-top RS-485 network. For example, if the messages are 10 bits in length (B=10) and the signaling rate is 9600 bits per second (t_{BIT} = 0.104 ms) then a positive pulse of duration 1.7 ms is sufficient (with margin to allow for network propagation delays) to enable the mast-top RS-485 drivers to distribute each received message. Figure 23 shows the assertion of direction control.

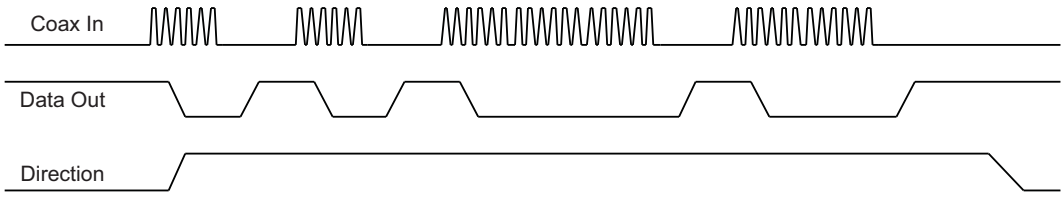


Figure 23. Assertion of Direction Control

10.1.3 Direction Control Time Constant

The time constant for the direction control function can be set by the control mode pins, DIRSET1 and DIRSET2. These pins should be set to correspond to the desired data rate. With no external connections to the control mode pins, the internal time constant is set to the maximum value, corresponding to the minimum data rate.

Application Information (continued)

10.1.4 Conversion Between dBm and Peak-to-Peak Voltage

$$dBm = 20 \times LOG10\ [Volts\text{-}pp / SQRT(0.008 \times Z_o)] = 20 \times LOG10\ [VPP / 0.63] \text{ for } Z_o = 50\ \Omega \quad (2)$$

$$VPP = SQRT(0.008 \times Z_o) \times 10^{(dBm/20)} = 0.63 \times 10^{(dBm/20)} \text{ for } Z_o = 50\ \Omega \quad (3)$$

Table 3 shows conversions between dBm and peak-to-peak voltage with a 50-Ω load, for various levels of interest including reference levels from the *3GPP TS 25.461 Technical Specification*.

Table 3. Conversions Between dBM and Peak-to-Peak Voltage

SIGNAL ON COAX	dBm	V_{PP}
Maximum Driver ON Signal	5	1.12
Nominal Driver ON Signal	3	0.89
Minimum Driver ON Signal	1	0.71
AISG Maximum Receiver Threshold	–12	0.16
Nominal Receiver Threshold	–15	0.11
Minimum Receiver Threshold	–18	0.08
Maximum Driver OFF Signal	–40	0.006

10.2 Typical Application

The AISG On-Off Keying (OOK) interface allows for command, control, and diagnostic information to be communicated between a base station and the corresponding tower-mounted antennae. Figure 24 shows a typical application.

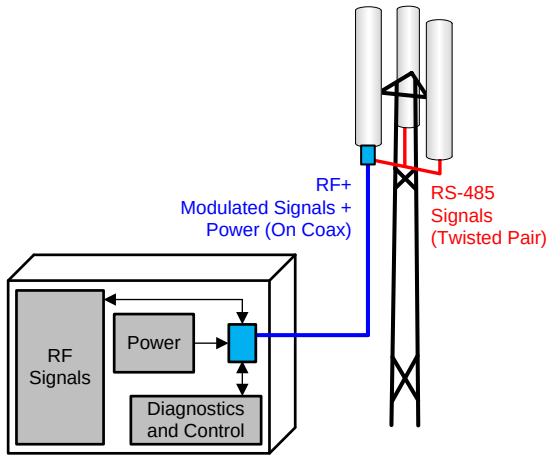


Figure 24. Typical AISG Application

10.2.1 Design Requirements

An AISG transceiver is used to convert between digital logic-level signals and RF signals. The AISG standard requires an RF carrier frequency of 2.176 MHz with 100-ppm accuracy. The output signal of the driver, when active, should be from 1 dBm to 5 dBm. The receiver must be designed such that the input threshold is from –18 dBm to –12 dBm.

10.2.2 Detailed Design Procedure

To ensure accuracy of the carrier frequency, an input reference frequency equal to four times the carrier (that is, 8.704 MHz) should be connected to the XTAL1 or XTAL2 inputs. This signal can come from a crystal (connected between XTAL1 and XTAL2) or from a PLL/clock generator circuit (connected to XTAL1 with XTAL2 grounded). The frequency accuracy must be within 100 ppm.

Typical Application (continued)

The driver output power level of the SN65HVD63 device can be adjusted through use of the RES pin. To align with AISG requirements, a nominal power level of 3 dBm should be configured by connecting a 4.1-kΩ resistor between RES and BIAS and a 10-kΩ resistor between RES and GND. Figure 25 shows an example schematic.

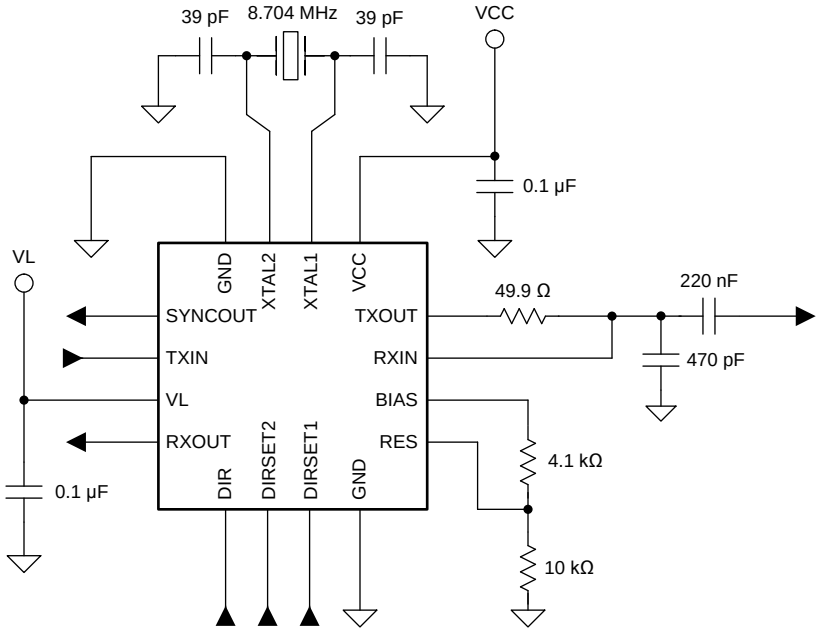


Figure 25. SN65HVD63 Schematic

10.2.3 Application Curve

Figure 26 shows the application curve for the SN65HVD63 device.

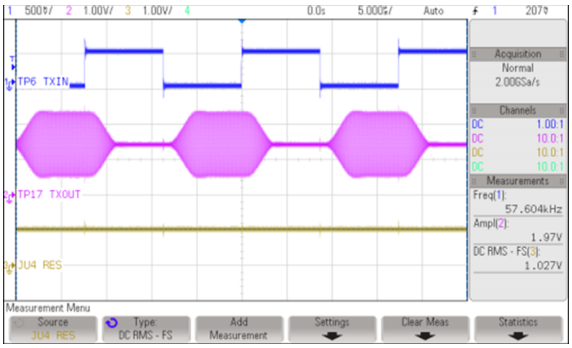


Figure 26. SN65HVD63 Application Curve

11 Power Supply Recommendations

The SN65HVD63 device has two power supply pins: V_{CC}, which provides power to the analog circuitry, and VL, which is a logic supply. V_{CC} should be operated from 3 V to 5.5 V, while VL can range from 1.6 V to 5.5 V to interface to different logic levels. Power supply decoupling capacitances of at least 0.1 µF should be placed as close as possible to each power supply pin.

12 Layout

12.1 Layout Guidelines

Best practices for high-speed PCB design should be observed because the coax interface to the SN65HVD63 device operates at RF. The RF signaling traces should have a controlled characteristic impedance that is well-matched to the coaxial line. A continuous reference plane should be used to avoid impedance discontinuities. Power and ground distribution should be done through planes rather than traces to decrease series resistance and increase the effective decoupling capacitance on the power rails.

12.2 Layout Example

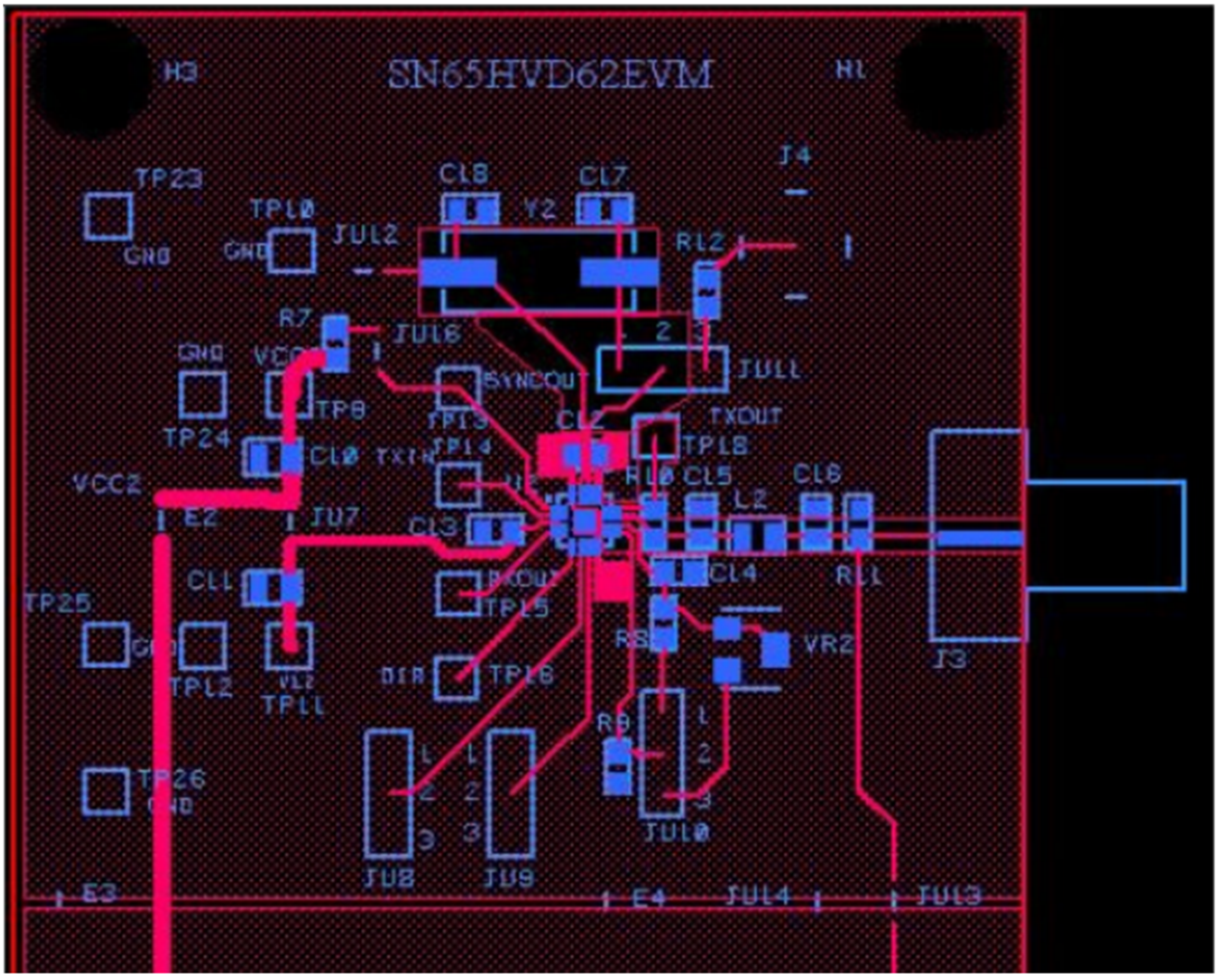


Figure 27. SN65HVD63 Layout

13 Device and Documentation Support

13.1 Related Documentation

Control Interface for Antenna Line Devices, Antenna Interface Standards Group, Standard No. AISG v2.0

13.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.3 Trademarks

E2E is a trademark of Texas Instruments.
AISG is a registered trademark of Antenna Interface Standards Group, Ltd.
All other trademarks are the property of their respective owners.

13.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65HVD63RGTR	ACTIVE	QFN	RGT	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 105	HVD63	Samples
SN65HVD63RGTT	ACTIVE	QFN	RGT	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 105	HVD63	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

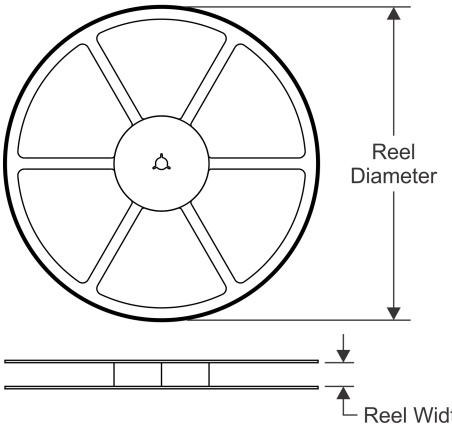
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

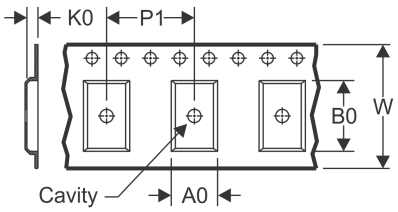
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

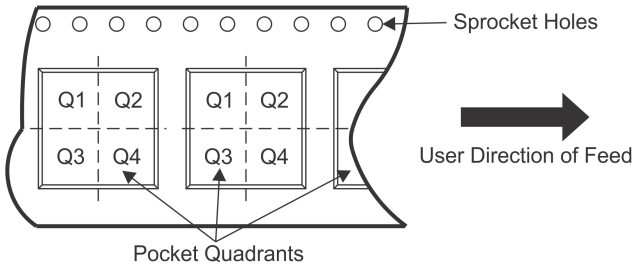


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

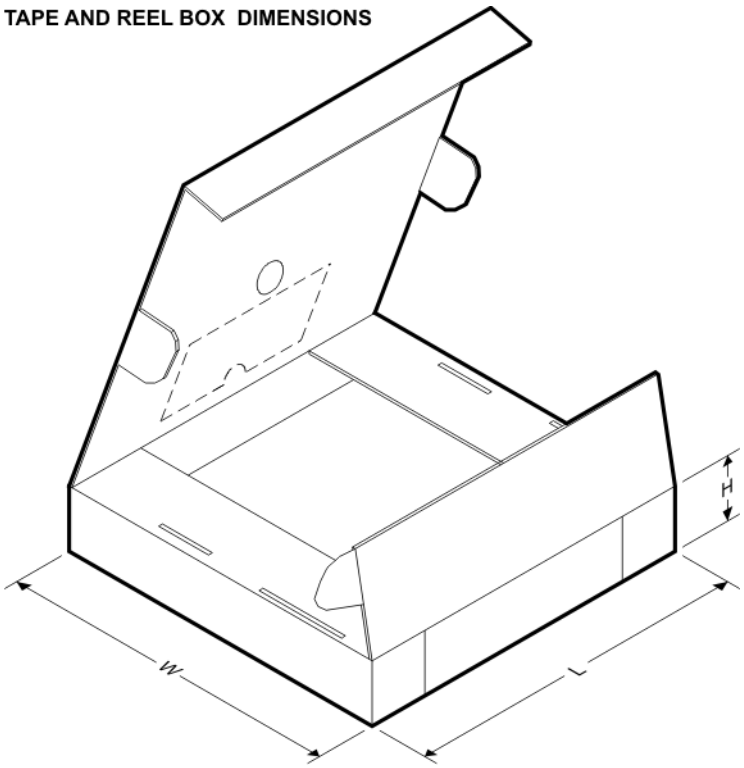
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65HVD63RGTR	QFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
SN65HVD63RGTT	QFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS

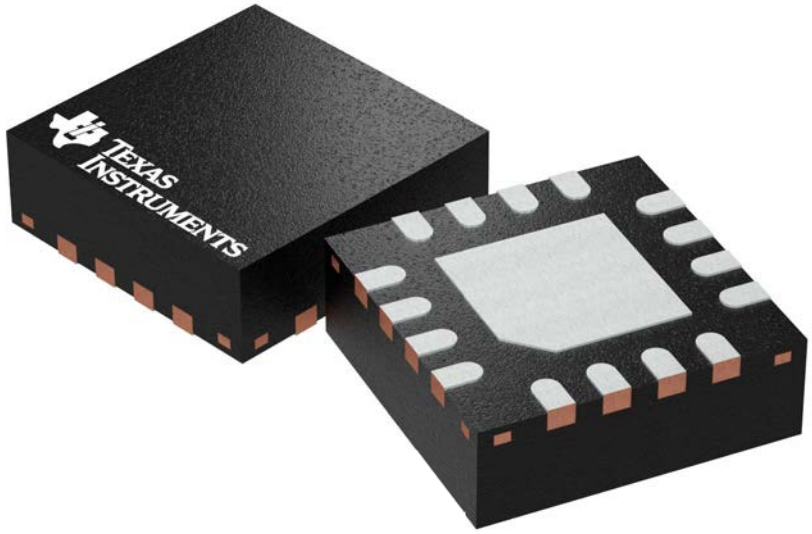


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65HVD63RGTR	QFN	RGT	16	3000	367.0	367.0	35.0
SN65HVD63RGTT	QFN	RGT	16	250	210.0	185.0	35.0

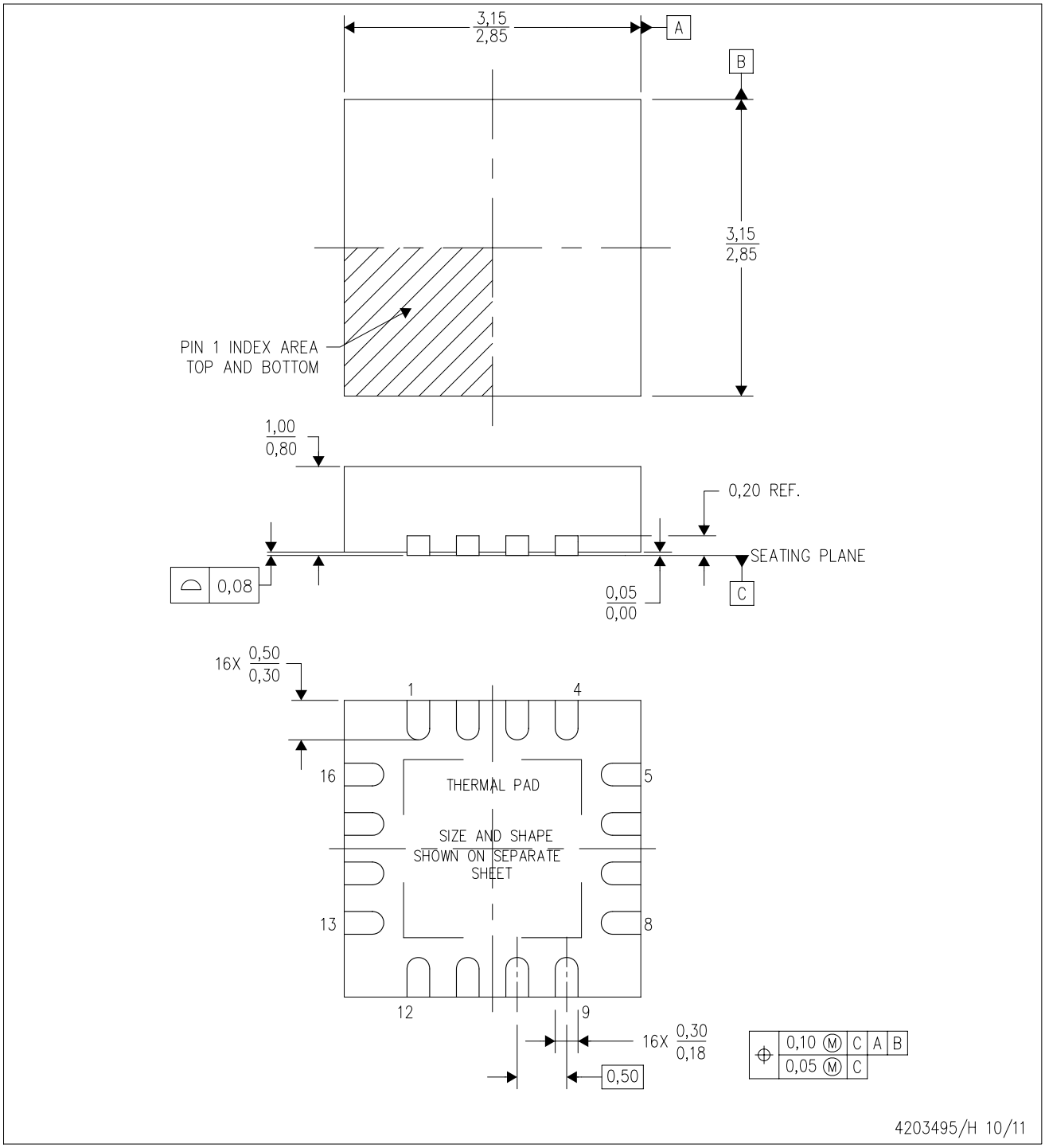
RGT 16 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

RGT (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

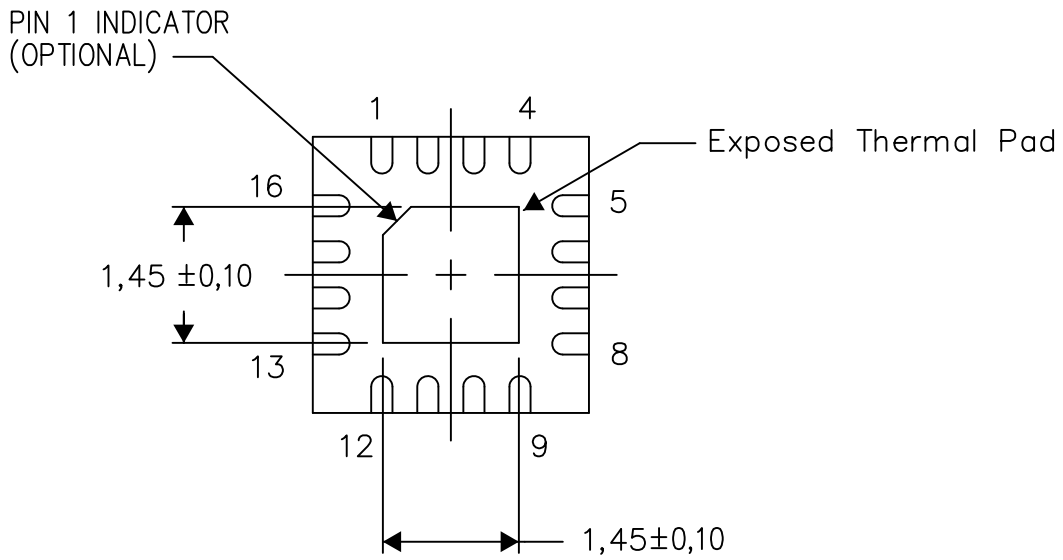
RGT (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4206349–2/Z 08/15

NOTE: All linear dimensions are in millimeters

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