# 20-BIT FET BUS SWITCH
## 2.5-V/3.3-V LOW-VOLTAGE BUS SWITCH WITH 5-V-TOLERANT LEVEL SHIFTER
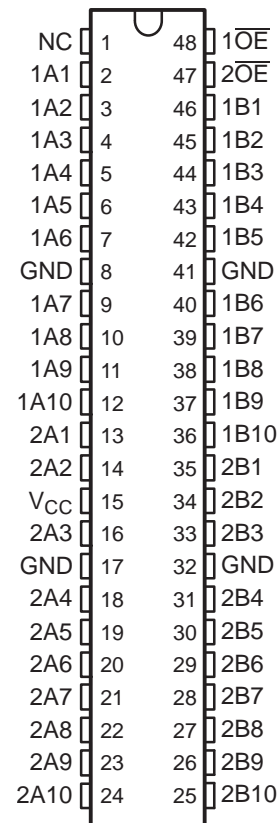
**Check for Samples: SN74CB3T16210**

## FEATURES

- **Member of the Texas Instruments Widebus™ Family**
- **Output Voltage Translation Tracks $V_{CC}$**
- **Supports Mixed-Mode Signal Operation on All Data I/O Ports**
  - **5-V Input Down to 3.3-V Output Level Shift With 3.3-V $V_{CC}$**
  - **5-V/3.3-V Input Down to 2.5-V Output Level Shift With 2.5-V $V_{CC}$**
- **5-V-Tolerant I/Os With Device Powered Up or Powered Down**
- **Bidirectional Data Flow With Near-Zero Propagation Delay**
- **Low ON-State Resistance ($r_{on}$) Characteristics ($r_{on}$ = 5 Ω Typ)**
- **Low Input/Output Capacitance Minimizes Loading ($C_{io(OFF)}$ = 5 pF Typ)**
- **Data and Control Inputs Provide Undershoot Clamp Diodes**
- **Low Power Consumption ($I_{CC}$ = 40 µA Max)**
- **$V_{CC}$ Operating Range From 2.3 V to 3.6 V**
- **Data I/Os Support 0- to 5-V Signaling Levels (0.8 V, 1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V, 5 V)**
- **Control Inputs Can Be Driven by TTL or 5-V/3.3-V CMOS Outputs**
- **$I_{off}$ Supports Partial-Power-Down Mode Operation**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Performance Tested Per JESD 22**
  - **2000-V Human-Body Model (A114-B, Class II)**
  - **1000-V Charged-Device Model (C101)**

- **Supports Digital Applications: Level Translation, PCI Interface, USB Interface, Memory Interleaving, and Bus Isolation**
- **Ideal for Low-Power Portable Equipment**

**DGG OR DGV PACKAGE**
**(TOP VIEW)**

| | | | |
|---|---|---|---|
| NC | 1 | 48 | 1$\overline{OE}$ |
| 1A1 | 2 | 47 | 2$\overline{OE}$ |
| 1A2 | 3 | 46 | 1B1 |
| 1A3 | 4 | 45 | 1B2 |
| 1A4 | 5 | 44 | 1B3 |
| 1A5 | 6 | 43 | 1B4 |
| 1A6 | 7 | 42 | 1B5 |
| GND | 8 | 41 | GND |
| 1A7 | 9 | 40 | 1B6 |
| 1A8 | 10 | 39 | 1B7 |
| 1A9 | 11 | 38 | 1B8 |
| 1A10 | 12 | 37 | 1B9 |
| 2A1 | 13 | 36 | 1B10 |
| 2A2 | 14 | 35 | 2B1 |
| $V_{CC}$ | 15 | 34 | 2B2 |
| 2A3 | 16 | 33 | 2B3 |
| GND | 17 | 32 | GND |
| 2A4 | 18 | 31 | 2B4 |
| 2A5 | 19 | 30 | 2B5 |
| 2A6 | 20 | 29 | 2B6 |
| 2A7 | 21 | 28 | 2B7 |
| 2A8 | 22 | 27 | 2B8 |
| 2A9 | 23 | 26 | 2B9 |
| 2A10 | 24 | 25 | 2B10 |

NC - No internal connection

## DESCRIPTION/ORDERING INFORMATION

The SN74CB3T16210 is a high-speed TTL-compatible FET bus switch with low ON-state resistance ($r_{on}$), allowing for minimal propagation delay. The device fully supports mixed-mode signal operation on all data I/O ports by providing voltage translation that tracks $V_{CC}$. The SN74CB3T16210 supports systems using 5-V TTL, 3.3-V LVTTL, and 2.5-V CMOS switching standards, as well as user-defined switching levels (see Figure 1).

⚠ Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Widebus is a trademark of Texas Instruments.

## DESCRIPTION/ORDERING INFORMATION (CONTINUED)

The SN74CB3T16210 is organized as two 10-bit bus switches with separate ouput-enable (1$\overline{OE}$, 2$\overline{OE}$) inputs. It can be used as two 10-bit bus switches or as one 20-bit bus switch. When $\overline{OE}$ is low, the associated 10-bit bus switch is ON, and the A port is connected to the B port, allowing bidirectional data flow between ports. When $\overline{OE}$ is high, the associated 10-bit bus switch is OFF, and a high-impedance state exists between the A and B ports.

This device is fully specified for partial-power-down applications using $I_{off}$. The $I_{off}$ feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to $V_{CC}$ through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

### ORDERING INFORMATION

| $T_A$ | PACKAGE[1] | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---|---|---|---|---|
| −40°C to 85°C | TSSOP − DGG | Tape and reel | SN74CB3T16210DGGR | CB3T16210 |
| | TVSOP − DGV | Tape and reel | SN74CB3T16210DGVR | KR210 |

(1)  Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

### FUNCTION TABLE
### (EACH 10-BIT BUS SWITCH)

| INPUT $\overline{OE}$ | INPUT/OUTPUT A | FUNCTION |
|---|---|---|
| L | B | A port = B port |
| H | Z | Disconnect |



**Input Voltages**          **Output Voltages**
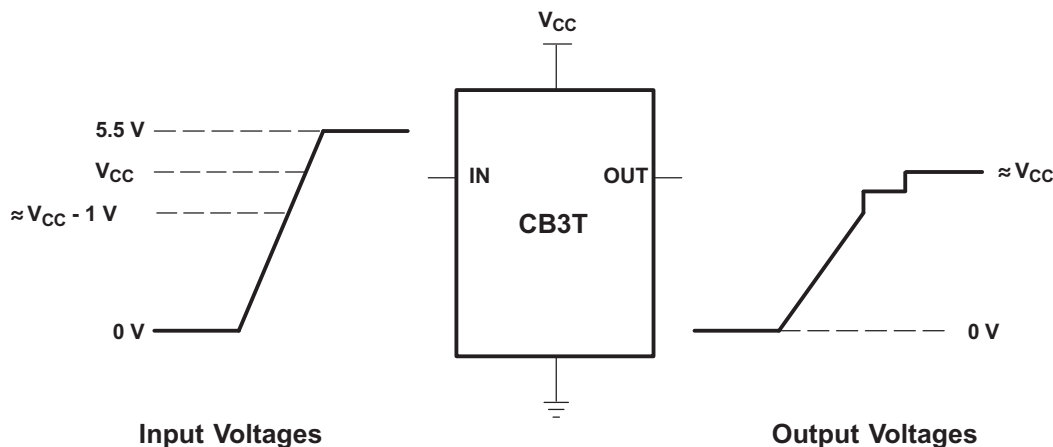
If the input high voltage ($V_{IH}$) level is greater than or equal to $V_{CC}$ + 1 V, and less than or equal to 5.5 V, the output high voltage ($V_{OH}$) level will be equal to approximately the $V_{CC}$ voltage level.

**Figure 1.  Typical DC Voltage Translation Characteristics**

**GQL PACKAGE**
**(TOP VIEW)**
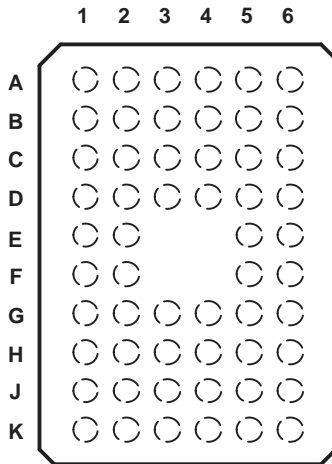
## TERMINAL ASSIGNMENTS[1]

|   | 1 | 2 | 3 | 4 | 5 | 6 |
|---|---|---|---|---|---|---|
| **A** | 1A2 | 1A1 | NC | 1$\overline{\text{OE}}$ | 2$\overline{\text{OE}}$ | 1B1 |
| **B** | 1A5 | 1A4 | 1A3 | 1B2 | 1B3 | 1B4 |
| **C** | NC | GND | 1A6 | 1B5 | 1B6 | NC |
| **D** | 1A8 | NC | 1A7 | NC | 1B7 | 1B8 |
| **E** | 1A10 | 1A9 | | | 1B9 | 1B10 |
| **F** | 2A1 | 2A2 | | | 2B2 | 2B1 |
| **G** | $V_{CC}$ | GND | 2A3 | GND | 2B4 | 2B3 |
| **H** | NC | NC | 2A4 | 2B5 | NC | NC |
| **J** | 2A5 | 2A6 | 2A7 | 2B7 | 2B6 | 2B5 |
| **K** | 2A8 | 2A9 | 2A10 | 2B10 | 2B9 | 2B8 |

(1)   NC - No internal connection

## LOGIC DIAGRAM (POSITIVE LOGIC)

# SN74CB3T16210
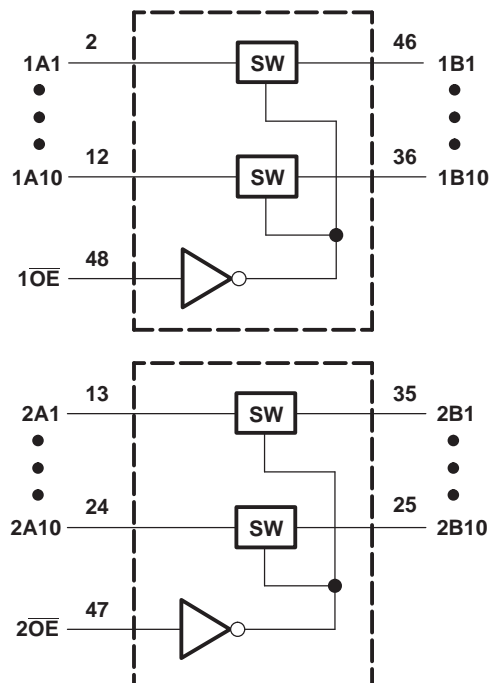
## SIMPLIFIED SCHEMATIC, EACH FET SWITCH (SW)
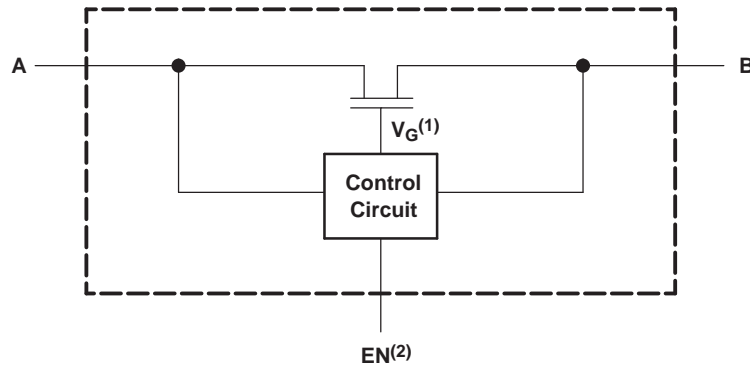


(1) Gate voltage ($V_G$) is equal to approximately $V_{CC} + V_T$ when the switch is ON and $V_I > V_{CC} + V_T$.
(2) EN is the internal enable signal applied to the switch.

## Absolute Maximum Ratings[1]

over operating free-air temperature range (unless otherwise noted)

|  |  |  | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage range |  | −0.5 | 7 | V |
| $V_{IN}$ | Control input voltage range[2][3] |  | −0.5 | 7 | V |
| $V_{I/O}$ | Switch I/O voltage range[2][3][4] |  | −0.5 | 7 | V |
| $I_{IK}$ | Control input clamp current | $V_{IN} < 0$ |  | −50 | mA |
| $I_{I/OK}$ | I/O port clamp current | $V_{I/O} < 0$ |  | −50 | mA |
| $I_{IO}$ | ON-state switch current[5] |  |  | ±128 | mA |
|  | Continuous current through $V_{CC}$ or GND |  |  | ±100 | mA |
| $\theta_{JA}$ | Package thermal impedance[6] | DGG package |  | 70 | °C/W |
|  |  | DGV package |  | 58 |  |
| $T_{stg}$ | Storage temperature range |  | −65 | 150 | °C |

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground unless otherwise specified.
(3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(4) $V_I$ and $V_O$ are used to denote specific conditions for $V_{I/O}$.
(5) $I_I$ and $I_O$ are used to denote specific conditions for $I_{I/O}$.
(6) The package thermal impedance is calculated in accordance with JESD 51-7.

Product Folder Link(s): *SN74CB3T16210*

## Recommended Operating Conditions[1]

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 2.3 | 3.6 | V |
| $V_{IH}$ | High-level control input voltage | $V_{CC}$ = 2.3 V to 2.7 V | 1.7 | 5.5 | V |
| | | $V_{CC}$ = 2.7 V to 3.6 V | 2 | 5.5 | |
| $V_{IL}$ | Low-level control input voltage | $V_{CC}$ = 2.3 V to 2.7 V | 0 | 0.7 | V |
| | | $V_{CC}$ = 2.7 V to 3.6 V | 0 | 0.8 | |
| $V_{I/O}$ | Data input/output voltage | | 0 | 5.5 | V |
| $T_A$ | Operating free-air temperature | | −40 | 85 | °C |

(1)   All unused control inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## Electrical Characteristics[1]

| PARAMETER | | TEST CONDITIONS | $T_A$ = −40°C TO 85°C | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MIN | TYP[2] | MAX | |
| $V_{IK}$ | | $V_{CC}$ = 3 V, $I_I$ = −18 mA | | | −1.2 | V |
| $V_{OH}$ | | See Figure 3 and Figure 4 | | | | |
| $I_{IN}$ | Control inputs | $V_{CC}$ = 3.6 V, $V_{IN}$ = 3.6 V to 5.5 V or GND | | | ±10 | µA |
| $I_I$ | | $V_{CC}$ = 3.6 V, Switch ON, $V_{IN}$ = $V_{CC}$ or GND | $V_I$ = $V_{CC}$ − 0.7 V to 5.5 V | | | ±20 | µA |
| | | | $V_I$ = 0.7 V to $V_{CC}$ − 0.7 V | | | −40 | |
| | | | $V_I$ = 0 to 0.7 V | | | ±5 | |
| $I_{OZ}$ [3] | | $V_{CC}$ = 3.6 V, $V_O$ = 0 to 5.5 V, $V_I$ = 0, Switch OFF, $V_{IN}$ = $V_{CC}$ or GND | | | ±10 | µA |
| $I_{off}$ | | $V_{CC}$ = 0, $V_O$ = 0 to 5.5 V, $V_I$ = 0, | | | 10 | µA |
| $I_{CC}$ | | $V_{CC}$ = 3.6 V, $I_{I/O}$ = 0, Switch ON or OFF, $V_{IN}$ = $V_{CC}$ or GND | $V_I$ = $V_{CC}$ or GND | | | 40 | µA |
| | | | $V_I$ = 5.5 V | | | 40 | |
| $\Delta I_{CC}$ [4] | Control inputs | $V_{CC}$ = 3 V to 3.6 V, One input at $V_{CC}$ − 0.6 V, Other inputs at $V_{CC}$ or GND | | | 300 | µA |
| $C_{in}$ | Control inputs | $V_{CC}$ = 3.3 V, $V_{IN}$ = $V_{CC}$ or GND | | 4 | | pF |
| $C_{io(OFF)}$ | | $V_{CC}$ = 3.3 V, $V_{I/O}$ = 5.5 V, 3.3 V, or GND, Switch OFF, $V_{IN}$ = $V_{CC}$ or GND | | 5 | | pF |
| $C_{io(ON)}$ | | $V_{CC}$ = 3.3 V, Switch ON, $V_{IN}$ = $V_{CC}$ or GND | $V_{I/O}$ = 5.5 V or 3.3 V | | 5 | | pF |
| | | | $V_{I/O}$ = GND | | 13 | | |
| $r_{on}$ [5] | | $V_{CC}$ = 2.3 V, TYP at $V_{CC}$ = 2.5 V, $V_I$ = 0 | $I_O$ = 24 mA | | 5 | 9.5 | Ω |
| | | | $I_O$ = 16 mA | | 5 | 9.5 | |
| | | $V_{CC}$ = 3 V, $V_I$ = 0 | $I_O$ = 64 mA | | 5 | 8.5 | |
| | | | $I_O$ = 32 mA | | 5 | 8.5 | |

(1)   $V_{IN}$ and $I_{IN}$ refer to control inputs. $V_I$, $V_O$, $I_I$, and $I_O$ refer to data pins.
(2)   All typical values are at $V_{CC}$ = 3.3 V (unless otherwise noted), $T_A$ = 25°C.
(3)   For I/O ports, the parameter $I_{OZ}$ includes the input leakage current.
(4)   This is the increase in supply current for each input that is at the specified TTL voltage level, rather than $V_{CC}$ or GND.
(5)   Measured by the voltage drop between A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

## Switching Characteristics
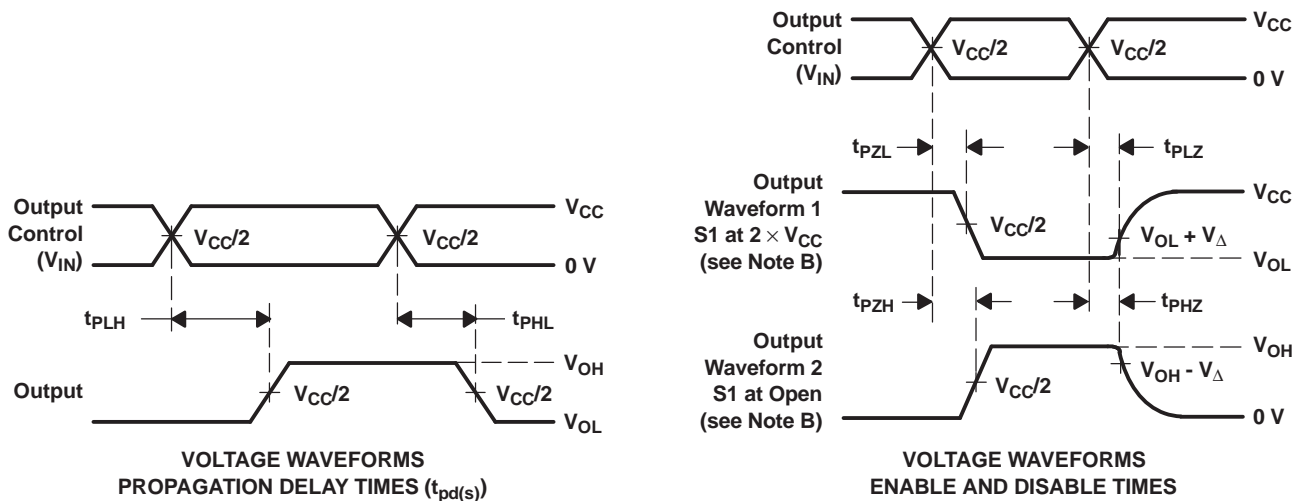
for $V_{CC}$ = 2.5 V ± 0.2 V (see Figure 2)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 2.5 V ± 0.2 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $t_{pd}$ [(1)] | A or B | B or A | | 0.15 | | 0.25 | ns |
| $t_{en}$ | $\overline{OE}$ | A or B | 1 | 12 | 1 | 10 | ns |
| $t_{dis}$ | $\overline{OE}$ | A or B | 1 | 7.5 | 1 | 8.5 | ns |

(1)  The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

Product Folder Link(s): *SN74CB3T16210*

![Texas Instruments logo]

## PARAMETER MEASUREMENT INFORMATION
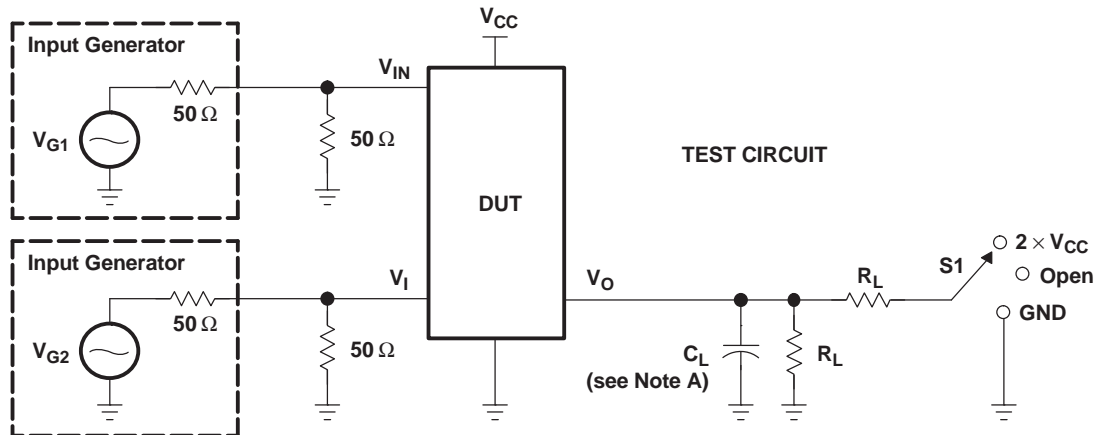


| TEST | V$_{CC}$ | S1 | R$_L$ | V$_I$ | C$_L$ | V$_{\Delta}$ |
|------|------|------|------|------|------|------|
| t$_{pd(s)}$ | 2.5 V ± 0.2 V | Open | 500 Ω | 3.6 V or GND | 30 pF | |
| | 3.3 V ± 0.3 V | Open | 500 Ω | 5.5 V or GND | 50 pF | |
| t$_{PLZ}$/t$_{PZL}$ | 2.5 V ± 0.2 V | 2 × V$_{CC}$ | 500 Ω | GND | 30 pF | 0.15 V |
| | 3.3 V ± 0.3 V | 2 × V$_{CC}$ | 500 Ω | GND | 50 pF | 0.3 V |
| t$_{PHZ}$/t$_{PZH}$ | 2.5 V ± 0.2 V | Open | 500 Ω | 3.6 V | 30 pF | 0.15 V |
| | 3.3 V ± 0.3 V | Open | 500 Ω | 5.5 V | 50 pF | 0.3 V |



**VOLTAGE WAVEFORMS**
**PROPAGATION DELAY TIMES (t$_{pd(s)}$)**



**VOLTAGE WAVEFORMS**
**ENABLE AND DISABLE TIMES**

NOTES:  A.  C$_L$ includes probe and jig capacitance.
B.  Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
   Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C.  All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z$_O$ = 50 Ω, t$_r$ ≤ 2.5 ns, t$_f$ ≤ 2.5 ns.
D.  The outputs are measured one at a time, with one transition per measurement.
E.  t$_{PLZ}$ and t$_{PHZ}$ are the same as t$_{dis}$.
F.  t$_{PZL}$ and t$_{PZH}$ are the same as t$_{en}$.
G.  t$_{PLH}$ and t$_{PHL}$ are the same as t$_{pd(s)}$. The tpd propagation delay is the calculated RC time constant of the typical ON-state resistance
   of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
H.  All parameters and waveforms are not applicable to all devices.

**Figure 2.  Test Circuit and Voltage Waveforms**

## TYPICAL CHARACTERISTICS
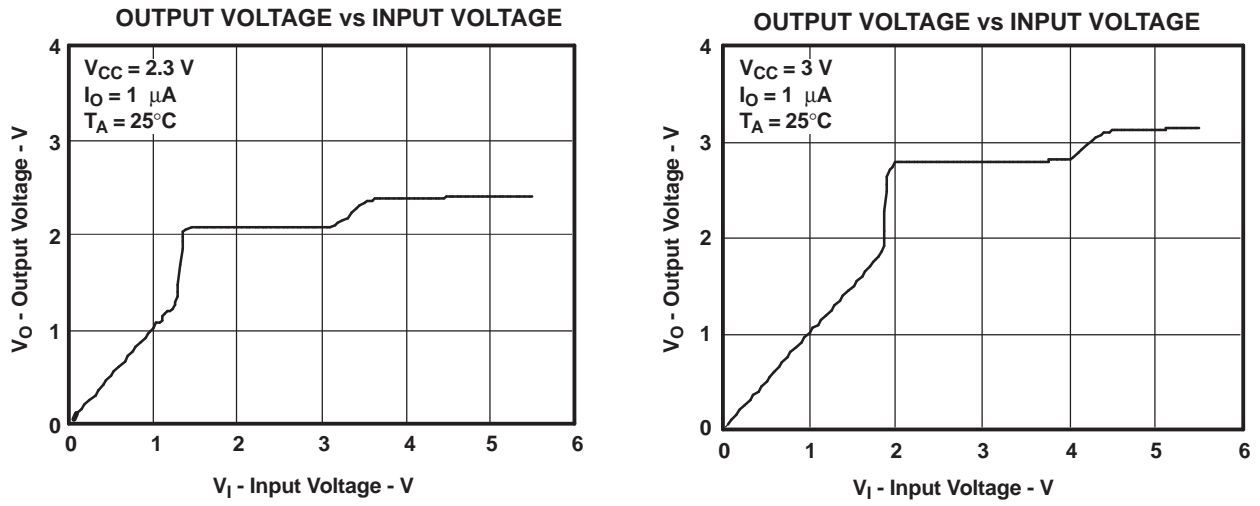


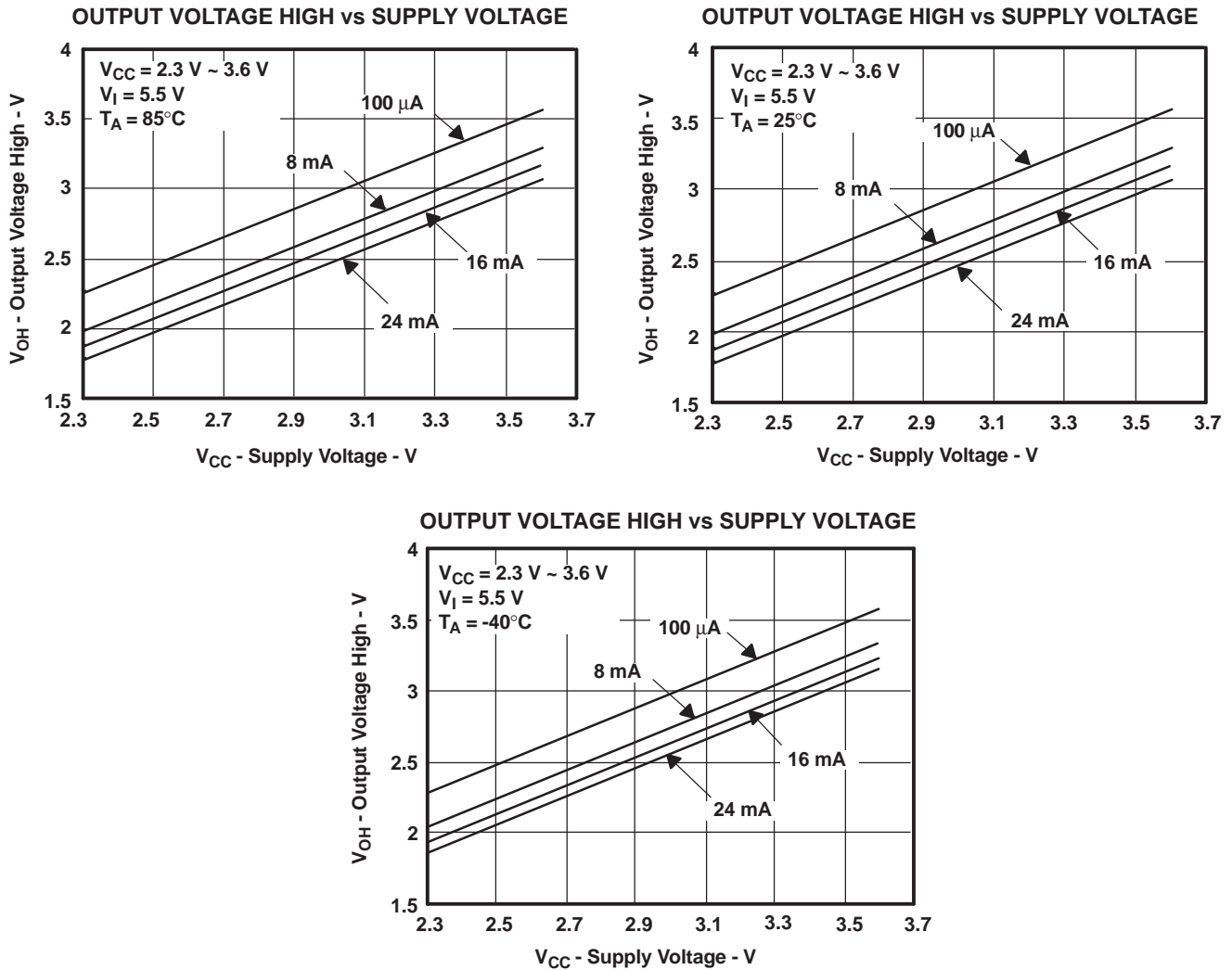**Figure 3.  Data Output Voltage vs Data Input Voltage**

Product Folder Link(s): *SN74CB3T16210*

**TEXAS INSTRUMENTS**

## TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE HIGH vs SUPPLY VOLTAGE



OUTPUT VOLTAGE HIGH vs SUPPLY VOLTAGE



OUTPUT VOLTAGE HIGH vs SUPPLY VOLTAGE



**Figure 4.  $V_{OH}$ Values**

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# REVISION HISTORY

**Changes from Revision A (March 2005) to Revision B**          **Page**

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Product Folder Link(s): *SN74CB3T16210*

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 74CB3T16210DGGRG4 | ACTIVE | TSSOP | DGG | 48 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CB3T16210 | Samples |
| SN74CB3T16210DGG | PREVIEW | TSSOP | DGG | 48 | | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CB3T16210 | |
| SN74CB3T16210DGGR | ACTIVE | TSSOP | DGG | 48 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CB3T16210 | Samples |
| SN74CB3T16210DGVR | ACTIVE | TVSOP | DGV | 48 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | KR210 | Samples |
| SN74CB3T16210DL | PREVIEW | SSOP | DL | 48 | 25 | TBD | Call TI | Call TI | -40 to 85 | | |
| SN74CB3T16210DLR | PREVIEW | SSOP | DL | 48 | 1000 | TBD | Call TI | Call TI | -40 to 85 | | |

**(1)** The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

**(2)** Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

**(3)** MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**(4)** There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

**(6)** Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF SN74CB3T16210 :**

● Automotive: SN74CB3T16210-Q1

NOTE: Qualified Version Definitions:

   ● Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

# PACKAGE MATERIALS INFORMATION

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

**TAPE DIMENSIONS**

| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74CB3T16210DGGR | TSSOP | DGG | 48 | 2000 | 330.0 | 24.4 | 8.6 | 13.0 | 1.8 | 12.0 | 24.0 | Q1 |
| SN74CB3T16210DGVR | TVSOP | DGV | 48 | 2000 | 330.0 | 16.4 | 7.1 | 10.2 | 1.6 | 12.0 | 16.0 | Q1 |

# PACKAGE MATERIALS INFORMATION

**TAPE AND REEL BOX DIMENSIONS**



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74CB3T16210DGGR | TSSOP | DGG | 48 | 2000 | 367.0 | 367.0 | 45.0 |
| SN74CB3T16210DGVR | TVSOP | DGV | 48 | 2000 | 367.0 | 367.0 | 38.0 |

DL (R−PDSO−G48)                    PLASTIC SMALL−OUTLINE PACKAGE

0.025 (0,635)

$\frac{0.0135\ (0,343)}{0.008\ (0,203)}$

⊕ 0.005 (0,13) Ⓜ

48                                      25

$\frac{0.420\ (10,67)}{0.395\ (10,03)}$

$\frac{0.299\ (7,59)}{0.291\ (7,39)}$

$\frac{0.010\ (0,25)}{0.005\ (0,13)}$

Gage Plane

0.010 (0,25)

0°−8°

$\frac{0.040\ (1,02)}{0.020\ (0,51)}$

1                                      24

$\frac{0.630\ (16,00)}{0.620\ (15,75)}$

0.110 (2,79) MAX              0.008 (0,20) MIN

Seating Plane

△ 0.004 (0,10)

4040048−3/F   05/13
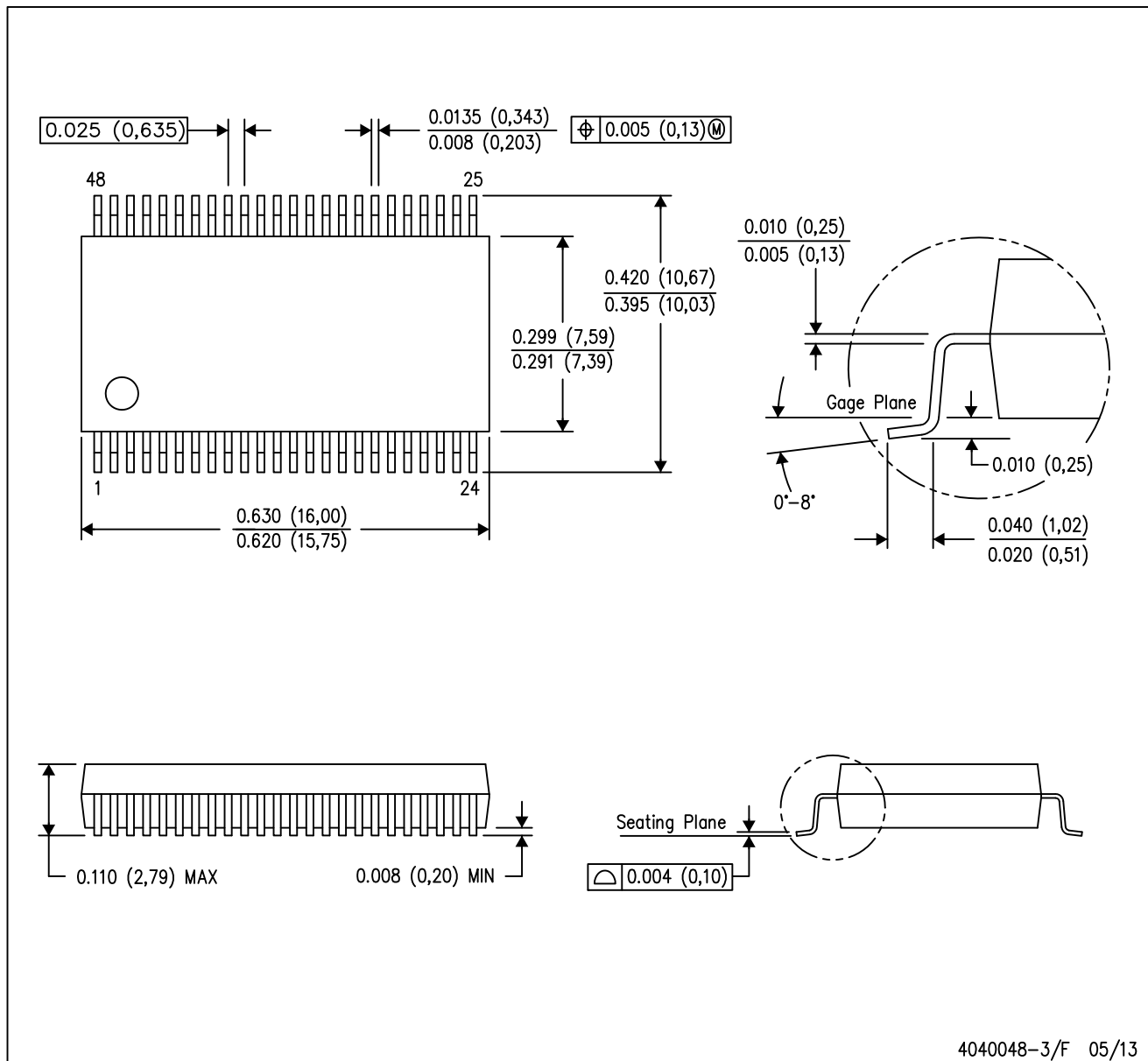
NOTES:   A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
         C.   Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
         D.   Falls within JEDEC MO−118

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# MECHANICAL DATA

MPDS006C – FEBRUARY 1996 – REVISED AUGUST 2000

**DGV (R-PDSO-G\*\*)**　　　　　　　　　　　　　　**PLASTIC SMALL-OUTLINE**

**24 PINS SHOWN**

0,40

0,23
0,13

⊕ | 0,07 Ⓜ

24　　　　　13

4,50
4,30

6,60
6,20

1　　　　12

A

0,16 NOM

Gage Plane

0°–8°

0,25

0,75
0,50

1,20 MAX

0,15
0,05

**Seating Plane**

◠ | 0,08

| PINS \*\*<br>DIM | 14 | 16 | 20 | 24 | 38 | 48 | 56 |
|---|---|---|---|---|---|---|---|
| A MAX | 3,70 | 3,70 | 5,10 | 5,10 | 7,90 | 9,80 | 11,40 |
| A MIN | 3,50 | 3,50 | 4,90 | 4,90 | 7,70 | 9,60 | 11,20 |

4073251/E 08/00

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

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**DGG (R-PDSO-G\*\*)**                                    **PLASTIC SMALL-OUTLINE PACKAGE**

**48 PINS SHOWN**



| PINS \*\* DIM | 48 | 56 | 64 |
|---|---|---|---|
| A  MAX | 12,60 | 14,10 | 17,10 |
| A  MIN | 12,40 | 13,90 | 16,90 |

**4040078 / F 12/97**

NOTES:  A.  All linear dimensions are in millimeters.
        B.  This drawing is subject to change without notice.
        C.  Body dimensions do not include mold protrusion not to exceed 0,15.
        D.  Falls within JEDEC MO-153

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