

## TL06xx Low-Power JFET-Input Operational Amplifiers

### 1 Features

- Very Low Power Consumption
- Typical Supply Current: 200  $\mu$ A (Per Amplifier)
- Wide Common-Mode and Differential Voltage Ranges
- Low Input Bias and Offset Currents
- Common-Mode Input Voltage Range Includes  $V_{CC+}$
- Output Short-Circuit Protection
- High Input Impedance: JFET-Input Stage
- Internal Frequency Compensation
- Latch-Up-Free Operation
- High Slew Rate: 3.5 V/ $\mu$ s Typical
- On Products Compliant to MIL-PRF-38535, All Parameters Are Tested Unless Otherwise Noted. On All Other Products, Production Processing Does Not Necessarily Include Testing of All Parameters.

### 2 Applications

- Tablets
- White goods
- Personal electronics
- Computers

### 3 Description

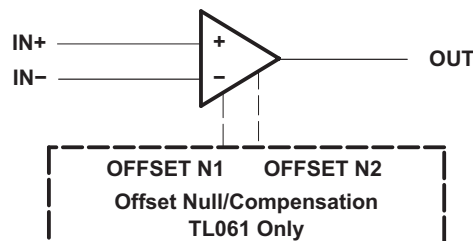
The JFET-input operational amplifiers of the TL06x series are designed as low-power versions of the TL08x series amplifiers. They feature high input impedance, wide bandwidth, high slew rate, and low input offset and input bias currents. The TL06x series features the same terminal assignments as the TL07x and TL08x series.

#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TL06xxD	SOIC (14)	8.65 mm x 3.91 mm
TL06xxJ	CDIP (14)	19.56 mm x 6.92 mm
TL06xxN	PDIP (14)	19.30 mm x 6.35 mm
TL06xxNS	SO (14)	10.30 mm x 5.30 mm
TL06xxPW	TSSOP (14)	5.00 mm x 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

#### Schematic Symbol



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## 4 Revision History

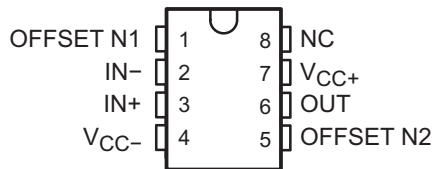
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Revision K (January 2014) to Revision L</b>	<b>Page</b>
• Added <i>Applications</i> .....	<b>1</b>
• Added <i>Pin Configuration and Functions</i> section, <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section .....	<b>1</b>

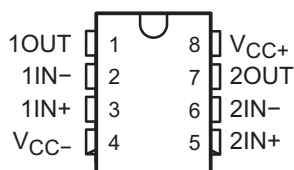
<b>Changes from Revision J (September 2004) to Revision K</b>	<b>Page</b>
• Updated document to new TI data sheet format - no specification changes. ....	<b>1</b>
• Deleted <i>Ordering Information</i> table. ....	<b>1</b>
• Updated <i>Features</i> with Military Disclaimer. ....	<b>1</b>

## 5 Pin Configuration and Functions

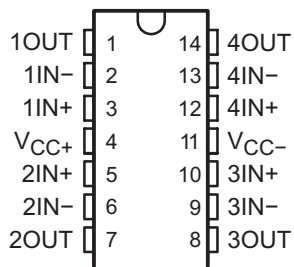
TL061x D, P, and PS Package  
8-Pin SOIC, PDIP, and SO  
Top View



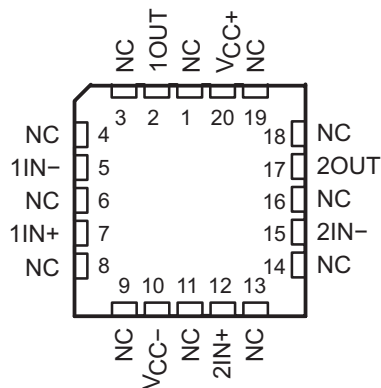
TL062x D, JG, P, PS, and PW Package  
8-Pin SOIC, CDIP, PDIP, SO, and TSSOP  
Top View



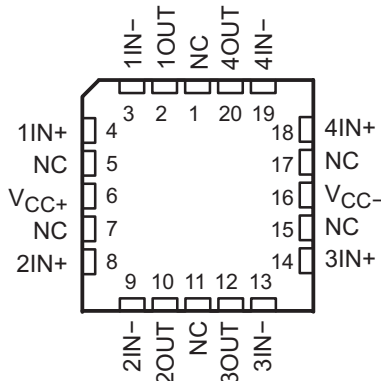
TL064x D, J, N, NS, PW, and W Package  
14-Pin SOIC, CDIP, PDIP, SO, TSSOP and CFP  
Top View



TL062 FK Package  
20-Pin LCCC  
Top View



TL064 FK Package  
20-Pin LCCC  
Top View



### Pin Functions

NAME	PIN					TYPE	DESCRIPTION
	TL061	TL062		TL064			
	D, P, PS	D, JG, P, PS, PW	FK	D, J, N, NS, PW, W	FK		
1IN-	—	2	5	2	3	I	Negative input
1IN+	—	3	7	3	4	I	Positive input
1OUT	—	1	2	1	2	O	Output
2IN-	—	6	15	6	9	I	Negative input
2IN+	—	5	12	5	8	I	Positive input
2OUT	—	7	17	7	10	O	Output
3IN-	—	—	—	9	13	I	Negative input
3IN+	—	—	—	10	14	I	Positive input
3OUT	—	—	—	8	12	O	Output
4IN-	—	—	—	13	19	I	Negative input
4IN+	—	—	—	12	18	I	Positive input
4OUT	—	—	—	14	20	O	Output
IN-	2	—	—	—	—	I	Negative input

Pin Functions (continued)

NAME	PIN					TYPE	DESCRIPTION
	TL061	TL062		TL064			
	D, P, PS	D, JG, P, PS, PW	FK	D, J, N, NS, PW, W	FK		
IN+	3	—	—	—	—	I	Positive input
NC	8	—	1	—	1	—	Do not connect
			3		5		
			4		7		
			6		11		
			8		15		
			9		17		
			11				
			13				
			14				
			16				
18							
19							
OFFSET N1	1	—	—	—	—	—	Input offset adjustment
OFFSET N2	5	—	—	—	—	—	Input offset adjustment
OUT	6	—	—	—	—	O	Output
V <sub>CC-</sub>	4	4	10	11	16	—	Power supply
V <sub>CC+</sub>	7	8	20	4	6	—	Power supply

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC+</sub>	Supply voltage <sup>(2)</sup>		18	V
V <sub>CC-</sub>			-18	
V <sub>ID</sub>	Differential input voltage <sup>(3)</sup>		±30	V
V <sub>I</sub>	Input voltage <sup>(2)(4)</sup>		±15	V
	Duration of output short circuit <sup>(5)</sup>		Unlimited	
T <sub>J</sub>	Operating virtual junction temperature		150	°C
	Case temperature for 60 seconds	FK package	260	°C
	Lead temperature 1.6 mm (1/16 inch) from case for 60 seconds	J, JG, U, or W package	300	°C
	Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds	D, N, NS, P, PS, or PW package	260	°C
T <sub>stg</sub>	Storage temperature	-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values, except differential voltages, are with respect to the midpoint between V<sub>CC+</sub> and V<sub>CC-</sub>.

(3) Differential voltages are at IN+, with respect to IN-.

(4) The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.

(5) The output may be shorted to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

## 6.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	2000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	2000

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT	
V <sub>CC+</sub>	Supply voltage	5	15	V	
V <sub>CC-</sub>	Supply voltage	-5	-15	V	
V <sub>CM</sub>	Common-mode voltage	V <sub>CC-</sub> + 4	V <sub>CC+</sub> - 4	V	
T <sub>A</sub>	Ambient temperature	TL06xM	-55	125	°C
		TL06xQ	-40	125	
		TL06xI	-40	85	
		TL06xC	0	70	

## 6.4 Thermal Information - 8 Pins

THERMAL METRIC <sup>(1)</sup>	TL06xx					UNIT	
	D (SOIC)	P (PDIP)	PS (SO)	PW (TSSOP)	JG (CDIP)		
	8 PINS	8 PINS	8 PINS	8 PINS	8 PINS		
R <sub>θJA</sub>	Junction-to-ambient thermal resistance <sup>(2)(3)</sup>	97	85	95	149	—	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance <sup>(4)(5)</sup>	—	—	—	—	14.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

(2) Maximum power dissipation is a function of T<sub>J(max)</sub>, R<sub>θJA</sub>, and T<sub>A</sub>. The maximum allowable power dissipation at any allowable ambient temperature is P<sub>D</sub> = (T<sub>J(max)</sub> - T<sub>A</sub>) / R<sub>θJA</sub>. Operating at the absolute maximum T<sub>J</sub> of 150°C can affect reliability.

(3) The package thermal impedance is calculated in accordance with JESD 51-7.

(4) Maximum power dissipation is a function of T<sub>J(max)</sub>, R<sub>θJC</sub>, and T<sub>C</sub>. The maximum allowable power dissipation at any allowable ambient temperature is P<sub>D</sub> = (T<sub>J(max)</sub> - T<sub>C</sub>) / R<sub>θJC</sub>. Operating at the absolute maximum T<sub>J</sub> of 150°C can affect reliability.

(5) The package thermal impedance is calculated in accordance with MIL-STD-883.

## 6.5 Thermal Information - 14 Pins

THERMAL METRIC <sup>(1)</sup>	TL06xx							UNIT	
	D (SOIC)	N (PDIP)	NS (SO)	PS (SO)	PW (TSSOP)	J (CDIP)	W (CFP)		
	14 PINS	14 PINS	14 PINS	8 PINS	14 PINS	14 PINS	14 PINS		
R <sub>θJA</sub>	Junction-to-ambient thermal resistance <sup>(2)(3)</sup>	86	80	76	95	113	—	—	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance <sup>(2)(3)</sup>	—	—	—	—	—	15.05	14.65	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

(2) Maximum power dissipation is a function of T<sub>J(max)</sub>, R<sub>θJC</sub>, and T<sub>C</sub>. The maximum allowable power dissipation at any allowable ambient temperature is P<sub>D</sub> = (T<sub>J(max)</sub> - T<sub>C</sub>) / R<sub>θJC</sub>. Operating at the absolute maximum T<sub>J</sub> of 150°C can affect reliability.

(3) The package thermal impedance is calculated in accordance with MIL-STD-883.

## 6.6 Thermal Information - 20 Pins

THERMAL METRIC <sup>(1)</sup>		TL06xx	UNIT
		FK (LCCC)	
		20 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance <sup>(2)(3)</sup>	—	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance <sup>(4)(5)</sup>	5.61	°C/W

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).
- (2) Maximum power dissipation is a function of T<sub>J(max)</sub>, R<sub>θJA</sub>, and T<sub>A</sub>. The maximum allowable power dissipation at any allowable ambient temperature is P<sub>D</sub> = (T<sub>J(max)</sub> – T<sub>A</sub>)/R<sub>θJA</sub>. Operating at the absolute maximum T<sub>J</sub> of 150°C can affect reliability.
- (3) The package thermal impedance is calculated in accordance with JESD 51-7.
- (4) Maximum power dissipation is a function of T<sub>J(max)</sub>, R<sub>θJC</sub>, and T<sub>C</sub>. The maximum allowable power dissipation at any allowable ambient temperature is P<sub>D</sub> = (T<sub>J(max)</sub> – T<sub>C</sub>) / R<sub>θJC</sub>. Operating at the absolute maximum T<sub>J</sub> of 150°C can affect reliability.
- (5) The package thermal impedance is calculated in accordance with MIL-STD-883.

## 6.7 Electrical Characteristics for TL06xC and TL06xxC

V<sub>CC±</sub> = ±15 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS <sup>(1)</sup>	TL061C, TL062C, TL064C			TL061AC, TL062AC, TL064AC			UNIT	
		MIN	TYP	MAX	MIN	TYP	MAX		
V <sub>IO</sub>	Input offset voltage V <sub>O</sub> = 0, R <sub>S</sub> = 50 Ω	T <sub>A</sub> = 25°C		3	15	3		6	mV
		T <sub>A</sub> = Full range					7.5		
α <sub>VIO</sub>	Temperature coefficient of input offset voltage V <sub>O</sub> = 0, R <sub>S</sub> = 50 Ω, T <sub>A</sub> = Full range	10			10			μV/°C	
I <sub>IO</sub>	Input offset current V <sub>O</sub> = 0	T <sub>A</sub> = 25°C		5	200	5		100	pA
		T <sub>A</sub> = Full range		5			3		nA
I <sub>IB</sub>	Input bias current <sup>(2)</sup> V <sub>O</sub> = 0	T <sub>A</sub> = 25°C		30	400	30		200	pA
		T <sub>A</sub> = Full range		10			7		nA
V <sub>ICR</sub>	Common-mode input voltage range T <sub>A</sub> = 25°C	±11	–12 to 15	±11		–12 to 15			V
V <sub>OM</sub>	Maximum peak output voltage swing R <sub>L</sub> = 10 kΩ, T <sub>A</sub> = 25°C	±10	±13.5	±10		±13.5			V
	R <sub>L</sub> ≥ 10 kΩ, T <sub>A</sub> = Full range	±10			±10				
A <sub>VD</sub>	Large-signal differential voltage amplification V <sub>O</sub> = ±10 V, R <sub>L</sub> ≥ 2 kΩ	T <sub>A</sub> = 25°C		3	6	4		6	V/mV
		T <sub>A</sub> = Full range		3			4		
B <sub>1</sub>	Unity-gain bandwidth R <sub>L</sub> = 10 kΩ, T <sub>A</sub> = 25°C	1			1				MHz
r <sub>i</sub>	Input resistance T <sub>A</sub> = 25°C	10 <sup>12</sup>			10 <sup>12</sup>				Ω
CMRR	Common-mode rejection ratio V <sub>IC</sub> = V <sub>ICRmin</sub> , V <sub>O</sub> = 0, R <sub>S</sub> = 50 Ω, T <sub>A</sub> = 25°C	70	86	80		86			dB
k <sub>SVR</sub>	Supply-voltage rejection ratio (ΔV <sub>CC±</sub> /ΔV <sub>IO</sub> ) V <sub>CC</sub> = ±9 V to ±15 V, V <sub>O</sub> = 0, R <sub>S</sub> = 50 Ω, T <sub>A</sub> = 25°C	70	95	80		95			dB
P <sub>D</sub>	Total power dissipation (each amplifier) V <sub>O</sub> = 0, No load, T <sub>A</sub> = 25°C	6		7.5	6		7.5		mW
I <sub>CC</sub>	Supply current (each amplifier) V <sub>O</sub> = 0, No load, T <sub>A</sub> = 25°C	200		250	200		250		μA
V <sub>O1</sub> /V <sub>O2</sub>	Crosstalk attenuation A <sub>VD</sub> = 100, T <sub>A</sub> = 25°C	120			120				dB

- (1) All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Full range for T<sub>A</sub> is 0°C to 70°C for TL06xC, TL06xAC, and TL06xBC and –40°C to 85°C for TL06xI.
- (2) Input bias currents of an FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive, as shown in [Figure 12](#). Pulse techniques are used to maintain the junction temperature as close to the ambient temperature as possible.

## 6.8 Electrical Characteristics for TL06xxC and TL06xl

 $V_{CC\pm} = \pm 15\text{ V}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS <sup>(1)</sup>	TL061BC, TL062BC, TL064BC			TL061I, TL062I, TL064I			UNIT	
		MIN	TYP	MAX	MIN	TYP	MAX		
$V_{IO}$	Input offset voltage $V_O = 0, R_S = 50\ \Omega$	$T_A = 25^\circ\text{C}$		2	3		3	6	mV
		$T_A = \text{Full range}$					5	9	
$\alpha_{VIO}$	Temperature coefficient of input offset voltage $V_O = 0, R_S = 50\ \Omega, T_A = \text{Full range}$	10			10			$\mu\text{V}/^\circ\text{C}$	
$I_{IO}$	Input offset current $V_O = 0$	$T_A = 25^\circ\text{C}$		5	100		5	100	pA
		$T_A = \text{Full range}$					10		nA
$I_{IB}$	Input bias current <sup>(2)</sup> $V_O = 0$	$T_A = 25^\circ\text{C}$		30	200		30	200	pA
		$T_A = \text{Full range}$					20		nA
$V_{ICR}$	Common-mode input voltage range $T_A = 25^\circ\text{C}$	$\pm 11$	-12 to 15	$\pm 11$	-12 to 15				V
$V_{OM}$	Maximum peak output voltage swing $R_L = 10\ \text{k}\Omega, T_A = 25^\circ\text{C}$	$\pm 10$	$\pm 13.5$	$\pm 10$	$\pm 13.5$				V
	$R_L \geq 10\ \text{k}\Omega, T_A = \text{Full range}$	$\pm 10$							
$A_{VD}$	Large-signal differential voltage amplification $V_O = \pm 10\ \text{V}, R_L \geq 2\ \text{k}\Omega$	$T_A = 25^\circ\text{C}$		4	6		4	6	V/mV
		$T_A = \text{Full range}$					4		
$B_1$	Unity-gain bandwidth $R_L = 10\ \text{k}\Omega, T_A = 25^\circ\text{C}$	1			1			MHz	
$r_i$	Input resistance $T_A = 25^\circ\text{C}$	$10^{12}$			$10^{12}$			$\Omega$	
CMRR	Common-mode rejection ratio $V_{IC} = V_{ICRmin}, V_O = 0, R_S = 50\ \Omega, T_A = 25^\circ\text{C}$	80	86	80	86				dB
$k_{SVR}$	Supply-voltage rejection ratio ( $\Delta V_{CC\pm}/\Delta V_{IO}$ ) $V_{CC} = \pm 9\ \text{V to } \pm 15\ \text{V}, V_O = 0, R_S = 50\ \Omega, T_A = 25^\circ\text{C}$	80	95	80	95				dB
$P_D$	Total power dissipation (each amplifier) $V_O = 0, \text{No load}, T_A = 25^\circ\text{C}$	6	7.5	6	7.5				mW
$I_{CC}$	Supply current (each amplifier) $V_O = 0, \text{No load}, T_A = 25^\circ\text{C}$	200	250	200	250				$\mu\text{A}$
$V_{O1}/V_{O2}$	Crosstalk attenuation $A_{VD} = 100, T_A = 25^\circ\text{C}$	120			120			dB	

- (1) All characteristics are measured under open-loop conditions with zero common-mode input voltage, unless otherwise specified. Full range for  $T_A$  is  $0^\circ\text{C}$  to  $70^\circ\text{C}$  for TL06xC, TL06xAC, and TL06xBC and  $-40^\circ\text{C}$  to  $85^\circ\text{C}$  for TL06xl.
- (2) Input bias currents of an FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive, as shown in Figure 12. Pulse techniques are used to maintain the junction temperature as close to the ambient temperature as possible.

## 6.9 Electrical Characteristics for TL06xM and TL064M

 $V_{CC\pm} = \pm 15\text{ V}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS <sup>(1)</sup>	TL061M, TL062M			TL064M			UNIT	
		MIN	TYP	MAX	MIN	TYP	MAX		
$V_{IO}$	Input offset voltage $V_O = 0, R_S = 50\ \Omega$	$T_A = 25^\circ\text{C}$		3	6		3	9	mV
		$T_A = -55^\circ\text{C to } 125^\circ\text{C}$					9	15	
$\alpha_{VIO}$	Temperature coefficient of input offset voltage $V_O = 0, R_S = 50\ \Omega, T_A = -55^\circ\text{C to } 125^\circ\text{C}$	10			10			$\mu\text{V}/^\circ\text{C}$	
$I_{IO}$	Input offset current $V_O = 0$	$T_A = 25^\circ\text{C}$		5	100		5	100	pA
		$T_A = -55^\circ\text{C}$		20 <sup>(2)</sup>			20 <sup>(2)</sup>		nA
		$T_A = 125^\circ\text{C}$		20			20		
$I_{IB}$	Input bias current <sup>(3)</sup> $V_O = 0$	$T_A = 25^\circ\text{C}$		30	200		30	200	pA
		$T_A = -55^\circ\text{C}$		50 <sup>(2)</sup>			50 <sup>(2)</sup>		nA
		$T_A = 125^\circ\text{C}$		50			50		
$V_{ICR}$	Common-mode input voltage range $T_A = 25^\circ\text{C}$	$\pm 11$	-12 to 15	$\pm 11$	-12 to 15				V

- (1) All characteristics are measured under open-loop conditions, with zero common-mode voltage, unless otherwise specified.
- (2) This parameter is not production tested.
- (3) Input bias currents of an FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive, as shown in Figure 12. Pulse techniques are used to maintain the junction temperature as close to the ambient temperature as possible.

## Electrical Characteristics for TL06xM and TL064M (continued)

$V_{CC\pm} = \pm 15\text{ V}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS <sup>(1)</sup>	TL061M, TL062M			TL064M			UNIT	
		MIN	TYP	MAX	MIN	TYP	MAX		
$V_{OM}$	Maximum peak output voltage swing	$R_L = 10\text{ k}\Omega, T_A = 25^\circ\text{C}$			$\pm 10$	$\pm 13.5$		V	
		$R_L \geq 10\text{ k}\Omega, T_A = -55^\circ\text{C to } 125^\circ\text{C}$			$\pm 10$				
$A_{VD}$	Large-signal differential voltage amplification	$V_O = \pm 10\text{ V}, R_L \geq 2\text{ k}\Omega$	$T_A = 25^\circ\text{C}$		4	6	4	6	V/mV
			$T_A = -55^\circ\text{C to } 125^\circ\text{C}$		4		4		
$B_1$	Unity-gain bandwidth	$R_L = 10\text{ k}\Omega, T_A = 25^\circ\text{C}$						MHz	
$r_i$	Input resistance	$T_A = 25^\circ\text{C}$				$10^{12}$	$10^{12}$	$\Omega$	
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICRmin}, V_O = 0, R_S = 50\ \Omega, T_A = 25^\circ\text{C}$			80	86	80	86	dB
$k_{SVR}$	Supply-voltage rejection ratio ( $\Delta V_{CC\pm}/\Delta V_{IO}$ )	$V_{CC} = \pm 9\text{ V to } \pm 15\text{ V}, V_O = 0, R_S = 50\ \Omega, T_A = 25^\circ\text{C}$			80	95	80	95	dB
$P_D$	Total power dissipation (each amplifier)	$V_O = 0, \text{No load}, T_A = 25^\circ\text{C}$			6	7.5	6	7.5	mW
$I_{CC}$	Supply current (each amplifier)	$V_O = 0, \text{No load}, T_A = 25^\circ\text{C}$			200	250	200	250	$\mu\text{A}$
$V_{O1}/V_{O2}$	Crosstalk attenuation	$A_{VD} = 100, T_A = 25^\circ\text{C}$			120		120		dB

## 6.10 Operating Characteristics

$V_{CC\pm} = \pm 15\text{ V}, T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain <sup>(1)</sup> $V_I = 10\text{ V}, R_L = 10\text{ k}\Omega,$ $C_L = 100\text{ pF},$ see <a href="#">Figure 16</a>	1.5	3.5		V/ $\mu\text{s}$
$t_r$	Rise-time		0.2		$\mu\text{s}$
	Overshoot factor		10%		
$V_n$	Equivalent input noise voltage $R_S = 20\ \Omega, f = 1\text{ kHz}$		42		nV/ $\sqrt{\text{Hz}}$

(1) Slew rate at  $-55^\circ\text{C to } 125^\circ\text{C}$  is 0.7 V/ $\mu\text{s}$  min.



## 6.11 Typical Characteristics

Data at high and low temperatures are applicable only within the specified operating free-air temperature ranges of the various devices.

**Table 1. Table of Graphs**

	<b>FIGURE</b>
Maximum peak output voltage versus Supply voltage	<a href="#">Figure 1</a>
Maximum peak output voltage versus Free-air temperature	<a href="#">Figure 2</a>
Maximum peak output voltage versus Load resistance	<a href="#">Figure 3</a>
Maximum peak output voltage versus Frequency	<a href="#">Figure 4</a>
Differential voltage amplification versus Free-air temperature	<a href="#">Figure 5</a>
Large-signal differential voltage amplification versus Frequency	<a href="#">Figure 6</a>
Phase shift versus Frequency	<a href="#">Figure 6</a>
Supply current versus Supply voltage	<a href="#">Figure 7</a>
Supply current versus Free-air temperature	<a href="#">Figure 8</a>
Total power dissipation versus Free-air temperature	<a href="#">Figure 9</a>
Common-mode rejection ratio versus Free-air temperature	<a href="#">Figure 10</a>
Normalized unity-gain bandwidth versus Free-air temperature	<a href="#">Figure 11</a>
Normalized slew rate versus Free-air temperature	<a href="#">Figure 11</a>
Normalized phase shift versus Free-air temperature	<a href="#">Figure 11</a>
Input bias current versus Free-air temperature	<a href="#">Figure 12</a>
Voltage-follower large-signal pulse response versus Time	<a href="#">Figure 13</a>
Output voltage versus Elapsed time	<a href="#">Figure 14</a>
Equivalent input noise voltage versus Frequency	<a href="#">Figure 15</a>

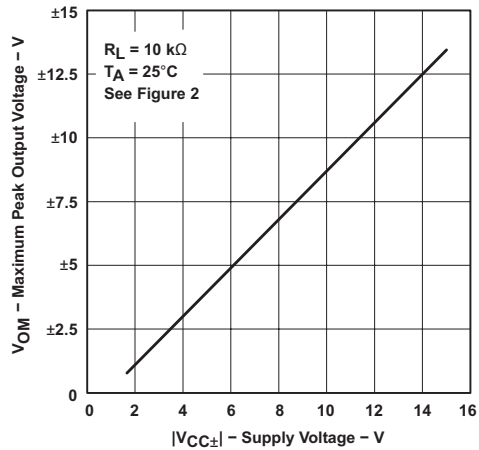


Figure 1. Maximum Peak Output Voltage vs Supply Voltage

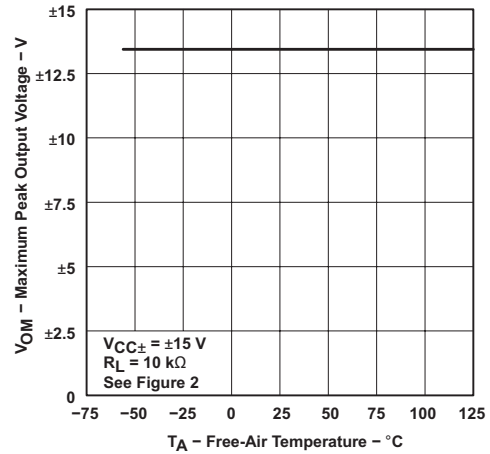


Figure 2. Maximum Peak Output Voltage vs Free-Air Temperature

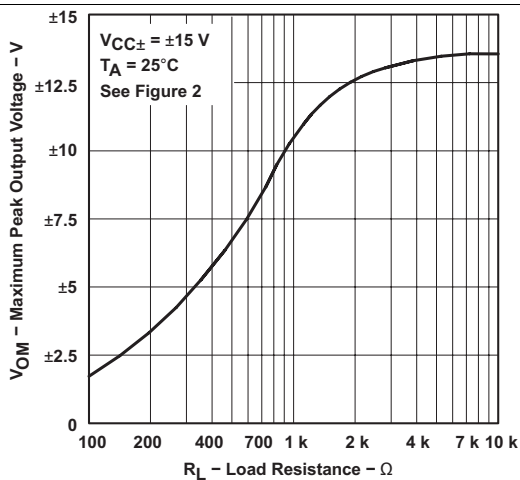


Figure 3. Maximum Peak Output Voltage vs Load Resistance

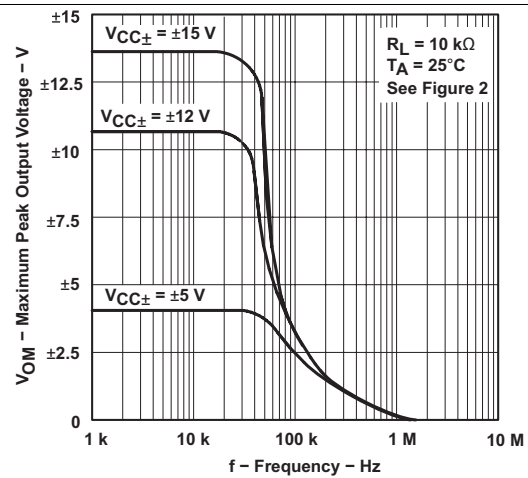


Figure 4. Maximum Peak Output Voltage vs Frequency

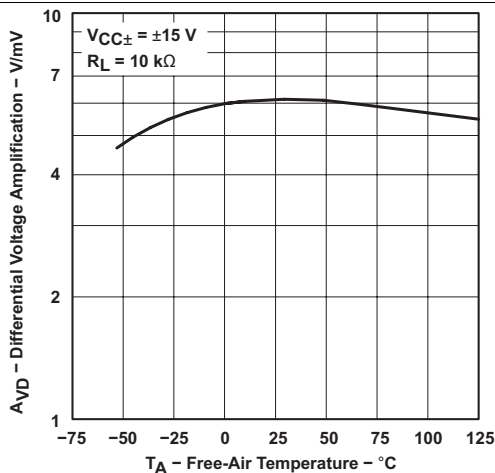


Figure 5. Differential Voltage Amplification vs Free-Air Temperature

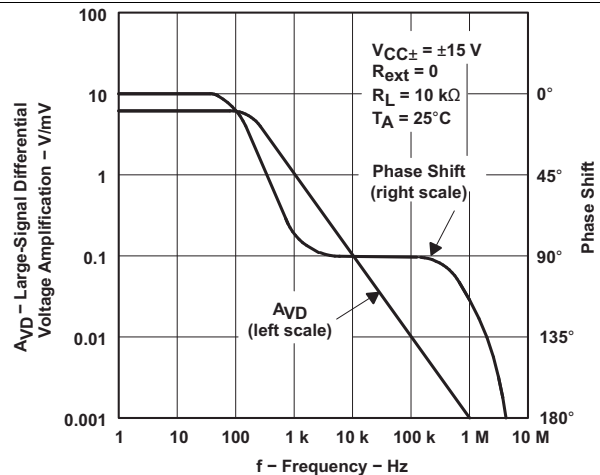


Figure 6. Large-Signal Differential Voltage Amplification and Phase Shift vs Frequency



Figure 7. Supply Current vs Supply Voltage



Figure 8. Supply Current vs Free-Air Temperature



Figure 9. Total Power Dissipation vs Free-Air Temperature



Figure 10. All Except TL06\_C Common-Mode Rejection Ratio vs Free-Air Temperature



Figure 11. Normalized Unity-Gain Bandwidth, Slew Rate, and Phase Shift vs Free-Air Temperature



Figure 12. Input Bias Current vs Free-Air Temperature

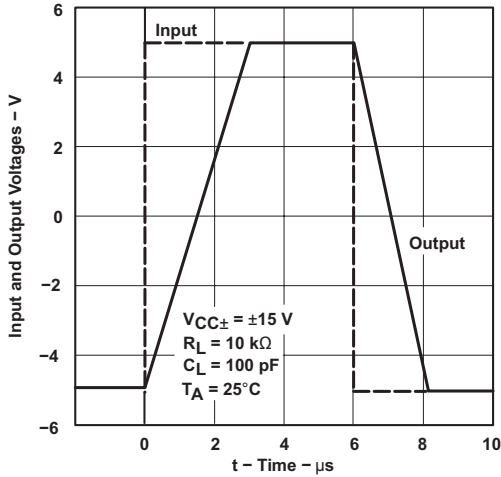


Figure 13. Voltage-Follower Large-Signal Pulse Response vs Time



Figure 14. Output Voltage vs Elapsed Time



Figure 15. Equivalent Input Noise Voltage vs Frequency

## 7 Parameter Measurement Information

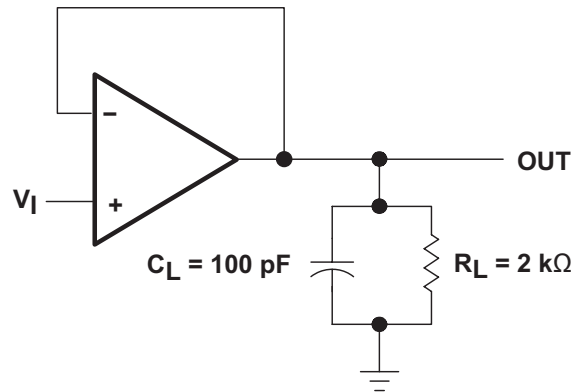


Figure 16. Unity-Gain Amplifier

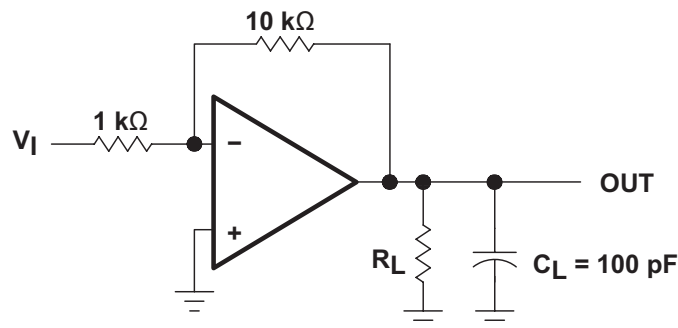


Figure 17. Gain-of-10 Inverting Amplifier

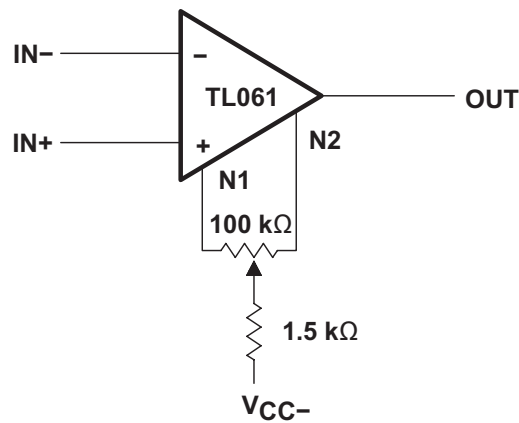


Figure 18. Input Offset-Voltage Null Circuit

## 8 Detailed Description

### 8.1 Overview

The JFET-input operational amplifiers of the TL06x series are designed as low-power versions of the TL08x series amplifiers. They feature high input impedance, wide bandwidth, high slew rate, and low input offset and input bias currents. The TL06x series features the same terminal assignments as the TL07x and TL08x series. Each of these JFET-input operational amplifiers incorporates well-matched, high-voltage JFET and bipolar transistors in an integrated circuit.

The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from –40°C to 85°C, and the M-suffix devices are characterized for operation over the full military temperature range of –55°C to 125°C.

### 8.2 Functional Block Diagram



TL061 Only  
 C1 = 10 pF on TL061, TL062, and TL064  
 Component values shown are nominal.

### 8.3 Feature Description

#### 8.3.1 Common-Mode Rejection Ratio

The common-mode rejection ratio (CMRR) of an amplifier is a measure of how well the device rejects unwanted input signals common to both input leads. It is found by taking the ratio of the change in input offset voltage to the change in the input voltage and converting to decibels. Ideally the CMRR is infinite, but in practice, amplifiers are designed to have it as high as possible. The CMRR of this device is 86 dB.

#### 8.3.2 Slew Rate

The slew rate is the rate at which an operational amplifier can change its output when there is a change on the input. These devices have a 3.5-V/ $\mu$ s slew rate.

## 8.4 Device Functional Modes

These devices are powered on when the supply is connected. This device can be operated as a single supply operational amplifier or dual supply amplifier depending on the application.

## 9 Applications and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

The TL06x series of operational amplifiers can be used in countless applications. The few applications in this section show principles used in all applications of these parts.

### 9.2 Typical Applications

#### 9.2.1 Inverting Amplifier Application

A typical application for an operational amplifier in an inverting amplifier. This amplifier takes a positive voltage on the input, and makes it a negative voltage of the same magnitude. In the same manner, it also makes negative voltages positive.



Figure 19. Schematic for Inverting Amplifier Application

##### 9.2.1.1 Design Requirements

The supply voltage must be chosen such that it is larger than the input voltage range and output range. For instance, this application will scale a signal of  $\pm 0.5$  V to  $\pm 1.8$  V. Setting the supply at  $\pm 12$  V is sufficient to accommodate this application.

##### 9.2.1.2 Detailed Design Procedure

Determine the gain required by the inverting amplifier:

$$A_v = \frac{V_{OUT}}{V_{IN}} \quad (1)$$

$$A_v = \frac{1.8}{-0.5} = -3.6 \quad (2)$$

Once the desired gain is determined, choose a value for  $R_I$  or  $R_F$ . Choosing a value in the kilohm range is desirable because the amplifier circuit will use currents in the milliamp range. This ensures the part will not draw too much current. This example will choose 10 k $\Omega$  for  $R_I$  which means 36 k $\Omega$  will be used for  $R_F$ . This was determined by Equation 3.

$$A_v = -\frac{R_F}{R_I} \quad (3)$$



## Typical Applications (continued)

### 9.2.1.3 Application Curve

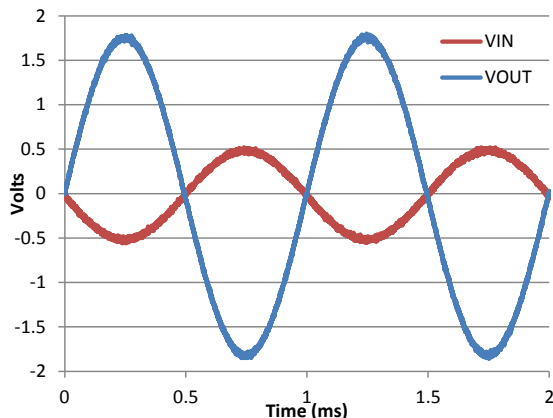


Figure 20. Input and Output Voltages of the Inverting Amplifier

## 9.3 System Examples

### 9.3.1 General Applications



Figure 21. Instrumentation Amplifier

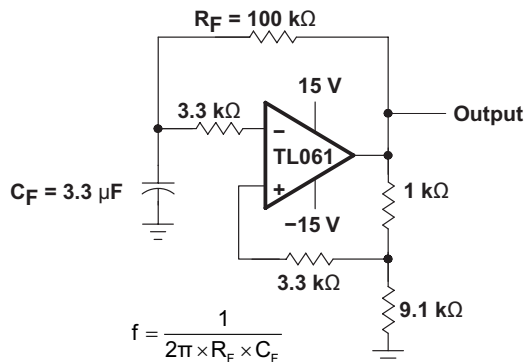


Figure 22. 0.5-Hz Square-Wave Oscillator



Figure 23. High-Q Notch Filter

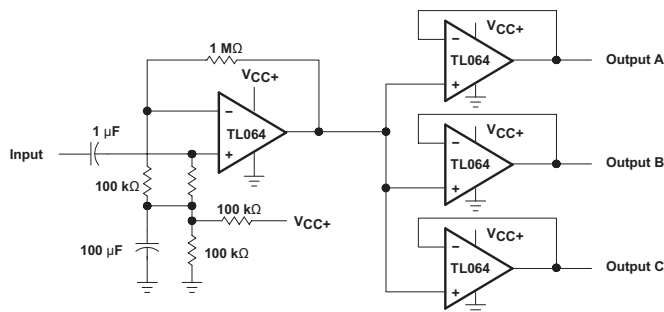


Figure 24. Audio-Distribution Amplifier

System Examples (continued)



Figure 25. Low-Level Light Detector Preamplifier



Figure 26. AC Amplifier



Figure 27. Microphone Preamplifier With Tone Control



Figure 28. Instrumentation Amplifier

System Examples (continued)

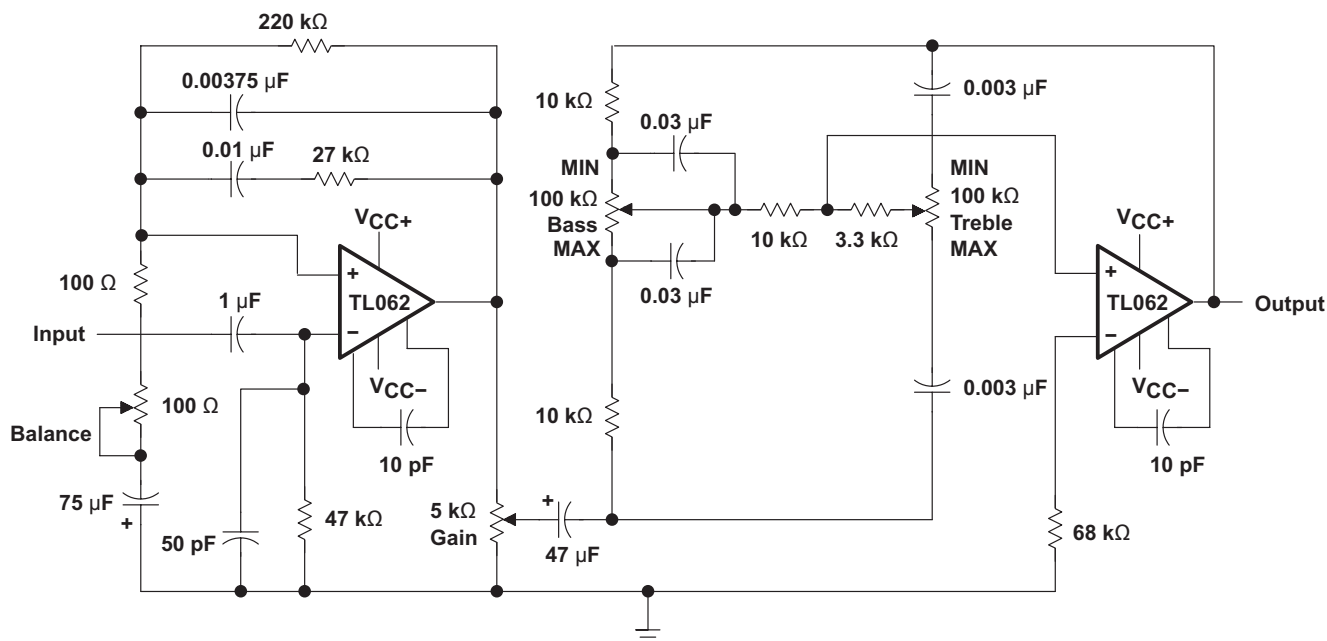
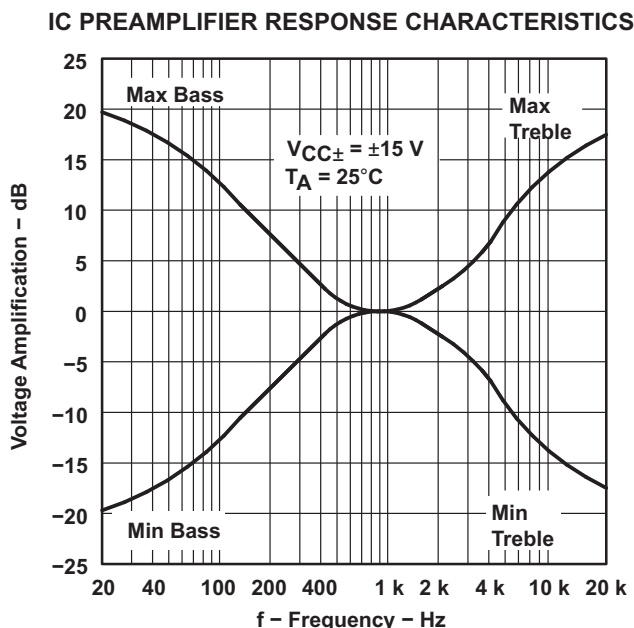


Figure 29. IC Preamplifier

10 Power Supply Recommendations

CAUTION

Supply voltages larger than 36 V for a single supply, or outside the range of  $\pm 18\text{ V}$  for a dual supply can permanently damage the device (see the [Absolute Maximum Ratings](#)).

Place 0.1- $\mu\text{F}$  bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high impedance power supplies. For more detailed information on bypass capacitor placement, refer to the [Layout](#).

## 11 Layout

### 11.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole, as well as the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1- $\mu$ F ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current. For more detailed information, refer to *Circuit Board Layout Techniques*, (SLOA089).
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keeping RF and RG close to the inverting input minimizes parasitic capacitance, as shown in *Layout Examples*.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

### 11.2 Layout Examples



Figure 30. Operational Amplifier Schematic for Noninverting Configuration

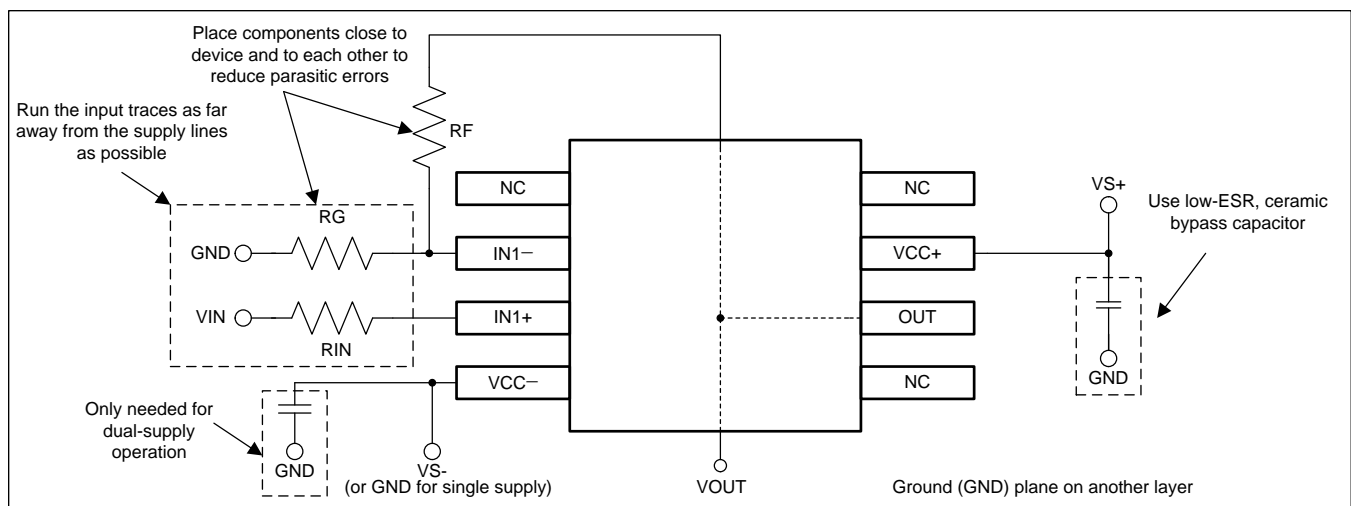


Figure 31. Operational Amplifier Board Layout for Noninverting Configuration

## 12 Device and Documentation Support

### 12.1 Documentation Support

#### 12.1.1 Related Documentation

For related documentation, see the following:

*Circuit Board Layout Techniques*, [SLOA089](#)

### 12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 2. Related Links**

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TL061	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
TL061A	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
TL061B	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
TL062	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
TL062A	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
TL062B	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
TL064	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
TL064A	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
TL064B	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>

### 12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 12.4 Trademarks

E2E is a trademark of Texas Instruments.

### 12.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 12.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
81023022A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	81023022A TL062MFKB	<a href="#">Samples</a>
8102302PA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	8102302PA TL062M	<a href="#">Samples</a>
81023032A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	81023032A TL064MFKB	<a href="#">Samples</a>
8102303CA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	8102303CA TL064MJB	<a href="#">Samples</a>
8102303DA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	8102303DA TL064MWB	<a href="#">Samples</a>
TL061ACD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	061AC	<a href="#">Samples</a>
TL061ACDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	061AC	<a href="#">Samples</a>
TL061ACDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	061AC	<a href="#">Samples</a>
TL061ACP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL061ACP	<a href="#">Samples</a>
TL061ACPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL061ACP	<a href="#">Samples</a>
TL061BCP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL061BCP	<a href="#">Samples</a>
TL061BCPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL061BCP	<a href="#">Samples</a>
TL061CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL061C	<a href="#">Samples</a>
TL061CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL061C	<a href="#">Samples</a>
TL061CP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL061CP	<a href="#">Samples</a>
TL061CPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL061CP	<a href="#">Samples</a>
TL061CPSR	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T061	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL061ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL061I	<a href="#">Samples</a>
TL061IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL061I	<a href="#">Samples</a>
TL061IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL061I	<a href="#">Samples</a>
TL061IP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	TL061IP	<a href="#">Samples</a>
TL061IPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	TL061IP	<a href="#">Samples</a>
TL062ACD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	062AC	<a href="#">Samples</a>
TL062ACDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	062AC	<a href="#">Samples</a>
TL062ACDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	062AC	<a href="#">Samples</a>
TL062ACDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	062AC	<a href="#">Samples</a>
TL062ACDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	062AC	<a href="#">Samples</a>
TL062ACP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL062ACP	<a href="#">Samples</a>
TL062ACPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL062ACP	<a href="#">Samples</a>
TL062ACPSR	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T062A	<a href="#">Samples</a>
TL062ACPSRG4	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T062A	<a href="#">Samples</a>
TL062BCD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	062BC	<a href="#">Samples</a>
TL062BCDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	062BC	<a href="#">Samples</a>
TL062BCDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	062BC	<a href="#">Samples</a>
TL062BCP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL062BCP	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL062BCPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL062BCP	<a href="#">Samples</a>
TL062CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL062C	<a href="#">Samples</a>
TL062CDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL062C	<a href="#">Samples</a>
TL062CDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL062C	<a href="#">Samples</a>
TL062CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL062C	<a href="#">Samples</a>
TL062CDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL062C	<a href="#">Samples</a>
TL062CDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL062C	<a href="#">Samples</a>
TL062CP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL062CP	<a href="#">Samples</a>
TL062CPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL062CP	<a href="#">Samples</a>
TL062CPSR	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T062	<a href="#">Samples</a>
TL062CPSRG4	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T062	<a href="#">Samples</a>
TL062CPW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T062	<a href="#">Samples</a>
TL062CPWG4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T062	<a href="#">Samples</a>
TL062CPWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T062	<a href="#">Samples</a>
TL062CPWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T062	<a href="#">Samples</a>
TL062ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL062I	<a href="#">Samples</a>
TL062IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL062I	<a href="#">Samples</a>
TL062IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL062I	<a href="#">Samples</a>



Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL062IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL062I	<a href="#">Samples</a>
TL062IP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	TL062IP	<a href="#">Samples</a>
TL062IPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	TL062IP	<a href="#">Samples</a>
TL062IPWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	Z062	<a href="#">Samples</a>
TL062IPWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	Z062	<a href="#">Samples</a>
TL062MFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	81023022A TL062MFKB	<a href="#">Samples</a>
TL062MJG	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	TL062MJG	<a href="#">Samples</a>
TL062MJGB	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	8102302PA TL062M	<a href="#">Samples</a>
TL064ACD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL064AC	<a href="#">Samples</a>
TL064ACDE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL064AC	<a href="#">Samples</a>
TL064ACDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL064AC	<a href="#">Samples</a>
TL064ACDRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL064AC	<a href="#">Samples</a>
TL064ACN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL064ACN	<a href="#">Samples</a>
TL064BCD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL064BC	<a href="#">Samples</a>
TL064BCDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL064BC	<a href="#">Samples</a>
TL064BCDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL064BC	<a href="#">Samples</a>
TL064BCN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL064BCN	<a href="#">Samples</a>
TL064BCNE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL064BCN	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL064CD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL064C	<a href="#">Samples</a>
TL064CDE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL064C	<a href="#">Samples</a>
TL064CDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL064C	<a href="#">Samples</a>
TL064CDRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL064C	<a href="#">Samples</a>
TL064CDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL064C	<a href="#">Samples</a>
TL064CN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL064CN	<a href="#">Samples</a>
TL064CNE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL064CN	<a href="#">Samples</a>
TL064CNSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL064	<a href="#">Samples</a>
TL064CNSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL064	<a href="#">Samples</a>
TL064CPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T064	<a href="#">Samples</a>
TL064CPWE4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T064	<a href="#">Samples</a>
TL064CPWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T064	<a href="#">Samples</a>
TL064CPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T064	<a href="#">Samples</a>
TL064CPWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T064	<a href="#">Samples</a>
TL064ID	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL064I	<a href="#">Samples</a>
TL064IDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL064I	<a href="#">Samples</a>
TL064IDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU   CU SN	Level-1-260C-UNLIM	-40 to 85	TL064I	<a href="#">Samples</a>
TL064IDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL064I	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL064IN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	TL064IN	<a href="#">Samples</a>
TL064INE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	TL064IN	<a href="#">Samples</a>
TL064INS	ACTIVE	SO	NS	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL064I	<a href="#">Samples</a>
TL064INSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL064I	<a href="#">Samples</a>
TL064IPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	Z064	<a href="#">Samples</a>
TL064MFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	81023032A TL064MFKB	<a href="#">Samples</a>
TL064MJ	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	TL064MJ	<a href="#">Samples</a>
TL064MJB	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	8102303CA TL064MJB	<a href="#">Samples</a>
TL064MWB	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	8102303DA TL064MWB	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF TL062, TL062M, TL064, TL064M :**

- Catalog: [TL062](#), [TL064](#)
- Military: [TL062M](#), [TL064M](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION



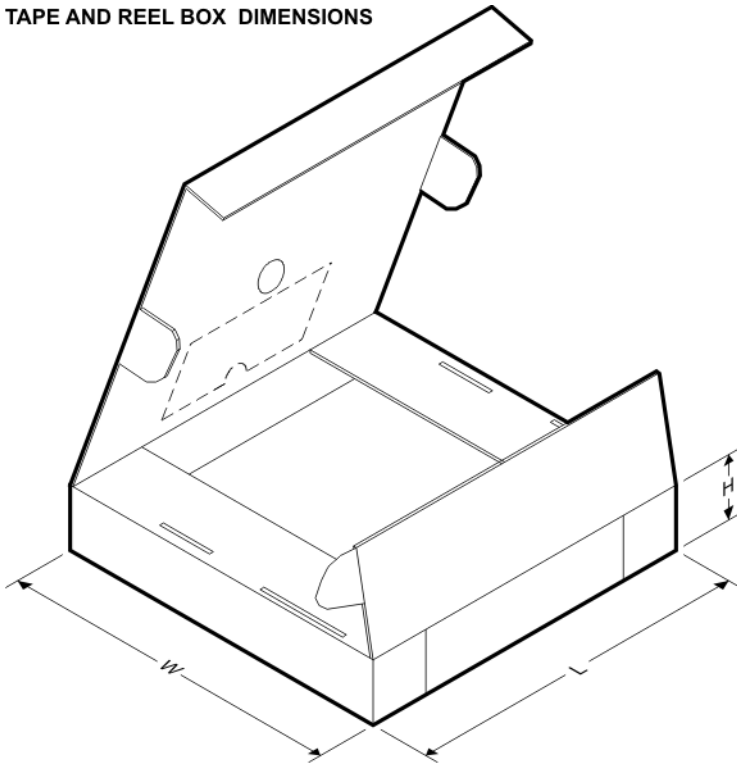
### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL061ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL061CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL061CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL061CPSR	SO	PS	8	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
TL061IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL061IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL062ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL062ACPSR	SO	PS	8	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
TL062BCDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL062CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL062CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL062CPSR	SO	PS	8	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
TL062CPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TL062CPWRG4	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TL062IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL062IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL062IPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TL064ACDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL064BCDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL064CPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TL064IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL064IDRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL064INSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
TL064IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL061ACDR	SOIC	D	8	2500	340.5	338.1	20.6
TL061CDR	SOIC	D	8	2500	340.5	338.1	20.6
TL061CDR	SOIC	D	8	2500	367.0	367.0	35.0
TL061CPSR	SO	PS	8	2000	367.0	367.0	38.0
TL061IDR	SOIC	D	8	2500	367.0	367.0	35.0
TL061IDR	SOIC	D	8	2500	340.5	338.1	20.6
TL062ACDR	SOIC	D	8	2500	340.5	338.1	20.6
TL062ACPSR	SO	PS	8	2000	367.0	367.0	38.0
TL062BCDR	SOIC	D	8	2500	340.5	338.1	20.6
TL062CDR	SOIC	D	8	2500	367.0	367.0	35.0
TL062CDR	SOIC	D	8	2500	340.5	338.1	20.6

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL062CPSR	SO	PS	8	2000	367.0	367.0	38.0
TL062CPWR	TSSOP	PW	8	2000	367.0	367.0	35.0
TL062CPWRG4	TSSOP	PW	8	2000	367.0	367.0	35.0
TL062IDR	SOIC	D	8	2500	367.0	367.0	35.0
TL062IDR	SOIC	D	8	2500	340.5	338.1	20.6
TL062IPWR	TSSOP	PW	8	2000	367.0	367.0	35.0
TL064ACDR	SOIC	D	14	2500	367.0	367.0	38.0
TL064BCDR	SOIC	D	14	2500	367.0	367.0	38.0
TL064CPWR	TSSOP	PW	14	2000	367.0	367.0	35.0
TL064IDR	SOIC	D	14	2500	367.0	367.0	38.0
TL064IDRG4	SOIC	D	14	2500	367.0	367.0	38.0
TL064INSR	SO	NS	14	2000	367.0	367.0	38.0
TL064IPWR	TSSOP	PW	14	2000	367.0	367.0	35.0

FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a metal lid.
  - Falls within JEDEC MS-004



# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK





- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within MIL STD 1835 GDFP1-F14

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040047-5/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  -  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE

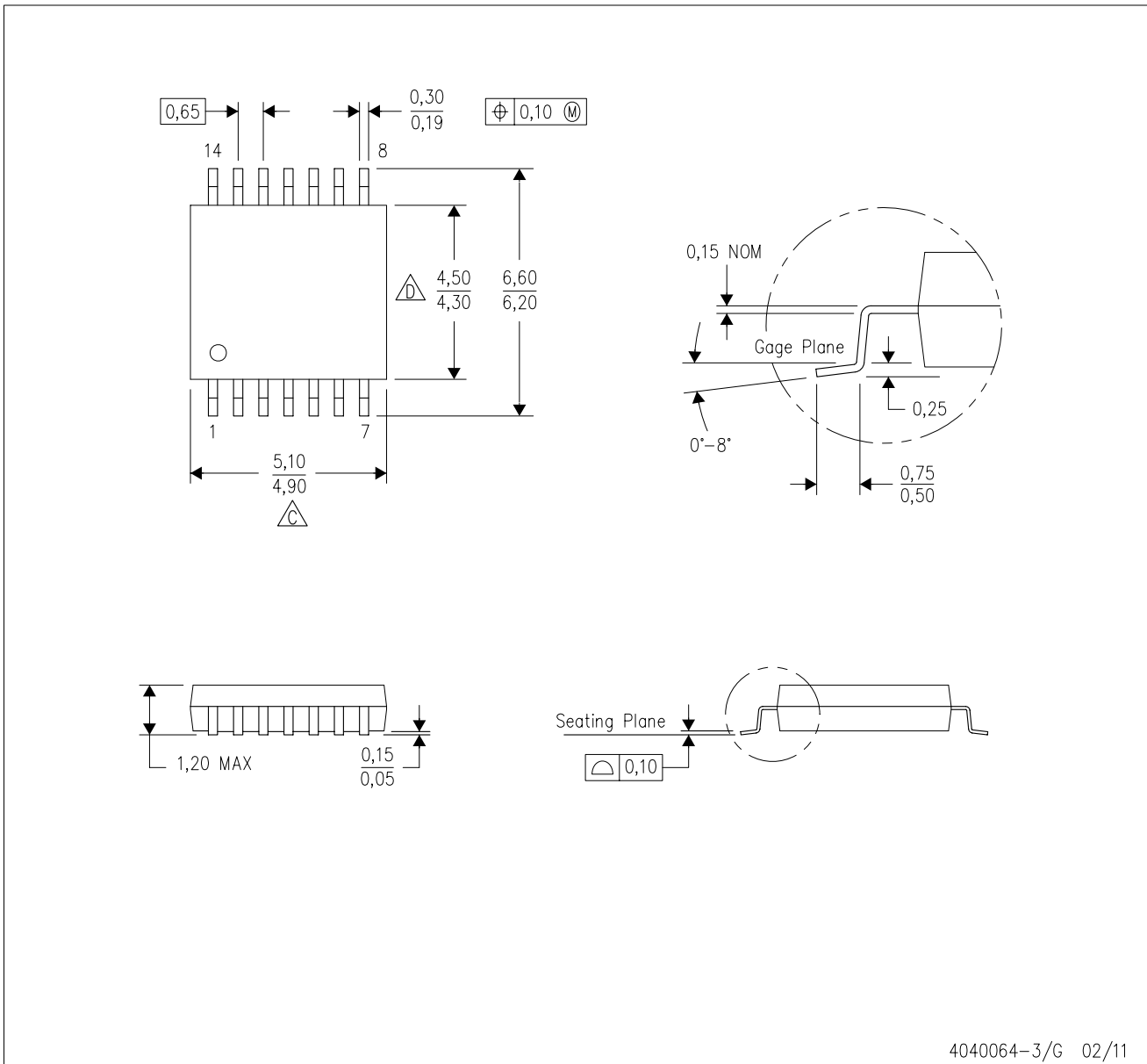


4211283-3/E 08/12

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040064-3/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - △ C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - △ D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.  
 D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.  
 E. Reference JEDEC MS-012 variation AA.



D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

# MECHANICAL DATA

PS (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PS (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

JG (R-GDIP-T8)

CERAMIC DUAL-IN-LINE



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. This package can be hermetically sealed with a ceramic lid using glass frit.  
 D. Index point is provided on cap for terminal identification.  
 E. Falls within MIL STD 1835 GDIP1-T8

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



4040082/E 04/2010

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MS-001 variation BA.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

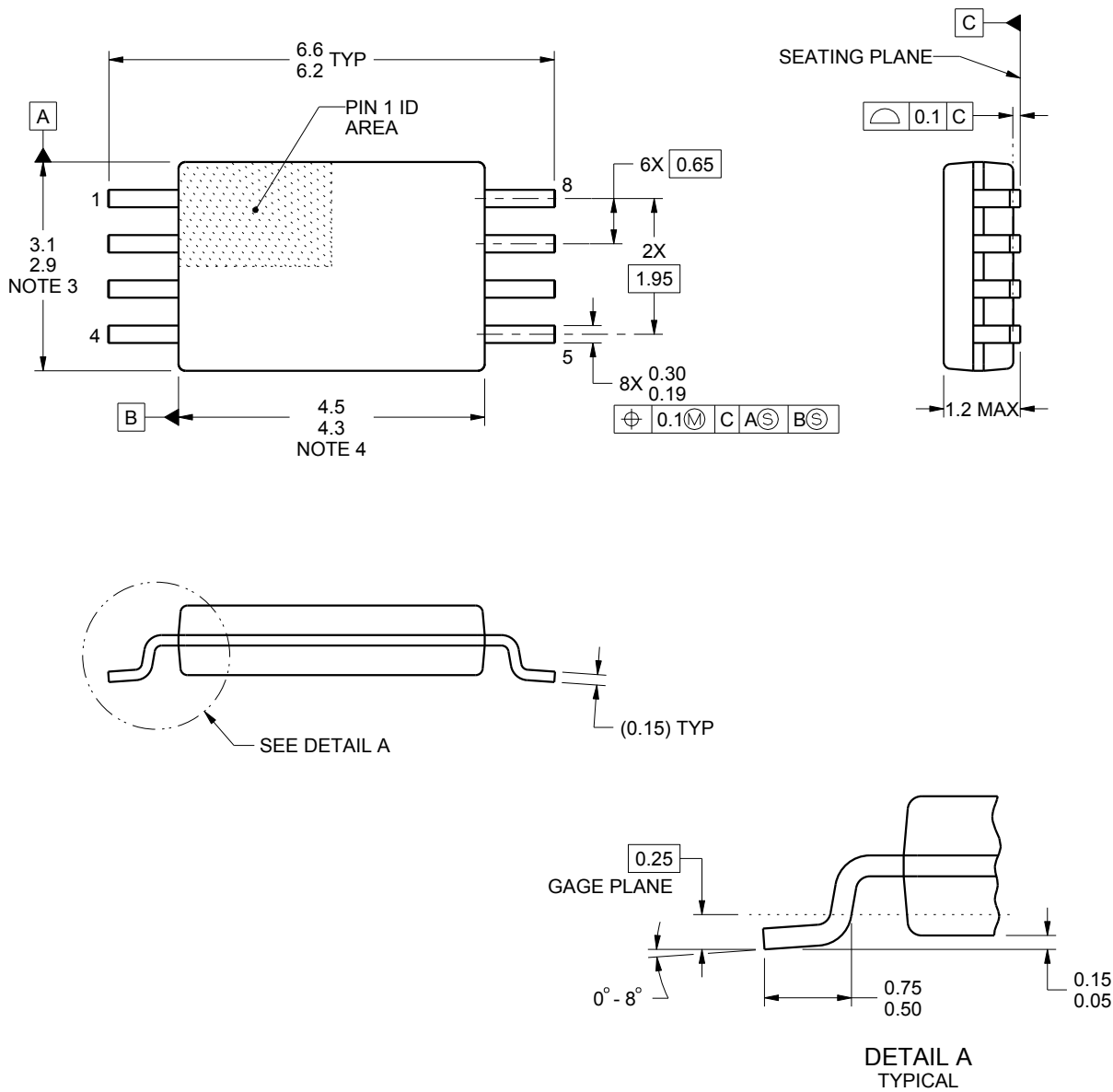
PW0008A



# PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4221848/A 02/2015

## NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.

# EXAMPLE BOARD LAYOUT

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:10X



SOLDER MASK DETAILS  
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



# EXAMPLE STENCIL DESIGN

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.