features

- **Analog Input Range**
  - **– TLC5510 . . . 2 V Full Scale**
  - **– TLC5510A . . . 4 V Full Scale**
- **8-Bit Resolution**
- **Integral Linearity Error**
  - **±0.75 LSB Max (25°C)**
  - **±1 LSB Max (–20°C to 75°C)**
- **Differential Linearity Error**
  - **±0.5 LSB Max (25°C)**
  - **±0.75 LSB Max (–20°C to 75°C)**
- **Maximum Conversion Rate**
  - **20 Mega-Samples per Second (MSPS) Max**
- **5-V Single-Supply Operation**
- **Low Power Consumption**
  - **TLC5510 . . . 127.5 mW Typ**
  - **TLC5510A . . . 150 mW Typ**
  - **(includes reference resistor dissipation)**
- **TLC5510 is Interchangeable With Sony CXD1175**

applications

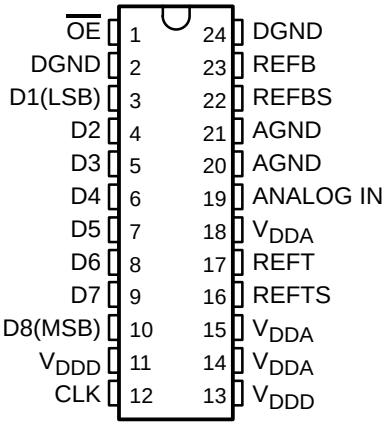
- **Digital TV**
- **Medical Imaging**
- **Video Conferencing**
- **High-Speed Data Conversion**
- **QAM Demodulators**

description

The TLC5510 and TLC5510A are CMOS, 8-bit, 20 MSPS analog-to-digital converters (ADCs) that utilize a semiflash architecture. The TLC5510 and TLC5510A operate with a single 5-V supply and typically consume only 130 mW of power. Included is an internal sample-and-hold circuit, parallel outputs with high-impedance mode, and internal reference resistors.

The semiflash architecture reduces power consumption and die size compared to flash converters. By implementing the conversion in a 2-step process, the number of comparators is significantly reduced. The latency of the data output valid is 2.5 clocks.

PW OR NS PACKAGE†
(TOP VIEW)



† Available in tape and reel only and ordered as the shown in the Available Options table below.

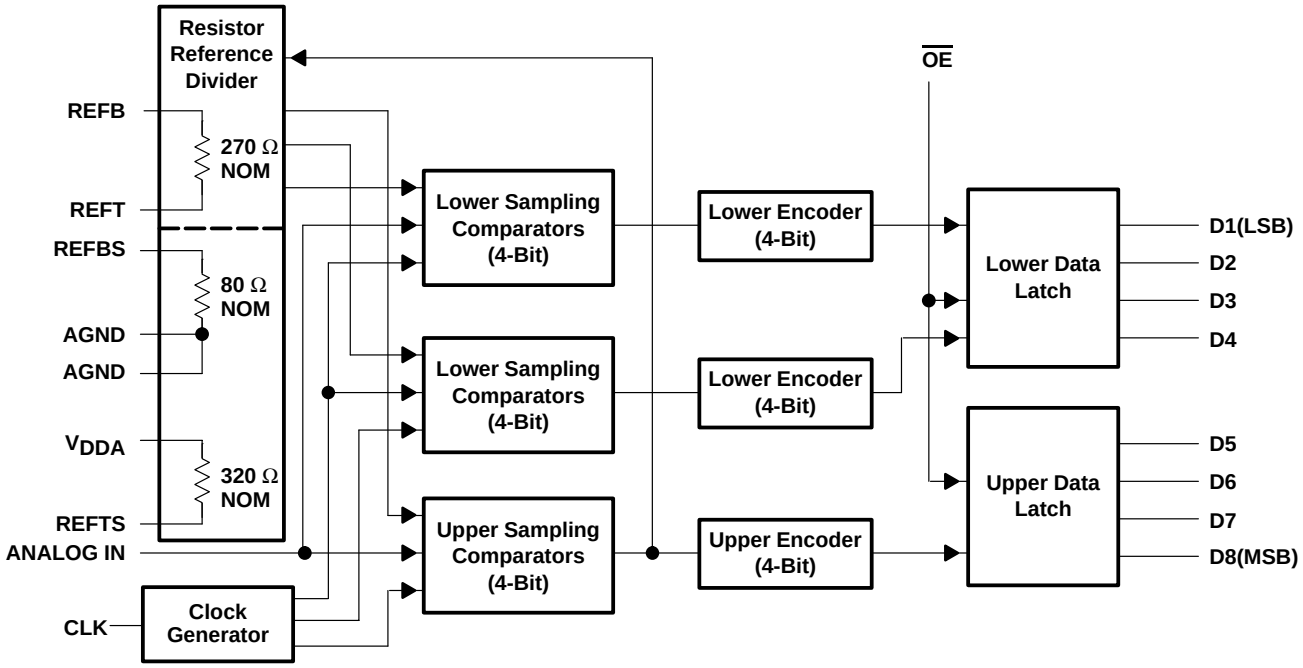
The TLC5510 uses the three internal reference resistors to create a standard, 2-V, full-scale conversion range using V_{DDA}. Only external jumpers are required to implement this option and eliminates the need for external reference resistors. The TLC5510A uses only the center internal resistor section with an externally applied 4-V reference such that a 4-V input signal can be used. Differential linearity is 0.5 LSB at 25°C and a maximum of 0.75 LSB over the full operating temperature range. Typical dynamic specifications include a differential gain of 1% and differential phase of 0.7 degrees.

The TLC5510 and TLC5510A are characterized for operation from –20°C to 75°C.

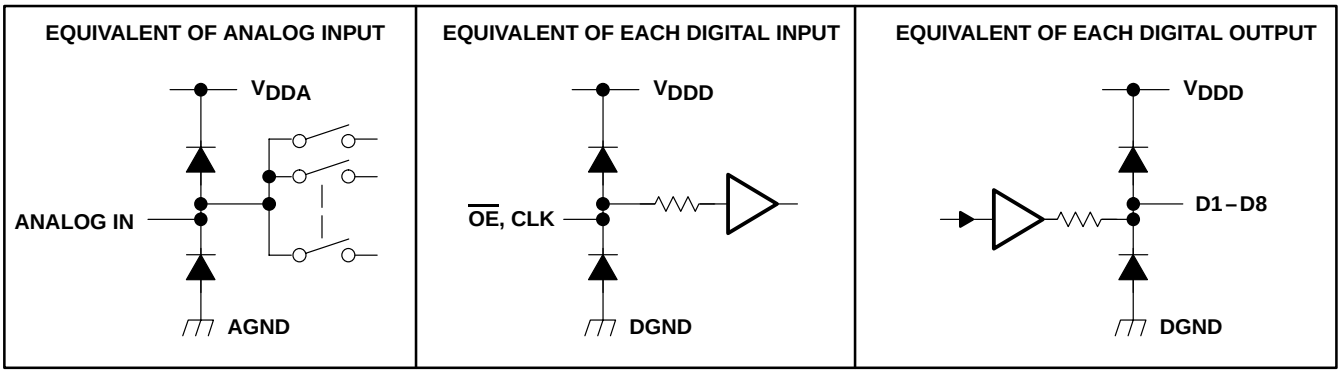
AVAILABLE OPTIONS

T_A	PACKAGE		MAXIMUM FULL-SCALE INPUT VOLTAGE
	TSSOP (PW)	SOP (NS) (TAPE AND REEL ONLY)	
–20°C to 75°C	TLC5510IPW	TLC5510INSLE	2 V
	–	TLC5510AINSLE	4 V

functional block diagram



schematics of inputs and outputs



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AGND	20, 21		Analog ground
ANALOG IN	19	I	Analog input
CLK	12	I	Clock input
DGND	2, 24		Digital ground
D1–D8	3–10	O	Digital data out. D1 = LSB, D8 = MSB
$\overline{OE}$	1	I	Output enable. When $\overline{OE}$ = low, data is enabled. When $\overline{OE}$ = high, D1–D8 is in high-impedance state.
V_{DDA}	14, 15, 18		Analog supply voltage
V_{DDD}	11, 13		Digital supply voltage
REFB	23	I	Reference voltage in bottom
REFBS	22		Reference voltage in bottom. When using the TLC5510 internal voltage divider to generate a nominal 2-V reference, REFBS is shorted to REFB (see Figure 3). When using the TLC5510A, REFBS is connected to ground.
REFT	17	I	Reference voltage in top
REFTS	16		Reference voltage in top. When using the TLC5510 internal voltage divider to generate a nominal 2-V reference, REFTS is shorted to REFT (see Figure 3). When using the TLC5510A, REFTS is connected to V_{DDA}.

absolute maximum ratings†

Supply voltage, V_{DDA}, V_{DDD} . . . . . 7 V
Reference voltage input range, V_{REFT}, V_{REFB} . . . . . AGND to V_{DDA}
Analog input voltage range, $V_{I(ANLG)}$ . . . . . AGND to V_{DDA}
Digital input voltage range, $V_{I(DGTL)}$ . . . . . DGND to V_{DDD}
Digital output voltage range, $V_{O(DGTL)}$ . . . . . DGND to V_{DDD}
Operating free-air temperature range, T_A . . . . . –20°C to 75°C
Storage temperature range, T_{stg} . . . . . –55°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage	V_{DDA}–AGND	4.75	5	5.25	V
	V_{DDD}–AGND	4.75	5	5.25	
	AGND–DGND	–100	0	100	mV
Reference input voltage (top), $V_{ref(T)}$‡	TLC5510A	V_{REFB}+2		4	V
Reference input voltage (bottom), $V_{ref(B)}$‡	TLC5510A	0		V_{REFT}–4	V
Analog input voltage range, $V_{I(ANLG)}$		V_{REFB}		V_{REFT}	V
High-level input voltage, V_{IH}		4			V
Low-level input voltage, V_{IL}				1	V
Pulse duration, clock high, $t_{w(H)}$ (see Figure 1)		25			ns
Pulse duration, clock low, $t_{w(L)}$ (see Figure 1)		25			ns

‡ The reference voltage levels for the TLC5510 are derived through an internal resistor divider between V_{DDA} and ground and therefore are not derived from a separate external voltage source (see the electrical characteristics and text). For the 4 V input range of the TLC5510A, the reference voltage is externally applied across the center divider resistor.

electrical characteristics at V_{DD} = 5 V, V_{REFT} = 2.5 V, V_{REFB} = 0.5 V, $f_{(CLK)}$ = 20 MHz, T_A = 25°C (unless otherwise noted)

digital I/O

PARAMETER		TEST CONDITIONS†			MIN	TYP	MAX	UNIT
I_{IH}	High-level input current	V_{DD} = MAX,	$V_{IH} = V_{DD}$				5	µA
I_{IL}	Low-level input current	V_{DD} = MAX,	V_{IL} = 0				5	µA
I_{OH}	High-level output current	$\overline{OE}$ = GND,	V_{DD} = MIN,	$V_{OH} = V_{DD}-0.5$ V	–1.5			mA
I_{OL}	Low-level output current	$\overline{OE}$ = GND,	V_{DD} = MIN,	V_{OL} = 0.4 V	2.5			mA
I_{OZH}	High-level high-impedance-state output leakage current	$\overline{OE} = V_{DD}$,	V_{DD} = MAX	$V_{OH} = V_{DD}$			16	µA
I_{OZL}	Low-level high-impedance-state output leakage current	$\overline{OE} = V_{DD}$,	V_{DD} = MIN	V_{OL} = 0			16	µA

† Conditions marked MIN or MAX are as stated in recommended operating conditions.

power

PARAMETER		TEST CONDITIONS†		MIN	TYP	MAX	UNIT
I_{DD}	Supply current	$f_{(CLK)}$ = 20 MHz, National Television System Committee (NTSC) ramp wave input, reference resistor dissipation is separate			18	27	mA
I_{ref}	Reference voltage current	TLC5510	V_{ref} = REFT – REFB = 2 V	5.2	7.5	10.5	mA
		TLC5510A	V_{ref} = REFT – REFB = 4 V	10.4	15	21	mA

† Conditions marked MIN or MAX are as stated in recommended operating conditions.

static performance

PARAMETER			TEST CONDITIONS†		MIN	TYP	MAX	UNIT
	Self-bias (1), at REFB		Short REFB to REFBS, Short REFT to REFTS		0.57	0.61	0.65	V
	Self-bias (2), REFT – REFB				1.9	2.02	2.15	V
	Self-bias (3), at REFT		Short REFB to AGND, Short REFT to REFTS		2.18	2.29	2.4	V
R_{ref}	Reference voltage resistor		Between REFT and REFB		190	270	350	Ω
C_i	Analog input capacitance		$V_{I(ANLG)}$ = 1.5 V + 0.07 V_{rms}			16		pF
	Integral nonlinearity (INL)	TLC5510	$f_{(CLK)}$ = 20 MHz, V_I = 0.5 V to 2.5 V	T_A = 25°C		±0.4	±0.75	LSB
				T_A = –20°C to 75°C			±1	LSB
		TLC5510A	$f_{(CLK)}$ = 20 MHz, V_I = 0 to 4 V	T_A = 25°C		±0.4	±0.75	LSB
				T_A = –20°C to 75°C			±1	LSB
	Differential nonlinearity (DNL)	TLC5510	$f_{(CLK)}$ = 20 MHz, V_I = 0.5 V to 2.5 V	T_A = 25°C		±0.3	±0.5	LSB
				T_A = –20°C to 75°C			±0.75	LSB
		TLC5510A	$f_{(CLK)}$ = 20 MHz, V_I = 0 to 4 V	T_A = 25°C		±0.3	±0.5	LSB
				T_A = –20°C to 75°C			±0.75	LSB
E_{ZS}	Zero-scale error	TLC5510	V_{ref} = REFT – REFB = 2 V		–18	–43	–68	mV
		TLC5510A	V_{ref}= REFT – REFB = 4 V		–36	–86	–136	mV
E_{FS}	Full-scale error	TLC5510	V_{ref} = REFT – REFB = 2 V		–20	0	20	mV
		TLC5510A	V_{ref} = REFT – REFB = 4 V		–40	0	40	mV

† Conditions marked MIN or MAX are as stated in recommended operating conditions.

operating characteristics at V_{DD} = 5 V, V_{REFT} = 2.5 V, V_{REFB} = 0.5 V, $f_{(CLK)}$ = 20 MHz, T_A = 25°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{conv}	Maximum conversion rate	TLC5510	f_I = 1-kHz ramp	$V_{I(ANLG)}$ = 0.5 V – 2.5 V			20	MSPS
		TLC5510A		$V_{I(ANLG)}$ = 0 V – 4 V			20	MSPS
BW	Analog input bandwidth		At – 1 dB			14		MHz
$t_{d(D)}$	Digital output delay time		C_L ≤ 10 pF (see Note 1 and Figure 1)			18	30	ns
	Differential gain		NTSC 40 Institute of Radio Engineers (IRE) modulation wave, f_{conv} = 14.3 MSPS			1%		
	Differential phase					0.7		degrees
t_{AJ}	Aperture jitter time					30		ps
$t_{d(s)}$	Sampling delay time					4		ns
t_{en}	Enable time, $\overline{OE}\downarrow$ to valid data		C_L = 10 pF			5		ns
t_{dis}	Disable time, $\overline{OE}\uparrow$ to high impedance		C_L = 10 pF			7		ns
	Spurious free dynamic range (SFDR)		Input tone = 1 MHz	T_A = 25°C		45		dB
				Full range		43		
			Input tone = 3 MHz	T_A = 25°C		45		
				Full range		46		
			Input tone = 6 MHz	T_A = 25°C		43		
				Full range		42		
			Input tone = 10 MHz	T_A = 25°C		39		
				Full range		39		
SNR	Signal-to-noise ratio		T_A = 25°C			46		dB
			Full range			44		

NOTE 1: C_L includes probe and jig capacitance.

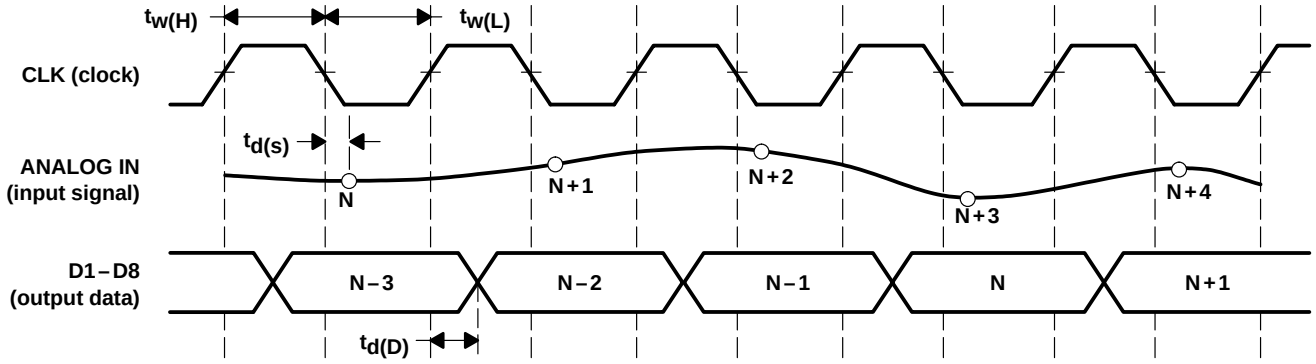


Figure 1. I/O Timing Diagram

PRINCIPLES OF OPERATION

functional description

The TLC5510 and TLC5510A are semiflash ADCs featuring two lower comparator blocks of four bits each.

As shown in Figure 2, input voltage $V_I(1)$ is sampled with the falling edge of CLK1 to the upper comparators block and the lower comparators block(A), S(1). The upper comparators block finalizes the upper data UD(1) with the rising edge of CLK2, and simultaneously, the lower reference voltage generates the voltage RV(1) corresponding to the upper data. The lower comparators block (A) finalizes the lower data LD(1) with the rising edge of CLK3. UD(1) and LD(1) are combined and output as OUT(1) with the rising edge of CLK4. As shown in Figure 2, the output data is delayed 2.5 clocks from the analog input voltage sampling point.

Input voltage $V_I(2)$ is sampled with the falling edge of CLK2. UD(2) is finalized with the rising edge of CLK3, and LD(2) is finalized with the rising edge of CLK4 at the lower comparators block(B). OUT(2) data appears with the rising edge of CLK5.

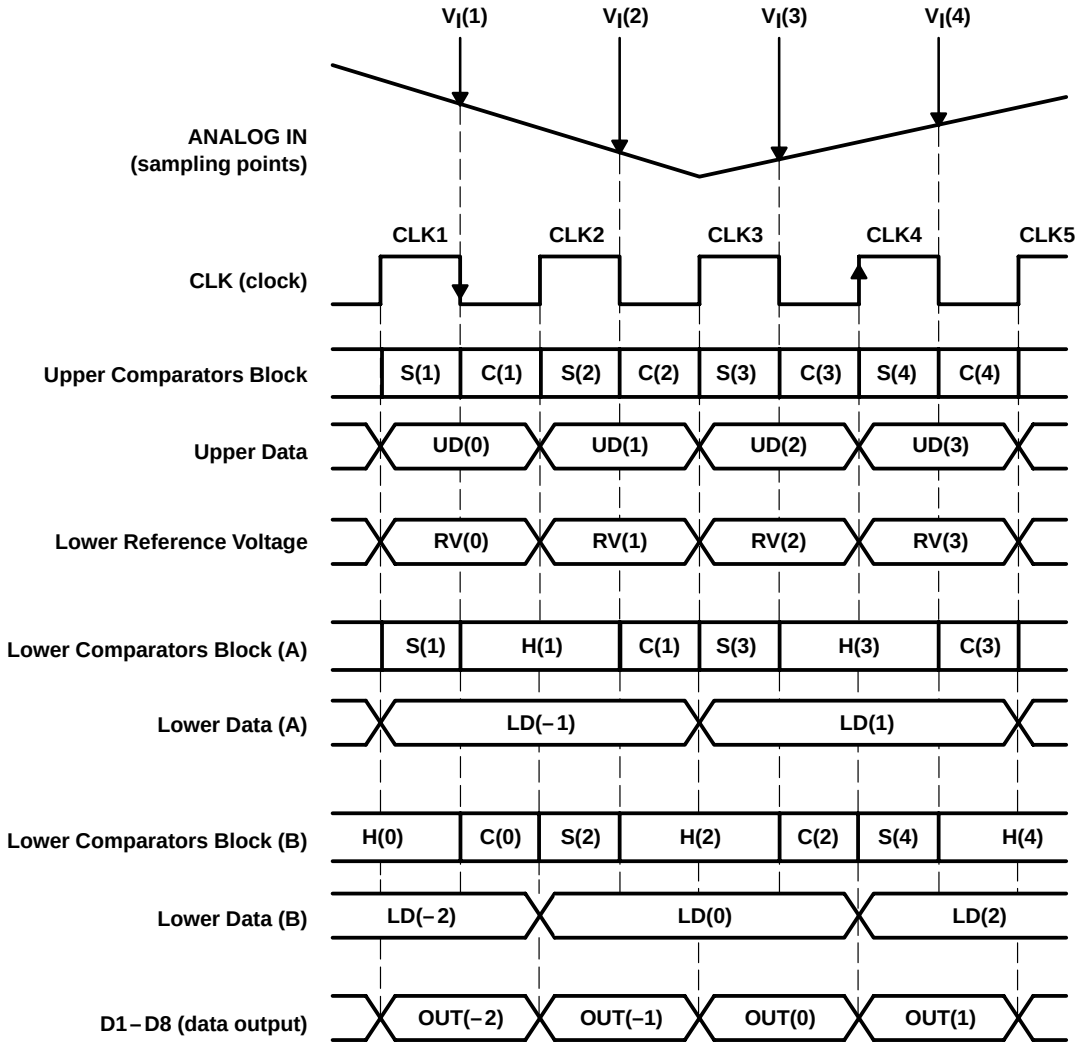


Figure 2. Internal Functional Timing Diagram

PRINCIPLES OF OPERATION

internal referencing

TLC5510

The three internal resistors shown with V_{DDA} can generate a 2-V reference voltage. These resistors are brought out on V_{DDA}, REFTS, REFT, REFB, REFBS, and AGND.

To use the internally generated reference voltage, terminal connections should be made as shown in Figure 3. This connection provides the standard video 2-V reference for the nominal digital output.

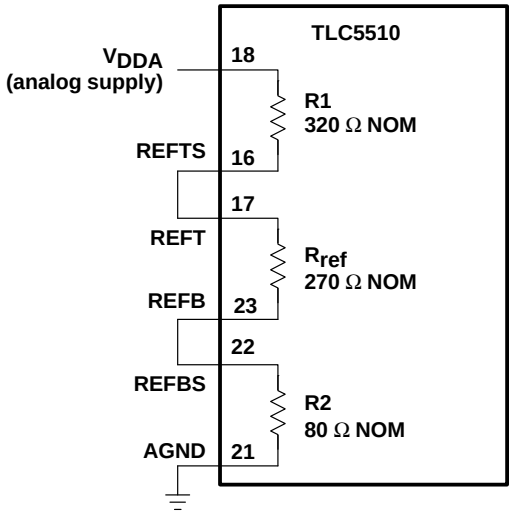


Figure 3. External Connections for a 2-V Analog Input Span Using the Internal-Reference Resistor Divider

TLC5510A

For an analog input span of 4 V, 4 V is supplied to REFT, and REFB is grounded and terminal connections should be made as shown in Figure 4. This connection provides the 4-V reference for the nominal zero to full-scale digital output with a 4 V_{pp} analog input at ANALOG IN.

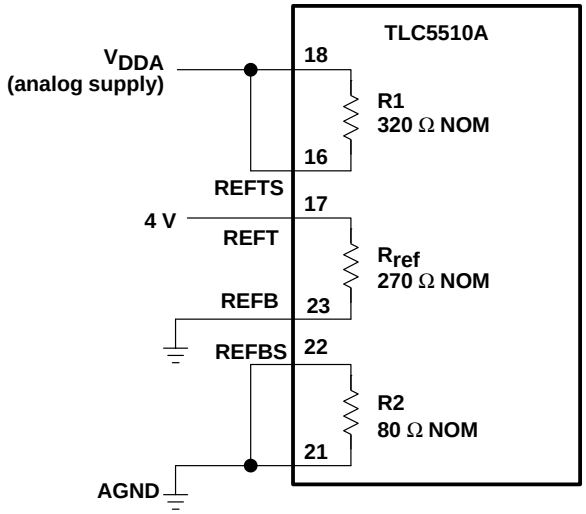


Figure 4. External Connections for 4-V Analog Input Span

PRINCIPLES OF OPERATION

functional operation

The output code change with input voltage is shown in Table 1.

Table 1. Functional Operation

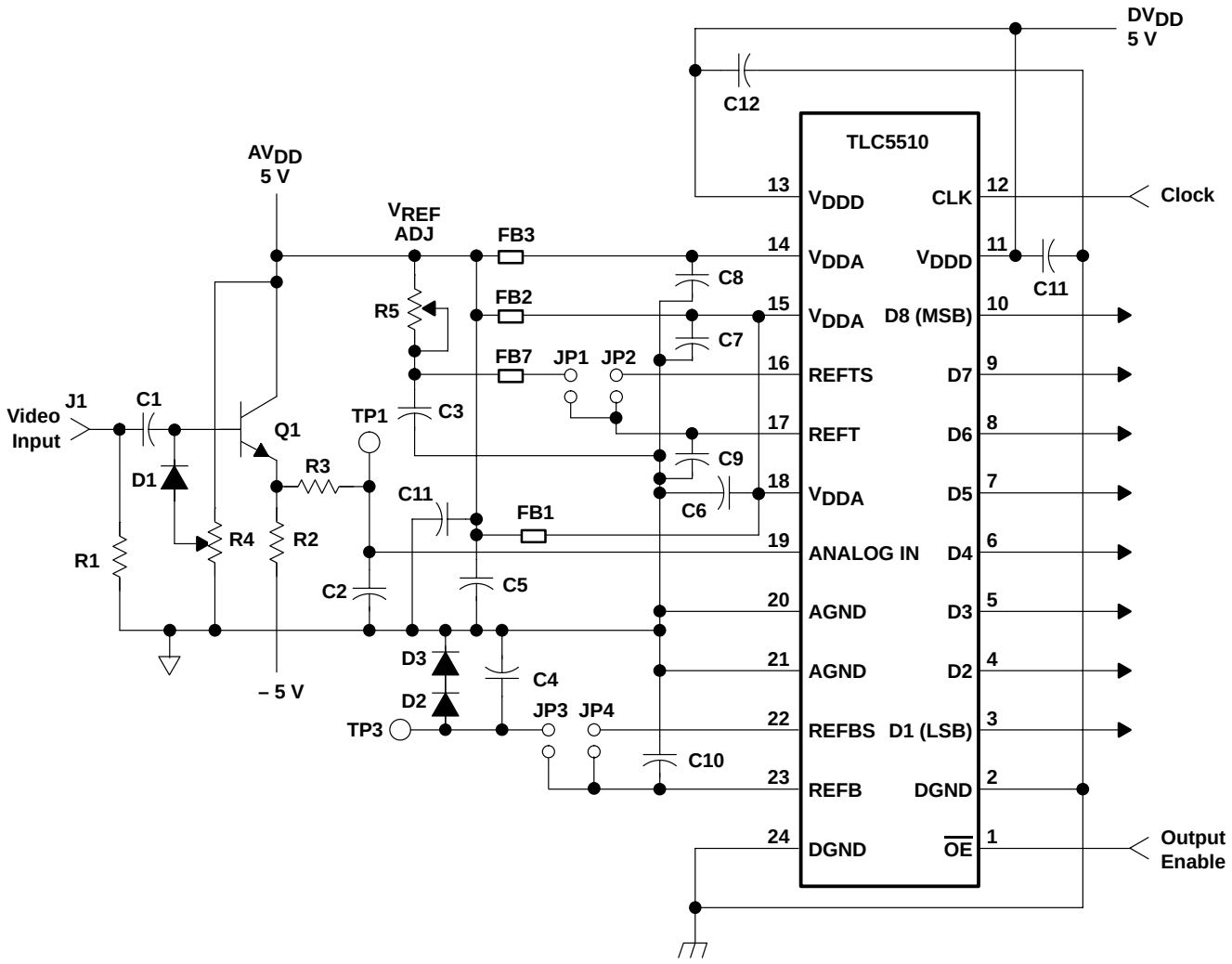
INPUT SIGNAL VOLTAGE	STEP	DIGITAL OUTPUT CODE							
		MSB							LSB
$V_{ref(B)}$	255	0	0	0	0	0	0	0	0
•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•
•	128	0	1	1	1	1	1	1	1
•	127	1	0	0	0	0	0	0	0
•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•
$V_{ref(T)}$	0	1	1	1	1	1	1	1	1

APPLICATION INFORMATION

The following notes are design recommendations that should be used with the device.

- External analog and digital circuitry should be physically separated and shielded as much as possible to reduce system noise.
- RF breadboarding or printed-circuit-board (PCB) techniques should be used throughout the evaluation and production process. Breadboards should be copper clad for bench evaluation.
- Since AGND and DGND are connected internally, the ground lead in must be kept as noise free as possible. A good method to use is twisted-pair cables for the supply lines to minimize noise pickup. An analog and digital ground plane should be used on PCB layouts when additional logic devices are used. The AGND and DGND terminals of the device should be tied to the analog ground plane.
- V_{DDA} to AGND and V_{DDD} to DGND should be decoupled with 1-μF and 0.01-μF capacitors, respectively, and placed as close as possible to the affected device terminals. A ceramic-chip capacitor is recommended for the 0.01-μF capacitor. Care should be exercised to ensure a solid noise-free ground connection for the analog and digital ground terminals.
- V_{DDA}, AGND, and ANALOG IN should be shielded from the higher frequency terminals, CLK and D0–D7. When possible, AGND traces should be placed on both sides of the ANALOG IN traces on the PCB for shielding.
- In testing or application of the device, the resistance of the driving source connected to the analog input should be 10 Ω or less within the analog frequency range of interest.

APPLICATION INFORMATION

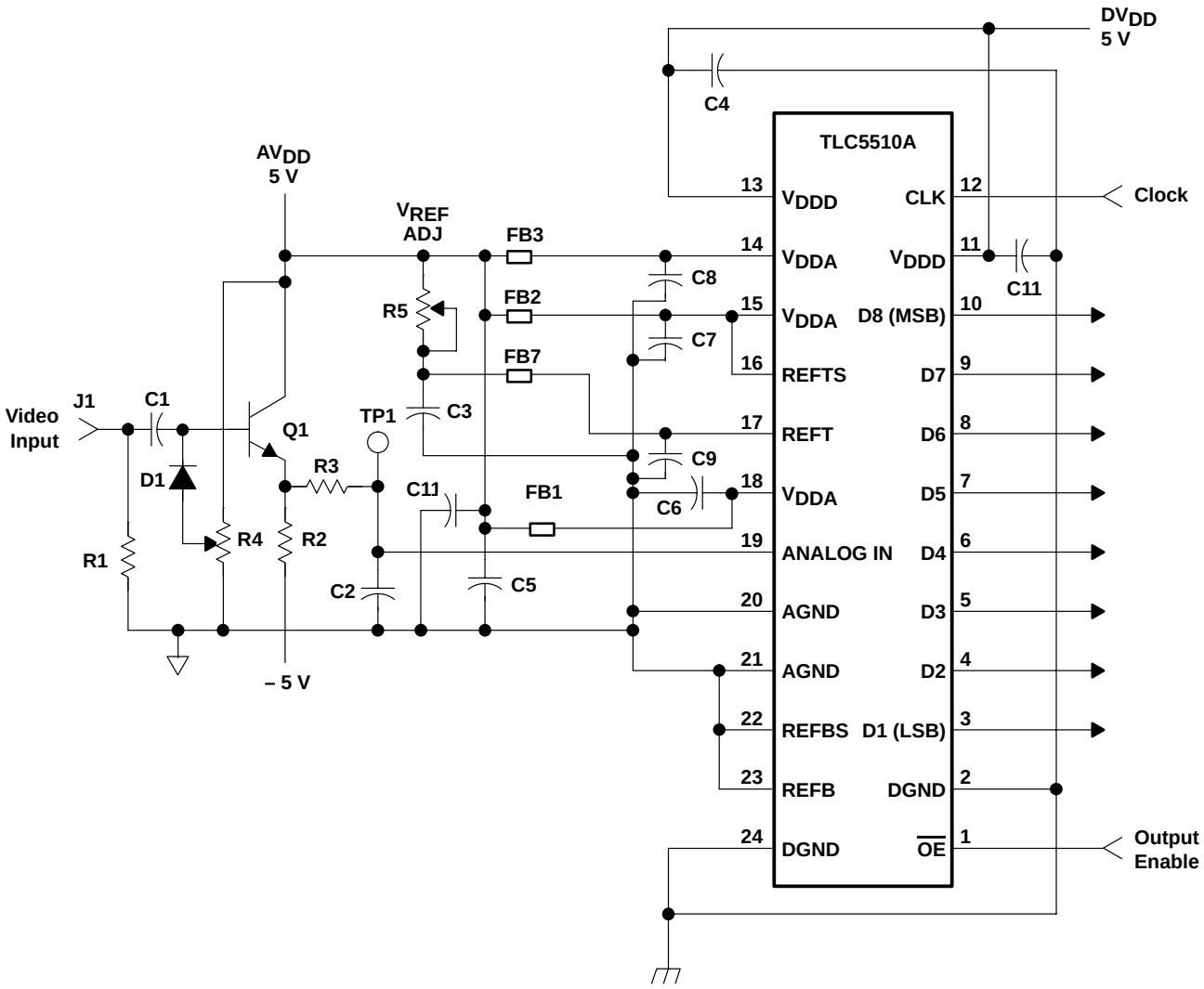


NOTE A: Shorting JP1 and JP3 allows adjustment of the reference voltage by R5 using temperature-compensating diodes D2 and D3 which compensate for D1 and Q1 variations. By shorting JP2 and JP4, the internal divider generates a nominal 2-V reference.

LOCATION	DESCRIPTION
C1, C3–C4, C6–C12	0.1-µF capacitor
C2	10-pF capacitor
C5	47-µF capacitor
FB1, FB2, FB3, FB7	Ferrite bead
Q1	2N3414 or equivalent
R1, R3	75-Ω resistor
R2	500-Ω resistor
R4	10-kΩ resistor, clamp voltage adjust
R5	300-Ω resistor, reference-voltage fine adjust

Figure 5. TLC5510 Evaluation and Test Schematic

APPLICATION INFORMATION

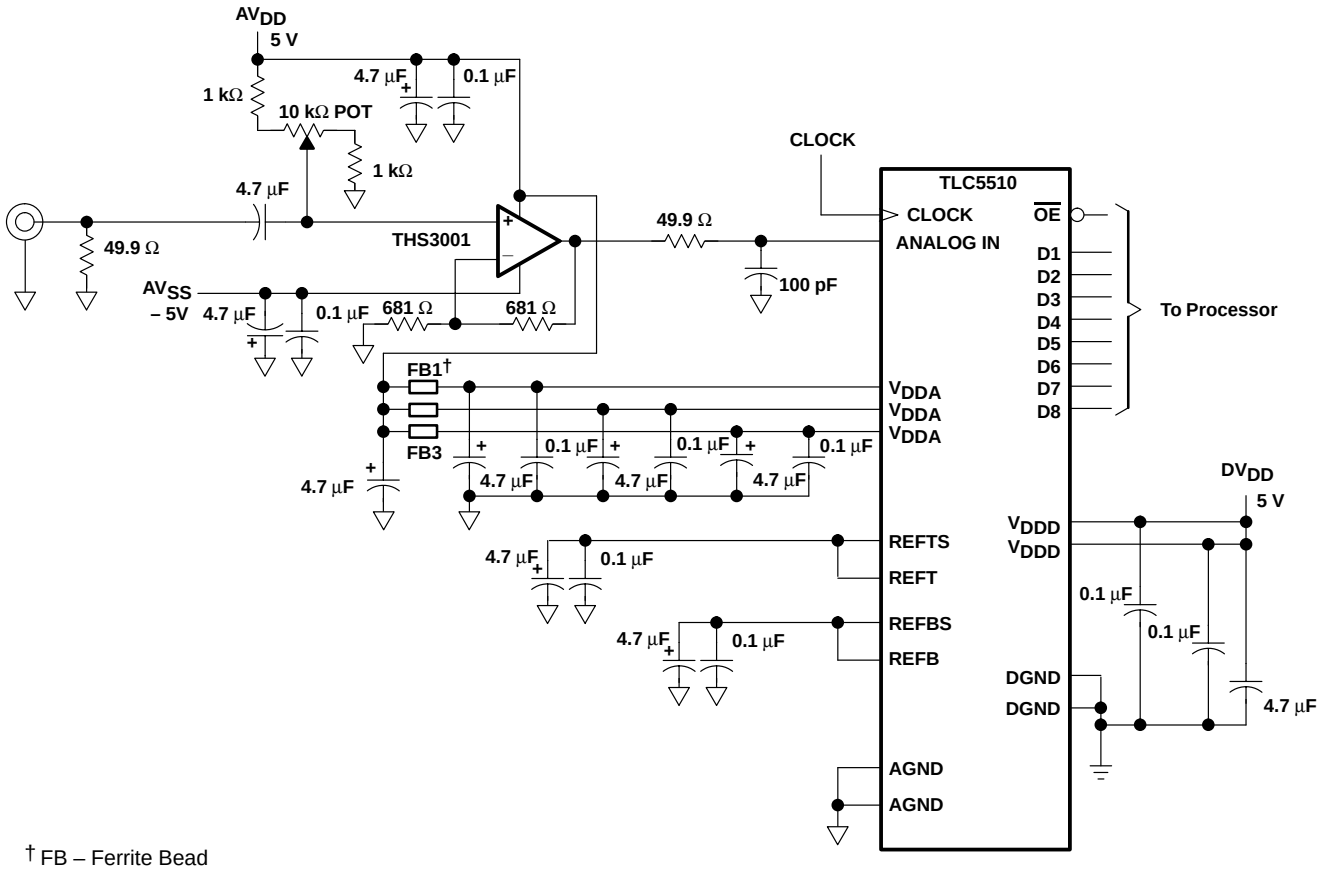


NOTE A: R5 allows adjustment of the reference voltage to 4 V. R4 adjusts for the desired Q1 quiescent operating point.

LOCATION	DESCRIPTION
C1, C3 – C4, C6 – C11	0.1-μF capacitor
C2	10-pF capacitor
C5	47-μF capacitor
FB1, FB2, FB3, FB7	Ferrite bead
Q1	2N3414 or equivalent
R1, R3	75-Ω resistor
R2	500-Ω resistor
R4	10-kΩ resistor, clamp voltage adjust
R5	300-Ω resistor, reference-voltage fine adjust

Figure 6. TLC5510A Evaluation and Test Schematic

APPLICATION INFORMATION



† FB – Ferrite Bead

Figure 7. TLC5510 Application Schematic

APPLICATION INFORMATION

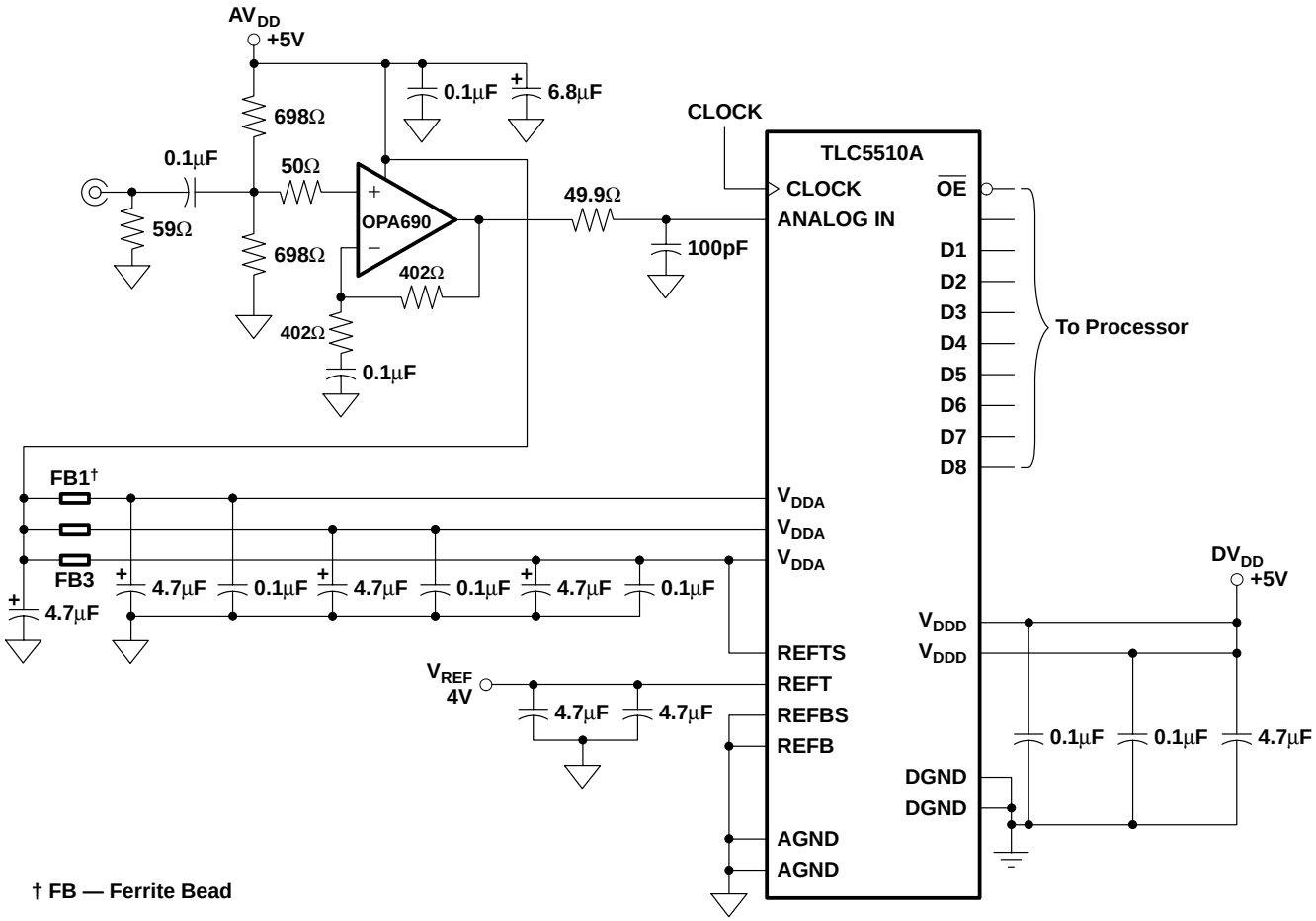


Figure 8. TLC5510A Application Schematic

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLC5510AINS	ACTIVE	SO	NS	24	34	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-20 to 75	TLC5510AI	Samples
TLC5510AINSR	ACTIVE	SO	NS	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-20 to 75	TLC5510AI	Samples
TLC5510INS	ACTIVE	SO	NS	24	34	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-20 to 75	TLC5510I	Samples
TLC5510INSR	ACTIVE	SO	NS	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-20 to 75	TLC5510I	Samples
TLC5510IPW	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-20 to 75	Y5510	Samples
TLC5510IPWR	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-20 to 75	Y5510	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

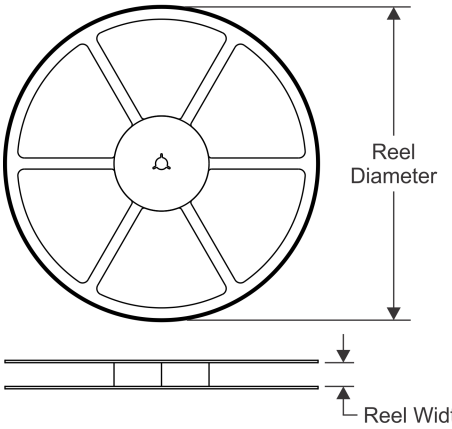
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

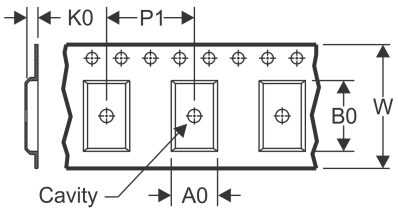
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

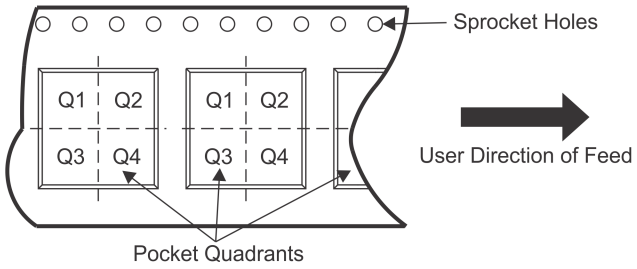


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

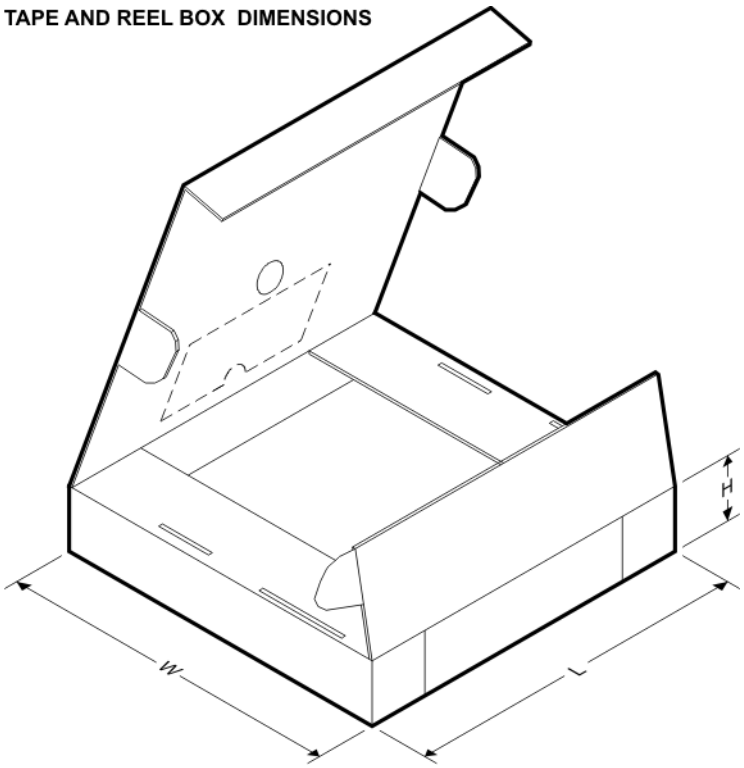
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC5510AINSR	SO	NS	24	2000	330.0	24.4	8.5	15.3	2.6	12.0	24.0	Q1
TLC5510INSR	SO	NS	24	2000	330.0	24.4	8.5	15.3	2.6	12.0	24.0	Q1
TLC5510IPWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



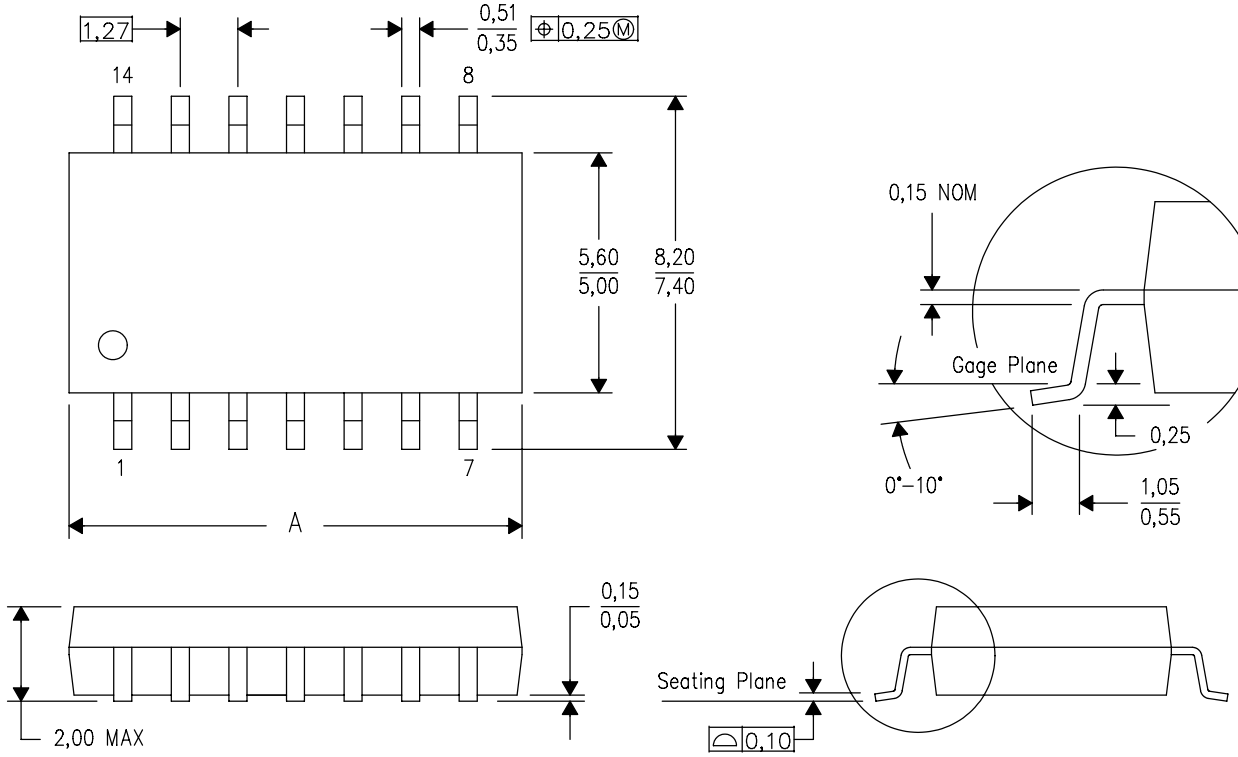
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC5510AINSR	SO	NS	24	2000	367.0	367.0	45.0
TLC5510INSR	SO	NS	24	2000	367.0	367.0	45.0
TLC5510IPWR	TSSOP	PW	24	2000	367.0	367.0	38.0

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN

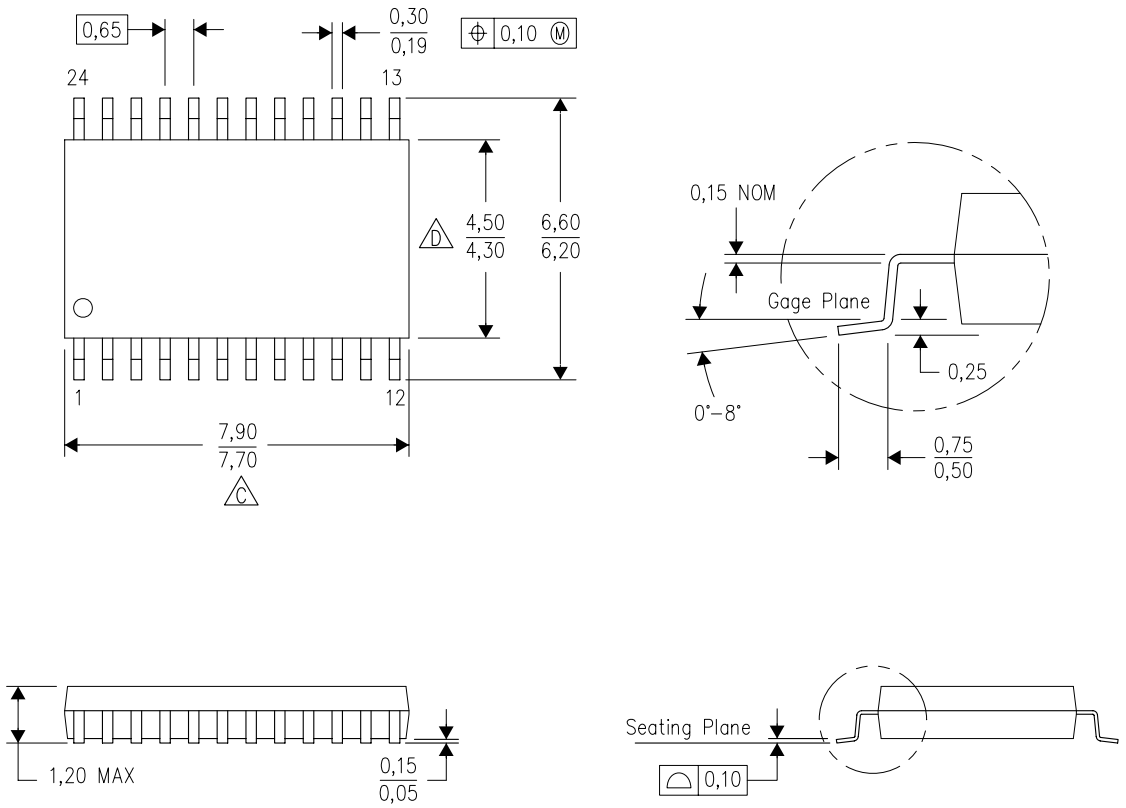


DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

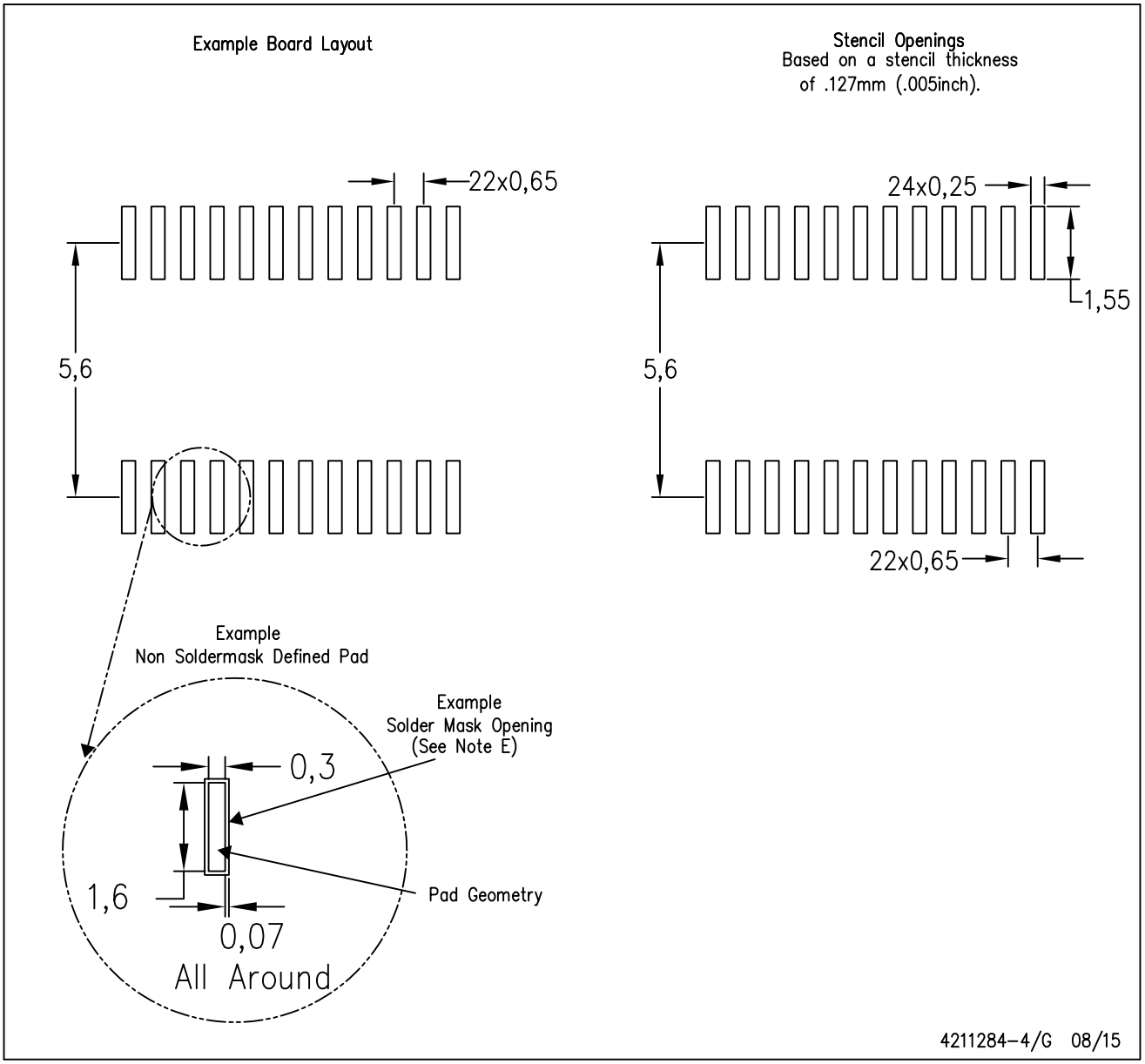
PW (R–PDSO–G24) PLASTIC SMALL OUTLINE



4040064–6/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G24) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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