24-Channel, Constant-Current LED Driver with Global Brightness Control and LED Open-Short Detection

FEATURES

- 24-Channel Constant-Current Sink Output with On/Off Control
- Current Capability:
  - 35 mA for 16 Channels
  - 26.2 mA for 8 Channels
- Global Brightness Control (BC) for Each Color Group: 7-Bit (128 Step), Three Groups
- LED Power-Supply Voltage up to 15 V
- V_{CC} = 3.0 V to 5.5 V
- Constant-Current Accuracy:
  - Channel-to-Channel = ±1%
  - Device-to-Device = ±3%
- CMOS Logic Level I/O
- Data Transfer Rate: 35 MHz
- BLANK Pulse Width: 15 ns
- Open Load, Short Load, and Over-Temperature Detection
- Thermal Shutdown (TSD) with Auto Restart
- Delay Switching to Prevent Inrush Current
- Operating Temperature: –40°C to +85°C
- Packages: HTSSOP-32, QFN-32

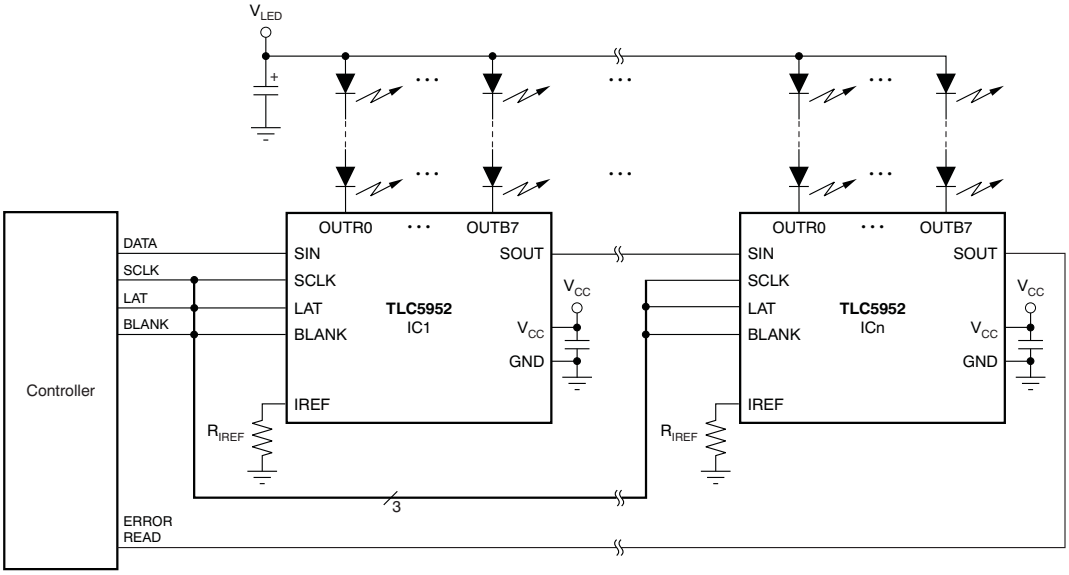
APPLICATIONS

- Full-Color LED Displays
- LED Signboards

DESCRIPTION

The TLC5952 is a 24-channel, constant-current sink driver. Each channel can be turned on/off with internal register data. The output channels are grouped into three groups of eight channels each. Each channel group has a 128-step global brightness control (BC) function. Both on/off data and BC are writable via a serial interface. The maximum current value of all 24 channels is set by a single external resistor.

The TLC5952 has three error detection circuits: LED open detection (LOD), LED short detection (LSD), and a thermal error flag (TEF). The error detection is read via a serial interface.



Typical Application Circuit (Multiple Daisy-Chained TLC5952s)

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
TLC5952	HTSSOP-32 PowerPAD™	TLC5952DAPR	Tape and Reel, 2000
		TLC5952DAP	Tube, 46
TLC5952	5-mm × 5-mm QFN-32(2)	TLC5952RHBR	Tape and Reel, 3000
		TLC5952RHBT	Tape and Reel, 250

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Product preview device.

ABSOLUTE MAXIMUM RATINGS(1)(2)

Over operating free-air temperature range, unless otherwise noted.

PARAMETER			TLC5952	UNIT
V_{CC}	Supply voltage	V_{CC}	–0.3 to +6.0	V
I_{OUT}	Output current (dc)	OUTR0-OUTR7, OUTG0-OUTG7	45	mA
		OUTB0-OUTB7	35	mA
V_{IN}	Input voltage range	SIN, SCLK, LAT, BLANK, IREF	–0.3 to V_{CC} + 0.3	V
V_{OUT}	Output voltage range	SOUT	–0.3 to V_{CC} + 0.3	V
		OUTR0-OUTR7, OUTG0-OUTG7, OUTB0-OUTB7	–0.3 to +16	V
$T_{J(max)}$	Operation junction temperature		+150	°C
T_{STG}	Storage temperature range		–55 to +150	°C
ESD rating		Human body model (HBM)	2000	V
		Charged device model (CDM)	500	V

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

DISSIPATION RATINGS

PACKAGE	DERATING FACTOR ABOVE T_A = +25°C	T_A < +25°C POWER RATING	T_A = +70°C POWER RATING	T_A = +85°C POWER RATING
HTSSOP-32 with PowerPAD soldered(1)	42.54 mW/°C	5318 mW	3403 mW	2765 mW
HTSSOP-32 with PowerPAD not soldered(2)	22.56 mW/°C	2820 mW	1805 mW	1466 mW
QFN-32(3)	27.86 mW/°C	3482 mW	2228 mW	1811 mW

(1) With PowerPAD soldered onto copper area on printed circuit board (PCB); 2-oz. copper. For more information, see SLMA002 (available for download at www.ti.com).
(2) With PowerPAD not soldered onto copper area on PCB.
(3) The package thermal impedance is calculated in accordance with JESD51-5.

RECOMMENDED OPERATING CONDITIONS

At T_A = –40°C to +85°C, unless otherwise noted.

PARAMETER			TLC5952 MIN	TLC5952 NOM	TLC5952 MAX	UNIT
DC CHARACTERISTICS: V_{CC} = 3 V to 5.5 V						
V_{CC}	Supply voltage		3.0		5.5	V
V_O	Voltage applied to output	OUTR0-OUTR7, OUTG0-OUTG7, OUTB0-OUTB7			15	V
V_{IH}	High level input voltage	SIN, SCLK, LAT, BLANK	0.7 × V_{CC}		V_{CC}	V
V_{IL}	Low level input voltage	SIN, SCLK, LAT, BLANK	GND		0.3 × V_{CC}	V
I_{OH}	High level output current	SOUT			–1	mA
I_{OL}	Low level output current	SOUT			1	mA
I_{OLC}	Constant output sink current	OUTR0-OUTR7, OUTG0-OUTG7			35	mA
		OUTB0-OUTB7			26.2	mA
T_A	Operating free-air temperature		–40		+85	°C
T_J	Operating junction temperature		–40		+125	°C
AC CHARACTERISTICS, V_{CC} = 3 V to 5.5 V						
$f_{CLK\ (SCLK)}$	Data shift clock frequency	SCLK			35	MHz
T_{WH0}	Pulse duration	SCLK	10			ns
T_{WL0}		SCLK	10			ns
T_{WH1}		LAT	15			ns
T_{WH2}		BLANK	15			ns
T_{WL2}		BLANK	15			ns
T_{SU0}	Setup time	SIN – SCLK↑	4			ns
T_{SU1}		LAT↑ – SCLK↑	150			ns
T_{H0}	Hold time	SIN – SCLK↑	3			ns
T_{H1}		LAT↑ – SCLK↑	10			ns

ELECTRICAL CHARACTERISTICS

At T_A = –40°C to +85°C, V_{CC} = 3 V to 5.5 V, and V_{LED} = 5 V, unless otherwise noted. Typical values are at T_A = +25°C and V_{CC} = 3.3 V.

PARAMETER		TEST CONDITIONS	TLC5952			UNIT
			MIN	TYP	MAX	
V_{OH}	High level output voltage	I_{OH} = –1 mA at SOUT	V_{CC} – 0.4		V_{CC}	V
V_{OL}	Low level output voltage	I_{OL} = 1 mA at SOUT			0.4	V
I_{IN}	Input current	V_I = V_{CC} or GND at SIN, SCLK, LAT, and BLANK	–1		1	µA
I_{CC1}	Supply current	SIN, SCLK, LAT = low, BLANK = high, $V_{OUTRn/Gn/Bn}$ = 1 V, BCR/G/B = 7Fh, R_{IREF} = 24 kΩ ($I_{OUTRn/Gn}$ = 2 mA target, I_{OUTBn} = 1.5 mA target)		1	3	mA
I_{CC2}		SIN, SCLK, LAT = low, BLANK = high, $V_{OUTRn/Gn/Bn}$ = 1 V, BCR/G/B = 7Fh, R_{IREF} = 2.4 kΩ ($I_{OUTRn/Gn}$ = 20 mA target, I_{OUTBn} = 15 mA target)		8	14	mA
I_{CC3}		SIN, SCLK, LAT = low, BLANK = low, all OUTRn/Gn/Bn = on, $V_{OUTRn/Gn/Bn}$ = 1 V, BCR/G/B = 7Fh, R_{IREF} = 2.4 kΩ ($I_{OUTRn/Gn}$ = 20 mA target, I_{OUTBn} = 15 mA target)		12	30	mA
I_{CC4}		SIN, SCLK, LAT = low, BLANK = low, all OUTRn/Gn/Bn = on, $V_{OUTRn/Gn/Bn}$ = 1 V, BCR/G/B = 7Fh, R_{IREF} = 1.5 kΩ ($I_{OUTRn/Gn}$ = 32 mA target, I_{OUTBn} = 24 mA target)		20	50	mA
I_{OLC}	Constant output current	At OUTR0-OUTR7 and OUTG0-OUTG7, All OUTRn/Gn/Bn = on, BCR/G/B = 7Fh, $V_{OUTRn/Gn/Bn}$ = V_{OUTfix} = 1 V, R_{IREF} = 1.5 kΩ ($I_{OUTRn/Gn}$ = 32 mA target)	29	32	35	mA
I_{OLC1}		At OUTB0-OUTB7, All OUTRn/Gn/Bn = on, BCR/G/B = 7Fh, $V_{OUTRn/Gn/Bn}$ = V_{OUTfix} = 1 V, R_{IREF} = 1.5 kΩ (I_{OUTBn} = 24 mA target)	21.8	24	26.2	mA
I_{OLKG}	Leakage output current	At OUTR0-OUTR7, OUTG0-OUTG7, and OUTB0-OUTB7, BLANK = high, $V_{OUTRn/Gn/Bn}$ = V_{OUTfix} = 15 V, R_{IREF} = 1.5 kΩ			0.1	µA
ΔI_{OLC}	Constant-current error(1) (channel-to-channel in same color group)	At OUTR0-OUTR7, OUTG0-OUTG7, and OUTB0-OUTB7, All OUTRn/Gn/Bn = on, BCR/G/B = 7Fh, $V_{OUTRn/Gn/Bn}$ = V_{OUTfix} = 1 V, R_{IREF} = 1.5 kΩ ($I_{OUTRn/Gn}$ = 32 mA target, I_{OUTBn} = 24 mA target), at same color group output		±1	±3	%
ΔI_{OLC1}	Constant current error(2) (device to device in same color group)	At OUTR0-OUTR7, OUTG0-OUTG7, and OUTB0-OUTB7, All OUTRn/Gn/Bn = on, BCR/G/B = 7Fh, $V_{OUTRn/Gn/Bn}$ = V_{OUTfix} = 1 V, R_{IREF} = 1.5 kΩ ($I_{OUTRn/Gn}$ = 32 mA target, I_{OUTBn} = 24 mA target), at same color group output		±3	±6	%

(1) The deviation of each output in the same color group from the average of the same color group (OUTR0-OUTR7, OUTG0-OUTG7, or OUTB0-OUTB7) constant current. The deviation is calculated by the formula (X = R, G, or B; n = 0-7):

$$\Delta\,(\%) = \left(\frac{I_{OUTXn}}{\frac{(I_{OUTX0} + I_{OUTX1} + \ldots + I_{OUTX6} + I_{OUTX7})}{8}} - 1 \right) \times 100$$

(2) The deviation of the constant-current average of each color group from the ideal constant-current value. The deviation is calculated by the formula (X = R, G, or B):

$$\Delta\,(\%) = \left(\frac{\frac{(I_{OUTX0} + I_{OUTX1} + \ldots + I_{OUTX7})}{8} - (\text{Ideal Output Current})}{\text{Ideal Output Current}} \right) \times 100$$

Ideal current is calculated by the following equation for OUTR0-OUTR7 and OUTG0-OUTG7 (X = R, G, or B):

$$I_{OUTRn/Gn(IDEAL,\,mA)} = 40 \times \left(\frac{1.20}{R_{IREF}\,(\Omega)} \right)$$

Ideal current is calculated by the following equation for OUTR0-OUTR7 and OUTG0-OUTG7 (X = R, G, or B):

$$I_{OUTBn(IDEAL,\,mA)} = 30 \times \left(\frac{1.20}{R_{IREF}\,(\Omega)} \right)$$

ELECTRICAL CHARACTERISTICS (continued)

At T_A = –40°C to +85°C, V_{CC} = 3 V to 5.5 V, and V_{LED} = 5 V, unless otherwise noted. Typical values are at T_A = +25°C and V_{CC} = 3.3 V.

PARAMETER		TEST CONDITIONS	TLC5952			UNIT
			MIN	TYP	MAX	
ΔI_{OLC2}	Line regulation(3)	At OUTR0-OUTR7, OUTG0-OUTG7, and OUTB0-OUTB7, All OUTRn/Gn/Bn = on, BCR/G/B = 7Fh, $V_{OUTRn/Gn/Bn}$ = V_{OUTfix} = 1 V, R_{IREF} = 1.5 kΩ		±0.5	±1	%
ΔI_{OLC3}	Load regulation(4)	At OUTR0-OUTR7, OUTG0-OUTG7, and OUTB0-OUTB7, All OUTRn/Gn/Bn = on, BCR/G/B = 7Fh, $V_{OUTRn/Gn/Bn}$ = 1 V to 3 V, V_{OUTfix} = 1 V, R_{IREF} = 1.5 kΩ		±1	±3	%/V
T_{TEF}	Thermal error flag threshold	Junction temperature(5)	+150	+165	+180	°C
T_{HYS}	Thermal error flag hysteresis	Junction temperature(5)	5	10	20	°C
V_{LOD0}	LED open detection threshold	All OUTRn/Gn/Bn = on, detection voltage select code = 0h	0.25	0.30	0.35	V
V_{LOD1}		All OUTRn/Gn/Bn = on, detection voltage select code = 1h	0.50	0.60	0.70	V
V_{LOD2}		All OUTRn/Gn/Bn = on, detection voltage select code = 2h	0.80	0.90	1.00	V
V_{LOD3}		All OUTRn/Gn/Bn = on, detection voltage select code = 3h	1.10	1.20	1.30	V
V_{LSD0}	LED short detection threshold	All OUTRn/Gn/Bn = on, detection voltage select code = 4h	0.55 × V_{CC}	0.60 × V_{CC}	0.65 × V_{CC}	V
V_{LSD1}		All OUTRn/Gn/Bn = on, detection voltage select code = 5h	0.65 × V_{CC}	0.70 × V_{CC}	0.75 × V_{CC}	V
V_{LSD2}		All OUTRn/Gn/Bn = on, detection voltage select code = 6h	0.75 × V_{CC}	0.80 × V_{CC}	0.85 × V_{CC}	V
V_{LSD3}		All OUTRn/Gn/Bn = on, detection voltage select code = 7h	0.85 × V_{CC}	0.90 × V_{CC}	0.95 × V_{CC}	V
V_{IREF}	Reference voltage output	R_{IREF} = 1.5 kΩ	1.17	1.20	1.23	V

(3) Line regulation is calculated by the following equation (X = R, G, or B; n = 0-7):

$$\Delta\ (\%/V) = \left(\frac{(I_{OUTXn} \text{ at } V_{CC} = 5.5\ V) - (I_{OUTXn} \text{ at } V_{CC} = 3.0\ V)}{(I_{OUTXn} \text{ at } V_{CC} = 3.0\ V)} \right) \times \frac{100}{5.5\ V - 3\ V}$$

(4) Load regulation is calculated by the following equation (X = R, G, or B; n = 0-7):

$$\Delta\ (\%/V) = \left(\frac{(I_{OUTXn} \text{ at } V_{OUTXn} = 3\ V) - (I_{OUTXn} \text{ at } V_{OUTXn} = 1\ V)}{(I_{OUTXn} \text{ at } V_{OUTXn} = 1\ V)} \right) \times \frac{100}{3\ V - 1\ V}$$

(5) Not tested; specified by design.

SWITCHING CHARACTERISTICS

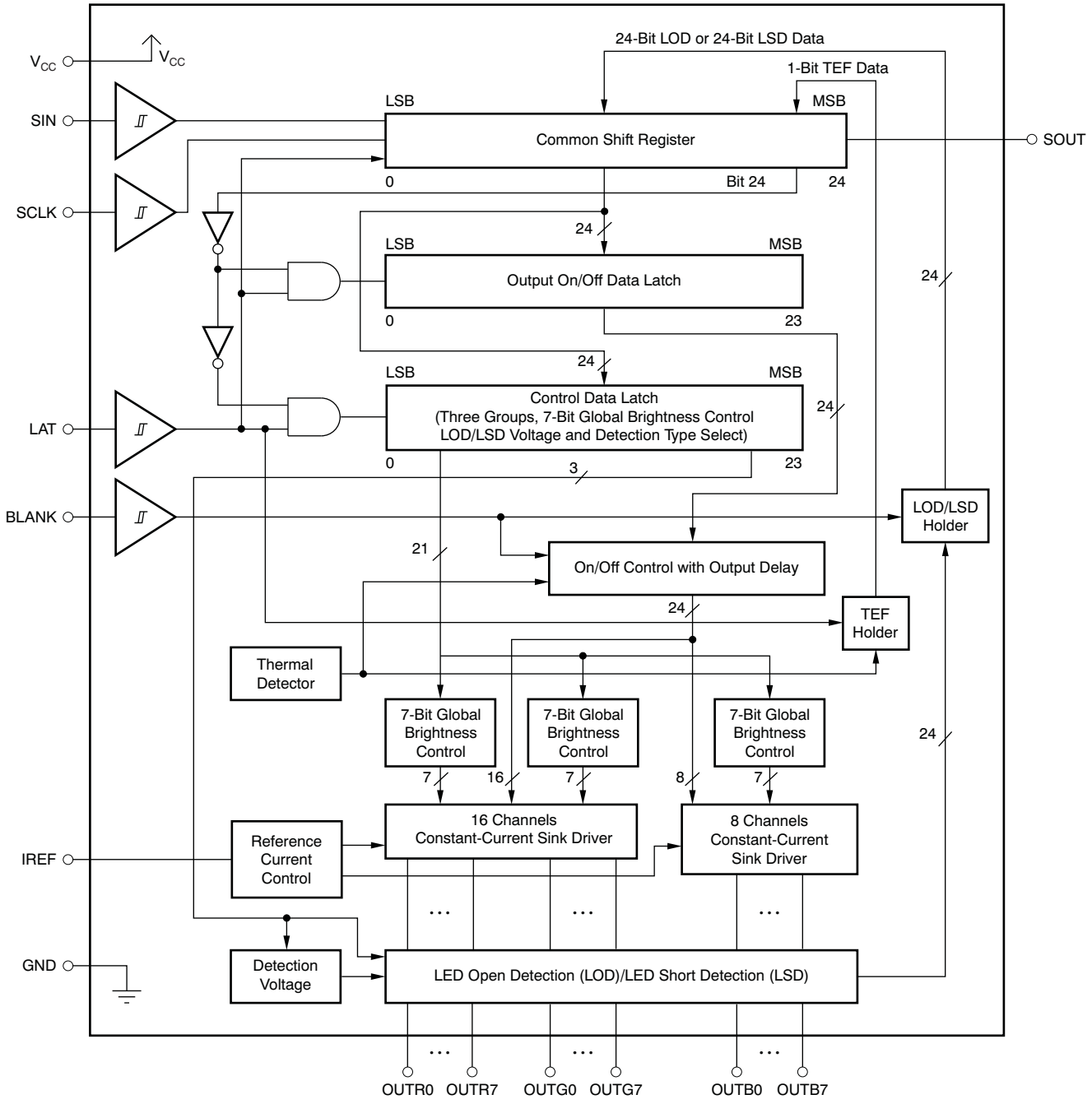
At T_A = –40°C to +85°C, V_{CC} = 3 V to 5.5 V, C_L = 15 pF, R_L = 120 Ω, R_{IREF} = 1.5 kΩ, and V_{LED} = 5.0 V, unless otherwise noted. Typical values are at T_A = +25°C and V_{CC} = 3.3 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{R0}	Rise time	SOUT		6	15	ns
t_{R1}		OUTR0-OUTR7, OUTG0-OUTG7, OUTB0-OUTB7, BCR/G/B = 7Fh		10	30	ns
t_{F0}	Fall time	SOUT		6	15	ns
t_{F1}		OUTR0-OUTR7, OUTG0-OUTG7, OUTB0-OUTB7, BCR/G/B = 7Fh		10	30	ns
t_{D0}	Propagation delay time(1)	SCLK↑ to SOUT		8	20	ns
t_{D1}		LAT↑ to OUTR0 on/off, BCR/G/B = 7Fh		22	45	ns
t_{D2}		BLANK↓↑ to OUTR0 on/off, BCR/G/B = 7Fh		15	30	ns
t_{D3}		OUTRn on to OUTGn on, OUTGn on to OUTBn on, OUTBn on to OUTRn + 1 on, BCR/G/B = 7Fh		3	6	ns
t_{D4}		OUTRn off to OUTGn off, OUTGn off to OUTBn off, OUTBn off to OUTRn + 1 off, BCR/G/B = 7Fh		3	6	ns
t_{D5}		LAT↑ to I_{OUTn} changing by global brightness control (BC data are 0Ch-72h or 72h-0Ch)		20	50	ns
t_{ON_ERR}	Output on-time error(2)	On/off latched data = '1', BCR/G/B = 7Fh, 20 ns BLANK low level one-shot pulse input	–11		5	ns

(1) Propagation delay, t_{D3} (OUTRn on to OUTGn on, OUTGn on to OUTBn on, OUTBn on to OUTRn + 1 on) is calculated by the formula:
t_{D3} (ns) = (the propagation delay between OUTR0 to OUTB7 = on)/23
t_{D4} (OUTRn to OUTGn = off, OUTGn to OUTBn = off, OUTBn to OUTRn + 1 = off) is calculated by the formula:
t_{D4} (ns) = (the propagation delay between OUTR0 to OUTB7 = off)/23

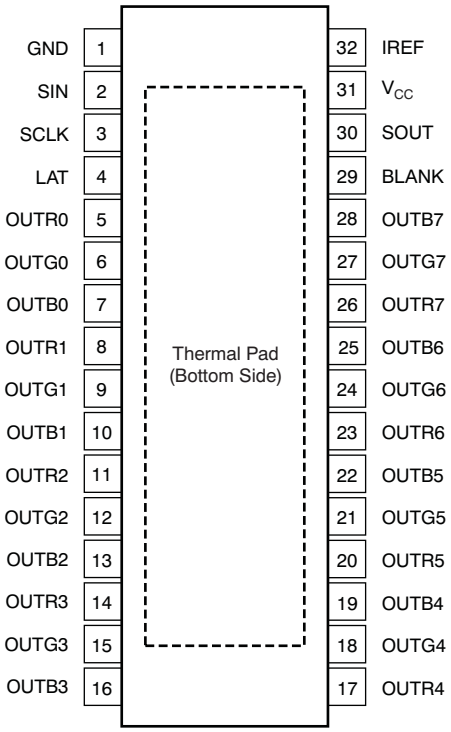
(2) Output on-time error is calculated by the formula: t_{ON_ERR} (ns) = t_{OUT_ON} – BLANK low-level pulse width. t_{OUT_ON} is the actual on-time of the constant current output.

FUNCTIONAL BLOCK DIAGRAM

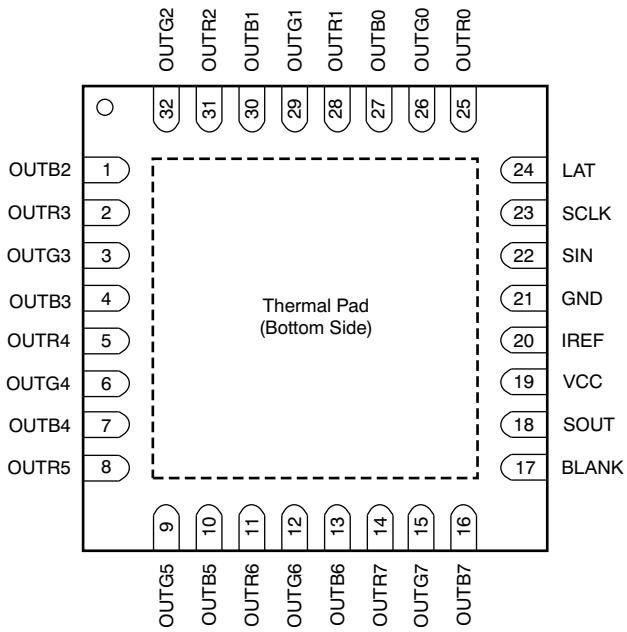


PIN CONFIGURATIONS

DAP PACKAGE
HTSSOP-32 PowerPAD
(TOP VIEW)



RHB PACKAGE(1)
5 mm × 5 mm QFN-32
(TOP VIEW)



(1) Product preview device.

TERMINAL FUNCTIONS

TERMINAL			I/O	DESCRIPTION
	NO.			
NAME	DAP	RHB[1]		
SIN	2	22	I	Serial data input for the 25-bit common shift register
SCLK	3	23	I	Serial data shift clock. Data present on SIN are shifted to the LSB of the common shift register with the rising edge of SCLK. Data in the shift register are shifted toward the MSB at each rising edge of SCLK. The MSB data of the common shift register appear on SOUT.
LAT	4	24	I	Edge triggered latch. The rising edge of LAT latches the data from the common shift register into the output on/off data latch. See the *Output On/Off Data Latch* section for more details.
BLANK	29	17	I	All outputs are blank. When BLANK is high, all constant-current outputs (OUTR0-OUTR7, OUTG0-OUTG7, and OUTB0-OUTB7) are forced off. When BLANK is low, all constant current outputs are controlled by the on/off control data in the data latch.
IREF	32	20	I/O	Reference current terminal. The maximum current for the outputs OUTR0-OUTR7, OUTG0-OUTG7, and OUTB0-OUTB7 is set with a resistor from IREF to GND.
SOUT	30	18	O	Serial data output. The MSB of the 25-bit common shift register is shifted out at the rising edge of SCLK.
OUTR0-OUTR7	5, 8, 11, 14, 17, 20, 23, 26	2, 5, 8, 11, 14, 25, 28, 31	O	Constant-current outputs for the RED LED group. Multiple outputs can be configured in parallel to increase the constant-current capability. Different voltages can be applied to each output. These outputs are turned on/off by the BLANK signal and the data in the output on/off control data latch.
OUTG0-OUTG7	6, 9, 12, 15, 18, 21, 24, 27	3, 6, 9, 12, 15, 26, 29, 32	O	Constant-current outputs for the GREEN LED group. Multiple outputs can be configured in parallel to increase the constant-current capability. Different voltages can be applied to each output. These outputs are turned on/off by the BLANK signal and the data in the output on/off control data latch.
OUTB0-OUTB7	7, 10, 13, 16, 19, 22, 25, 28	1, 4, 7, 10, 13, 16, 27, 30	O	Constant-current outputs for the BLUE LED group. Multiple outputs can be configured in parallel to increase the constant-current capability. Different voltages can be applied to each output. These outputs are turned on/off by the BLANK signal and the data in the output on/off control data latch.
V_{CC}	31	19	—	Power-supply voltage
GND	1	21	—	Power ground

(1) Product preview device.

PARAMETER MEASUREMENT INFORMATION

PIN EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS

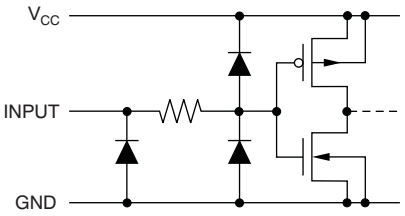


Figure 1. SIN, SCLK, LAT, BLANK

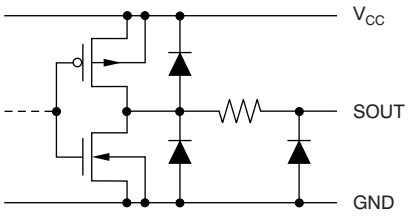


Figure 2. SOUT

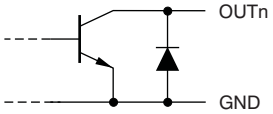
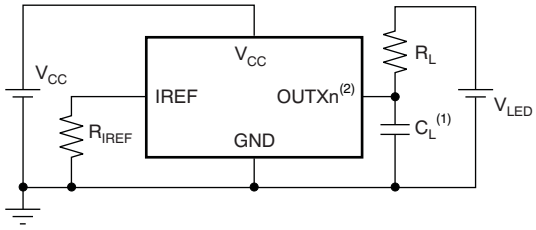


Figure 3. OUTR0/G0/B0 Through OUTR7/G7/B7

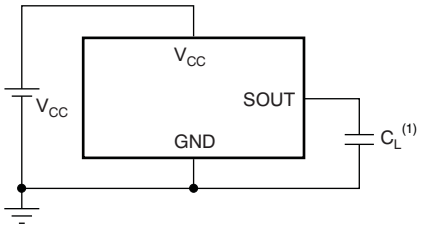
TEST CIRCUITS



(1) C_L includes measurement probe and jig capacitance.

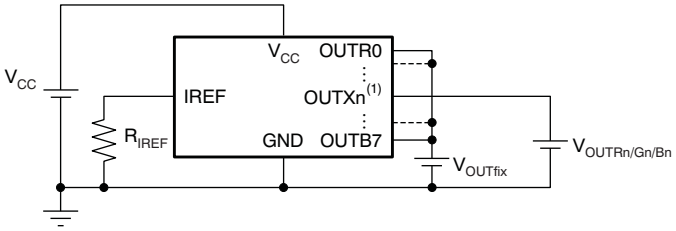
(2) X = R, G, or B; n = 0-7.

Figure 4. Rise Time and Fall Time Test Circuit for OUTRn/Gn/Bn



(1) C_L includes measurement probe and jig capacitance.

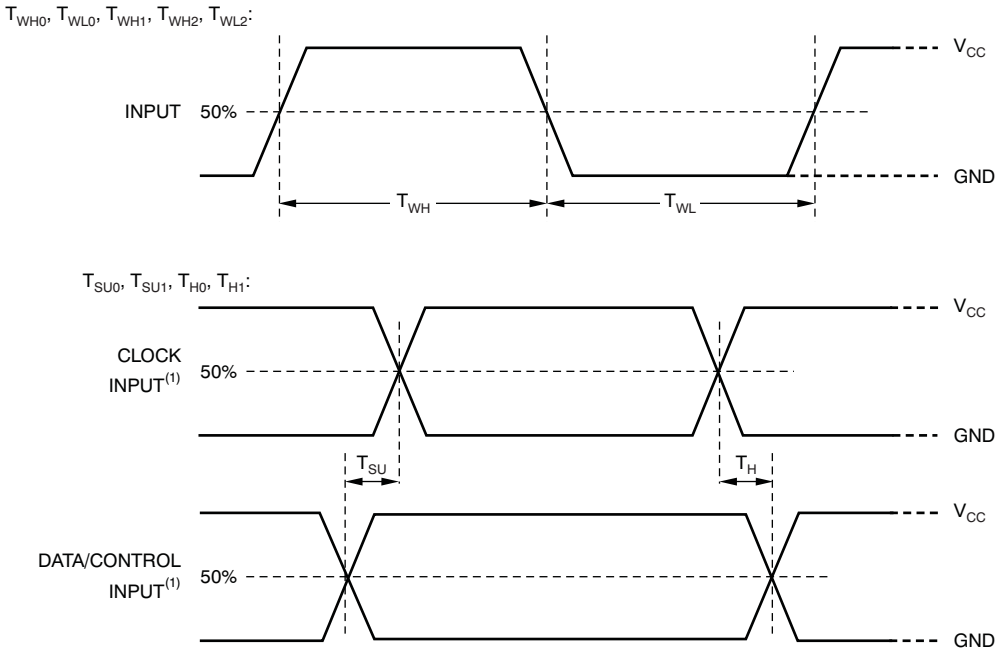
Figure 5. Rise Time and Fall Time Test Circuit for SOUT



(1) X = R, G, or B; n = 0-7.

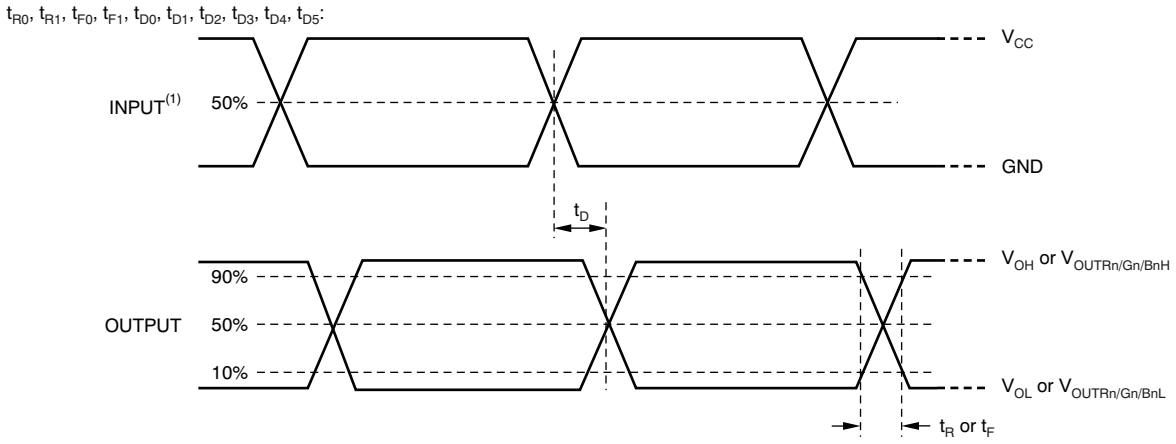
Figure 6. Constant-Current Test Circuit for OUTRn/Gn/Bn

TIMING DIAGRAMS



(1) Input pulse rise and fall time is 1 ns to 3 ns.

Figure 7. Input Timing



(1) Input pulse rise and fall time is 1 ns to 3 ns.

Figure 8. Output Timing

TIMING DIAGRAMS (continued)

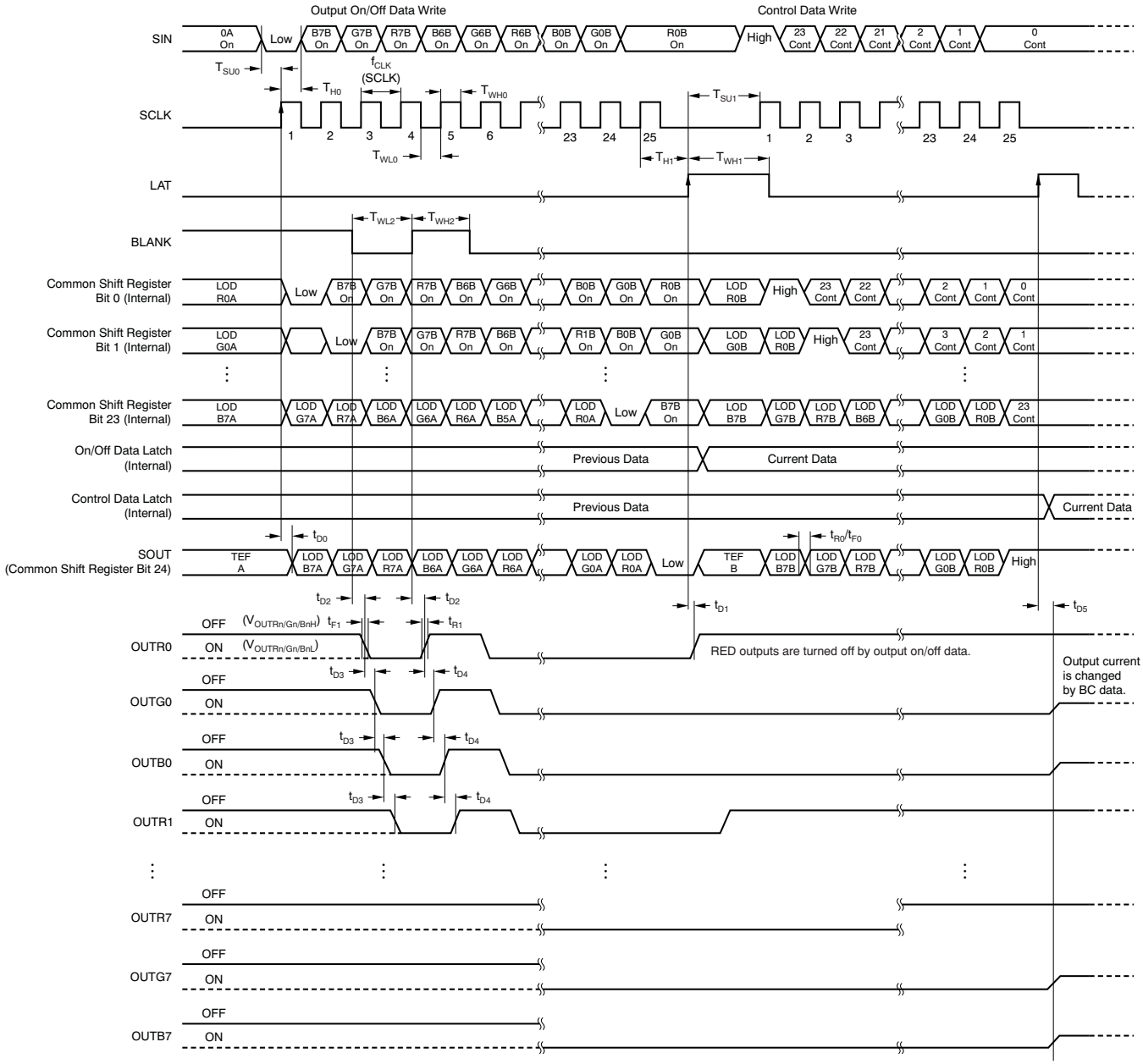


Figure 9. Timing Diagram

TYPICAL CHARACTERISTICS

At T_A = +25°C and V_{CC} = 3.3 V, unless otherwise noted.

REFERENCE RESISTOR vs OUTPUT CURRENT (RED and GREEN Color Group)

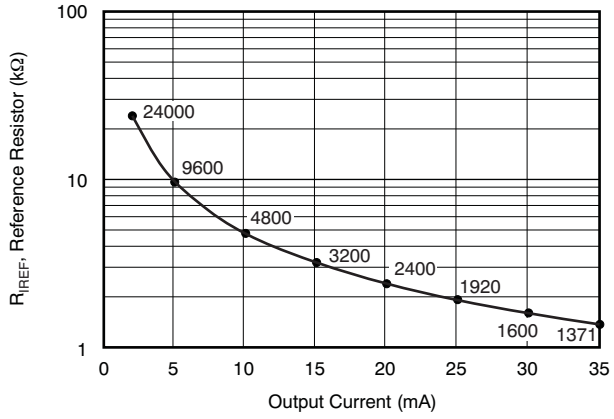


Figure 10.

REFERENCE RESISTOR vs OUTPUT CURRENT (BLUE Color Group)

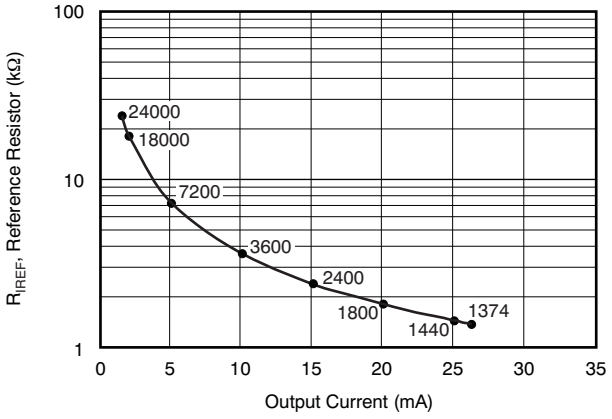


Figure 11.

POWER DISSIPATION RATE

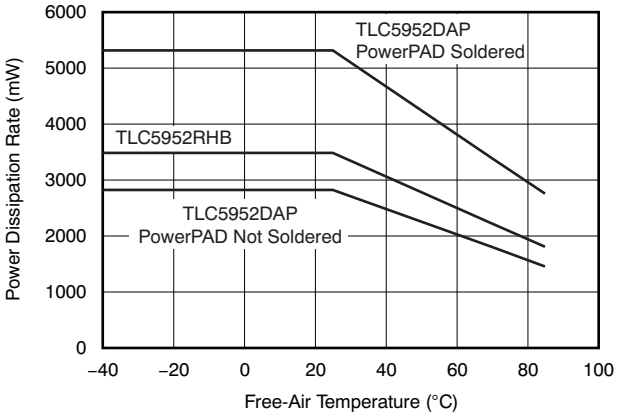


Figure 12.

OUTPUT CURRENT vs OUTPUT VOLTAGE (RED and GREEN Color Group)

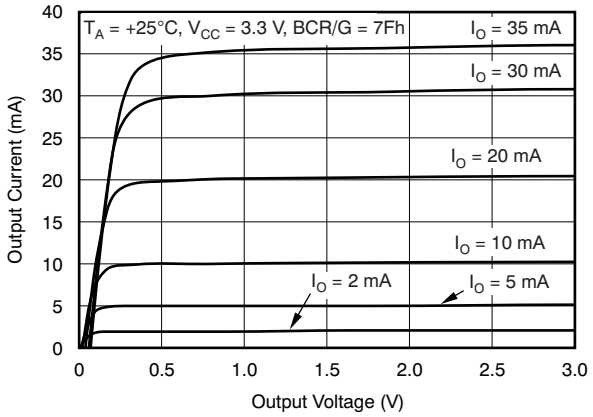


Figure 13.

OUTPUT CURRENT vs OUTPUT VOLTAGE (BLUE Color Group)

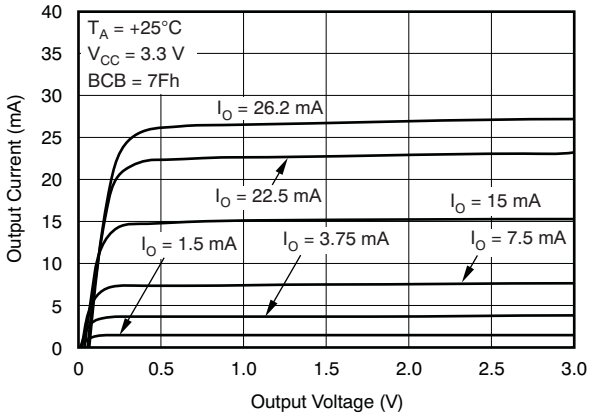


Figure 14.

OUTPUT CURRENT vs OUTPUT VOLTAGE (RED and GREEN Color Group)

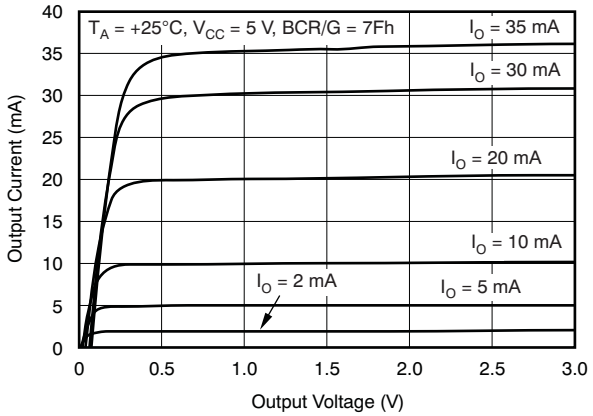


Figure 15.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C and V_{CC} = 3.3 V, unless otherwise noted.

OUTPUT CURRENT vs OUTPUT VOLTAGE (BLUE Color Group)

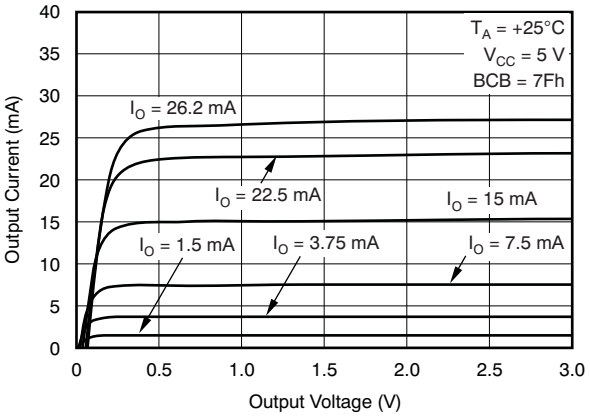


Figure 16.

OUTPUT CURRENT vs OUTPUT VOLTAGE (RED and GREEN Color Group)

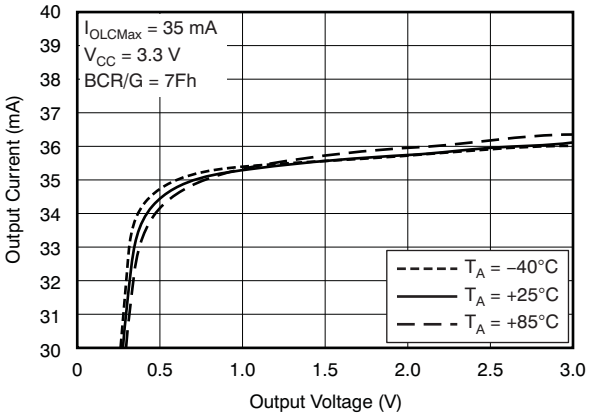


Figure 17.

OUTPUT CURRENT vs OUTPUT VOLTAGE (BLUE Color Group)

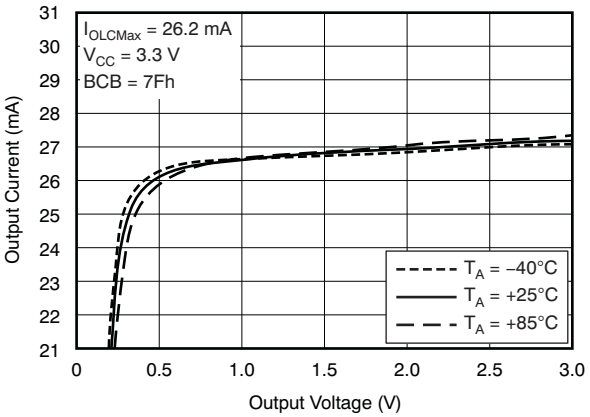


Figure 18.

OUTPUT CURRENT vs OUTPUT VOLTAGE (RED and GREEN Color Group)

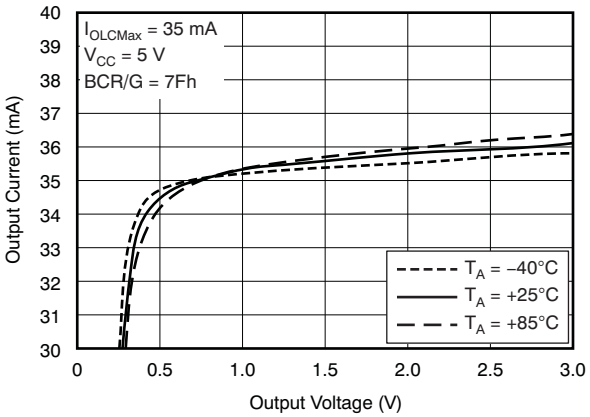


Figure 19.

OUTPUT CURRENT vs OUTPUT VOLTAGE (BLUE Color Group)

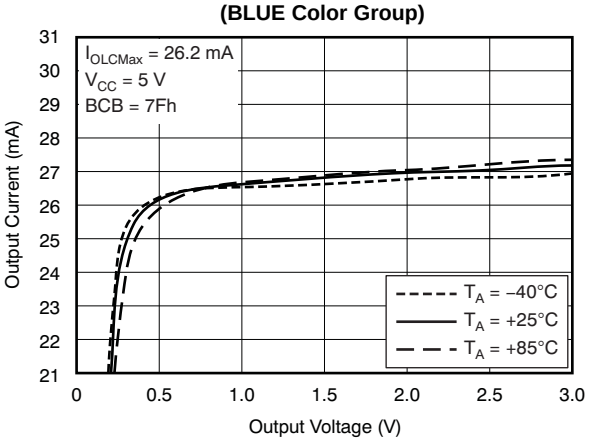


Figure 20.

CONSTANT-CURRENT ERROR vs OUTPUT CURRENT (Channel-to-Channel in RED Color Group)

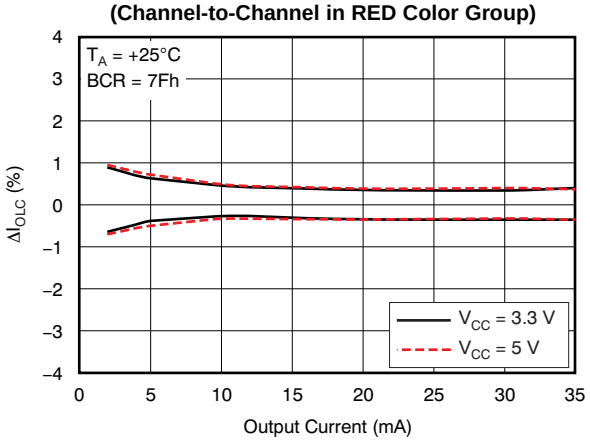


Figure 21.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C and V_{CC} = 3.3 V, unless otherwise noted.

CONSTANT-CURRENT ERROR vs OUTPUT CURRENT (Channel-to-Channel in GREEN Color Group)

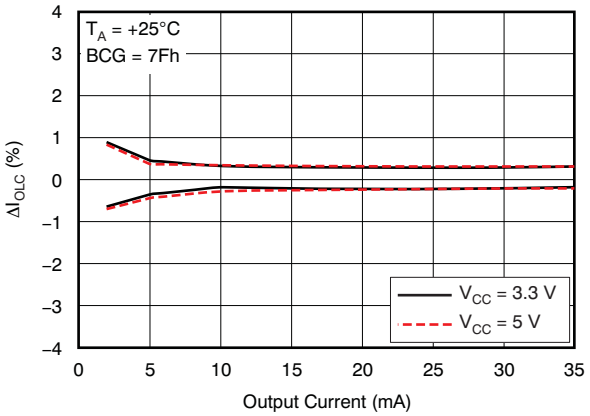


Figure 22.

CONSTANT-CURRENT ERROR vs OUTPUT CURRENT (Channel-to-Channel in BLUE Color Group)

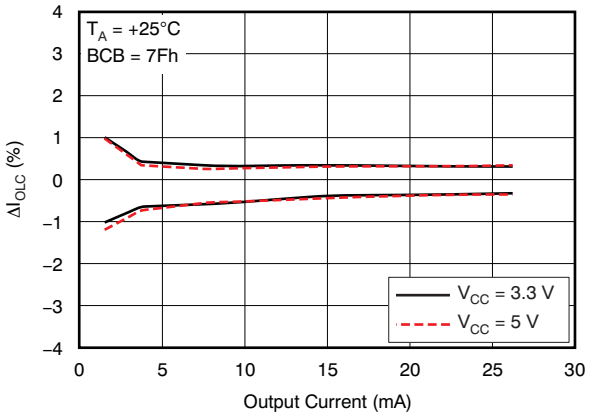


Figure 23.

CONSTANT-CURRENT ERROR vs AMBIENT TEMPERATURE (Channel-to-Channel in RED Color Group)

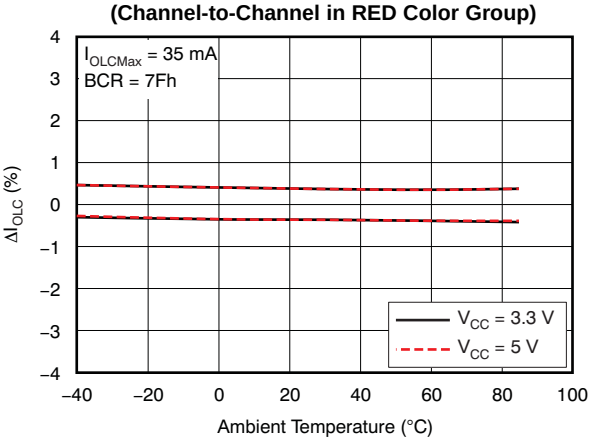


Figure 24.

CONSTANT-CURRENT ERROR vs AMBIENT TEMPERATURE (Channel-to-Channel in GREEN Color Group)

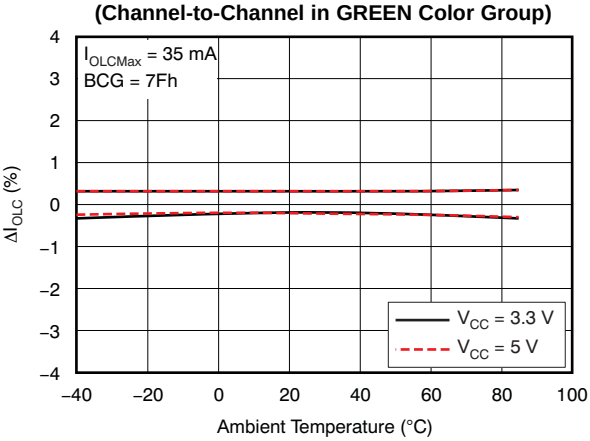


Figure 25.

CONSTANT-CURRENT ERROR vs AMBIENT TEMPERATURE (Channel-to-Channel in BLUE Color Group)

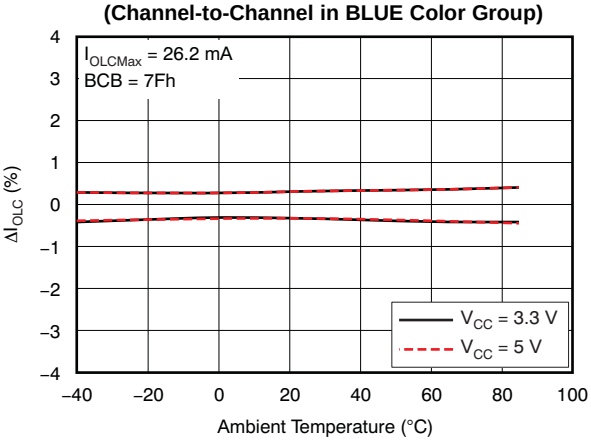


Figure 26.

GLOBAL BRIGHTNESS CONTROL LINEARITY (RED and GREEN Color Group)

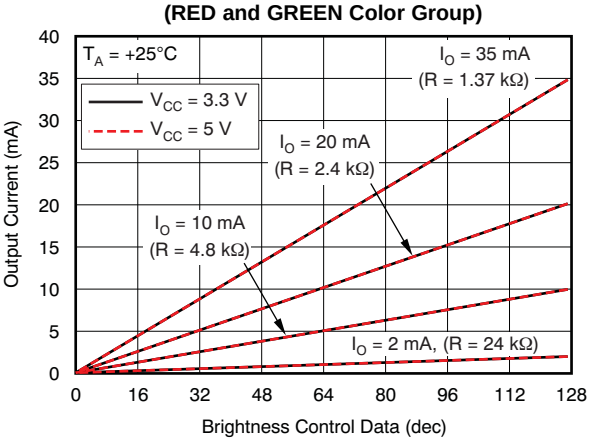


Figure 27.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C and V_{CC} = 3.3 V, unless otherwise noted.

GLOBAL BRIGHTNESS CONTROL LINEARITY (BLUE Color Group)

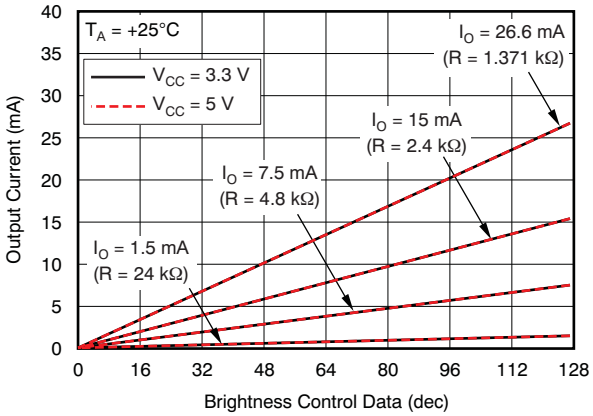


Figure 28.

SUPPLY CURRENT vs OUTPUT CURRENT (RED and GREEN Color Group)

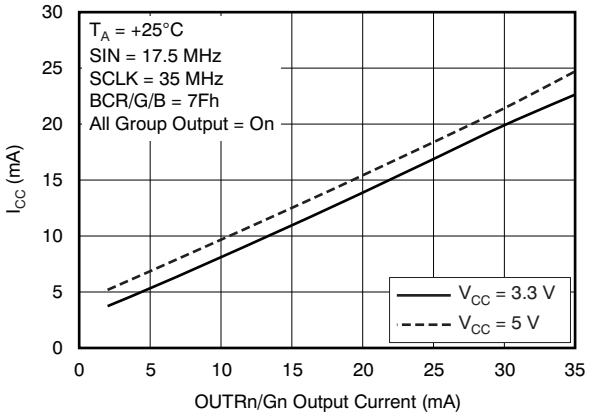


Figure 29.

SUPPLY CURRENT vs OUTPUT CURRENT (BLUE Color Group)

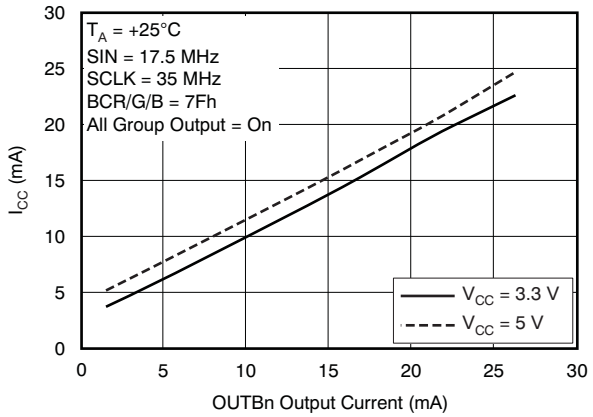


Figure 30.

SUPPLY CURRENT vs AMBIENT TEMPERATURE

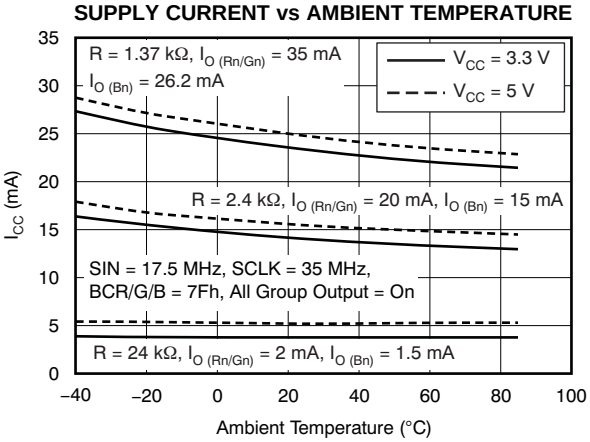


Figure 31.

CONSTANT-CURRENT OUTPUT VOLTAGE WAVEFORM

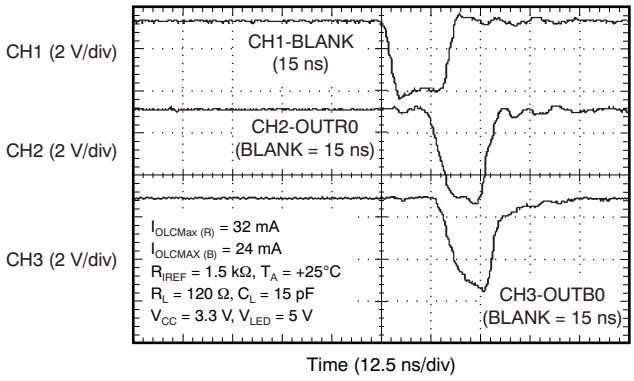


Figure 32.

DETAILED DESCRIPTION

MAXIMUM CONSTANT SINK CURRENT VALUE

The maximum output current per channel, I_{OLCMax}, is programmed by a single resistor, R_{IREF}, which is placed between the IREF and GND pins. The voltage on IREF is set by an internal band-gap V_{IREF}, with a typical value of 1.20 V. The maximum channel current is equivalent to the current flowing through R_{IREF} multiplied by a factor of 40 for OUTRn/Gn and 30 for OUTBn. The maximum output current per channel can be calculated by Equation 1.

$$R_{IREF}\ (k\Omega) = \frac{V_{IREF}\ (V)}{I_{OLCMax}\ (mA)} \times 40 \text{ (for OUTRn/Gn)}$$

$$= \frac{V_{IREF}\ (V)}{I_{OLCMax}\ (mA)} \times 30 \text{ (for OUTBn)} \quad (1)$$

Where:

V_{IREF} = the internal reference voltage on IREF (1.20 V, typical)

I_{OLCMax} = 2 mA to 35 mA at OUTRn/Gn and 1.5 mA to 26.2 mA at OUTBn

I_{OLCMax} is the largest current for each output. Each output sinks the I_{OLCMax} current when it is turned on and the global brightness control data are set to the maximum value of 7Fh (127d). Each output sink current can be reduced by lowering the output global brightness control (BC) value.

R_{IREF} must be between 1.37 kΩ and 24 kΩ to hold I_{OLCMax} between 35 mA (typ) and 2 mA (typ) for OUTRn/Gn and between 26.2 mA (typ) and 1.5 mA (typ) for OUTBn. Otherwise, the output may be unstable. Output currents lower than 2 mA (or 1.5 mA for OUTBn) can be achieved by setting I_{OLCMax} to 2 mA or higher and then using global brightness control to lower the output current.

Table 1 shows the characteristics of the constant-current sink versus the external resistor, R_{IREF}.

Table 1. Maximum Constant Current Output versus External Resistor Value

I_{OLCMax} (mA)		R_{IREF} (kΩ)
OUTRn, OUTGn	OUTBn	
35	26.28	1.37
30	22.5	1.6
25	18.75	1.92
20	15	2.4
15	11.25	3.2
10	7.5	4.8
5	3.75	9.6
2	1.5	24

GLOBAL BRIGHTNESS CONTROL (BC) FUNCTION: SINK CURRENT CONTROL

The TLC5952 is able to adjust the output current of each of the three color groups OUTR0-OUTR7, OUTG0-OUTG7, and OUTB0-OUTB7. This function is called *global brightness control* (BC). The BC function allows users to adjust the global brightness of LEDs connected to the three output groups (OUTR0-OUTR7, OUTG0-OUTG7, and OUTB0-OUTB7). All color group output currents can be adjusted in 128 steps from 0% to 100% of the maximum output current, I_{OLCMax}. The brightness control data are entered into the TLC5952 via the serial interface. When the BC data change, the output current also changes immediately. When the IC is powered on, the data in the common shift register and the control data latch are not set to any default values. Therefore, BC data must be written to the control data latch before turning on the constant-current output.

Equation 2 determines the output sink current for each color group. Table 2 summarizes the BC data versus current ratio and set current value.

$$I_{OUT}\ (mA) = I_{OLCMax}\ (mA) \times \left(\frac{BCR/G/B}{127d} \right) \quad (2)$$

Where:

I_{OLCMax} = the maximum channel current for each channel determined by R_{IREF}

BCR/G/B = the global brightness control value in the control data latch for each output color group

Table 2. BC Data versus Current Ratio and Set Current Value

BC DATA (Binary)	BC DATA (Decimal)	BC DATA (Hex)	RATIO OF OUTPUT CURRENT TO I_{OLCMax} (mA, Typical)	I_{OUT}, mA (I_{OLCMax} = 35 mA, Typical)	I_{OUT}, mA (I_{OLCMax} = 2 mA, Typical)
000 0000	0	00	0	0	0
000 0001	1	01	0.8	0.28	0.02
000 0010	2	02	1.6	0.55	0.03
—	—	—	—	—	—
111 1101	125	7D	98.4	34.45	1.97
111 1110	126	7E	99.2	34.72	1.98
111 1111	127	7F	100.0	35.00	2.00

CONSTANT-CURRENT OUTPUT ON/OFF CONTROL

When BLANK is low, each output is controlled by the data in the output on/off data latch. When data corresponding to an output are equal to '1', the output turns on; when the data corresponding to an output are equal to '0', the output turns off. When BLANK is high, all outputs are forced off.

When the IC is powered on, the data in the output on/off data latch are not set to any default values. Therefore, on/off data must be written to the output on/off data latch before turning on the constant-current output and pulling BLANK low.

If there are any OUTRn/Bn/Bn outputs not connected to an LED, including open for short-to-ground failures, the on/off data corresponding to the unconnected output should be set to '0' before the LED is turned on. Otherwise, the V_{CC} supply current (I_{CC}) increases while the LEDs are on. A truth table for the on/off control data is shown in Table 3.

Table 3. On/Off Control Data Truth Table

ON/OFF CONTROL DATA	CONSTANT-CURRENT OUTPUT STATUS
0	Off
1	On

REGISTER AND DATA LATCH CONFIGURATION

The TLC5952 has two writable data latches: the output on/off data latch and the control data latch. Both data latches are 24 bits in length. If the common shift register MSB is '0', the least significant 24 bits of data from the 25-bit common shift register are latched into the output on/off data latch. If the MSB is '1', the data are latched into the control data latch. Figure 33 shows the common shift register and the control data latch configuration.

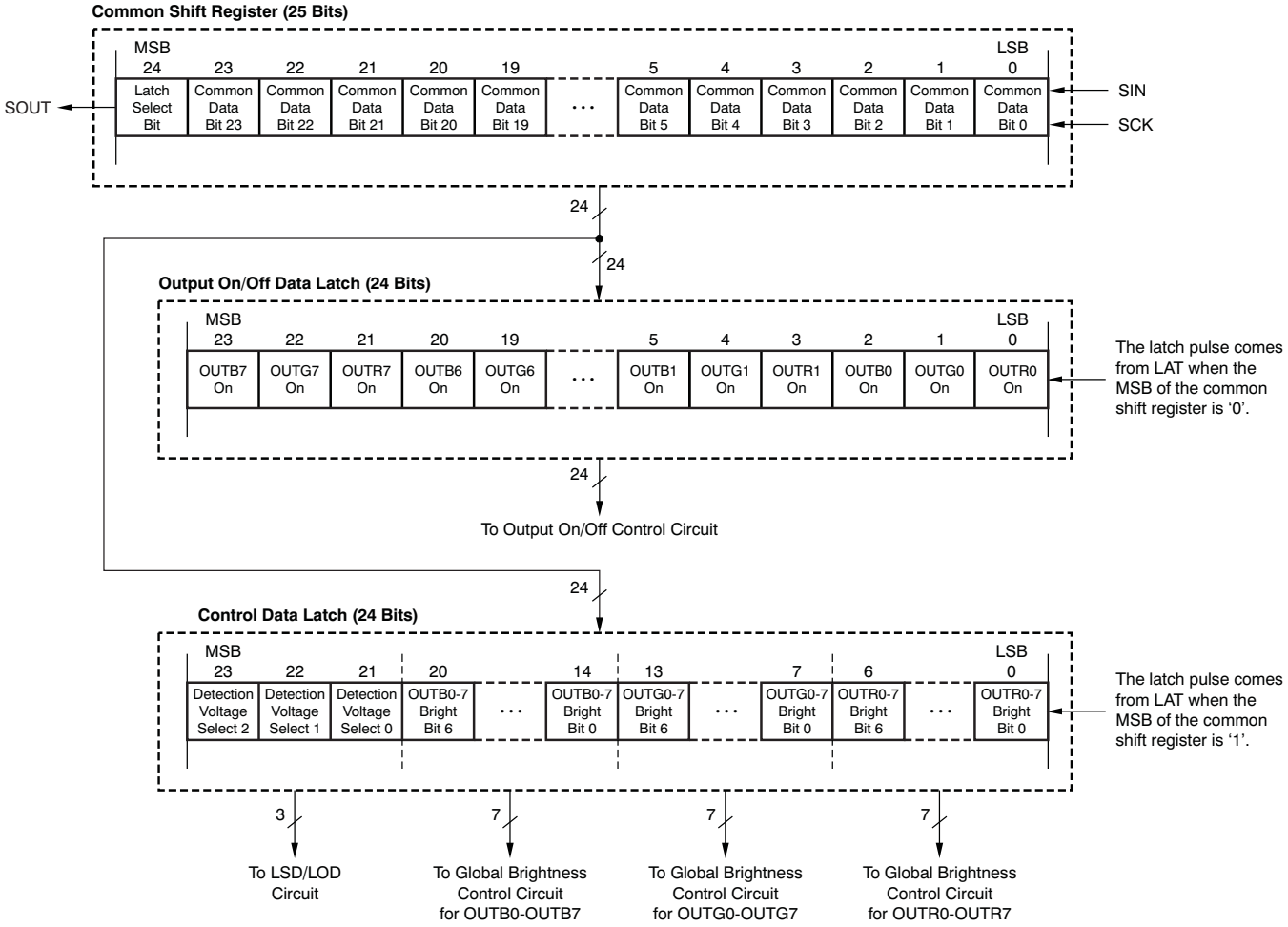


Figure 33. Grayscale Shift Register and Data Latch Configuration

Output On/Off Data Latch

The output on/off data latch is 24 bits long. This latch is used to turn each output current sink (OUTRn/Gn/Bn) on or off. When the MSB of the common shift register is set to '0', the lower 24 bits are written to the output on/off data latch on the rising edge of LAT. If the output on/off data latch bit corresponding to an output is '0', the output is turned off; if the bit is a '1', the output is turned on.

When the IC is powered on, the data in the output on/off data latch are not set to any default value. Therefore, the on/off control data should be written to the data latch before the constant-current outputs are turned on.

Control Data Latch

The control data latch is 24 bits long and is used to adjust the LED current for each color group (OUTR0-OUTR7, OUTG0-OUTG7, and OUTB0-OUTB7). The LED current for each group can be adjusted between 0% and 100% of I_{OLCMAX} in 128 steps (7-bit resolution). This data latch is also used to select the error detection type, LED open detection (LOD) or LED short detection (LSD), and the threshold voltage. When the MSB of the common shift register is set to '1', the lower 24 bits are written to the control data latch on the rising edge of LAT. Table 4 shows the control data latch bit assignment.

When the IC is powered on, the data in the control data latch are not set to a default value. Therefore, the control data latch data should be written to the latch before the constant-current outputs are turned on.

Table 4. Data Bit Assignment

BITS	DESCRIPTION
6-0	Global brightness control data for RED group (OUTR0-OUTR7, data = 00h to 7Fh)
13-7	Global brightness control data for GREEN group (OUTG0-OUTG7, data = 00h to 7Fh)
20-14	Global brightness control data for BLUE group (OUTB0-OUTB7, data = 00h to 7Fh)
23-21	Detection voltage and type select (data = 0h to 7h) 0 = LED open detection with 0.3 V (typ) threshold 1 = LED open detection with 0.6 V (typ) threshold 2 = LED open detection with 0.9 V (typ) threshold 3 = LED open detection with 1.2 V (typ) threshold 4 = LED short detection with V_{CC} × 60% (typ) threshold 5 = LED short detection with V_{CC} × 70% (typ) threshold 6 = LED short detection with V_{CC} × 80% (typ) threshold 7 = LED short detection with V_{CC} × 90% (typ) threshold

Figure 34 shows the operation to write data into the common shift register and control data latch.

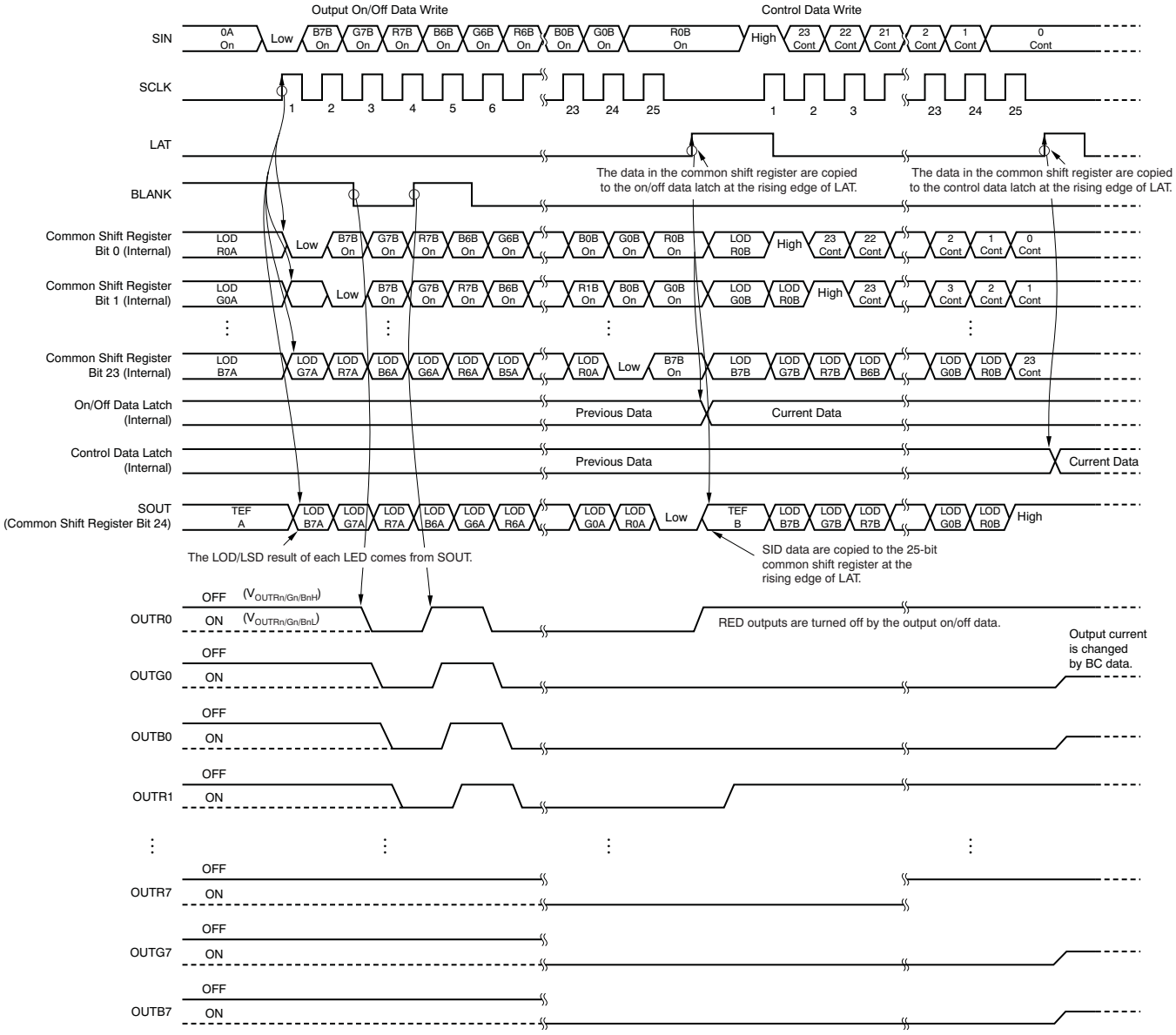


Figure 34. Data Write Operation

STATUS INFORMATION DATA (SID)

The 25-bit word status information data (SID) contains the status of the LED open detection (LOD) or LED short detection (LSD), and thermal error flag (TEF). When the MSB of the common shift register is set to '0', the SID overwrites the common shift register data at the rising edge of LAT after the data in the common shift register are copied to the output on/off data latch. If the common shift register MSB is '1', the SID data are not copied to the common shift register.

After being copied into the common shift register, new SID data are not available until new data are written into the common shift register. If new data are not written, the LAT signal is ignored. To recheck SID data without changing the constant-current output on/off data, reprogram the common shift register with the same data that are currently programmed into the output on/off data latch. When LAT goes high, the output on/off data do not change, but new SID data are loaded into the common shift register. LOD, LSD, and TEF are shifted out of SOUT with each rising edge of SCLK.

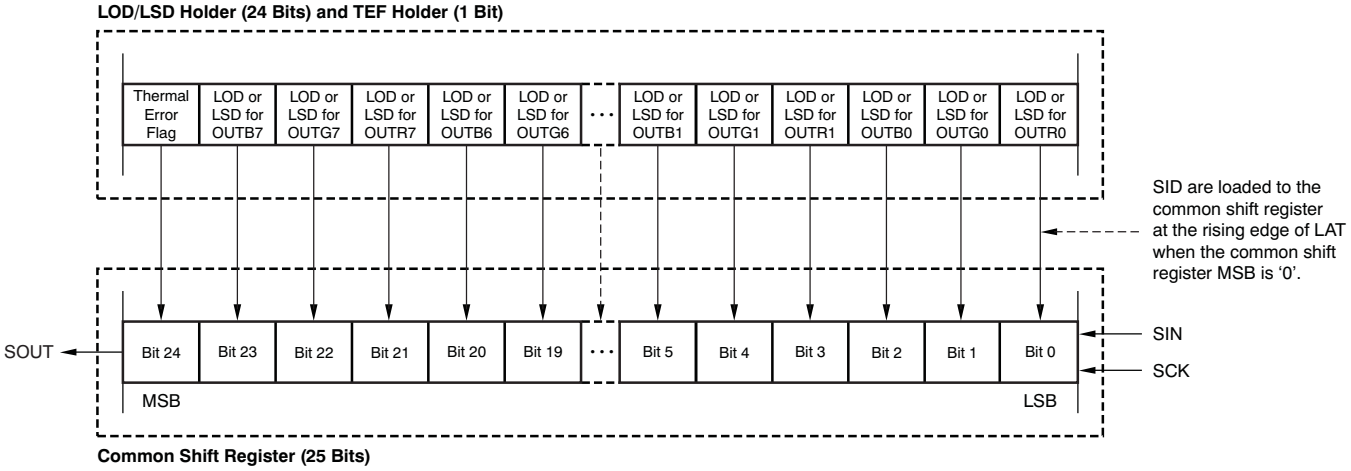


Figure 35. SID Load Assignment

LED OPEN DETECTION (LOD), LED SHORT DETECTION (LSD), AND THERMAL ERROR FLAG (TEF)

LOD detects a fault caused by an LED open circuit or a short from OUTRn/Gn/Bn to ground by comparing the OUTRn/Gn/Bn voltage to the LOD detection threshold voltage level set in the control data latch (Table 4). If the OUTRn/Gn/Bn voltage is lower than the programmed voltage, that output LOD bit is set to '1' to indicate an open LED. Otherwise, the LOD bit is set to '0'. LOD data are only valid for outputs programmed to be on. LOD data for outputs programmed to be off are always '0'.

LSD data detects a fault caused by a shorted LED by comparing the OUTRn/Gn/Bn voltage to the LSD detection threshold voltage level set in the control data latch (Table 4). If the OUTRn/Gn/Bn voltage is higher than the programmed voltage, that output LOD bit is set to '1' to indicate a shorted LED. Otherwise, the LSD bit is set to '0'. LSD data are only valid for outputs programmed to be on. LSD data for outputs programmed to be off are always '0'.

LOD/LSD data are not valid until 1 μs after the falling edge of BLANK. Therefore, BLANK must be low for at least 1 μs before going high. At the rising edge of BLANK, the LOD/LSD detection data are latched in the LOD/LSD holder. Changes in the LOD/LSD data while BLANK is low are directly connected to the output of the LOD/LSD holder, but are only valid 1 μs after the change. The rising edge of LAT transfers the output data of the LOD/LSD holder to the common shift register.

As shown in Table 5, LOD and LSD data cannot be checked simultaneously. LOD/LSD data are not valid when TEF is active because all outputs are forced off.

The TEF bit indicates that the IC junction temperature exceeds the temperature threshold (T_{TEF} = +165°C, typ). The TEF bit also indicates that the IC has turned off all drivers to avoid overheating. The IC automatically turns the drivers back on when the IC temperature decreases to less than $T_{TEF} – T_{HYS}$. The TEF data are held in the TEF holder latch until the TEF data are loaded into the common shift register by the rising edge of LAT. If the IC temperature falls below $T_{TEF} – T_{HYS}$ when LAT goes high, the TEF data in the TEF holder become '0'. If the IC temperature is not below $T_{TEF} – T_{HYS}$ when LAT goes high, then the TEF data remain '1'. Table 5 shows a truth table for LOD/LSD and TEF. Figure 36 to Figure 39 show different examples of LOD/LSD/TEF operation.

Table 5. LOD/LSD/TEF Truth Table

SID DATA	CONDITION		
	LED OPEN DETECTION (LOD, Voltage Select Data = 0h to 3h)	**LED SHORT DETECTION (LSD, Voltage Select Data = 4h to 7h)**	**THERMAL ERROR FLAG (TEF)**
0	LED is not open or the output is off ($V_{OUTRn/Gn/Bn}$ is greater than the voltage selected by the detection voltage select bit in the control data latch)	LED is not shorted or the output is off ($V_{OUTRn/Gn/Bn}$ is less than or equal to the voltage selected by the detection voltage select bit in the control data latch)	Junction temperature is lower than the detect temperature (T_{TEF}) before TEF is undetected or the detect temperature ($T_{TEF} – T_{HYS}$) after TEF is detected
1	LED is open or shorted to GND ($V_{OUTRn/Gn/Bn}$ is less than or equal to the voltage selected by the detection voltage select bit in the control data latch)	LED terminal is short or OUTn is short to higher voltage (V_{OUTn} is greater than The selected voltage by detection voltage select bit in the control data latch)	Junction temperature is higher than the detect temperature (T_{TEF})

THERMAL SHUTDOWN (TSD)

The thermal shutdown (TSD) function turns off all constant-current outputs when the IC junction temperature (T_J) exceeds the temperature threshold (T_{TEF} = +165°C, typ). The outputs remain disabled as long as the over-temperature condition exists. The outputs are turned on again after the IC junction temperature drops below ($T_{TEF} – T_{HYS}$).

NOISE REDUCTION

Large surge currents may flow through the IC and the board on which the device is mounted if all 24 LED channels turn on simultaneously when BLANK goes low. These large current surges could induce detrimental noise and electromagnetic interference (EMI) into other circuits. The TLC5952 turns the LED channels on in a series delay to provide a circuit soft-start feature.

A small delay circuit is implemented between each output. When all bits of the on/off data latch are set to '1', each constant-current output turns on in order (OUTR0, OUTG0, OUTB0, OUTR1, OUTG1, OUTB1, OUTR2-OUTB6, OUTR7, OUTG7, and OUTB7) with a small delay between each output after BLANK goes low or LAT goes high; see Figure 34. Both turn-on and turn-off are delayed.

CAPACITOR SELECTION

Connect at least one 10-nF ceramic capacitor as close as possible between the V_{CC} pin and ground. Additional capacitors are needed on the LED power supply to reduce ripple on the LED power supply to a minimum.

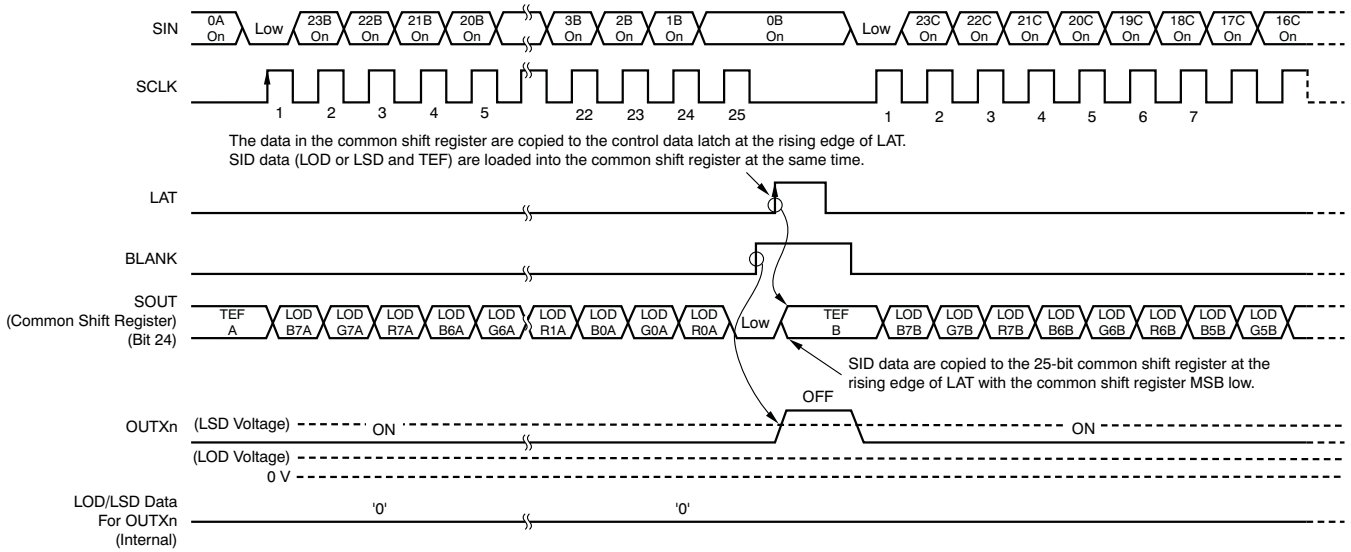


Figure 36. LOD/LSD/TEF Operation (No LED Error)

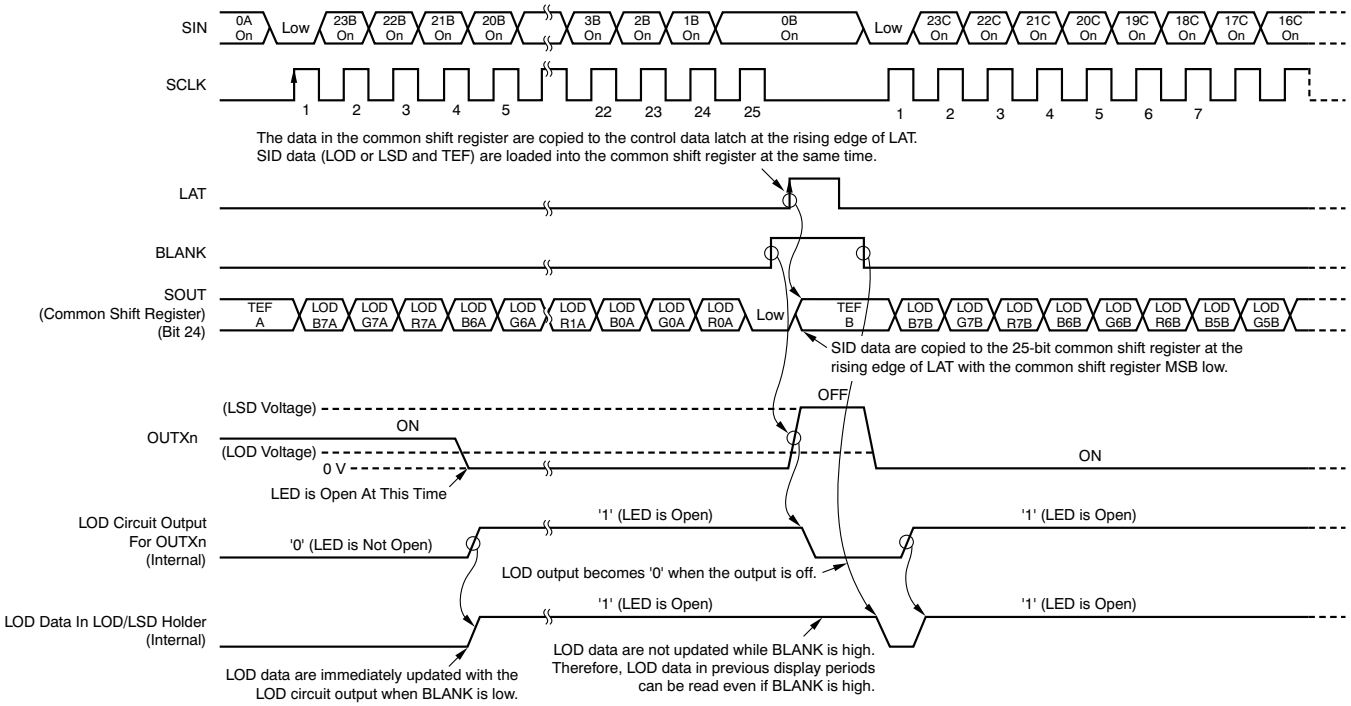


Figure 37. LOD/LSD/TEF Operation (LED Open Error)

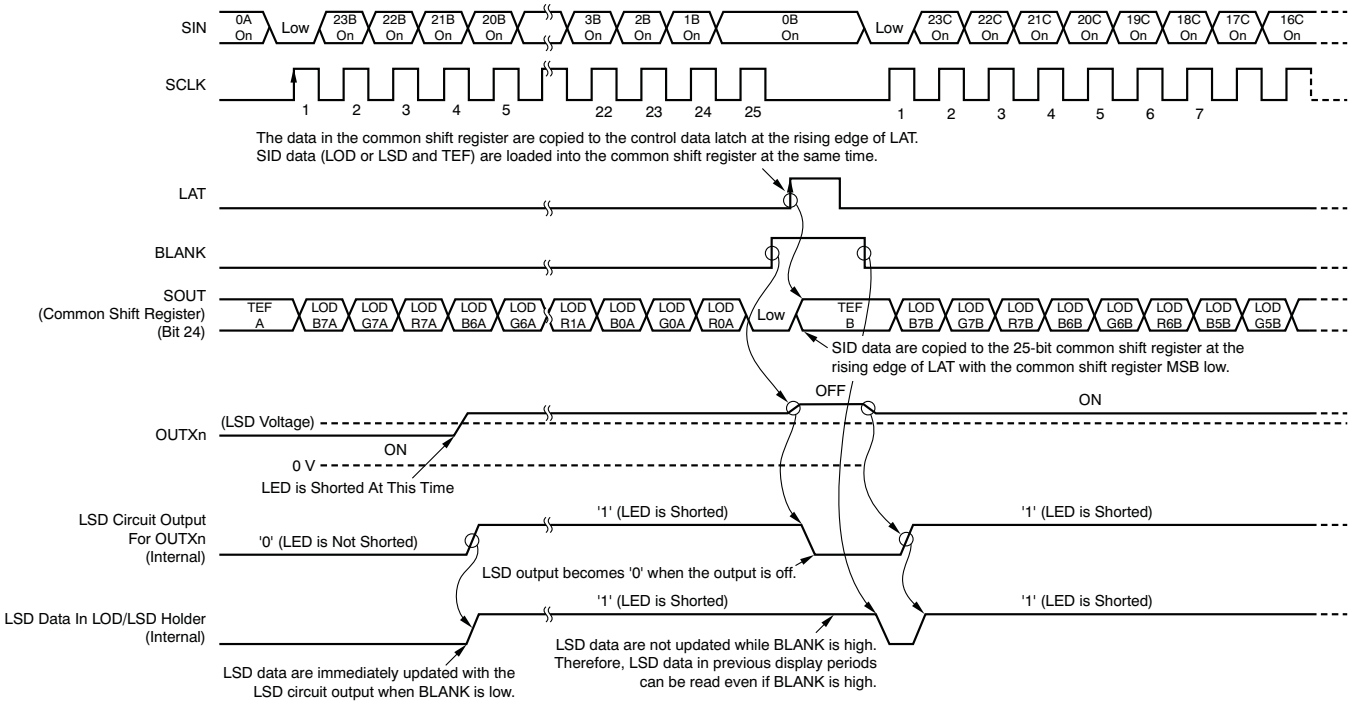


Figure 38. LOD/LSD/TEF Operation (LED Short Error)

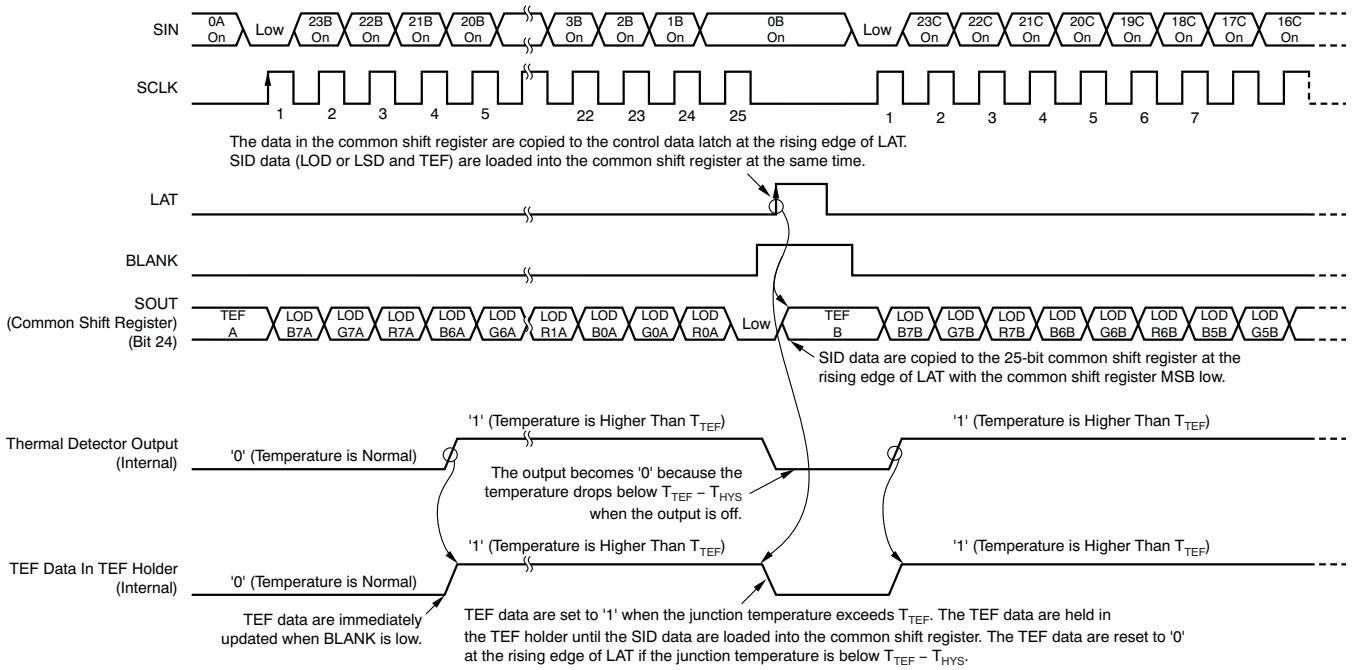


Figure 39. LOD/LSD/TEF Operation (Thermal Error)

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TLC5952DAP	ACTIVE	HTSSOP	DAP	32	46	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	TLC5952	Samples
TLC5952DAPR	ACTIVE	HTSSOP	DAP	32	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	TLC5952	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

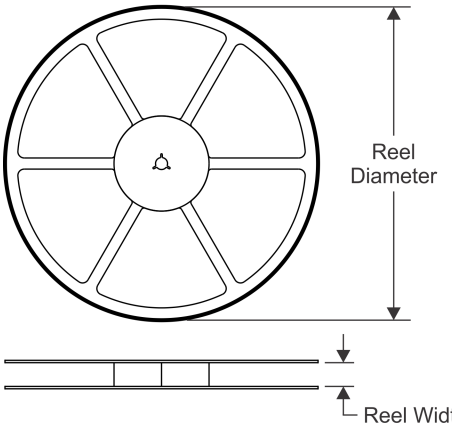
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

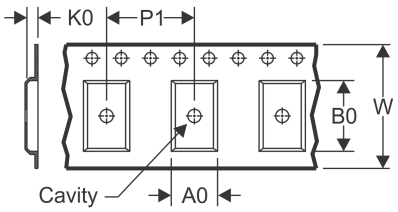
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

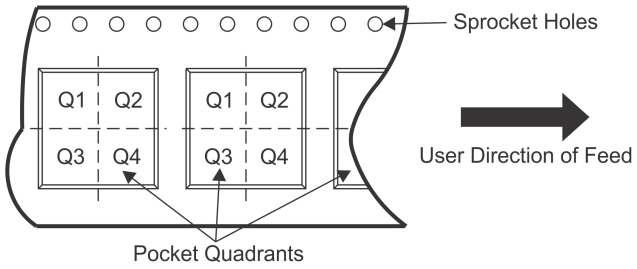


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

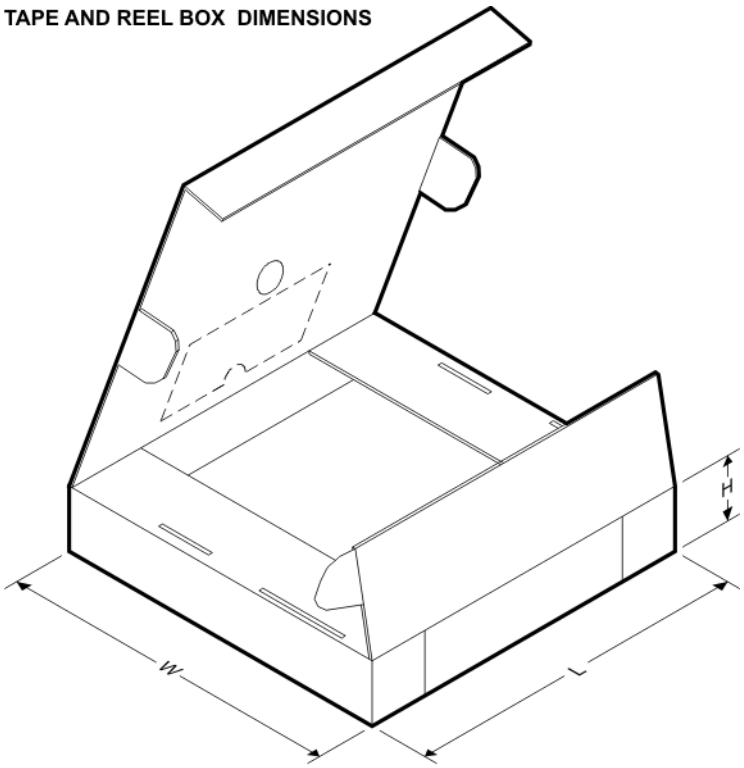
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC5952DAPR	HTSSOP	DAP	32	2000	330.0	24.4	8.6	11.5	1.6	12.0	24.0	Q1

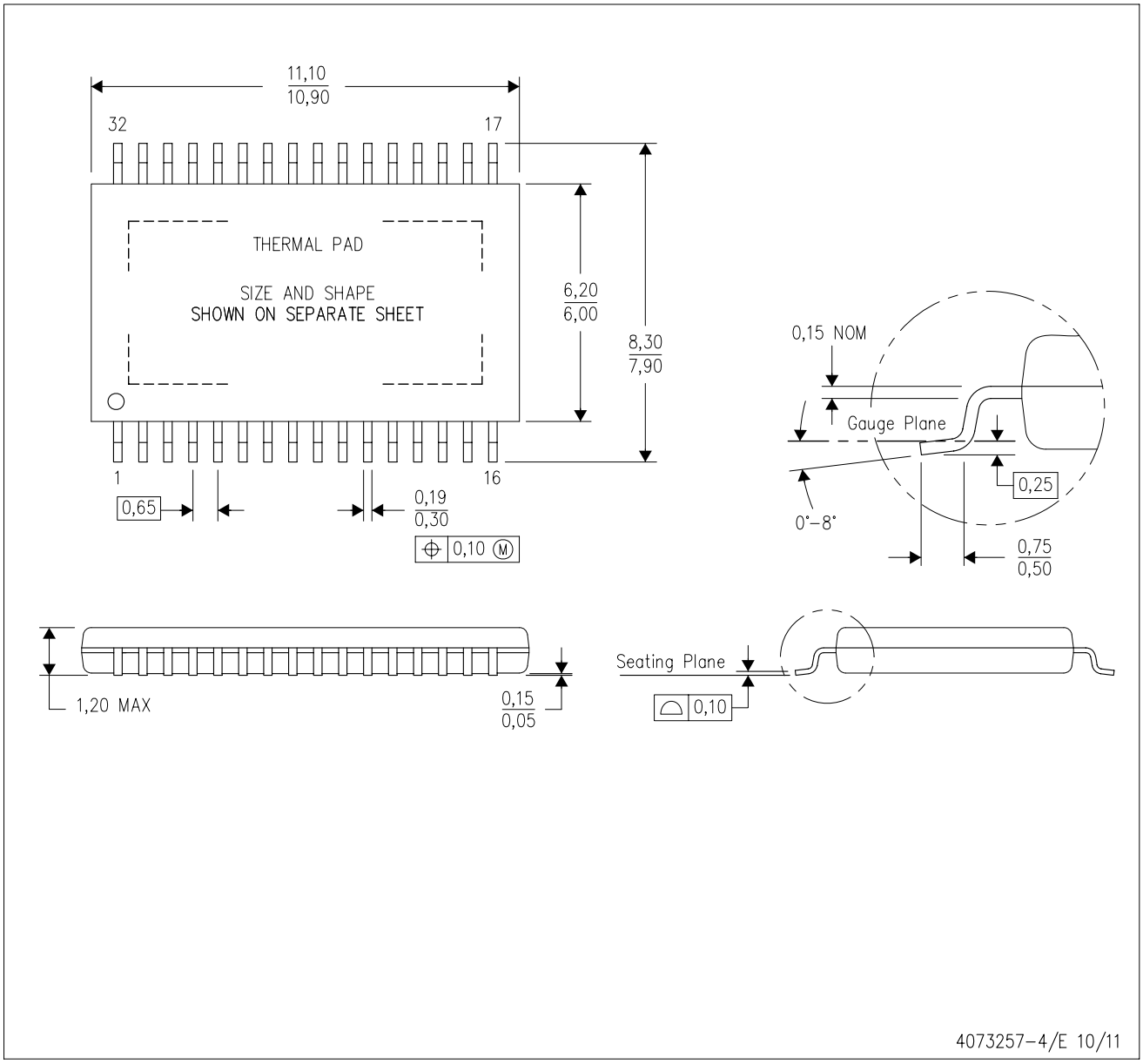
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC5952DAPR	HTSSOP	DAP	32	2000	367.0	367.0	45.0

DAP (R–PDSO–G32) PowerPAD™ PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
F. Falls within JEDEC MO–153 Variation DCT.

PowerPAD is a trademark of Texas Instruments.

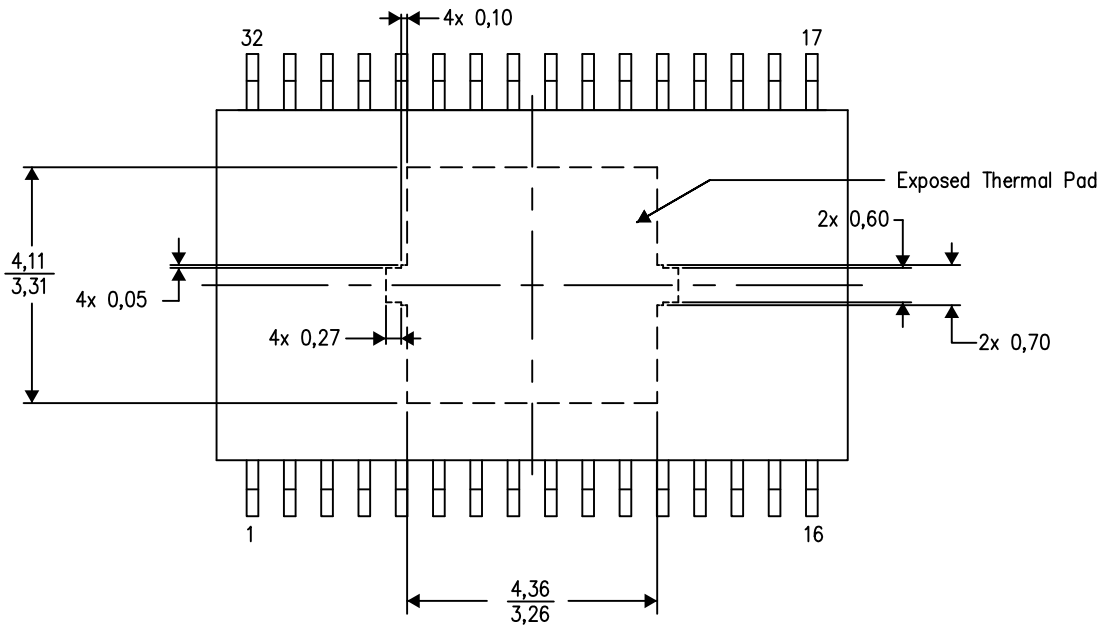
DAP (R–PDSO–G32) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

4206319–3/M 09/13

NOTE: All linear dimensions are in millimeters

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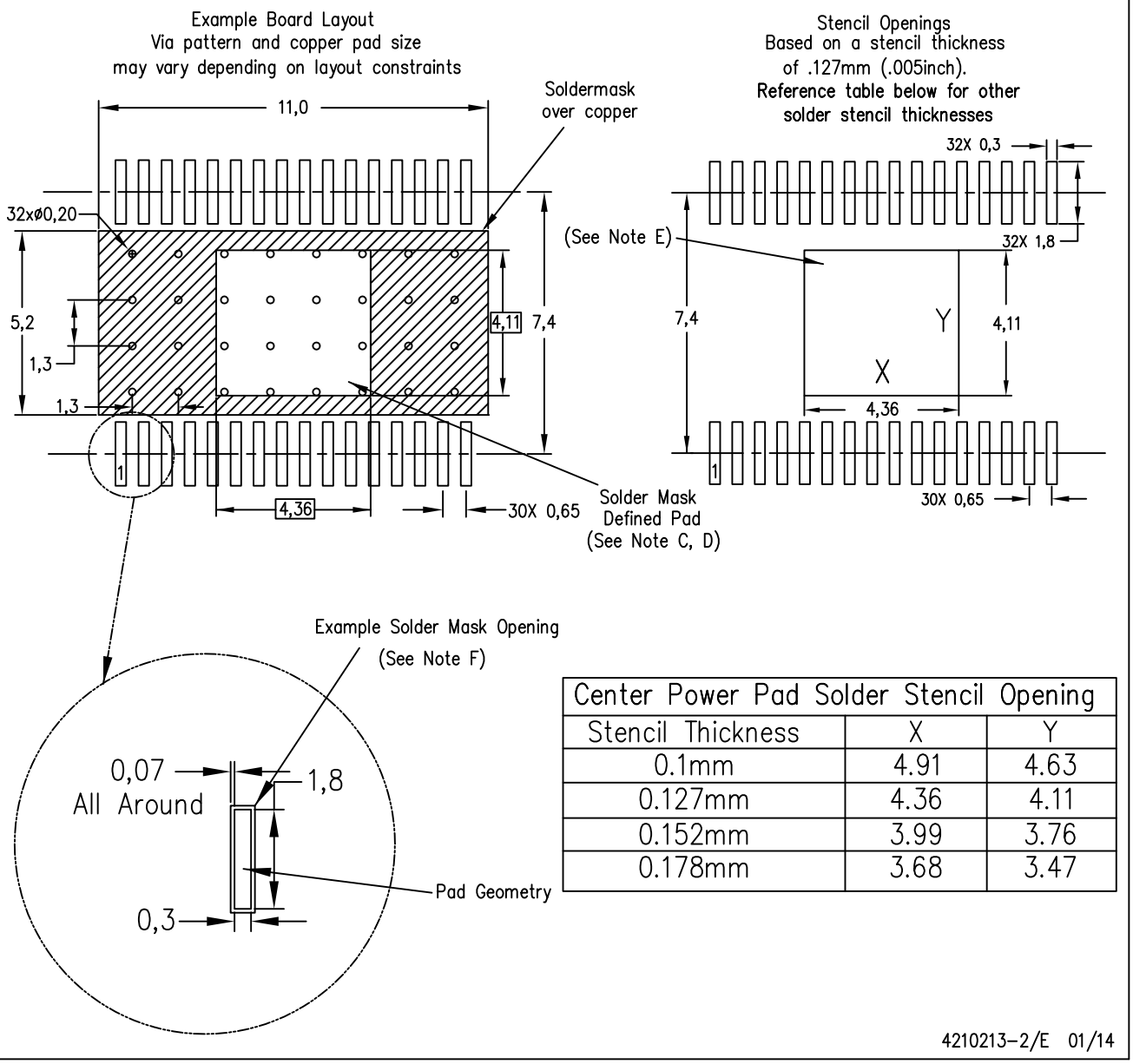
DAP (R–PDSO–G32) PowerPAD™ PLASTIC SMALL OUTLINE PACKAGE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	4.91	4.63
0.127mm	4.36	4.11
0.152mm	3.99	3.76
0.178mm	3.68	3.47

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
F. Contact the board fabrication site for recommended soldermask tolerances.

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