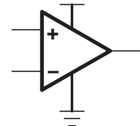
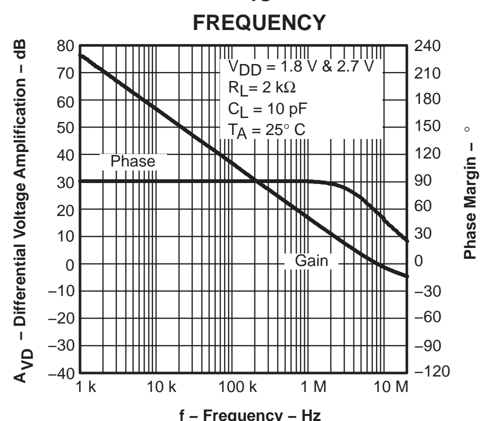
- **Supply Voltage Range . . . 1.8 V to 3.6 V**
- **Rail-to-Rail Input/Output**
- **High Bandwidth . . . 8 MHz**
- **High Slew Rate . . . 4.8 V/μs**
- **$V_{ICR}$ Exceeds Rails . . . –0.2 V to $V_{DD}$+ 0.2**
- **Supply Current . . . 650 μA/Channel**
- **Input Noise Voltage . . . 9 nV/√Hz at 10 kHz**
- **Specified Temperature Range:**
  **0°C to 70°C . . . Commercial Grade**
  **–40°C to 125°C . . . Industrial Grade**
- **Ultrasmall Packaging**
- **Universal Operational Amplifier EVM**

**Operational Amplifier**




**DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE**
**vs**
**FREQUENCY**




## description

The TLV278x single supply operational amplifiers provide rail-to-rail input and output capability. The TLV278x takes the minimum operating supply voltage down to 1.8 V over the extended industrial temperature range (–40°C to 125°C) while adding the rail-to-rail output swing feature. The TLV278x also provides 8 MHz bandwidth from only 650 μA of supply current. The maximum recommended supply voltage is 3.6 V, which allows the devices to be operated from (±1.8 V supplies down to ±0.9 V) two rechargeable cells.

The combination of wide bandwidth, low noise, and low distortion makes it ideal for high speed and high resolution data converter applications.

All members are available in PDIP, SOIC, and the newer, smaller SOT-23 (singles), MSOP (duals), and TSSOP (quads).

**FAMILY PACKAGE TABLE**

| DEVICE | $V_{DD}$ [V] | $V_{IO}$ [μV] | $I_{DD}$/ch [μA] | $I_{IB}$ [pA] | GBW [MHz] | SLEW RATE [V/μs] | $V_n$, 1 kHz [nV/√Hz] | $I_O$ [mA] | SHUTDOWN | RAIL-TO-RAIL |
|---|---|---|---|---|---|---|---|---|---|---|
| TLV278x(A) | 1.8–3.6 | 250 | 650 | 2.5 | 8 | 5 | 18 | 10 | Y | I/O |
| TLV276x(A) | 1.8–3.6 | 550 | 20 | 3 | 0.5 | 0.23 | 95 | 5 | Y | I/O |
| TLV246x(A) | 2.7–6 | 150 | 550 | 1300 | 6.4 | 1.6 | 11 | 25 | Y | I/O |
| TLV247x(A) | 2.7–6 | 250 | 600 | 2.5 | 2.8 | 1.5 | 15 | 20 | Y | I/O |
| TLV244x(A) | 2.7–10 | 300 | 750 | 1 | 1.81 | 1.4 | 16 | 2 | — | O |
| TLV277x(A) | 2.5–5.5 | 360 | 1000 | 2 | 5.1 | 10.5 | 17 | 6 | Y | O |

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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**TLV2780 and TLV2781 AVAILABLE OPTIONS(1)**

| $T_A$ | $V_{IO}$max AT 25°C | PACKAGED DEVICES | | | |
|---|---|---|---|---|---|
| | | SMALL OUTLINE (D)† | SOT-23 (DBV)‡ | SOT-23 SYMBOL | PLASTIC DIP (P) |
| 0°C to 70°C | 3000 µV | TLV2780CD<br>TLV2781CD | TLV2780CDBV<br>TLV2781CDBV | VASC<br>VATC | —<br>— |
| -40°C to 125°C | 3000 µV | TLV2780ID<br>TLV2781ID | TLV2780IDBV<br>TLV2781IDBV | VASI<br>VATI | TLV2780IP<br>TLV2781IP |
| | 2000 µV | TLV2780AID<br>TLV2781AID | —<br>— | —<br>— | —<br>— |

† This package is available taped and reeled. To order this packaging option, add an **R** suffix to the part number (e.g., TLV2780CDR).
‡ This package is only available taped and reeled. For standard quantities (3,000 pieces per reel), add an **R** suffix (i.e., TLV2780CDBVR). For smaller quantities (250 pieces per mini-reel), add a **T** suffix to the part number (e.g. TLV2780CDBVT).

**TLV2782 and TLV2783 AVAILABLE OPTIONS(1)**

| $T_A$ | $V_{IO}$max AT 25°C | PACKAGED DEVICES | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | SMALL OUTLINE† (D) | MSOP (DGK)† | MSOP SYMBOL | MSOP (DGS)† | MSOP SYMBOL | PLASTIC DIP (N) | PLASTIC DIP (P) |
| 0°C to 70°C | 3000 µV | TLV2782CD<br>TLV2783CD | TLV2782CDGK<br>— | xxTIADL<br>— | —<br>TLV2783CDGS | —<br>xxTIADN | —<br>— | —<br>— |
| −40°C to 125°C | 3000 µV | TLV2782ID<br>TLV2783ID | TLV2782IDGK<br>— | xxTIADM<br>— | —<br>TLV2783IDGS | —<br>xxTIADO | —<br>TLV2783IN | TLV2782IP<br>— |
| | 2000 µV | TLV2782AID<br>TLV2783AID | —<br>— | —<br>— | —<br>— | —<br>— | —<br>— | —<br>— |

† This package is available taped and reeled. To order this packaging option, add an **R** suffix to the part number (e.g., TLV2782CDR).

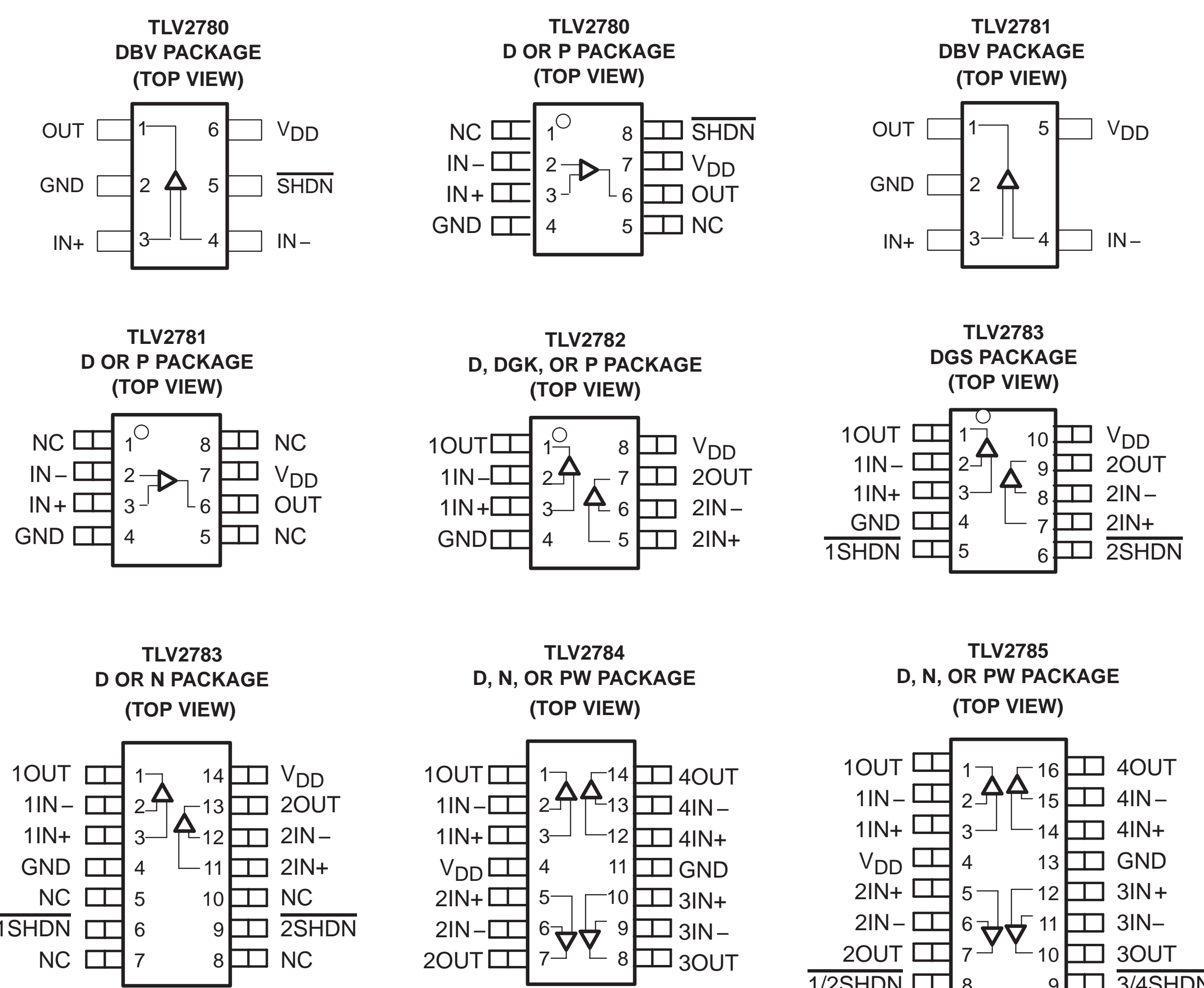
**TLV2784 and TLV2785 AVAILABLE OPTIONS(1)**

| $T_A$ | $V_{IO}$max AT 25°C | PACKAGED DEVICES | | |
|---|---|---|---|---|
| | | SMALL OUTLINE (D) | PLASTIC DIP (N) | TSSOP† (PW) |
| 0°C to 70°C | 3000 µV | TLV2784CD<br>TLV2785CD | —<br>— | TLV2784CPW<br>TLV2785CPW |
| −40°C to 125°C | 3000 µV | TLV2784ID<br>TLV2785ID | TLV2784IN<br>TLV2785IN | TLV2784IPW<br>TLV2785IPW |
| | 2000 µV | TLV2784AID<br>TLV2785AID | —<br>— | TLV2784AIPW<br>TLV2785AIPW |

† This package is available taped and reeled. To order this packaging option, add an **R** suffix to the part number (e.g., TLV2784CDR).

1. For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

## TLV278x PACKAGE PINOUTS




NC – No internal connection

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, $V_{DD}$ (see Note 1) . . . 4 V
Differential input voltage, $V_{ID}$ . . . $\pm V_{DD}$
Input current, $I_I$ (any input) . . . ± 10 mA
Output current, $I_O$ . . . ± 10 mA
Continuous total power dissipation . . . See Dissipation Rating Table
Operating free-air temperature range, $T_A$: C-suffix . . . 0°C to 70°C
I-suffix . . . −40°C to 125°C
Maximum junction temperature, $T_J$ . . . 150°C
Storage temperature range, $T_{stg}$ . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values, except differential voltages, are with respect to GND.

**DISSIPATION RATING TABLE**

| PACKAGE | $\Theta_{JC}$ (°C/W) | $\Theta_{JA}$ (°C/W) | $T_A \leq 25°C$ POWER RATING | $T_A = 125°C$ POWER RATING |
|---|---|---|---|---|
| D (8) | 38.3 | 176 | 710 mW | 142 mW |
| D (14) | 26.9 | 122.3 | 1022 mW | 204.4 mW |
| D (16) | 25.7 | 114.7 | 1090 mW | 218 mW |
| DBV (5) | 55 | 324.1 | 385 mW | 77.1 mW |
| DBV (6) | 55 | 294.3 | 425 mW | 85 mW |
| DGK (8) | 54.2 | 259.9 | 481 mW | 96.2 mW |
| DGS (10) | 54.1 | 257.7 | 485 mW | 97 mW |
| N (14, 16) | 32 | 78 | 1600 mW | 320.5 mW |
| P (8) | 41 | 104 | 1200 mW | 240.4 mW |
| PW (14) | 29.3 | 173.6 | 720 mW | 144 mW |
| PW (16) | 28.7 | 161.4 | 774 mW | 154.9 mW |

## recommended operating conditions

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| Supply voltage, $V_{DD}$ | Single supply | | 1.8 | 3.6 | V |
| | Split supply | | ±0.9 | ±1.8 | |
| Common-mode input voltage range, $V_{ICR}$ | | | −0.2 | $V_{DD}$+0.2 | V |
| Operating free-air temperature, $T_A$ | C-suffix | | 0 | 70 | °C |
| | I-suffix | | −40 | 125 | |
| Shutdown on/off voltage level‡ | $V_{IH}$ | $V_{DD}$ < 2.7 V | $0.75V_{DD}$ | | V |
| | | $V_{DD}$ = 2.7 to 3.6 V | 2 | | |
| | $V_{IL}$ | | | 0.6 | |

‡ Relative to GND.

## electrical characteristics at specified free-air temperature, $V_{DD}$ = 1.8 V, 2.7 V (unless otherwise noted)

### dc performance

| PARAMETER | | TEST CONDITIONS | | $T_A$† | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{IO}$ | Input offset voltage | $V_O = V_{DD}/2$, $R_L$ = 2 kΩ, $R_S$ = 50 Ω | TLV278x | 25°C | | 250 | 3000 | µV |
| | | | | Full range | | | 4500 | |
| | | | TLV278xA | 25°C | | 250 | 2000 | |
| | | | | Full range | | | 3000 | |
| $\alpha_{VIO}$ | Temperature coefficient of input offset voltage | | | | | 8 | | µV/°C |
| CMRR | Common-mode rejection ratio | $V_{IC}$ = 0 to $V_{DD}$, $R_S$ = 50 Ω | $V_{DD}$ = 1.8 V | 25°C | 50 | 76 | | dB |
| | | | | Full range | 50 | | | |
| | | | $V_{DD}$ = 2.7 V/ 3.6 V | 25°C | 55 | 80 | | |
| | | | | Full range | 50 | | | |
| | | $V_{IC}$ = 1.2 V to $V_{DD}$, $R_S$ = 50 Ω | $V_{DD}$ = 2.7 V/ 3.6 V | 25°C | 70 | 100 | | |
| | | | | Full range | 70 | | | |
| $A_{VD}$ | Large-signal differential voltage amplification | $R_L$ = 2 kΩ, $V_{O(PP)}$ = 1 V | $V_{DD}$ = 1.8 V | 25°C | 200 | 600 | | V/mV |
| | | | | Full range | 50 | | | |
| | | | $V_{DD}$ = 2.7 V/ 3.6 V | 25°C | 200 | 1000 | | |
| | | | | Full range | 70 | | | |

† Full range is 0°C to 70°C for the C-suffix and –40°C to 125°C for the I-suffix. If not specified, full range is –40°C to 125°C.

### input characteristics

| PARAMETER | | TEST CONDITIONS | | $T_A$† | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $I_{IO}$ | Input offset current | $V_O = V_{DD}/2$, $R_L$ = 2 kΩ, $R_S$ = 50 Ω | | 25°C | | 2.5 | 15 | pA |
| | | | TLV278xC | Full range | | | 100 | |
| | | | TLV278xI | Full range | | | 300 | |
| $I_{IB}$ | Input bias current | | | 25°C | | 2.5 | 15 | pA |
| | | | TLV278xC | Full range | | | 100 | |
| | | | TLV278xI | Full range | | | 300 | |
| $r_{i(d)}$ | Differential input resistance | | | 25°C | | 1000 | | GΩ |
| $C_{i(c)}$ | Common-mode input capacitance | f = 1 kHz | | 25°C | | 19 | | pF |

† Full range is 0°C to 70°C for the C-suffix and –40°C to 125°C for the I-suffix. If not specified, full range is –40°C to 125°C.

## electrical characteristics at specified free-air temperature, $V_{DD}$ = 1.8 V, 2.7 V (unless otherwise noted) (continued)

### output characteristics

| PARAMETER | | TEST CONDITIONS | | $T_A$† | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = –1 mA | $V_{DD}$ = 1.8 V | 25°C | 1.7 | 1.77 | | V |
| | | | | Full range | 1.63 | | | |
| | | | $V_{DD}$ = 2.7 V | 25°C | 2.6 | 2.68 | | |
| | | | | Full range | 2.6 | | | |
| | | | $V_{DD}$ = 3.6 V | 25°C | | 3.58 | | |
| | | $I_{OH}$ = –5 mA | $V_{DD}$ = 1.8 V | 25°C | 1.5 | 1.55 | | |
| | | | | Full range | 1.46 | | | |
| | | | $V_{DD}$ = 2.7 V | 25°C | 2.5 | 2.55 | | |
| | | | | Full range | 2.45 | | | |
| | | | $V_{DD}$ = 3.6 V | 25°C | | 3.55 | | |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 1 mA | | 25°C | | | 70 | mV |
| | | | | Full range | | | 80 | |
| | | $I_{OL}$ = 5 mA | $V_{DD}$ = 1.8 V | 25°C | | 180 | 240 | |
| | | | | Full range | | | 290 | |
| | | | $V_{DD}$ = 2.7 V | 25°C | | 120 | 170 | |
| | | | | Full range | | | 200 | |
| $I_O$ | Output current | $V_{DD}$ = 1.8 V, VO = 0.5 V from | Positive rail | 25°C | | 10 | | mA |
| | | | Negative rail | | | 15 | | |
| | | $V_{DD}$ = 2.7 V, VO = 0.5 V from | Positive rail | | | 17 | | |
| | | | Negative rail | | | 23 | | |
| $I_{OS}$ | Short-circuit output current | Sourcing | $V_{DD}$ = 1.8 V | 25°C | | 13 | | mA |
| | | | $V_{DD}$ = 2.7 V | | | 35 | | |
| | | Sinking | $V_{DD}$ = 1.8 V | | | 21 | | |
| | | | $V_{DD}$ = 2.7 V | | | 45 | | |

† Full range is 0°C to 70°C for the C-suffix and –40°C to 125°C for the I-suffix. If not specified, full range is –40°C to 125°C.

### power supply

| PARAMETER | | TEST CONDITIONS | | $T_A$† | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $I_{DD}$ | Supply current (per channel) | $V_O = V_{DD}/2$, | $\overline{SHDN} = V_{DD}$ | 25°C | | 650 | 770 | µA |
| | | | | Full range | | | 820 | |
| $k_{SVR}$ | Supply voltage rejection ratio ($\Delta V_{DD} / \Delta V_{IO}$) | $V_{DD}$ = 1.8 V to 2.7 V, $V_{IC} = V_{DD}/2$ | No load, | 25°C | 60 | 75 | | dB |
| | | | | Full range | 58 | | | |
| | | $V_{DD}$ = 2.7 V to 3.6 V, $V_{IC} = V_{DD}/2$ | No load, | 25°C | 75 | 90 | | |
| | | | | Full range | 70 | | | |
| | | $V_{DD}$ = 1.8 V to 3.6 V, $V_{IC} = V_{DD}/2$ | No load, | 25°C | 65 | 80 | | |
| | | | | Full range | 60 | | | |

† Full range is 0°C to 70°C for the C-suffix and –40°C to 125°C for the I-suffix. If not specified, full range is –40°C to 125°C.

## electrical characteristics at specified free-air temperature, $V_{DD}$ = 1.8 V, 2.7 V (unless otherwise noted) (continued)

### dynamic performance

| PARAMETER | | TEST CONDITIONS | | $T_A$† | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| UGBW | Unity gain bandwidth | $R_L$ = 2 kΩ, | $C_L$ = 25 pF | 25°C | | 8 | | MHz |
| SR+ | Positive slew rate at unity gain | $V_{O(PP)}$ = 1 V, $R_L$ = 2 kΩ, $C_L$ = 50 pF | $V_{DD}$ = 1.8 V | 25°C | 3.3 | 4.3 | | V/μs |
| | | | | Full range | 3.1 | | | |
| | | | $V_{DD}$ = 2.7 V | 25°C | 3.8 | 4.8 | | |
| | | | | Full range | 3.5 | | | |
| | | | $V_{DD}$ = 3.6 V | 25°C | 4 | 5 | | |
| | | | | Full range | 3.6 | | | |
| SR– | Negative slew rate at unity gain | $V_{O(PP)}$ = 1 V, $R_L$ = 2 kΩ, $C_L$ = 50 pF | $V_{DD}$ = 1.8 V | 25°C | 2.1 | 2.8 | | |
| | | | | Full range | 1.89 | | | |
| | | | $V_{DD}$ = 2.7 V | 25°C | 2.2 | 2.8 | | |
| | | | | Full range | 1.97 | | | |
| | | | $V_{DD}$ = 3.6 V | 25°C | 3.5 | 4.2 | | |
| | | | | Full range | 3.4 | | | |
| $\phi_m$ | Phase margin | $R_L$ = 2 kΩ, | $C_L$ = 25 pF | 25°C | | 58° | | |
| | Gain margin | | | | | 8 | | dB |
| $t_s$ | Settling time | $V_{DD}$ = 1.8 V, $V_{(STEP)PP}$ = 1 V, $A_V$ = –1, $C_L$ = 10 pF, $R_L$ = 2 kΩ | 0.1% | 25°C | | 1.7 | | μs |
| | | | 0.01% | | | 2.8 | | |
| | | $V_{DD}$ = 2.7 V, $V_{(STEP)PP}$ = 1 V, $A_V$ = –1, $C_L$ = 10 pF, $R_L$ = 2 kΩ | 0.1% | | | 1.7 | | |
| | | | 0.01% | | | 2.4 | | |

† Full range is 0°C to 70°C for the C-suffix and –40°C to 125°C for the I-suffix. If not specified, full range is –40°C to 125°C.

### noise/distortion performance

| PARAMETER | | TEST CONDITIONS | | $T_A$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| THD + N | Total harmonic distortion plus noise | $V_{O(PP)}$ = $V_{DD}$/2, $R_L$ = 2 kΩ, f = 10 kHz | $A_V$ = 1 | 25°C | | 0.055% | | |
| | | | $A_V$ = 10 | | | 0.08% | | |
| | | | $A_V$ = 100 | | | 0.45% | | |
| $V_n$ | Equivalent input noise voltage | f = 1 kHz | | | | 18 | | nV/√Hz |
| | | f = 10 kHz | | | | 9 | | |
| $I_n$ | Equivalent input noise current | f = 1 kHz | | | | 0.9 | | fA/√Hz |

### shutdown characteristics

| PARAMETER | | TEST CONDITIONS | $T_A$† | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{DD(SHDN)}$ | Supply current, per channel in shutdown mode (TLV2780, TLV2783, TLV2785) | $\overline{SHDN}$ = 0 V | 25°C | | 900 | 1400 | nA |
| | | | Full range | | | 1700 | |
| $t_{(on)}$ | Amplifier turnon time‡ | $R_L$ = 2 kΩ | 25°C | | 800 | | ns |
| $t_{(off)}$ | Amplifier turnoff time‡ | $R_L$ = 2 kΩ | | | 200 | | |

† Full range is 0°C to 70°C for the C-suffix and –40°C to 125°C for the I-suffix. If not specified, full range is –40°C to 125°C.
‡ Disable time and enable time are defined as the interval between application of the logic signal to $\overline{SHDN}$ and the point at which the supply current has reached half its final value.

## TYPICAL CHARACTERISTICS

### Table of Graphs

| | | | FIGURE |
|---|---|---|---|
| $V_{IO}$ | Input offset voltage | vs Common-mode input voltage | 1, 2 |
| CMRR | Common-mode rejection ratio | vs Frequency | 3 |
| $V_{OH}$ | High-level output voltage | vs High-level output current | 4, 6 |
| $V_{OL}$ | Low-level output voltage | vs Low-level output current | 5, 7 |
| $V_{O(PP)}$ | Maximum peak-to-peak output voltage | vs Frequency | 8 |
| $Z_o$ | Output impedance | vs Frequency | 9 |
| $I_{DD}$ | Supply current | vs Supply voltage | 10 |
| $I_{DD}$ | Supply current | vs Free-air temperature | 11 |
| PSRR | Power supply rejection ratio | vs Frequency | 12 |
| $A_{VD}$ | Differential voltage amplification & phase | vs Frequency | 13 |
| | Gain-bandwidth product | vs Free-air temperature | 14 |
| SR | Slew rate | vs Supply voltage | 15 |
| | | vs Free-air temperature | 16, 17 |
| $\phi_m$ | Phase margin | vs Load capacitance | 18 |
| $V_n$ | Equivalent input noise voltage | vs Frequency | 19 |
| | Voltage-follower large-signal pulse response | vs Time | 20 |
| | Voltage-follower small-signal pulse response | vs Time | 21 |
| | Inverting large-signal pulse response | vs Time | 22 |
| | Inverting small-signal pulse response | vs Time | 23 |
| | Crosstalk | vs Frequency | 24 |
| | Shutdown forward & reverse isolation | vs Frequency | 25 |
| $I_{DD(SHDN)}$ | Shutdown supply current | vs Free-air temperature | 26 |
| $I_{DD(SHDN)}$ | Shutdown supply current | vs Supply voltage | 27 |
| $I_{DD(SHDN)}$ | Shutdown supply current/output voltage | vs Time | 28 |

## TYPICAL CHARACTERISTICS

**INPUT OFFSET VOLTAGE vs COMMON-MODE INPUT VOLTAGE**

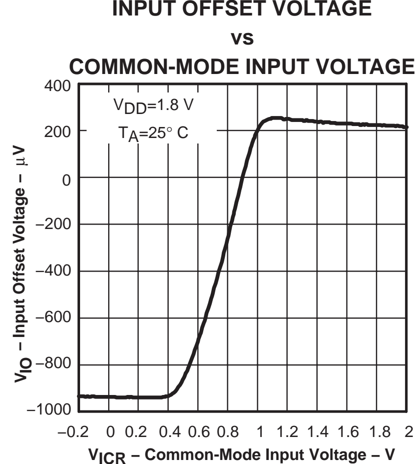



Figure 1

**INPUT OFFSET VOLTAGE vs COMMON-MODE INPUT VOLTAGE**

Figure 2

**COMMON-MODE REJECTION RATIO vs FREQUENCY**

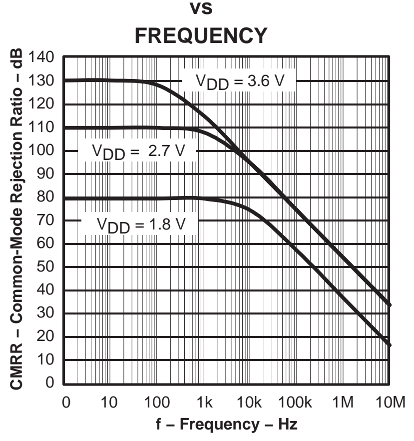



Figure 3

**HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT**

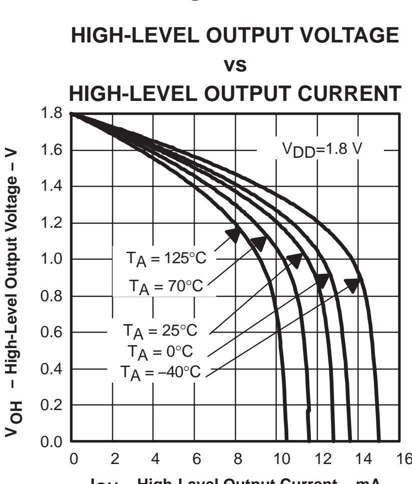



Figure 4

**LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT**

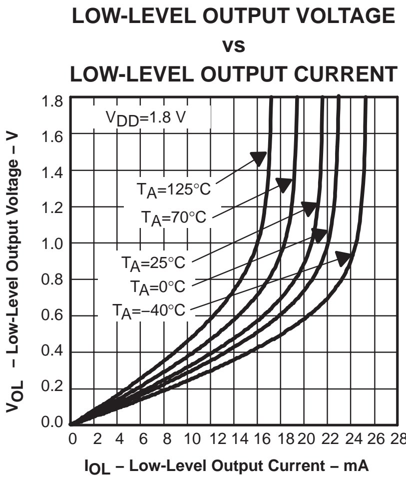



Figure 5

**HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT**

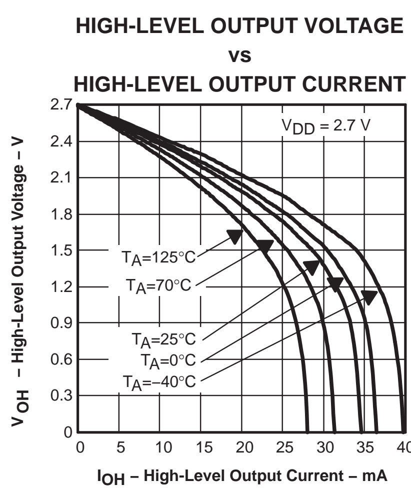



Figure 6

**LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT**

Figure 7

**MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs FREQUENCY**

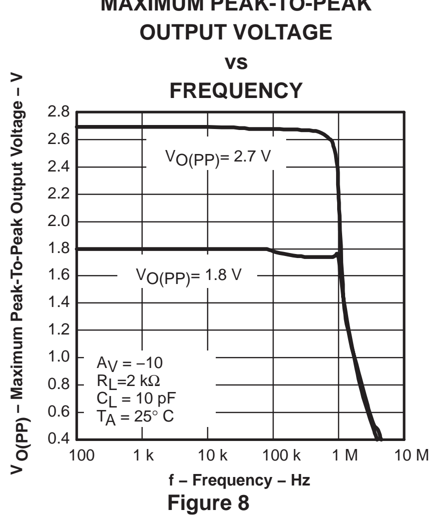



Figure 8

**OUTPUT IMPEDANCE vs FREQUENCY**

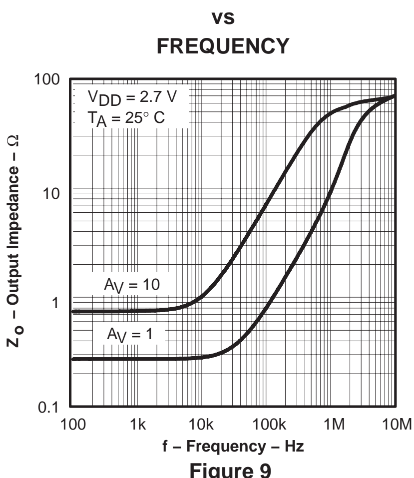



Figure 9

## TYPICAL CHARACTERISTICS

**SUPPLY CURRENT vs SUPPLY VOLTAGE**

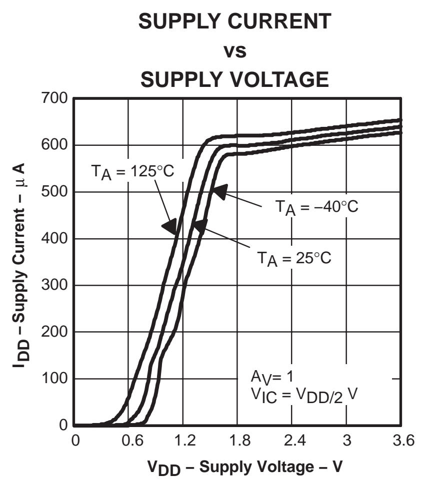



Figure 10

**SUPPLY CURRENT vs FREE-AIR TEMPERATURE**

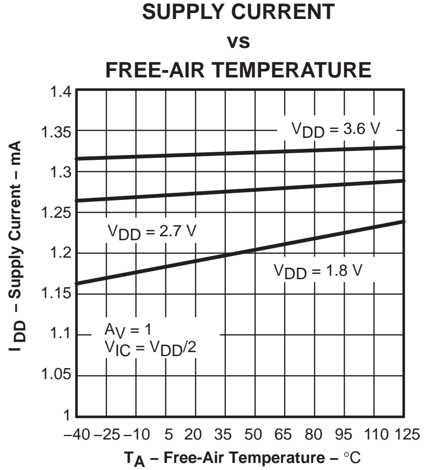



Figure 11

**POWER SUPPLY REJECTION RATIO vs FREQUENCY**

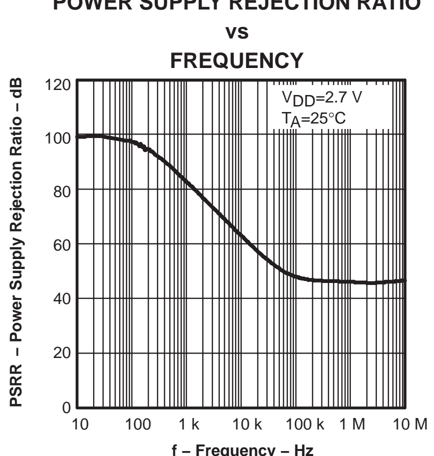



Figure 12

**DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE vs FREQUENCY**

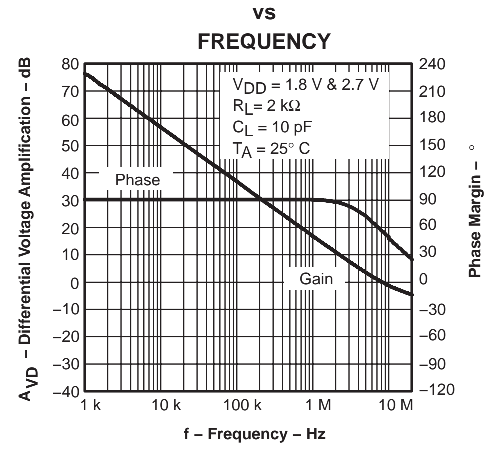



Figure 13

**GAIN-BANDWIDTH PRODUCT vs FREE-AIR TEMPERATURE**

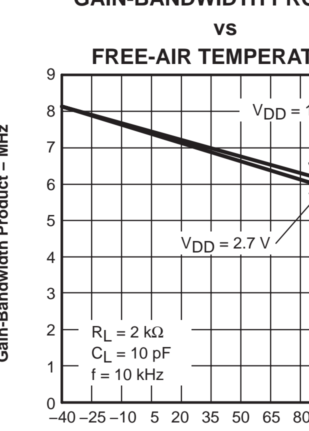



Figure 14

**SLEW RATE vs SUPPLY VOLTAGE**

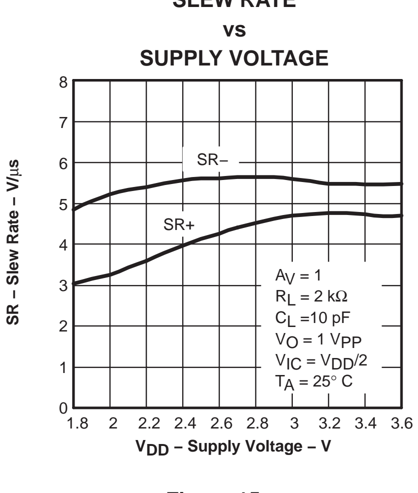



Figure 15

**SLEW RATE vs FREE-AIR TEMPERATURE**

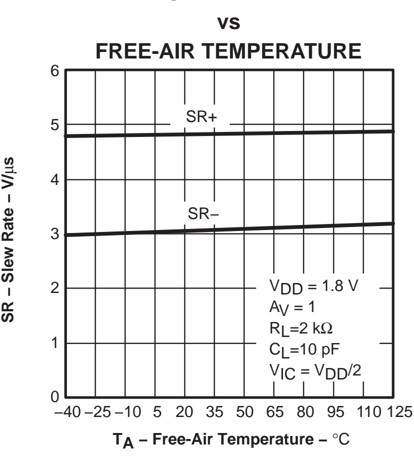



Figure 16

**SLEW RATE vs FREE-AIR TEMPERATURE**

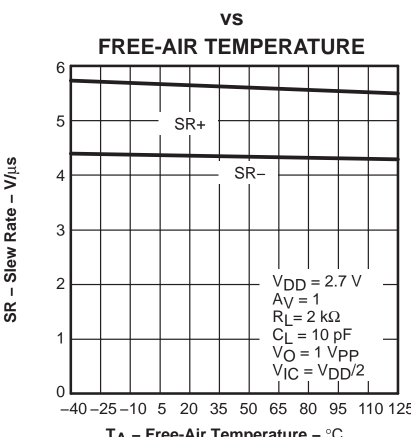



Figure 17

## TYPICAL CHARACTERISTICS

**PHASE MARGIN vs LOAD CAPACITANCE**

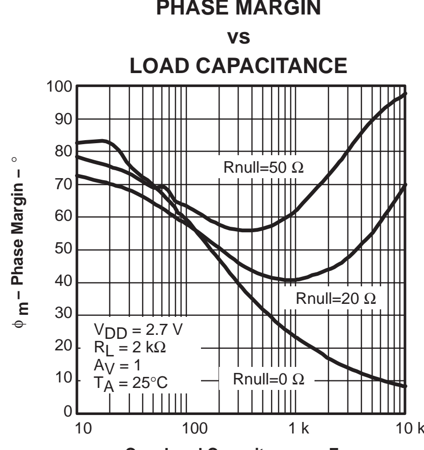



Figure 18

**EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY**

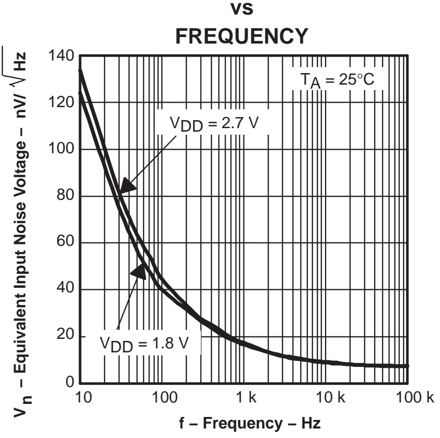



Figure 19

**VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE vs TIME**

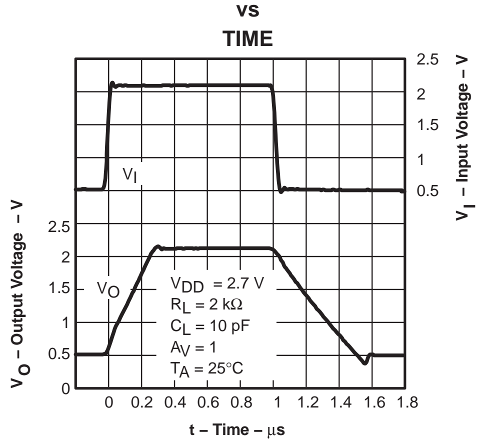



Figure 20

**VOLTAGE-FOLLOWER SMALL-SIGNAL PULSE RESPONSE vs TIME**

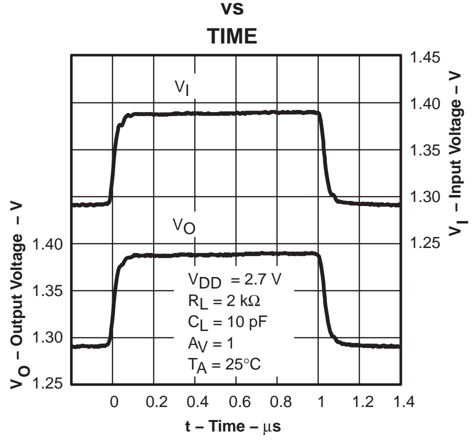



Figure 21

**INVERTING LARGE-SIGNAL PULSE RESPONSE vs TIME**

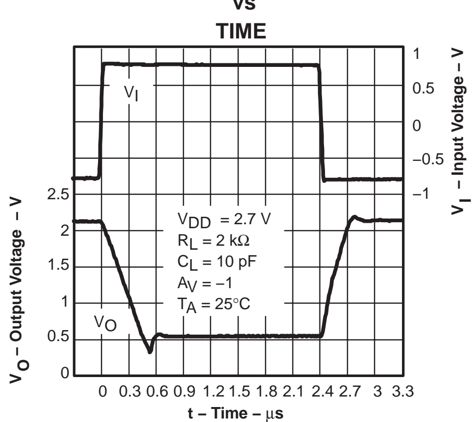



Figure 22

**INVERTING SMALL-SIGNAL PULSE RESPONSE vs TIME**

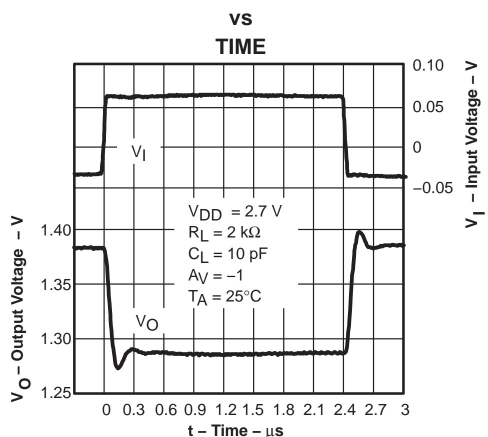



Figure 23

## TYPICAL CHARACTERISTICS

**CROSSTALK vs FREQUENCY**

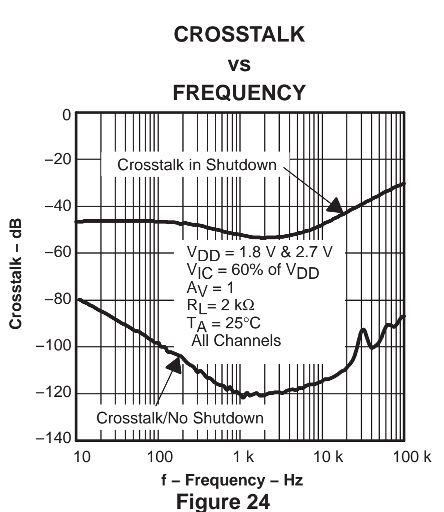



**Figure 24**

**SHUTDOWN FORWARD AND REVERSE ISOLATION vs FREQUENCY**

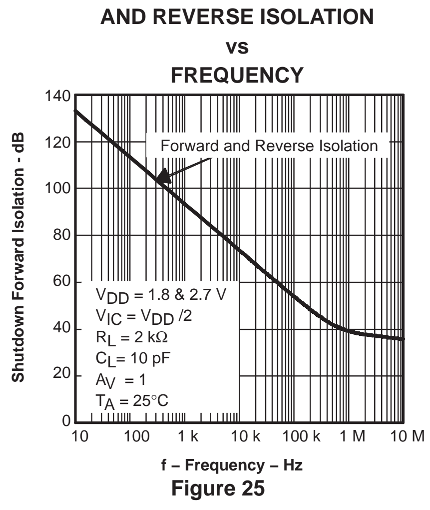



**Figure 25**

**SHUTDOWN SUPPLY CURRENT vs FREE-AIR TEMPERATURE**

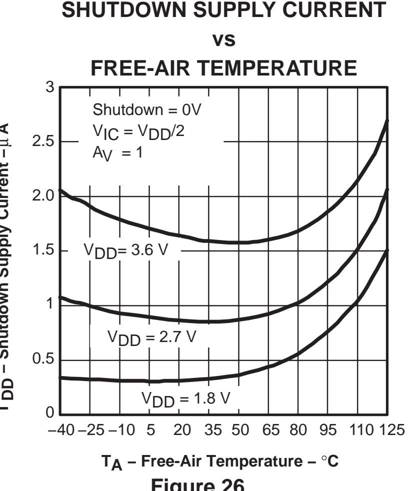



**Figure 26**

**SHUTDOWN SUPPLY CURRENT vs SUPPLY VOLTAGE**

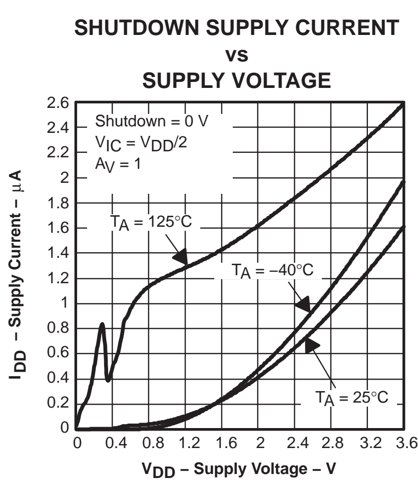


**Figure 27**

**SHUTDOWN SUPPLY CURRENT / OUTPUT VOLTAGE vs TIME**

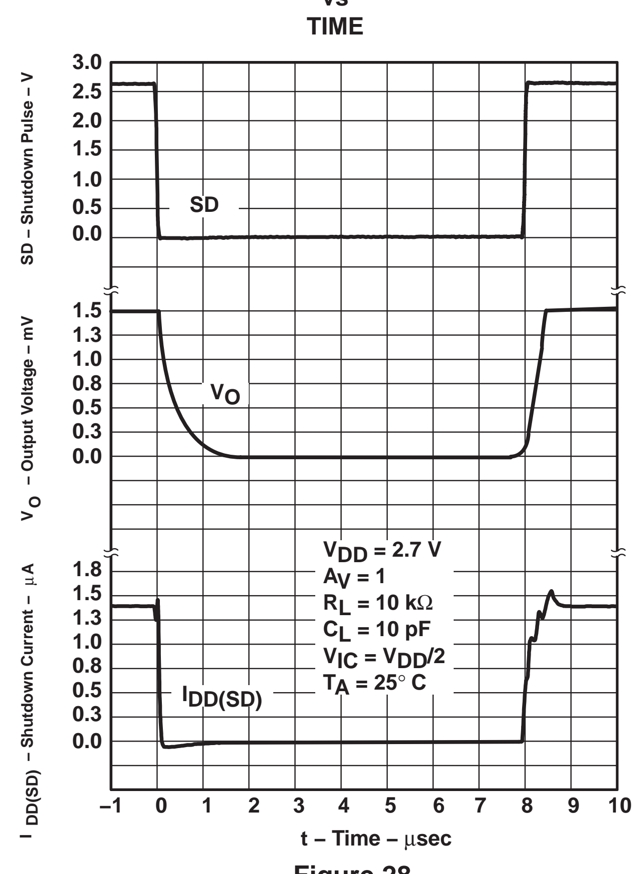



**Figure 28**

## PARAMETER MEASUREMENT INFORMATION

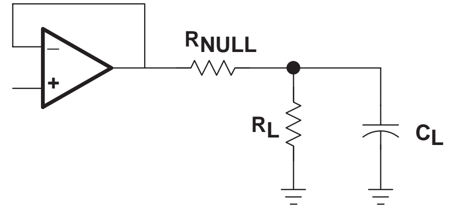



Figure 29

## APPLICATION INFORMATION

### driving a capacitive load

When the amplifier is configured in this manner, capacitive loading directly on the output will decrease the device's phase margin leading to high frequency ringing or oscillations. Therefore, for capacitive loads of greater than 10 pF, it is recommended that a resistor be placed in series ($R_{NULL}$) with the output of the amplifier, as shown in Figure 30.

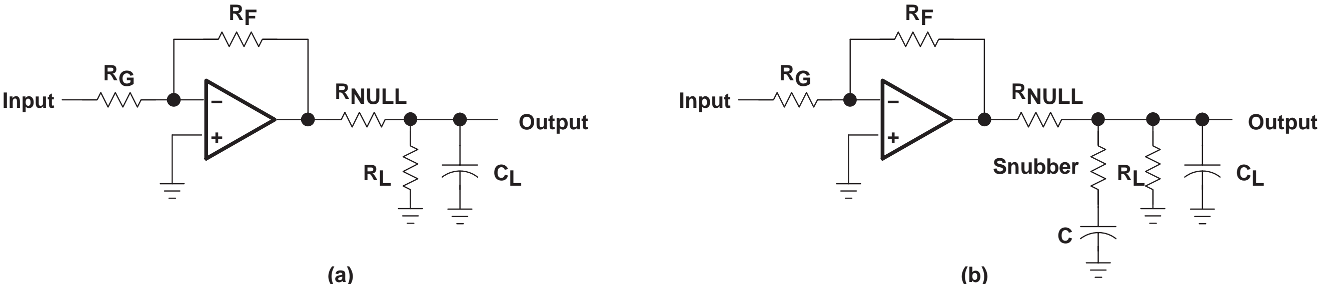
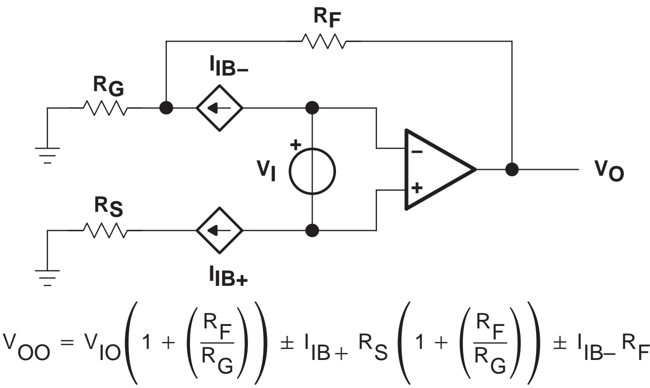



Figure 30. Driving a Capacitive Load

### offset voltage

The output offset voltage, ($V_{OO}$) is the sum of the input offset voltage ($V_{IO}$) and both input bias currents ($I_{IB}$) times the corresponding gains. The following schematic and formula can be used to calculate the output offset voltage:



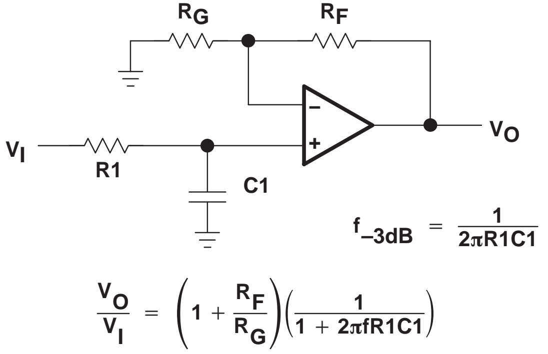

$$V_{OO} = V_{IO}\left(1 + \left(\frac{R_F}{R_G}\right)\right) \pm I_{IB+} R_S \left(1 + \left(\frac{R_F}{R_G}\right)\right) \pm I_{IB-} R_F$$

Figure 31. Output Offset Voltage Model

## APPLICATION INFORMATION

### general configurations

When receiving low-level signals, limiting the bandwidth of the incoming signals into the system is often required. The simplest way to accomplish this is to place an RC filter at the noninverting terminal of the amplifier (see Figure 32).

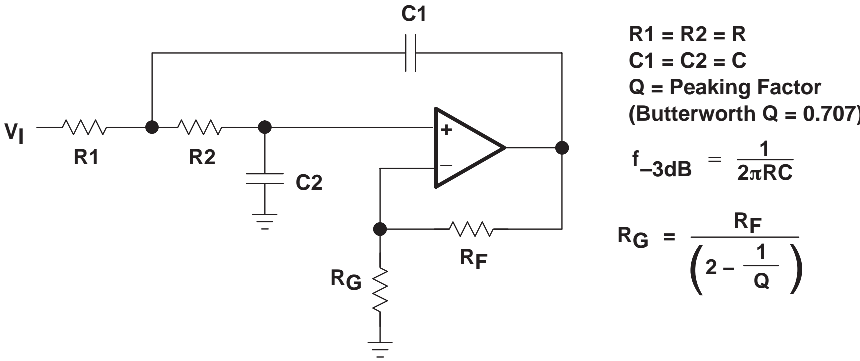



$$f_{-3dB} = \frac{1}{2\pi R1C1}$$

$$\frac{V_O}{V_I} = \left(1 + \frac{R_F}{R_G}\right)\left(\frac{1}{1 + 2\pi fR1C1}\right)$$

**Figure 32. Single-Pole Low-Pass Filter**

If even more attenuation is needed, a multiple pole filter is required. The Sallen-Key filter can be used for this task. For best results, the amplifier should have a bandwidth that is 8 to 10 times the filter frequency bandwidth. Failure to do this can result in phase shift of the amplifier.




R1 = R2 = R
C1 = C2 = C
Q = Peaking Factor
(Butterworth Q = 0.707)

$$f_{-3dB} = \frac{1}{2\pi RC}$$

$$R_G = \frac{R_F}{\left(2 - \frac{1}{Q}\right)}$$

**Figure 33. 2-Pole Low-Pass Sallen-Key Filter**

## APPLICATION INFORMATION

### circuit layout considerations

To achieve the levels of high performance of the TLV278x, follow proper printed-circuit board design techniques. A general set of guidelines is given in the following.

- Ground planes – It is highly recommended that a ground plane be used on the board to provide all components with a low inductive ground connection. However, in the areas of the amplifier inputs and output, the ground plane can be removed to minimize the stray capacitance.
- Proper power supply decoupling – Use a 6.8-µF tantalum capacitor in parallel with a 0.1-µF ceramic capacitor on each supply terminal. It may be possible to share the tantalum among several amplifiers depending on the application, but a 0.1-µF ceramic capacitor should always be used on the supply terminal of every amplifier. In addition, the 0.1-µF capacitor should be placed as close as possible to the supply terminal. As this distance increases, the inductance in the connecting trace makes the capacitor less effective. The designer should strive for distances of less than 0.1 inches between the device power terminals and the ceramic capacitors.
- Sockets – Sockets can be used but are not recommended. The additional lead inductance in the socket pins will often lead to stability problems. Surface-mount packages soldered directly to the printed-circuit board is the best implementation.
- Short trace runs/compact part placements – Optimum high performance is achieved when stray series inductance has been minimized. To realize this, the circuit layout should be made as compact as possible, thereby minimizing the length of all trace runs. Particular attention should be paid to the inverting input of the amplifier. Its length should be kept as short as possible. This will help to minimize stray capacitance at the input of the amplifier.
- Surface-mount passive components – Using surface-mount passive components is recommended for high performance amplifier circuits for several reasons. First, because of the extremely low lead inductance of surface-mount components, the problem with stray series inductance is greatly reduced. Second, the small size of surface-mount components naturally leads to a more compact layout, thereby minimizing both stray inductance and capacitance. If leaded components are used, it is recommended that the lead lengths be kept as short as possible.

### shutdown function

Three members of the TLV278x family (TLV2780/3/5) have a shutdown terminal for conserving battery life in portable applications. When the shutdown terminal is tied low, the supply current is reduced to 900 nA/channel, the amplifier is disabled, and the outputs are placed in a high impedance mode. To enable the amplifier, the shutdown terminal can either be left floating or pulled high. When the shutdown terminal is left floating, care should be taken to ensure that parasitic leakage current at the shutdown terminal does not inadvertently place the operational amplifier into shutdown.

## APPLICATION INFORMATION

### general power dissipation considerations

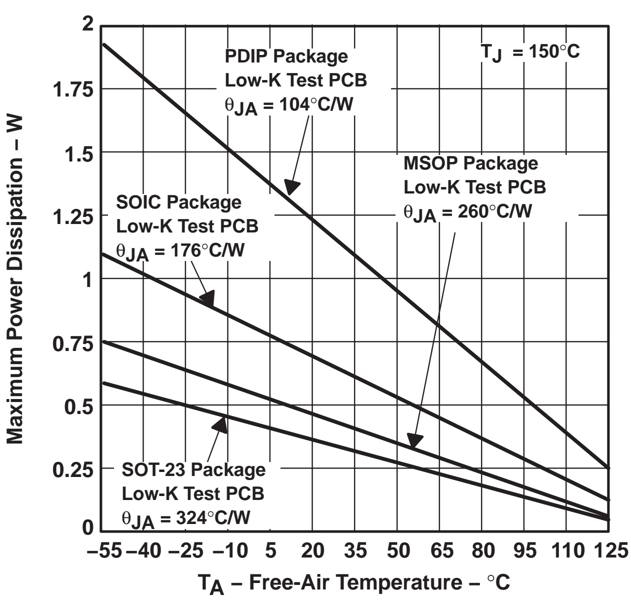
For a given $\theta_{JA}$, the maximum power dissipation is shown in Figure 34 and is calculated by the following formula:

$$P_D = \left(\frac{T_{MAX} - T_A}{\theta_{JA}}\right)$$

Where:

$P_D$ = Maximum power dissipation of TLV278x IC (watts)
$T_{MAX}$ = Absolute maximum junction temperature (150°C)
$T_A$ = Free-ambient air temperature (°C)
$\theta_{JA} = \theta_{JC} + \theta_{CA}$
$\theta_{JC}$ = Thermal coefficient from junction to case
$\theta_{CA}$ = Thermal coefficient from case to ambient air (°C/W)

MAXIMUM POWER DISSIPATION
vs
FREE-AIR TEMPERATURE




NOTE A: Results are with no air flow and using JEDEC Standard Low-K test PCB.

**Figure 34. Maximum Power Dissipation vs Free-Air Temperature**

## APPLICATION INFORMATION

### macromodel information

Macromodel information provided was derived using Microsim *Parts*™ Release 9.1, the model generation software used with Microsim *PSpice*™. The Boyle macromodel (see Note 2) and subcircuit in Figure 35 are generated using TLV278x typical electrical and operating characteristics at $T_A$ = 25°C. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 2: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, “Macromodeling of Integrated Circuit Operational Amplifiers,” *IEEE Journal of Solid-State Circuits,* SC-9, 353 (1974).

```
* TLV2782_HVDD operational amplifier ”macromodel” subcircuit
* created using Model Editor release 9.1 on 03/3/00 at 9:47
* Model Editor is an OrCAD product.
*
* connections:   non−inverting input
*                             | inverting input
*                             | | positive power supply
*                             | | | negative power supply
*                             | | | | output
*                             | | | | |
.subckt TLV2782_HVDD          1 2 3 4 5
*
      c1      11    12    49.58E−15
      c2      6     7     10.200E−12
      css     10    99    1.0000E−30
      dc      5     53    dy
      de      54    5     dy
      dlp     90    91    dx
      dln     92    90    dx
      dp      4     3     dx
      egnd    99    0     poly(2) (3,0) (4,0) 0 .5 .5
      fb      7     99    poly(5) vb vc ve vlp vln 0
                          41.096E6 −1E3 1E3 41E6
                          −41E6
ga      6     0     11 12  544.75E−6
gcm     0     6     10 99 1.1538E−9
iss     10    4     dc 56.957E−6
hlim    90    0     vlim 1K
j1      11    2     10 jx1
J2      12    1     10 jx2
r2      6     9     100.00E3
rd1     3     11    1.8357E3
rd2     3     12    1.8357E3
ro1     8     5     10
ro2     7     99    10
rp      3     4     2.1845E3
rss     10    99    3.5114E6
vb      9     0     dc 0
vc      3     53    dc .81911
ve      54    4     dc .81911
vlim    7     8     dc 0
vlp     91    0     dc 45.400
vln     0     92    dc 45.400
.model  dx    D(Is=800.00E−18)
.model  dy    D(Is=800.00E−18 Rs=1m Cjo=10p)
.model  jx1   NJF(Is=500.00E−15 Beta=5.2102E−3 Vto=−1)
.model  jx2   NJF(Is=500.00E−15 Beta=5.2102E−3 Vto=−1)
.ends
```

**Figure 35. Boyle Macromodel and Subcircuit**

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## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TLV2780CDBVR | ACTIVE | SOT-23 | DBV | 6 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | VASC | Samples |
| TLV2780CDBVT | ACTIVE | SOT-23 | DBV | 6 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | VASC | Samples |
| TLV2780CDBVTG4 | ACTIVE | SOT-23 | DBV | 6 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | VASC | Samples |
| TLV2780IDBVR | ACTIVE | SOT-23 | DBV | 6 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | VASI | Samples |
| TLV2780IDBVT | ACTIVE | SOT-23 | DBV | 6 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | VASI | Samples |
| TLV2780IDR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | T2780I | Samples |
| TLV2781CDBVR | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | VATC | Samples |
| TLV2781CDBVT | ACTIVE | SOT-23 | DBV | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | VATC | Samples |
| TLV2781CDBVTG4 | ACTIVE | SOT-23 | DBV | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | VATC | Samples |
| TLV2781ID | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | T2781I | Samples |
| TLV2781IDBVR | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | VATI | Samples |
| TLV2781IDBVRG4 | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | VATI | Samples |
| TLV2781IDBVT | ACTIVE | SOT-23 | DBV | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | VATI | Samples |
| TLV2781IDG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | T2781I | Samples |
| TLV2781IDR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | T2781I | Samples |
| TLV2782AID | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2782AI | Samples |
| TLV2782CD | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 2782C | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TLV2782CDG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 2782C | Samples |
| TLV2782CDGK | ACTIVE | VSSOP | DGK | 8 | 80 | Green (RoHS & no Sb/Br) | CU NIPDAU \| CU NIPDAUAG | Level-1-260C-UNLIM | 0 to 70 | ADL | Samples |
| TLV2782CDGKR | ACTIVE | VSSOP | DGK | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU \| CU NIPDAUAG | Level-1-260C-UNLIM | 0 to 70 | ADL | Samples |
| TLV2782CDGKRG4 | ACTIVE | VSSOP | DGK | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | ADL | Samples |
| TLV2782CDR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 2782C | Samples |
| TLV2782ID | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2782I | Samples |
| TLV2782IDGK | ACTIVE | VSSOP | DGK | 8 | 80 | Green (RoHS & no Sb/Br) | CU NIPDAU \| CU NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | ADM | Samples |
| TLV2782IDGKR | ACTIVE | VSSOP | DGK | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU \| CU NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | ADM | Samples |
| TLV2782IDR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2782I | Samples |
| TLV2782IP | ACTIVE | PDIP | P | 8 | 50 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -40 to 125 | TLV2782IP | Samples |
| TLV2783CDR | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TLV2783C | Samples |
| TLV2783IDGS | ACTIVE | VSSOP | DGS | 10 | 80 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | ADO | Samples |
| TLV2783IDGSG4 | ACTIVE | VSSOP | DGS | 10 | 80 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | ADO | Samples |
| TLV2783IDGSR | ACTIVE | VSSOP | DGS | 10 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | ADO | Samples |
| TLV2783IN | ACTIVE | PDIP | N | 14 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -40 to 125 | TLV2783I | Samples |
| TLV2784AID | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2784AI | Samples |
| TLV2784AIDR | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2784AI | Samples |
| TLV2784CPWR | ACTIVE | TSSOP | PW | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 2784C | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TLV2784ID | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | TLV2784I | Samples |
| TLV2784IDR | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | TLV2784I | Samples |
| TLV2784IPW | ACTIVE | TSSOP | PW | 14 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2784I | Samples |
| TLV2784IPWR | ACTIVE | TSSOP | PW | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2784I | Samples |
| TLV2785AID | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2785AI | Samples |
| TLV2785CPWR | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 2785C | Samples |
| TLV2785IDR | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | TLV2785I | Samples |
| TLV2785IN | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -40 to 125 | TLV2785I | Samples |
| TLV2785INE4 | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -40 to 125 | TLV2785I | Samples |
| TLV2785IPWR | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2785I | Samples |
| TLV2785IPWRG4 | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2785I | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

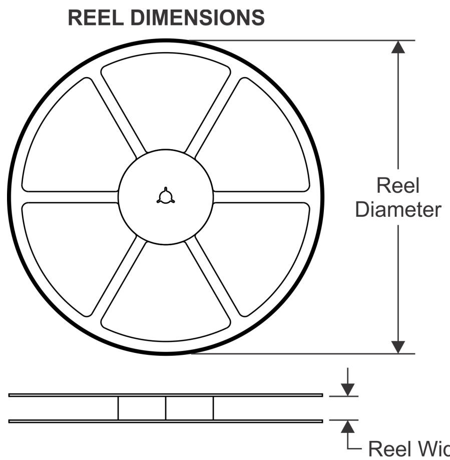
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

### REEL DIMENSIONS

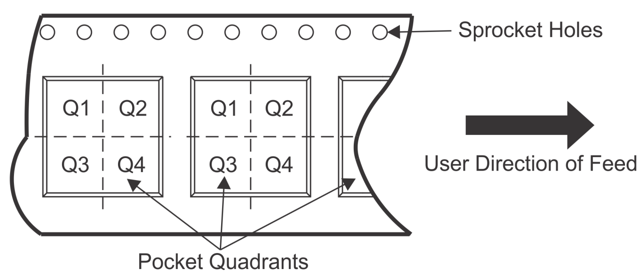



### TAPE DIMENSIONS

K0 P1 B0 W Cavity A0

| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

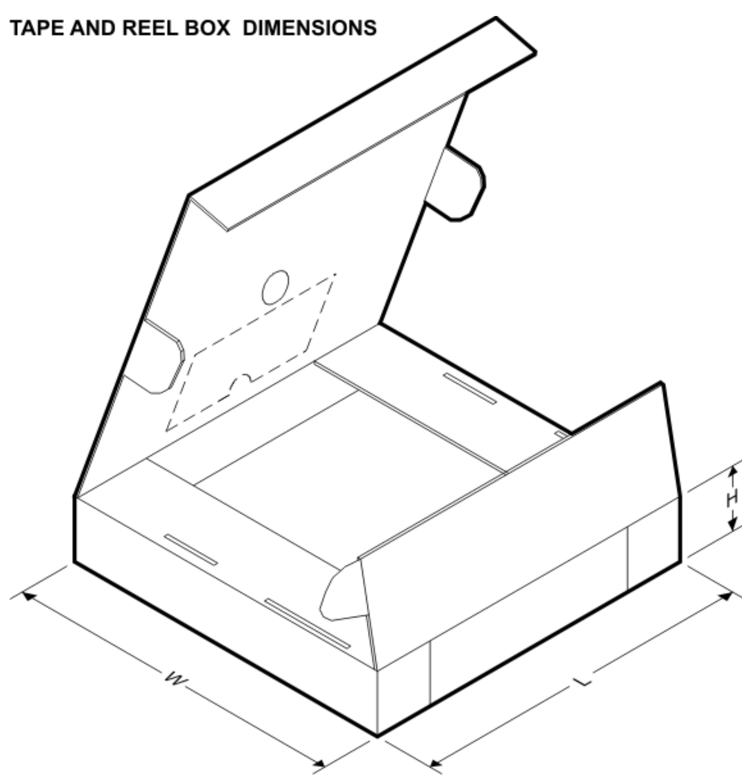
### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TLV2780CDBVR | SOT-23 | DBV | 6 | 3000 | 180.0 | 9.0 | 3.15 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV2780CDBVT | SOT-23 | DBV | 6 | 250 | 180.0 | 9.0 | 3.15 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV2780IDBVR | SOT-23 | DBV | 6 | 3000 | 180.0 | 9.0 | 3.15 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV2780IDBVT | SOT-23 | DBV | 6 | 250 | 180.0 | 9.0 | 3.15 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV2780IDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TLV2781CDBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 9.0 | 3.15 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV2781CDBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 9.0 | 3.15 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV2781IDBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 9.0 | 3.15 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV2781IDBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 9.0 | 3.15 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV2781IDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TLV2782CDGKR | VSSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| TLV2782CDGKR | VSSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| TLV2782CDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TLV2782IDGKR | VSSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| TLV2782IDGKR | VSSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| TLV2782IDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TLV2783CDR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| TLV2783IDGSR | VSSOP | DGS | 10 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TLV2784AIDR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| TLV2784CPWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| TLV2784IDR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| TLV2784IPWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| TLV2785CPWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| TLV2785IDR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| TLV2785IPWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TLV2780CDBVR | SOT-23 | DBV | 6 | 3000 | 182.0 | 182.0 | 20.0 |
| TLV2780CDBVT | SOT-23 | DBV | 6 | 250 | 182.0 | 182.0 | 20.0 |
| TLV2780IDBVR | SOT-23 | DBV | 6 | 3000 | 182.0 | 182.0 | 20.0 |
| TLV2780IDBVT | SOT-23 | DBV | 6 | 250 | 182.0 | 182.0 | 20.0 |
| TLV2780IDR | SOIC | D | 8 | 2500 | 367.0 | 367.0 | 38.0 |
| TLV2781CDBVR | SOT-23 | DBV | 5 | 3000 | 182.0 | 182.0 | 20.0 |
| TLV2781CDBVT | SOT-23 | DBV | 5 | 250 | 182.0 | 182.0 | 20.0 |
| TLV2781IDBVR | SOT-23 | DBV | 5 | 3000 | 182.0 | 182.0 | 20.0 |
| TLV2781IDBVT | SOT-23 | DBV | 5 | 250 | 182.0 | 182.0 | 20.0 |
| TLV2781IDR | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TLV2782CDGKR | VSSOP | DGK | 8 | 2500 | 358.0 | 335.0 | 35.0 |
| TLV2782CDGKR | VSSOP | DGK | 8 | 2500 | 364.0 | 364.0 | 27.0 |
| TLV2782CDR | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |
| TLV2782IDGKR | VSSOP | DGK | 8 | 2500 | 364.0 | 364.0 | 27.0 |
| TLV2782IDGKR | VSSOP | DGK | 8 | 2500 | 358.0 | 335.0 | 35.0 |
| TLV2782IDR | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |
| TLV2783CDR | SOIC | D | 14 | 2500 | 367.0 | 367.0 | 38.0 |
| TLV2783IDGSR | VSSOP | DGS | 10 | 2500 | 358.0 | 335.0 | 35.0 |
| TLV2784AIDR | SOIC | D | 14 | 2500 | 367.0 | 367.0 | 38.0 |
| TLV2784CPWR | TSSOP | PW | 14 | 2000 | 367.0 | 367.0 | 35.0 |
| TLV2784IDR | SOIC | D | 14 | 2500 | 367.0 | 367.0 | 38.0 |
| TLV2784IPWR | TSSOP | PW | 14 | 2000 | 367.0 | 367.0 | 35.0 |
| TLV2785CPWR | TSSOP | PW | 16 | 2000 | 367.0 | 367.0 | 35.0 |
| TLV2785IDR | SOIC | D | 16 | 2500 | 367.0 | 367.0 | 38.0 |
| TLV2785IPWR | TSSOP | PW | 16 | 2000 | 367.0 | 367.0 | 35.0 |

DBV (R-PDSO-G6) PLASTIC SMALL-OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
- E. Falls within JEDEC MO-178 Variation AB, except minimum lead width.

DBV (R-PDSO-G6) PLASTIC SMALL OUTLINE

Example Board Layout

Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).

1,00

0,55

2,7

2,7

0,95

0,95

0,6

Solder Mask Opening

1,05

Pad Geometry

0,07
All Around

4209593-4/C 08/11

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE

0.394 (10,00)
0.386 (9,80) C

16 9

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80) D

1 8

Pin 1
Index Area

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)
0.010 (0,25) M

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.005 (0,13)

Gauge Plane

Seating Plane

0.004 (0,10)

0.010 (0,25)

0°–8°

0.050 (1,27)
0.016 (0,40)

4040047–6/M 06/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16) PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)

14x1,27

5,40

Stencil Openings
(Note D)

16x0,55

14x1,27

16x1,50

5.40

Example
Non Soldermask Defined Pad

Example
Pad Geometry
(See Note C)

0,60

1,55

Example
Solder Mask Opening
(See Note E)

0,07
All Around

4211283-4/E 08/12

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE

0.344 (8,75)
0.337 (8,55)
C
14
8
0.244 (6,20)
0.228 (5,80)
0.157 (4,00)
0.150 (3,80)
D
1
7
Pin 1
Index Area
0.050 (1,27)
0.020 (0,51)
0.012 (0,31)
0.010 (0,25) M
0.069 (1,75) Max
0.010 (0,25)
0.004 (0,10)
0.010 (0,25)
0.005 (0,13)
Gauge Plane
0.004 (0,10)
Seating Plane
0.010 (0,25)
0°–8°
0.050 (1,27)
0.016 (0,40)

4040047–5/M 06/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14) PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)

12x1,27

5,40

Stencil Openings
(Note D)

14x0,55

12x1,27

14x1,50

5,40

Example
Non Soldermask Defined Pad

Example
Pad Geometry
(See Note C)

0,60

1,55

Example
Solder Mask Opening
(See Note E)

0.07
All Around

4211283-3/E 08/12

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14) PLASTIC SMALL OUTLINE

4040064-3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO-153

PW (R-PDSO-G14) PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)

12x0,65

5,60

Stencil Openings
(Note D)

14x0,30

12x0,65

14x1,55

5,60

Example
Non Soldermask Defined Pad

Example
Pad Geometry
(See Note C)

0,35

1,60

Example
Solder Mask Opening
(See Note E)

0,07
All Around

4211284-2/G 08/15

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G16) PLASTIC SMALL OUTLINE

4040064-4/G 02/11

NOTES:

A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

B. This drawing is subject to change without notice.

C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.

D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.

E. Falls within JEDEC MO-153

PW (R–PDSO–G16) PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)

14x0,65

5,60

Stencil Openings
(Note D)

16x0,30

14x0,65

16x1,55

5,60

Example
Non Soldermask Defined Pad

Example
Pad Geometry
(See Note C)

0,35

1,60

Example
Solder Mask Opening
(See Note E)

0,07
All Around

4211284–3/G 08/15

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE

0.197 (5,00)
0.189 (4,80)
C
8
5
0.244 (6,20)
0.228 (5,80)
0.157 (4,00)
0.150 (3,80)
D
Pin 1 Index Area
1
4
0.050 (1,27)
0.020 (0,51)
0.012 (0,31)
0.010 (0,25) M
0.069 (1,75) Max
0.010 (0,25)
0.004 (0,10)
0.010 (0,25)
0.005 (0,13)
Gauge Plane
0.004 (0,10)
Seating Plane
0.010 (0,25)
0°–8°
0.050 (1,27)
0.016 (0,40)

4040047–3/M 06/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS-012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)

6x1,27

5,40

Stencil Openings
(Note D)

8x0,55

6x1,27

8x1,50

5,40

Example
Non Soldermask Defined Pad

Example
Pad Geometry
(See Note C)

0,60

1,55

Example
Solder Mask Opening
(See Note E)

0,07
All Around

4211283–2/E 08/12

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE

0.400 (10,16)
0.355 (9,02)
8
5
0.260 (6,60)
0.240 (6,10)
1
4
0.070 (1,78)
0.045 (1,14)
0.045 (1,14)
0.030 (0,76)
0.020 (0,51) MIN
0.200 (5,08) MAX
Seating Plane
0.125 (3,18) MIN
0.100 (2,54)
0.021 (0,53)
0.015 (0,38)
⌖ 0.010 (0,25) Ⓜ
0.325 (8,26)
0.300 (7,62)
0.015 (0,38)
Gauge Plane
0.010 (0,25) NOM
0.430 (10,92)
MAX

4040082/E 04/2010

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

# N (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS–001 VARIATION (C) | AA | BB | AC | AD |

A
16
9
1
8
0.260 (6,60)
0.240 (6,10)
0.070 (1,78)
0.045 (1,14) (D)
0.045 (1,14)
0.030 (0,76) (D)
0.020 (0,51) MIN
0.200 (5,08) MAX
Seating Plane
0.125 (3,18) MIN
0.100 (2,54)
0.021 (0,53)
0.015 (0,38)
⌖ 0.010 (0,25) Ⓜ
14/18 Pin Only
20 Pin vendor option (D)
0.325 (8,26)
0.300 (7,62)
0.015 (0,38)
Gauge Plane
0.010 (0,25) NOM
0.430 (10,92) MAX

4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
(C) Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
(D) The 20 pin end lead shoulder width is a vendor option, either half or full width.

DBV (R-PDSO-G5) PLASTIC SMALL-OUTLINE PACKAGE

4073253-4/N 12/14

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Falls within JEDEC MO-178 Variation AA.

DBV (R-PDSO-G5) PLASTIC SMALL OUTLINE

Example Board Layout

Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).

1,90

1,90

1,00

0,55

2,7

2,7

0,95

0,95

0,6

Solder Mask Opening

1,05

Pad Geometry

0,07
All Around

4209593-3/C 08/11

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC-7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

## DGK (S-PDSO-G8) PLASTIC SMALL-OUTLINE PACKAGE

4073329/E 05/06

NOTES:

A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.

D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.

E. Falls within JEDEC MO-187 variation AA, except interlead flash.

DGK (S-PDSO-G8) PLASTIC SMALL OUTLINE PACKAGE

Example Board Layout

(0,65)TYP.

8 5

PKG ℄ (4,4)

1 4

PKG ℄

Example
Non Soldermask Defined Pad

(0,45)

(1,45)

(0,05)
All Around

Example
Solder Mask Opening
(See Note E)

Pad Geometry
(See Note C)

Example Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).
(See Note D)

8X(0,45)

(0,65)TYP.

8X(1,45)

PKG ℄ (4,4)

PKG ℄

4221236/A 11/13

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## DGS (S-PDSO-G10) PLASTIC SMALL-OUTLINE PACKAGE

4073272/C 02/04

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion.
- D. Falls within JEDEC MO-187 variation BA.

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