TEXAS INSTRUMENTS

TLV3401, TLV3402, TLV3404

SLCS135B – AUGUST 2000 – REVISED JANUARY 2017

# TLV340x Family of Nanopower, Open-Drain Output Comparators

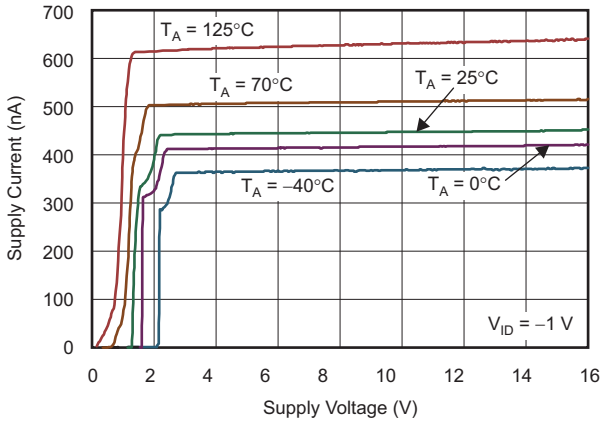
## 1 Features

- Low Supply Current: 470 nA Per Channel
- Input Common-Mode Range Exceeds the Rails: –0.1 V to $V_{CC}$ + 5 V
- Supply Voltage Range: 2.5 V to 16 V
- Reverse Battery Protection Up to 18 V
- Open-Drain CMOS Output Stage
- Specified Temperature Range:
  - Commercial Grade: 0°C to +70°C
  - Industrial Grade: –40°C to +125°C
- Ultra-Small Packaging:
  - 5-Pin SOT-23 (TLV3401)
  - 8-Pin MSOP (TLV3402)
- Universal Op Amp EVM (See *Universal Operational Amplifier Evaluation Module Selection Guide* For More Information)

## 2 Applications

- Portable Medical Equipment
- Wireless Security Systems
- Remote Control Systems
- Handheld Instruments
- Ultra-Low Power Systems

**Supply Current vs Supply Voltage**




## 3 Description

The TLV340x is TI's first family of nanopower comparators with only 470 nA per channel supply current, which makes this device ideal for battery-powered and wireless handset applications.

The TLV340x has a minimum operating supply voltage of 2.7 V over the extended industrial temperature range ($T_A$ = –40°C to +125°C), while having an input common-mode range of –0.1 to $V_{CC}$ + 5 V. The low supply current makes it an ideal choice for battery-powered portable applications where quiescent current is the primary concern. Reverse battery protection guards the amplifier from an overcurrent condition due to improper battery installation. For harsh environments, the inputs can be taken 5 V above the positive supply rail without damage to the device.

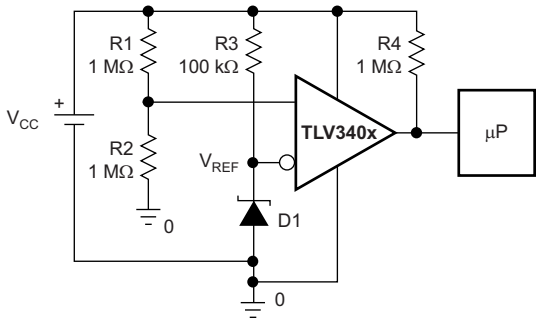
All members are available in PDIP and SOIC with the single versions in the small SOT-23 package, dual versions in the VSSOP package, and quad versions in the TSSOP package.

**Device Information(1)**

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| TLV3401 | SOT-23 (5) | 2.90 mm × 1.60 mm |
| TLV3401, TLV3402 | SOIC (8) | 4.90 mm × 3.91 mm |
| TLV3401, TLV3402 | PDIP (8) | 9.81 mm × 6.35 mm |
| TLV3402 | VSSOP (8) | 3.00 mm × 3.00 mm |
| TLV3404 | SOIC (14) | 8.65 mm × 3.91 mm |
| | TSSOP (14) | 5.00 mm × 4.40 mm |
| | PDIP (14) | 19.30 mm × 6.35 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

**High-Side Voltage Sense Circuit**



# Table of Contents



## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision A (November 2000) to Revision B | Page |
|---|---|
| • Added *ESD Rating* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section; | 1 |
| • Deleted *Available Options* tables; refer to *Package Option Addendum* at the end of this data sheet | 3 |
| • Deleted *Dissipation Ratings* table | 6 |

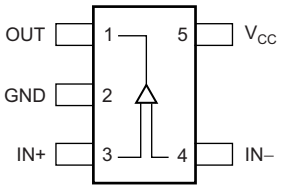
# 5 Device Comparison Table

| DEVICE(1) | $V_{CC}$ (V) | $V_{IO}$ (µV) | $I_{CC}$/Ch (µA) | $I_{IB}$ (pA) | $t_{PLH}$ (µs) | $t_{PHL}$ (µs) | $t_F$ (µs) | $t_R$ (µs) | RAIL-TO-RAIL | OUTPUT STAGE |
|---|---|---|---|---|---|---|---|---|---|---|
| TLV340x | 2.5 to 16 | 250 | 0.47 | 80 | 55 | 30 | 5 | — | Input | OD |
| TLV370x | 2.5 to 16 | 250 | 0.47 | 80 | 25 | 30 | 5 | 3.5 | Input | PP |
| TLC3702/4 | 3 to 16 | 1200 | 9 | 5 | 1.1 | 0.65 | 0.5 | 0.125 | — | PP |
| TLC393/339 | 3 to 16 | 1400 | 11 | 5 | 1.1 | 0.55 | 0.22 | — | — | OD |
| TLC372/4 | 3 to 16 | 1000 | 75 | 5 | 0.65 | 0.65 | — | — | — | OD |

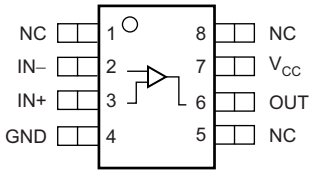
(1) All specifications are typical values measured at 5 V.

# 6 Pin Configuration and Functions

**TLV3401: DBV Package**
**5-Pin SOT-23**
**Top View**



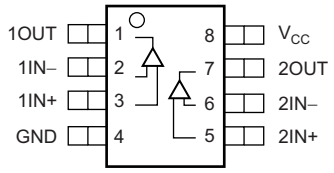

**TLV3401: D and P Packages**
**8-Pin SOIC and VSSOP**
**Top View**




**Pin Functions: TLV3401**

| PIN | | | I/O | DESCRIPTION |
|---|---|---|---|---|
| NAME | TLV3401 | | | |
| | SOT-23 | SOIC, PDIP | | |
| GND | 2 | 4 | — | Ground |
| IN– | 4 | 2 | I | Negative (inverting) input |
| IN+ | 3 | 3 | I | Positive (noninverting) input |
| NC | — | 1, 5, 8 | — | No internal connection (can be left floating) |
| OUT | 1 | 6 | O | Output |
| $V_{CC}$ | 5 | 7 | — | Positive power supply |

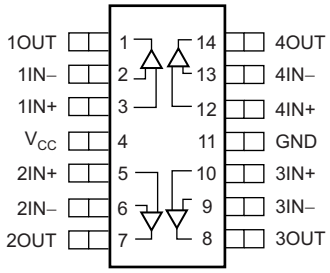
**TLV3402: D, DGK, and P Packages**
**8-PIN SOIC, PDIP, and VSSOP**
**Top View**




**Pin Functions: TLV3402**

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | TLV3402 | | |
| | SOIC, PDIP, VSSOP | | |
| GND | 4 | — | Ground |
| 1IN– | 2 | I | Inverting input, channel 1 |
| 2IN– | 6 | I | Inverting input, channel 2 |
| 1IN+ | 3 | I | Noninverting input, channel 1 |
| 2IN+ | 5 | I | Noninverting input, channel 2 |
| 1OUT | 1 | O | Output, channel 1 |
| 2OUT | 7 | O | Output, channel 2 |
| $V_{CC}$ | 8 | — | Positive power supply |

**TLV3404: D, N, and PW Packages**
**14-PIN SOIC, PDIP, TSSOP**
**Top View**




## Pin Functions: TLV3404

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | TLV3404 SOIC, PDIP, TSSOP | | |
| GND | 11 | — | Ground |
| 1IN– | 2 | I | Inverting input, channel 1 |
| 2IN– | 6 | I | Inverting input, channel 2 |
| 3IN– | 9 | I | Inverting input, channel 3 |
| 4IN– | 13 | I | Inverting input, channel 4 |
| 1IN+ | 3 | I | Noninverting input, channel 1 |
| 2IN+ | 5 | I | Noninverting input, channel 2 |
| 3IN+ | 10 | I | Noninverting input, channel 3 |
| 4IN+ | 12 | I | Noninverting input, channel 4 |
| 1OUT | 1 | O | Output, channel 1 |
| 2OUT | 7 | O | Output, channel 2 |
| 3OUT | 8 | O | Output, channel 3 |
| 4OUT | 14 | O | Output, channel 4 |
| $V_{CC}$ | 4 | — | Positive power supply |

# 7 Specifications

## 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| Voltage | Supply, $V_{CC}$(2) | | | 17 | V |
| | Differential input, $V_{ID}$ | | –20 | 20 | |
| | Input, $V_I$(2)(3) | | 0 | $V_{CC}$ + 5 | |
| Current | Input, $I_I$ | | –10 | 10 | mA |
| | Output, $I_O$ | | –10 | 10 | |
| Temperature | Operating, $T_A$ | C-suffix versions | 0 | 70 | °C |
| | | I-suffix versions | –40 | 125 | |
| | Junction, $T_J$ | | | 150 | |
| | Storage, $T_{stg}$ | | –65 | 150 | |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to GND.
(3) Input voltage range is limited to 20 V or $V_{CC}$ + 5 V, whichever is smaller.

## 7.2 ESD Ratings

| | | VALUE | UNIT |
|---|---|---|---|
| $V_{(ESD)}$ Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±2000 | V |
| | Charged-device model (CDM), per JEDEC specification JESD22-C101(2) | ±1500 | |
| | Machine model (MM) | ±100 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 7.3 Recommended Operating Conditions

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| Supply voltage, $V_{CC}$ | Single supply | C-suffix versions | 2.5 | 16 | V |
| | | I-suffix versions | 2.7 | 16 | |
| | Split supply | C-suffix versions | ±1.25 | ±8 | |
| | | I-suffix versions | ±1.35 | ±8 | |
| Common-mode input voltage, $V_{ICR}$ | | | –0.1 | $V_{CC}$ + 5 | V |
| Operating free-air temperature, $T_A$ | C-suffix versions | | 0 | 70 | °C |
| | I-suffix versions | | –40 | 125 | |

## 7.4 Thermal Information: TLV3401

| THERMAL METRIC(1) | | TLV3401 | | | UNIT |
|---|---|---|---|---|---|
| | | D (SOIC) | DBV (SOT-23) | P (PDIP) | |
| | | 8 PINS | 5 PINS | 8 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 201.9 | 237.8 | 58.5 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 92.5 | 108.7 | 48.3 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 123.3 | 64.1 | 35.6 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 23 | 12.1 | 25.9 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 212.6 | 63.3 | 35.5 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | — | — | — | °C/W |

(1) For more information about traditional and new thermal metrics, see the application report, *Semiconductor and IC Package Thermal Metrics*

## 7.5 Thermal Information: TLV3402

| THERMAL METRIC(1) | | TLV3402 | | | UNIT |
|---|---|---|---|---|---|
| | | D (SOIC) | DGK (VSSOP) | P (PDIP) | |
| | | 8 PINS | 8 PINS | 8 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 201.9 | 186.8 | 58.5 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 92.5 | 77.5 | 48.3 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 123.3 | 107.8 | 35.6 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 23 | 15.7 | 25.9 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 212.6 | 106.2 | 35.5 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | — | — | — | °C/W |

(1) For more information about traditional and new thermal metrics, see the application report, *Semiconductor and IC Package Thermal Metrics*

## 7.6 Thermal Information: TLV3404

| THERMAL METRIC(1) | | TLV3404 | | | UNIT |
|---|---|---|---|---|---|
| | | D (SOIC) | N (PDIP) | PW (TSSOP) | |
| | | 14 PINS | 14 PINS | 14 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 83.8 | 65.5 | 120.8 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 70.7 | 20.0 | 34.3 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 59.5 | 25.9 | 62.8 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 11.6 | 1.9 | 1 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 37.7 | 25.3 | 56.5 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | — | — | — | °C/W |

(1) For more information about traditional and new thermal metrics, see the application report, *Semiconductor and IC Package Thermal Metrics*

## 7.7 Electrical Characteristics

At specified free-air temperature and $V_{CC}$ = 2.7 V, 5 V, 15 V, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | | $T_A$ (1) | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| **DC PERFORMANCE** | | | | | | | | |
| $V_{IO}$ | Input offset voltage | $V_{IC} = V_{CC}/2$, $R_S$ = 50 Ω, $R_P$ = 1 MΩ | | $T_A$ = 25°C | | 250 | 3600 | µV |
| | | | | Full range | | | 4400 | |
| $\alpha_{VIO}$ | Offset voltage drift | $V_{IC} = V_{CC}/2$, $R_S$ = 50 Ω, $R_P$ = 1 MΩ | | $T_A$ = 25°C | | 3 | | µV/°C |
| CMRR | Common-mode rejection ratio | $V_{IC}$ = 0 V to 2.7 V, $R_S$ = 50 Ω | | $T_A$ = 25°C | 55 | 72 | | dB |
| | | | | Full range | 50 | | | |
| | | $V_{IC}$ = 0 V to 5 V, $R_S$ = 50 Ω | | $T_A$ = 25°C | 60 | 76 | | |
| | | | | Full range | 55 | | | |
| | | $V_{IC}$ = 0 V to 15 V, $R_S$ = 50 Ω | | $T_A$ = 25°C | 65 | 88 | | |
| | | | | Full range | 60 | | | |
| $A_{VD}$ | Large-signal differential voltage amplification | $R_P$ = 1 MΩ | | $T_A$ = 25°C | | 1000 | | V/mV |
| **INPUT/OUTPUT CHARACTERISTICS** | | | | | | | | |
| $I_{IO}$ | Input offset current | $V_{IC} = V_{CC}/2$, $R_S$ = 50 Ω, $R_P$ = 1 MΩ | | $T_A$ = 25°C | | 20 | 100 | pA |
| | | | | Full range | | | 1000 | |
| $I_{IB}$ | Input bias current | $V_{IC} = V_{CC}/2$, $R_S$ = 50 Ω, $R_P$ = 1 MΩ | | $T_A$ = 25°C | | 80 | 250 | pA |
| | | | | Full range | | | 1500 | |
| $r_{i(d)}$ | Differential input resistance | | | $T_A$ = 25°C | | 300 | | MΩ |
| $I_{OZ}$ | High-impedance output leakage current | $V_{IC} = V_{CC}/2$, $V_O = V_{CC}$, $V_{ID}$ = 1 V | | $T_A$ = 25°C | | 50 | | pA |
| $V_{OL}$ | Low-level output voltage | $V_{IC} = V_{CC}/2$, $I_{OL}$ = 2 µA, $V_{ID}$ = –1 V | | $T_A$ = 25°C | | 8 | | mV |
| | | $V_{IC} = V_{CC}/2$, $I_{OL}$ = 50 µA, $V_{ID}$ = –1 V | | $T_A$ = 25°C | | 80 | 200 | |
| | | | | Full range | | | 300 | |
| **POWER SUPPLY** | | | | | | | | |
| $I_{CC}$ | Supply current (per channel) | $R_P$ = no pullup | Output state low | $T_A$ = 25°C | | 470 | 550 | nA |
| | | | | Full range | | | 750 | |
| | | | Output state high | $T_A$ = 25°C | | 560 | 640 | |
| | | | | Full range | | | 950 | |
| PSRR | Power-supply rejection ratio | $V_{IC} = V_{CC}/2$, no load | $V_{CC}$ = 2.7 V to 5 V | $T_A$ = 25°C | 75 | 100 | | dB |
| | | | | Full range | 70 | | | |
| | | | $V_{CC}$ = 5 V to 15 V | $T_A$ = 25°C | 85 | 105 | | |
| | | | | Full range | 80 | | | |

(1) Full range is 0°C to 70°C for the C-suffix and –40°C to 125°C for the I-suffix. If not specified, full range is –40°C to 125°C.

## 7.8 Switching Characteristics

At $T_A$ = 25°C, recommended operating conditions, and $V_{CC}$ = 2.7 V, 5 V, 15 V, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | | $T_A$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $t_{(PLH)}$ | Propagation delay time, low-to-high-level output | f = 10 kHz, $V_{STEP}$ = 1 V, $R_P$ = 1 MΩ, $C_L$ = 10 pF | Overdrive = 2 mV | $T_A$ = 25°C | | 175 | | µs |
| | | | Overdrive = 10 mV | $T_A$ = 25°C | | 80 | | |
| | | | Overdrive = 50 mV | $T_A$ = 25°C | | 55 | | |
| $t_{(PHL)}$ | Propagation delay time, high-to-low-level output | f = 10 kHz, $V_{STEP}$ = 1 V, $R_P$ = 1 MΩ, $C_L$ = 10 pF | Overdrive = 2 mV | $T_A$ = 25°C | | 300 | | µs |
| | | | Overdrive = 10 mV | $T_A$ = 25°C | | 60 | | |
| | | | Overdrive = 50 mV | $T_A$ = 25°C | | 30 | | |
| $t_F$ | Fall time | $R_P$ = 1 MΩ, $C_L$ = 10 pF | | $T_A$ = 25°C | | 5 | | µs |

## 7.9 Typical Characteristics

**Table 1. Table of Graphs**

| DESCRIPTION | | | FIGURE NO. |
|---|---|---|---|
| | Input bias/offset current | vs Free-air temperature | Figure 1 |
| | Open collector leakage current | vs Free-air temperature | Figure 2 |
| $V_{OL}$ | Low-level output voltage | vs Low-level output current | Figure 3, Figure 4, Figure 5 |
| $I_{DD}$ | Supply current | vs Supply voltage | Figure 6 |
| $I_{DD}$ | Supply current | vs Free-air temperature | Figure 7 |
| | Low-to-high level output response for various input overdrives | | Figure 8, Figure 9, Figure 10 |
| | High-to-low level output response for various input overdrives | | Figure 11, Figure 12, Figure 13 |
| | Output fall time | vs Supply voltage | Figure 14 |

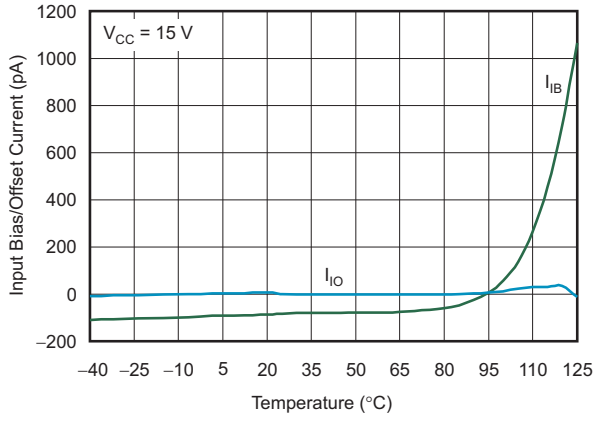



**Figure 1. Input Bias/Offset Current vs Free-Air Temperature**

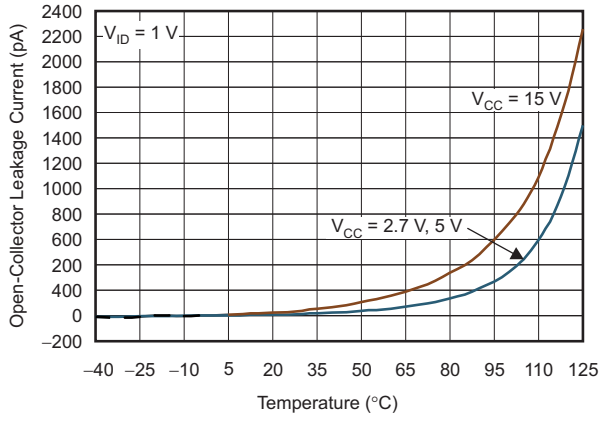



**Figure 2. Open-Collector Leakage Current vs Free-Air Temperature**

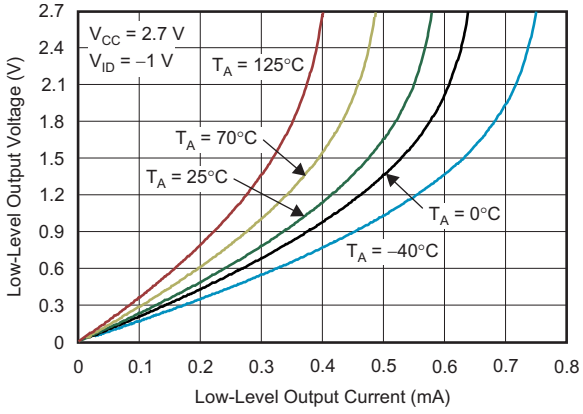



**Figure 3. Low-Level Output Voltage vs Low-Level Output Current**

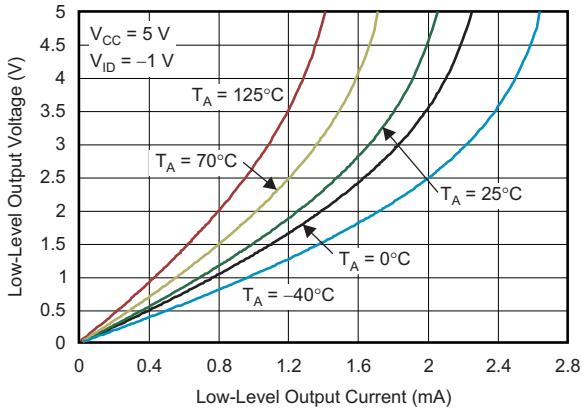



**Figure 4. Low-Level Output Voltage vs Low-Level Output Current**

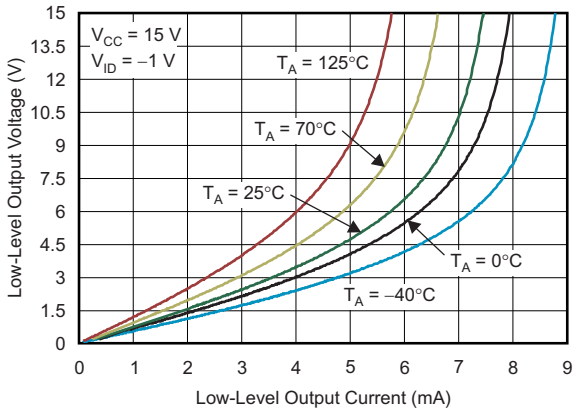



**Figure 5. Low-Level Output Voltage vs Low-Level Output Current**

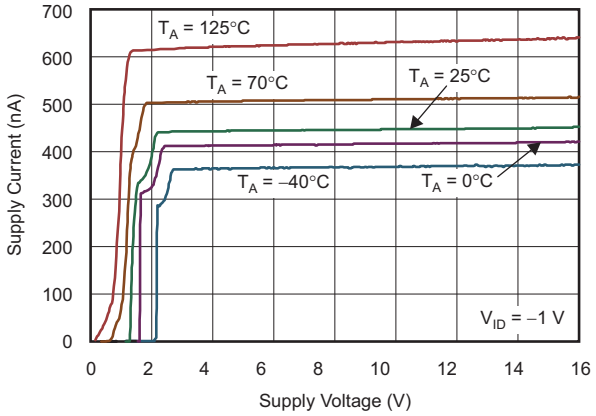



**Figure 6. Supply Current vs Supply Voltage**

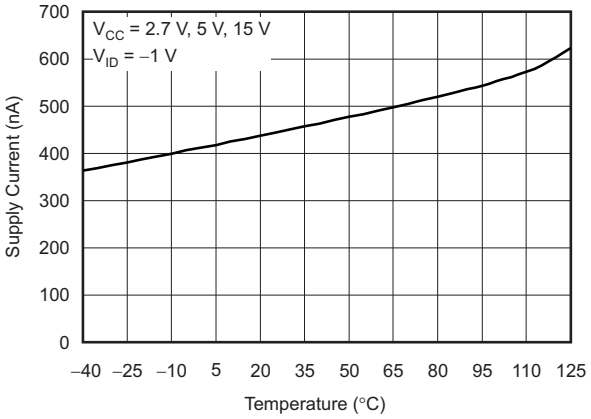



**Figure 7. Supply Current vs Free-Air Temperature**

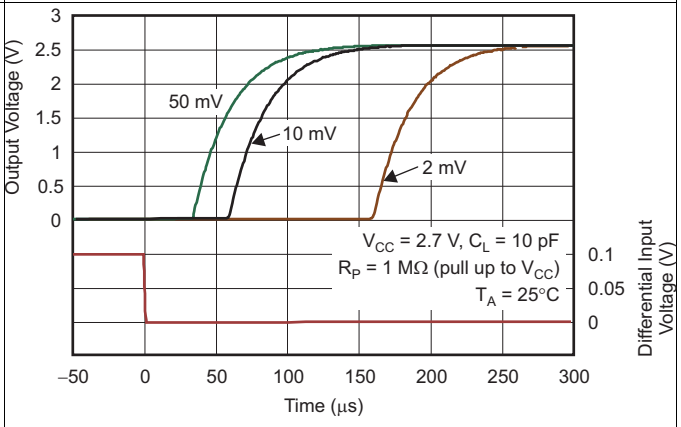



**Figure 8. Low-to-High Level Output Response for Various Input Overdrives**

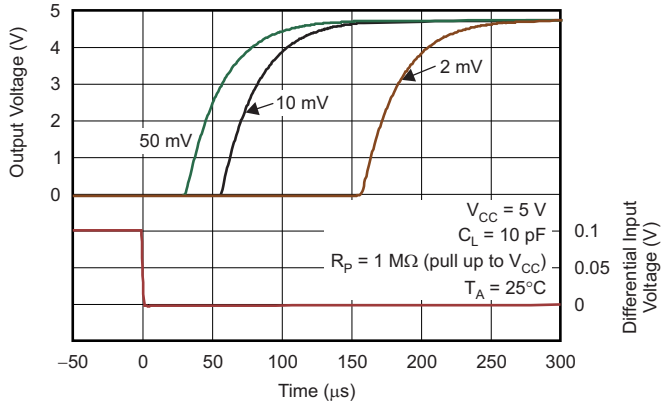



**Figure 9. Low-to-High Level Output Response for Various Input Overdrives**

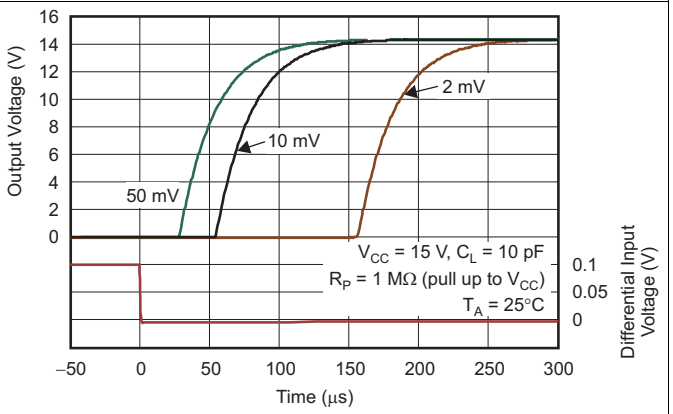



**Figure 10. Low-to-High Level Output Response for Various Input Overdrives**

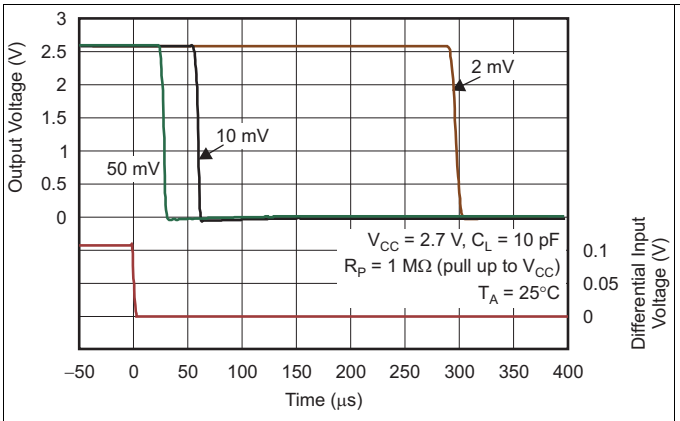



**Figure 11. High-to-Low Level Output Response for Various Input Overdrives**

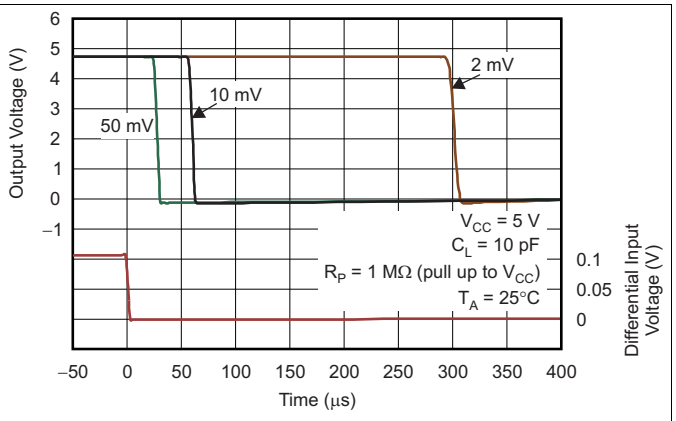



**Figure 12. High-to-Low Level Output Response for Various Input Overdrives**

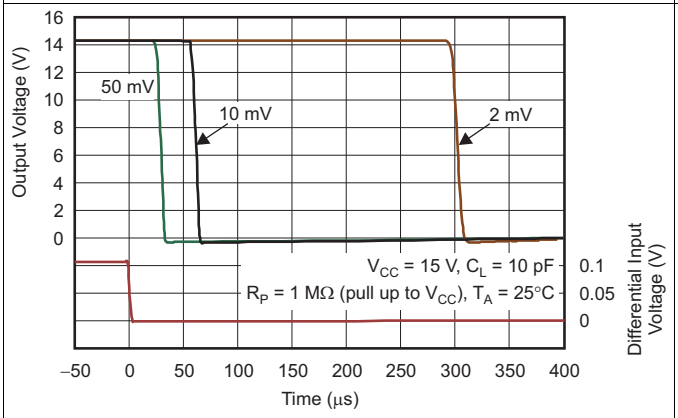



**Figure 13. High-to-Low Level Output Response for Various Input Overdrives**

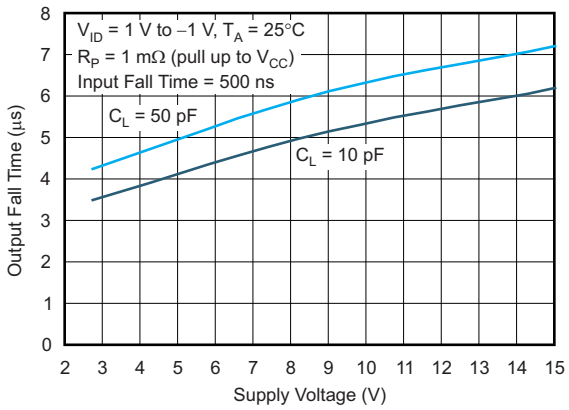


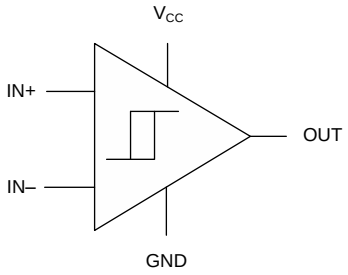

**Figure 14. Output Fall Time vs Supply Voltage**

# 8 Detailed Description

## 8.1 Overview

The TLV340x is a family of nanopower comparators drawing only 470 nA per channel supply current. Having a minimum operating supply voltage of 2.7 V over the extended industrial temperature range ($T_A$ = –40°C to +125°C), while having an input common-mode range of –0.1 to $V_{CC}$ + 5 V makes this device ideal for battery-powered and wireless handset applications.

## 8.2 Functional Block Diagram






## 8.3 Feature Description

### 8.3.1 Operating Voltage

The TLV340x comparators are specified for use on a single supply from 2.5 V to 16 V (or a dual supply from ±1.25 V to ±16 V) over a temperature range of −40°C to +125°C.

### 8.3.2 Setting the Threshold

Using a low-power, stable reference is important when setting the transition point for the TLV340x devices. The REF3312, as shown in Figure 15, provides a 1.25-V reference voltage with low drift and only 3.9 µA of quiescent current.

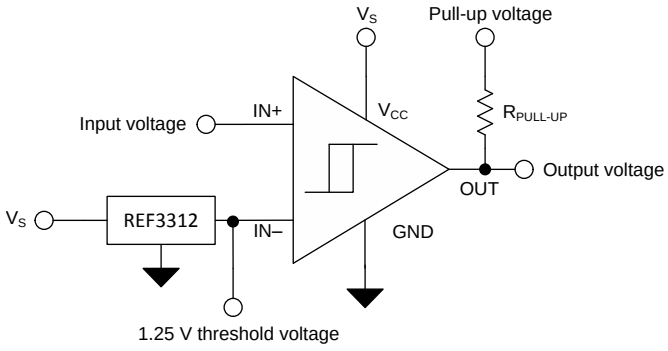





**Figure 15. Setting the Threshold**

## 8.4 Device Functional Modes

The TLV340x has a single functional mode and is operational when the power supply voltage applied ranges from 2.5 V (±1.25 V) to 16 V (±8 V).

# 9 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 9.1 Application Information

Many applications require the detection of a signal (voltage or current) that exceeds a particular threshold voltage or current. Using a comparator to make that threshold detection is the easiest, lowest power and highest speed way to make a threshold detection.

## 9.2 Typical Application

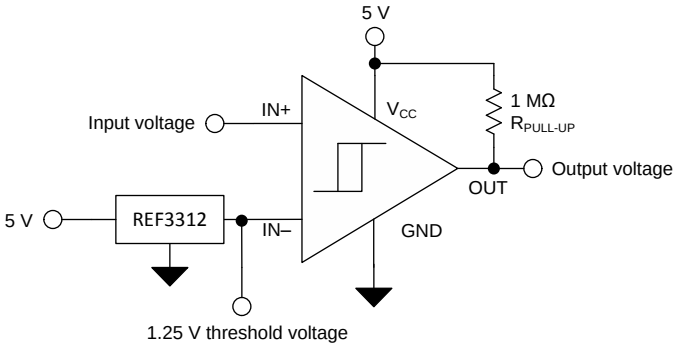





**Figure 16. 1.25-V Threshold Detector**

### 9.2.1 Design Requirements

- Detect when a signal is above or below 1.25 V
- Operate from a single 5-V power supply
- Rail-to-rail input voltage range from 0 to 5 V
- Rail-to-rail output voltage range from 0 to 5 V

### 9.2.2 Detailed Design Procedure

The input voltage range in the circuit illustrated in Figure 16 is limited only by the power supply applied to the TV3401. In this example with the selection of a 5-V, single-supply power supply, the input voltage range is limited to 0 to $V_S$ + 5 V, or 0 to 10 V. The threshold voltage of 1.25 V can de derived in a variety of ways. As the TLV3401 is a very low-power device, it is desirable to also use very low power to create the threshold voltage. The REF3312 series voltage reference is selected for its stable output voltage of 1.25 V and its low power consumption of only 3.9 µA. The TLV3401 is an open-drain output comparator, requiring a pullup resistor from output to the power supply. Proper selection of the pullup resistor value requires maximizing the output voltage swing while at the same time minimizing power dissipated in the resistor when the output voltage is low. Too small of a pullup resistor can result in too much power dissipation, while too large of a pullup resistor can result in slower response times. The TLV3401 is fully specified with a 1-MΩ pullup resistor and using a 1-MΩ pullup resistor results in meeting the performance specifications listed in the *Electrical Characteristics*.

## Typical Application (continued)

### 9.2.3 Application Curve

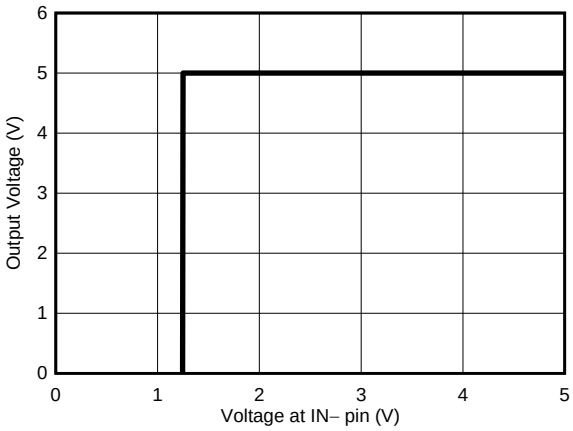



**Figure 17. Transfer Function for the Threshold Detector**

# 10 Power Supply Recommendations

The TLV340x device is specified for operation from 2.5 V to 16 V (±1.25 to ±8 V); many specifications apply from –40°C to +125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in *Typical Characteristics*.

# 11 Layout

## 11.1 Layout Guidelines

Figure 18 shows the typical connections for the TLV340x. To minimize supply noise, power supplies must be capacitively decoupled by a 0.01-µF ceramic capacitor in parallel with a 10-µF electrolytic capacitor. Comparators are very sensitive to input noise. Proper grounding (the use of a ground plane) helps to maintain the specified performance of the TLV340x family.

For best results, maintain the following layout guidelines:

1. Use a printed-circuit board (PCB) with a good, unbroken low-inductance ground plane.
2. Place a decoupling capacitor (0.1-µF ceramic, surface-mount capacitor) as close as possible to $V_{CC}$.
3. On the inputs and the output, keep lead lengths as short as possible to avoid unwanted parasitic feedback around the comparator. Keep inputs away from the output.
4. Solder the device directly to the PCB rather than using a socket.
5. For slow-moving input signals, take care to prevent parasitic feedback. A small capacitor (1000 pF or less) placed between the inputs can help eliminate oscillations in the transition region. This capacitor causes some degradation to propagation delay when the impedance is low. The top-side ground plane runs between the output and inputs.
6. The ground pin ground trace runs under the device up to the bypass capacitor, shielding the inputs from the outputs.

## 11.2 Layout Example

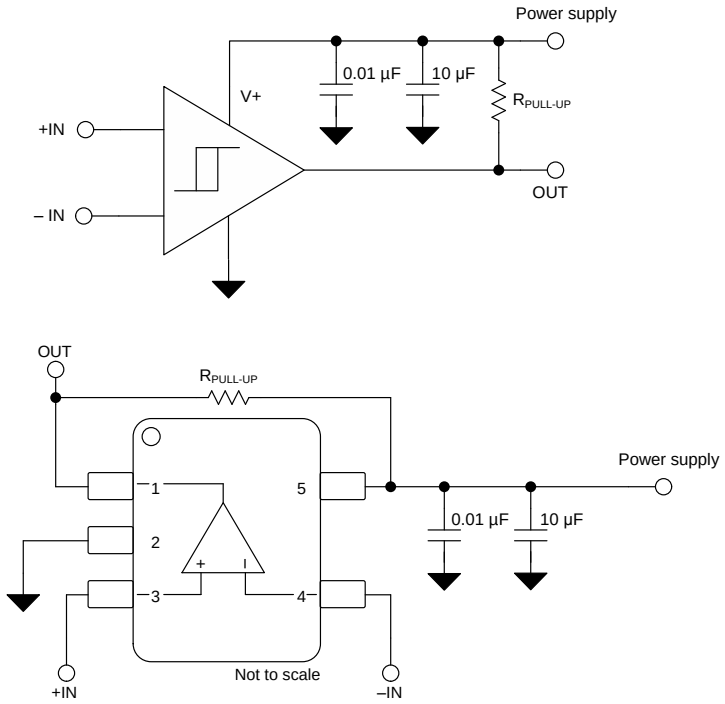





**Figure 18. TLV340x Layout Example**

# 12 Device and Documentation Support

## 12.1 Device Support

### 12.1.1 Development Support

#### *12.1.1.1 DIP Adapter EVM*

The DIP Adapter EVM tool provides an easy, low-cost way to prototype small surface mount ICs. The evaluation tool these TI packages: D or U (8-pin SOIC), PW (8-pin TSSOP), DGK (8-pin MSOP), DBV (6-pin SOT-23, 5-pin SOT23, and 3-pin SOT-23), DCK (6-pin SC-70 and 5-pin SC-70), and DRL (6-pin SOT-563). The DIP Adapter EVM may also be used with terminal strips or may be wired directly to existing circuits.

#### *12.1.1.2 Universal Op Amp EVM*

The Universal Op Amp EVM is a series of general-purpose, blank circuit boards that simplify prototyping circuits for a variety of IC package types. The evaluation module board design allows many different circuits to be constructed easily and quickly. Five models are offered, with each model intended for a specific package type. PDIP, SOIC, MSOP, TSSOP, and SOT-23 packages are all supported.

**NOTE**

These boards are unpopulated, so users must provide their own ICs. TI recommends requesting several op amp device samples when ordering the Universal Op Amp EVM.

## 12.2 Documentation Support

### 12.2.1 Related Documentation

The following documents are relevant for using the TLV340x devices and are recommended for reference. All are available for download at www.ti.com (unless otherwise noted):

- *Universal Op Amp EVM User Guide* (SLOU060)
- *Hardware Pace using Slope Detection* (SLAU511)
- *Bipolar High-voltage Differential Interface for Low-voltage Comparators* (TIDU039)
- *AC-Coupled Single Supply Comparator* (SLAU505)
- *ECG Implementation on the TMS320VC5505 DSP Medical Development Kit* (SPRAB36)
- *REF33xx 3.9-μA, SC70-3, SOT-23-3, and UQFN-8, 30-ppm/ °C Drift Voltage Reference* (SBOS392)

## 12.3 Related Links

Table 2 lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 2. Related Links**

| PARTS | PRODUCT FOLDER | SAMPLE & BUY | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|---|---|---|---|---|---|
| TLV3401 | Click here | Click here | Click here | Click here | Click here |
| TLV3402 | Click here | Click here | Click here | Click here | Click here |
| TLV3404 | Click here | Click here | Click here | Click here | Click here |

## 12.4 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 12.5 Community Resource

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 12.6 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

### 12.7 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 12.8 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TLV3401CD | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 3401C | Samples |
| TLV3401CDBVR | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | VBDC | Samples |
| TLV3401CDBVRG4 | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | VBDC | Samples |
| TLV3401CDBVT | ACTIVE | SOT-23 | DBV | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | VBDC | Samples |
| TLV3401CDBVTG4 | ACTIVE | SOT-23 | DBV | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | VBDC | Samples |
| TLV3401CDG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 3401C | Samples |
| TLV3401ID | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 3401I | Samples |
| TLV3401IDBVR | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | VBDI | Samples |
| TLV3401IDBVRG4 | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | VBDI | Samples |
| TLV3401IDBVT | ACTIVE | SOT-23 | DBV | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | VBDI | Samples |
| TLV3401IDBVTG4 | ACTIVE | SOT-23 | DBV | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | VBDI | Samples |
| TLV3401IDR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 3401I | Samples |
| TLV3401IP | ACTIVE | PDIP | P | 8 | 50 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -40 to 125 | TLV3401I | Samples |
| TLV3402CD | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 3402C | Samples |
| TLV3402CDG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 3402C | Samples |
| TLV3402CDGK | ACTIVE | VSSOP | DGK | 8 | 80 | Green (RoHS & no Sb/Br) | CU NIPDAU \| CU NIPDAUAG | Level-1-260C-UNLIM | 0 to 70 | AJJ | Samples |
| TLV3402CDGKG4 | ACTIVE | VSSOP | DGK | 8 | 80 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | AJJ | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TLV3402CDGKR | ACTIVE | VSSOP | DGK | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU \| CU NIPDAUAG | Level-1-260C-UNLIM | 0 to 70 | AJJ | Samples |
| TLV3402CDGKRG4 | ACTIVE | VSSOP | DGK | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | AJJ | Samples |
| TLV3402CDR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 3402C | Samples |
| TLV3402CDRG4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 3402C | Samples |
| TLV3402ID | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 3402I | Samples |
| TLV3402IDG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 3402I | Samples |
| TLV3402IDGK | ACTIVE | VSSOP | DGK | 8 | 80 | Green (RoHS & no Sb/Br) | CU NIPDAU \| CU NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | AJK | Samples |
| TLV3402IDGKG4 | ACTIVE | VSSOP | DGK | 8 | 80 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AJK | Samples |
| TLV3402IDGKR | ACTIVE | VSSOP | DGK | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU \| CU NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | AJK | Samples |
| TLV3402IDGKRG4 | ACTIVE | VSSOP | DGK | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AJK | Samples |
| TLV3402IDR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 3402I | Samples |
| TLV3402IDRG4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 3402I | Samples |
| TLV3402IP | ACTIVE | PDIP | P | 8 | 50 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -40 to 125 | TLV3402I | Samples |
| TLV3404CD | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 3404C | Samples |
| TLV3404CDR | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 3404C | Samples |
| TLV3404CDRG4 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 3404C | Samples |
| TLV3404CPW | ACTIVE | TSSOP | PW | 14 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 3404C | Samples |
| TLV3404CPWR | ACTIVE | TSSOP | PW | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 3404C | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TLV3404CPWRG4 | ACTIVE | TSSOP | PW | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 3404C | Samples |
| TLV3404ID | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 3404I | Samples |
| TLV3404IDG4 | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 3404I | Samples |
| TLV3404IDR | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 3404I | Samples |
| TLV3404IDRG4 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 3404I | Samples |
| TLV3404IN | ACTIVE | PDIP | N | 14 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -40 to 125 | TLV3404I | Samples |
| TLV3404IPW | ACTIVE | TSSOP | PW | 14 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 3404I | Samples |
| TLV3404IPWG4 | ACTIVE | TSSOP | PW | 14 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 3404I | Samples |
| TLV3404IPWR | ACTIVE | TSSOP | PW | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 3404I | Samples |
| TLV3404IPWRG4 | ACTIVE | TSSOP | PW | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 3404I | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

**(3)** MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

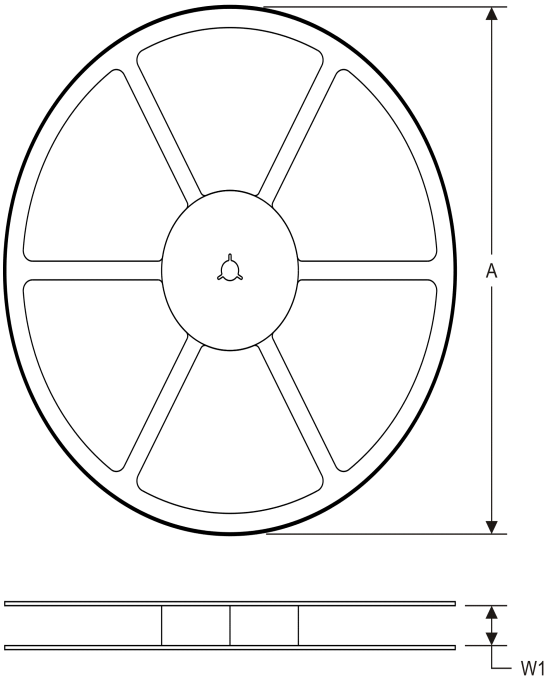
**(4)** There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

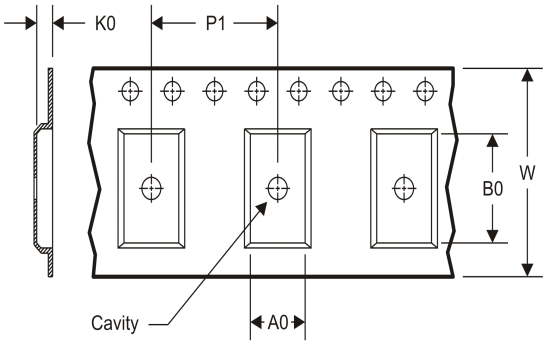
**(6)** Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**




**TAPE DIMENSIONS**



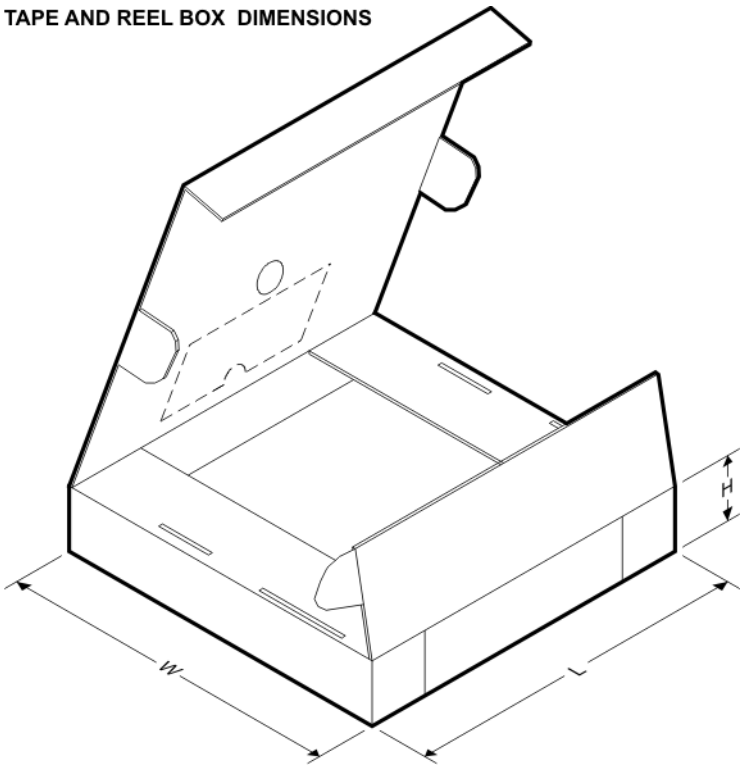

| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**TAPE AND REEL INFORMATION**

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TLV3401CDBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 9.0 | 3.15 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV3401CDBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 9.0 | 3.15 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV3401IDBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 9.0 | 3.15 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV3401IDBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 9.0 | 3.15 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV3401IDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TLV3402CDGKR | VSSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| TLV3402CDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TLV3402IDGKR | VSSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| TLV3402IDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TLV3404CDR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| TLV3404CPWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| TLV3404IDR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| TLV3404IPWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

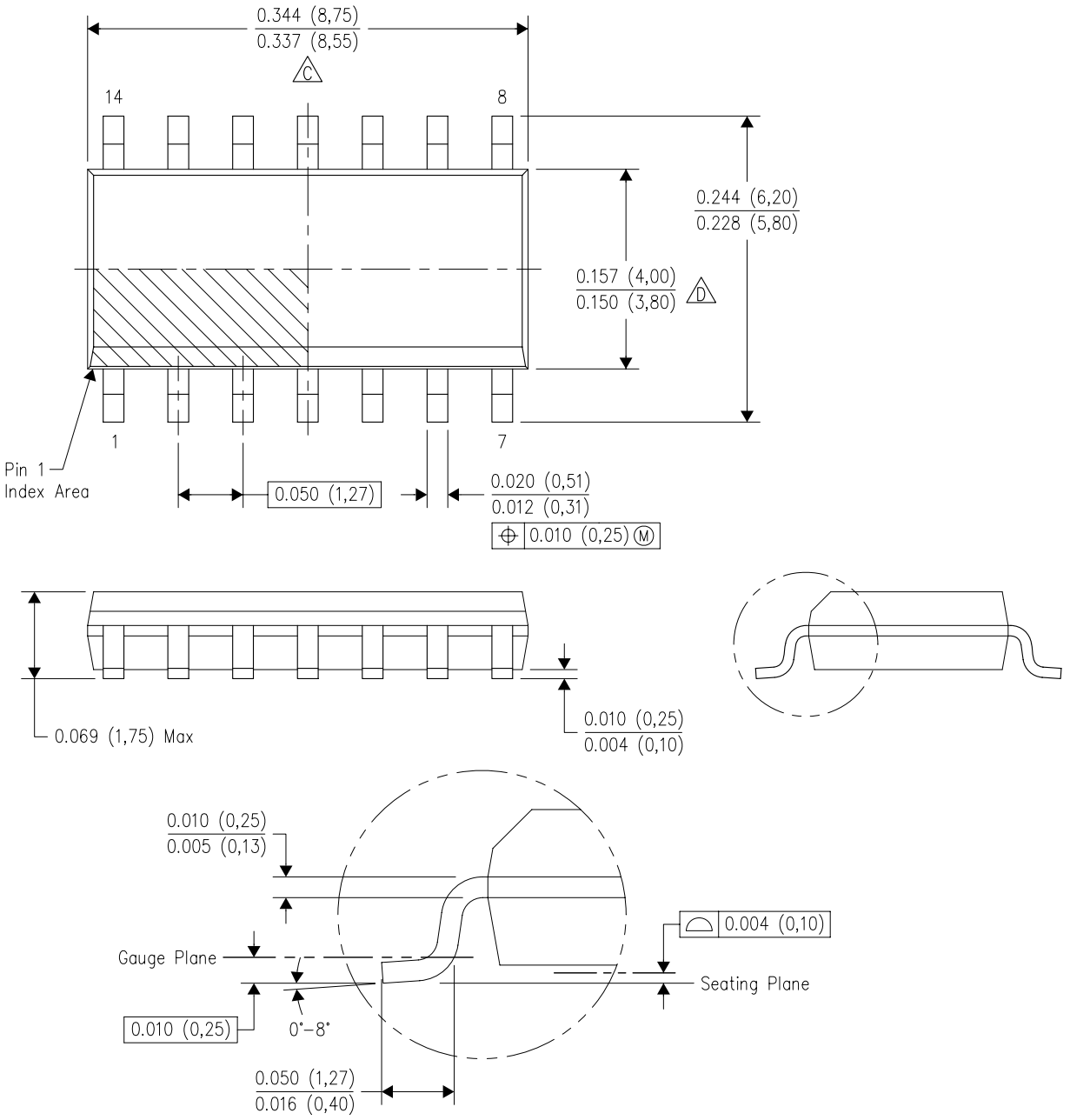
**TAPE AND REEL BOX DIMENSIONS**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TLV3401CDBVR | SOT-23 | DBV | 5 | 3000 | 182.0 | 182.0 | 20.0 |
| TLV3401CDBVT | SOT-23 | DBV | 5 | 250 | 182.0 | 182.0 | 20.0 |
| TLV3401IDBVR | SOT-23 | DBV | 5 | 3000 | 182.0 | 182.0 | 20.0 |
| TLV3401IDBVT | SOT-23 | DBV | 5 | 250 | 182.0 | 182.0 | 20.0 |
| TLV3401IDR | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |
| TLV3402CDGKR | VSSOP | DGK | 8 | 2500 | 364.0 | 364.0 | 27.0 |
| TLV3402CDR | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |
| TLV3402IDGKR | VSSOP | DGK | 8 | 2500 | 364.0 | 364.0 | 27.0 |
| TLV3402IDR | SOIC | D | 8 | 2500 | 533.4 | 186.0 | 36.0 |
| TLV3404CDR | SOIC | D | 14 | 2500 | 333.2 | 345.9 | 28.6 |
| TLV3404CPWR | TSSOP | PW | 14 | 2000 | 367.0 | 367.0 | 35.0 |
| TLV3404IDR | SOIC | D | 14 | 2500 | 333.2 | 345.9 | 28.6 |
| TLV3404IPWR | TSSOP | PW | 14 | 2000 | 367.0 | 367.0 | 35.0 |

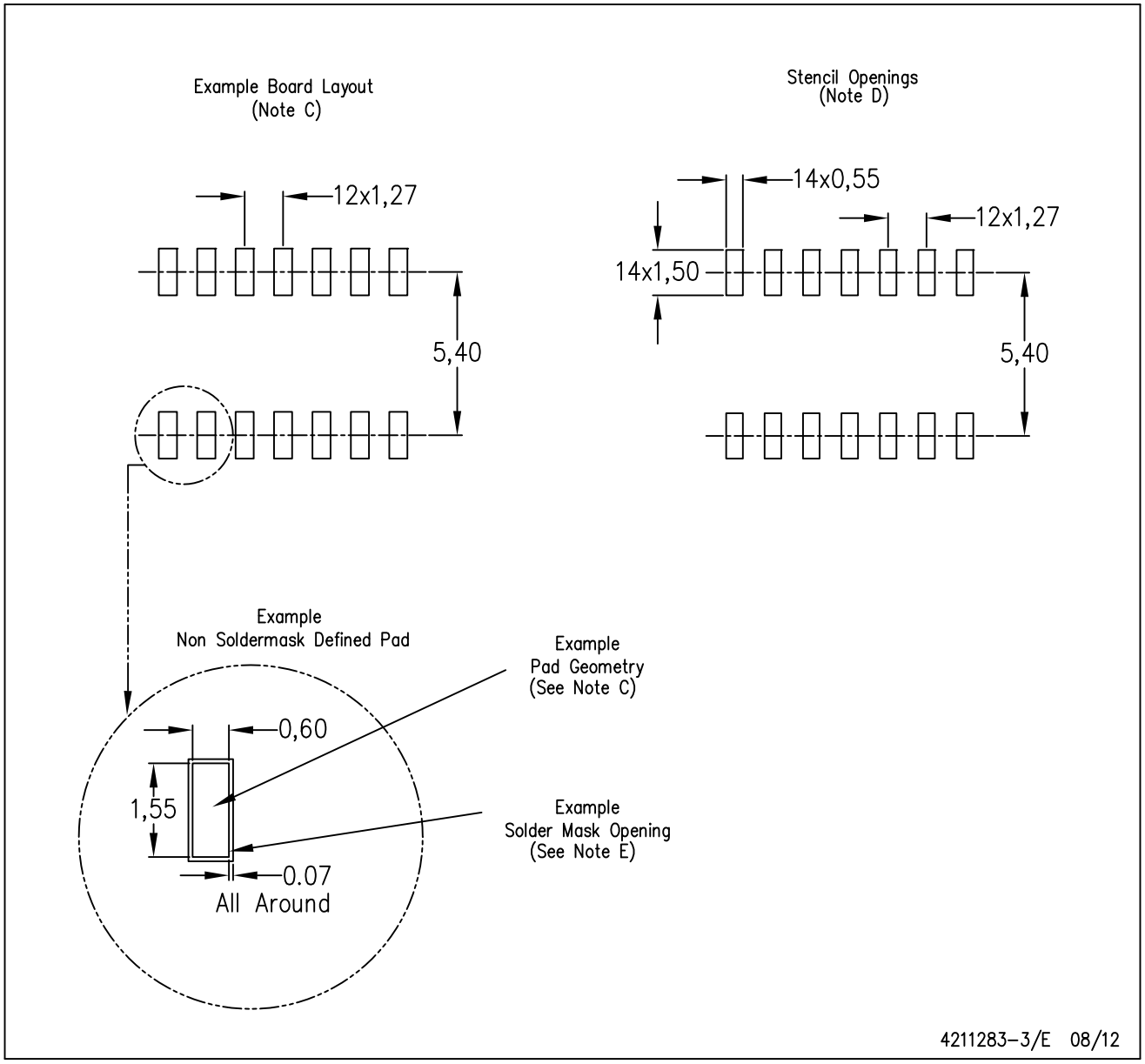
D (R–PDSO–G14) PLASTIC SMALL OUTLINE




4040047–5/M 06/11

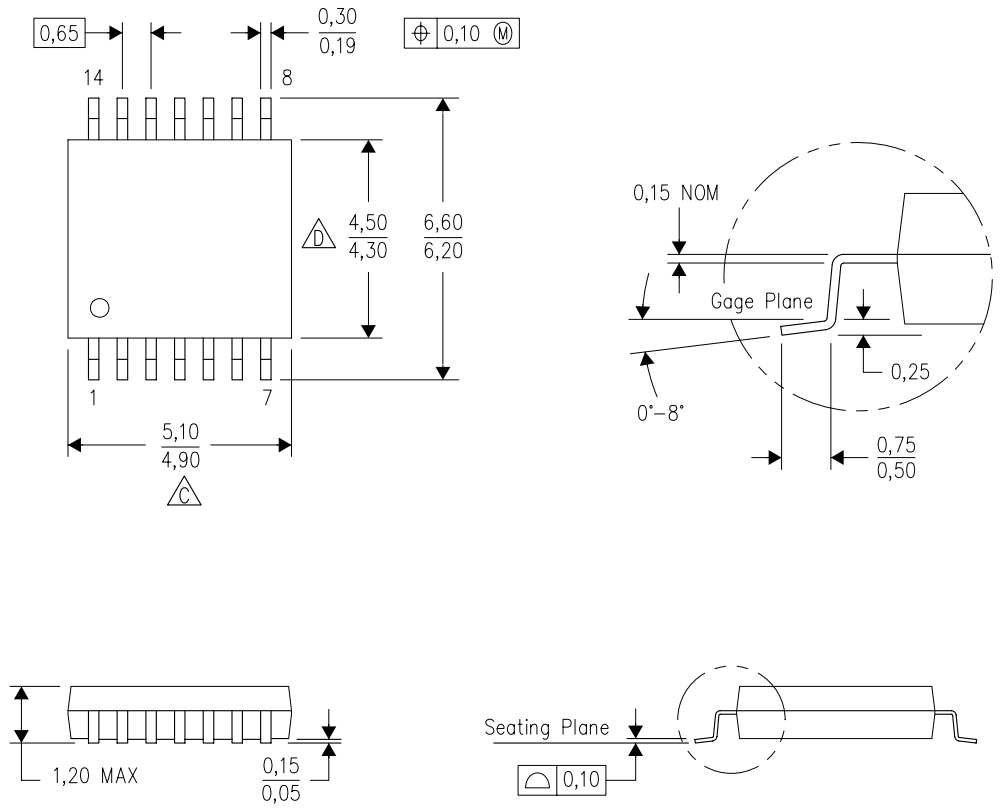
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

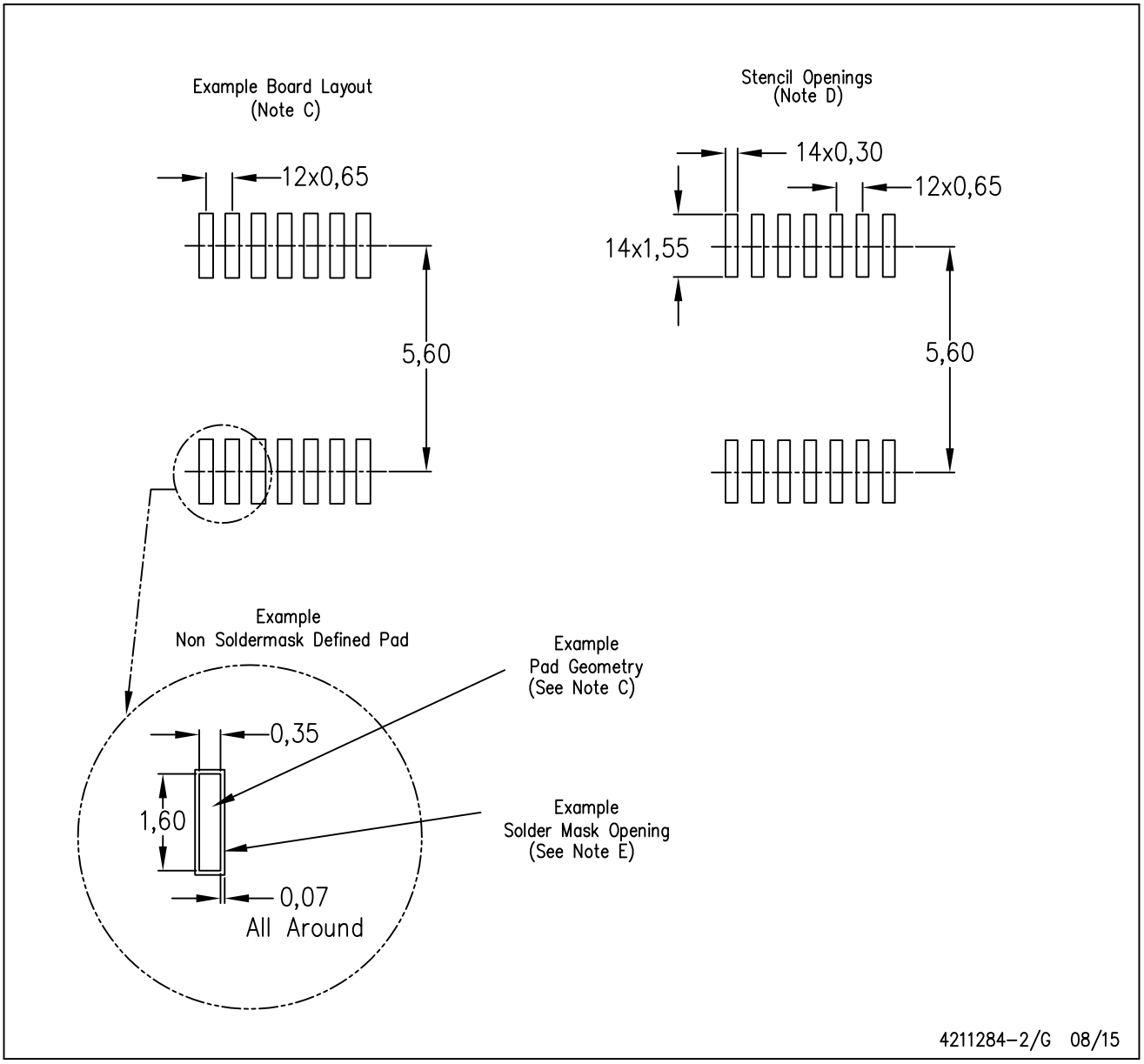
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE




4040064–3/G 02/11

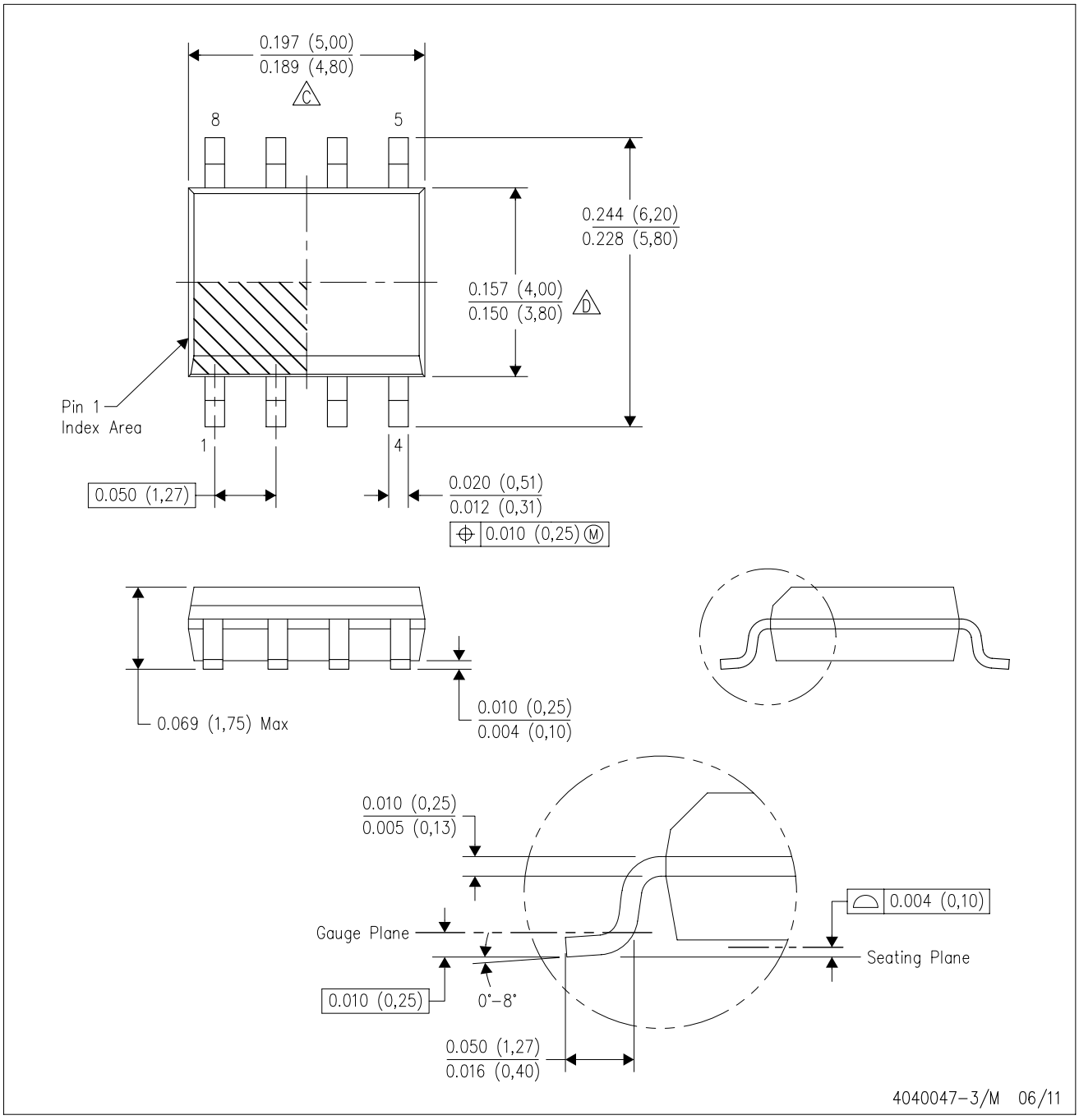
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



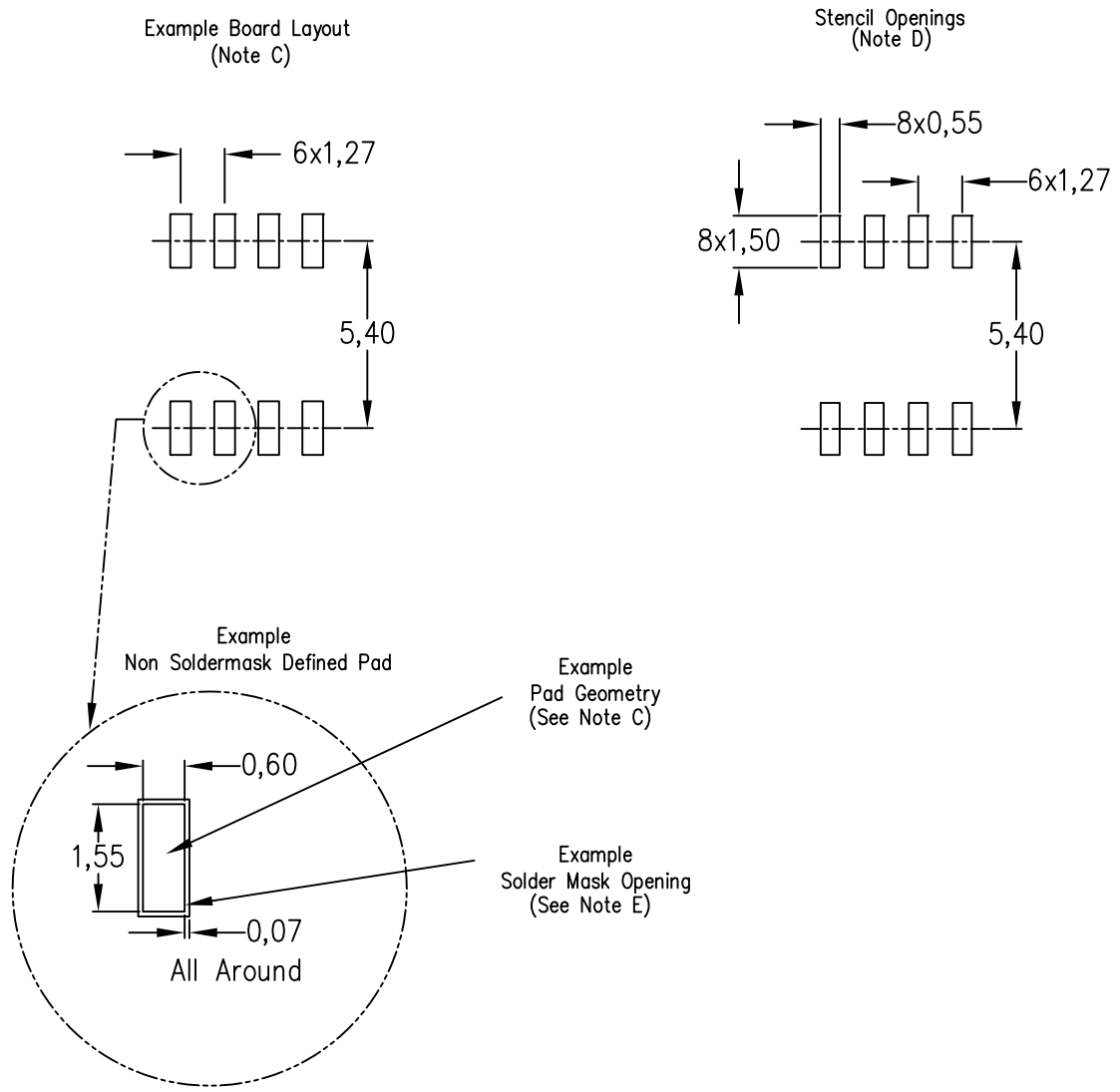

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



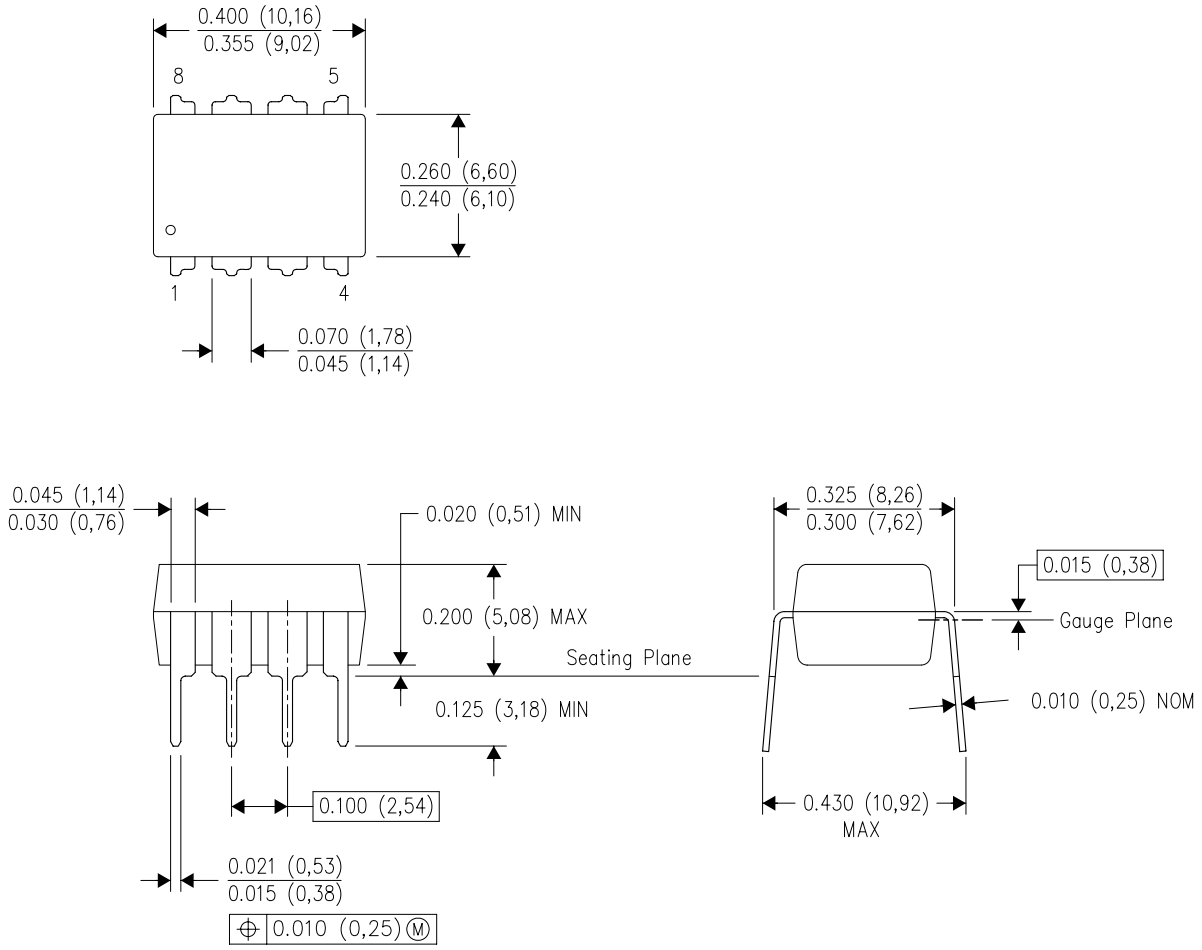

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE

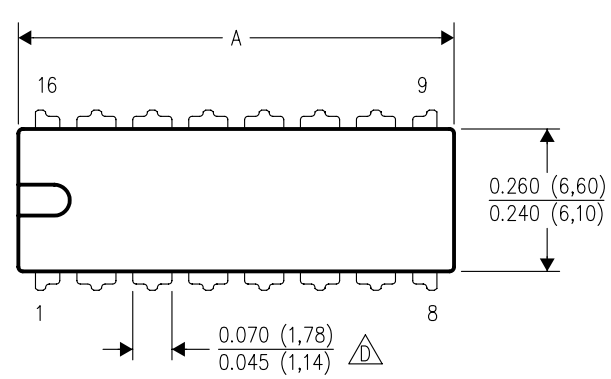



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

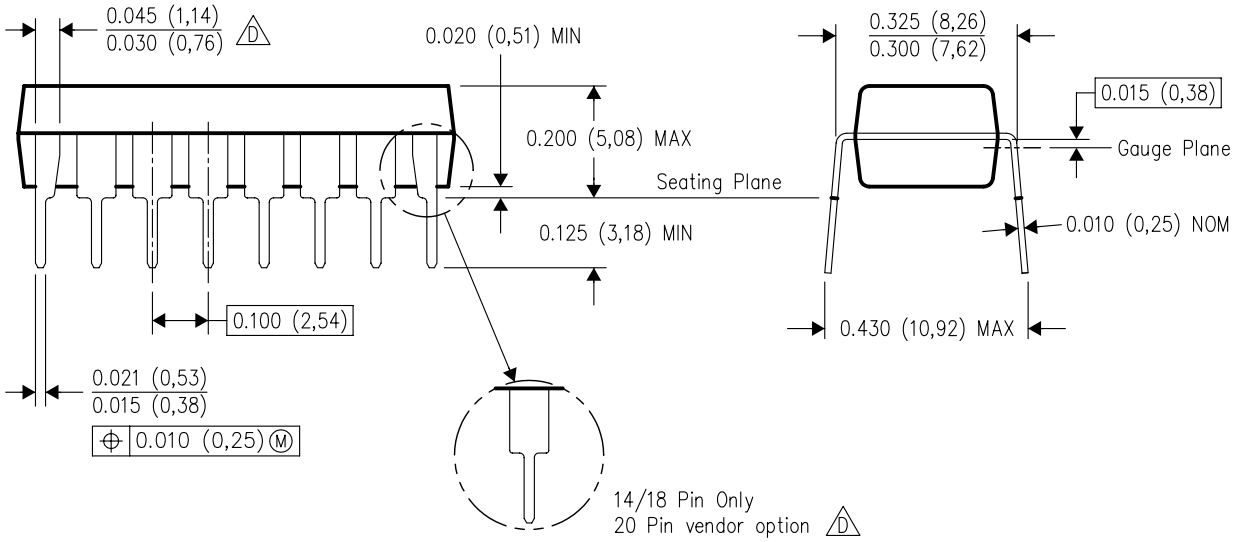
## N (R–PDIP–T**)

## PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



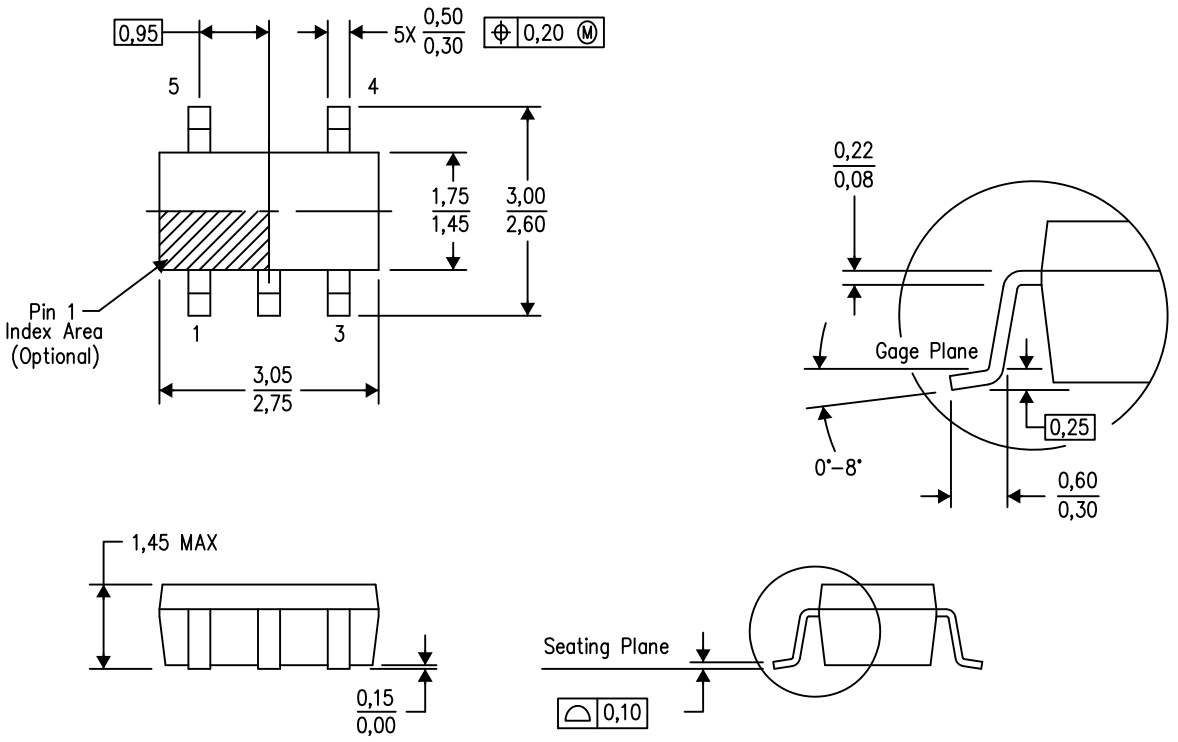

| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS–001 VARIATION (C) | AA | BB | AC | AD |




4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

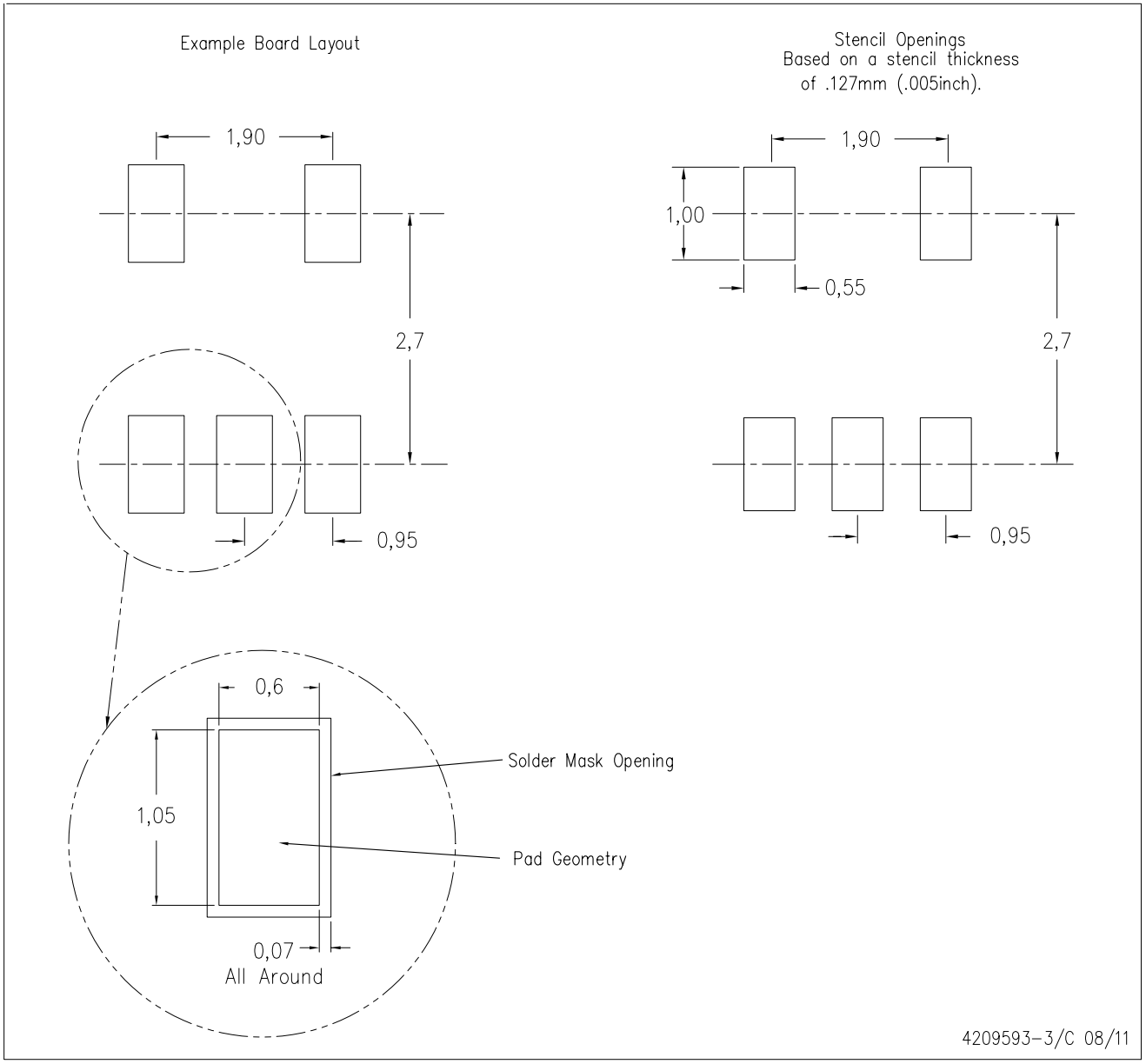
DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE




4073253–4/N 12/14

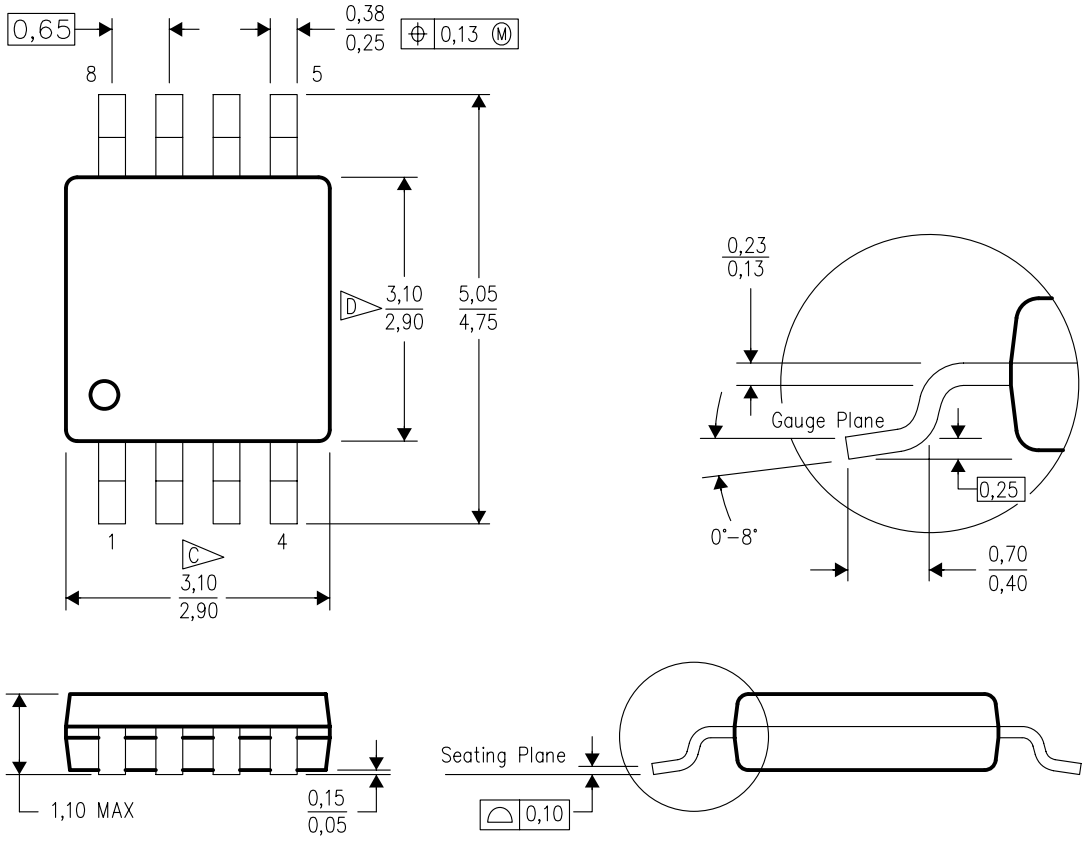
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–178 Variation AA.

DBV (R–PDSO–G5) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

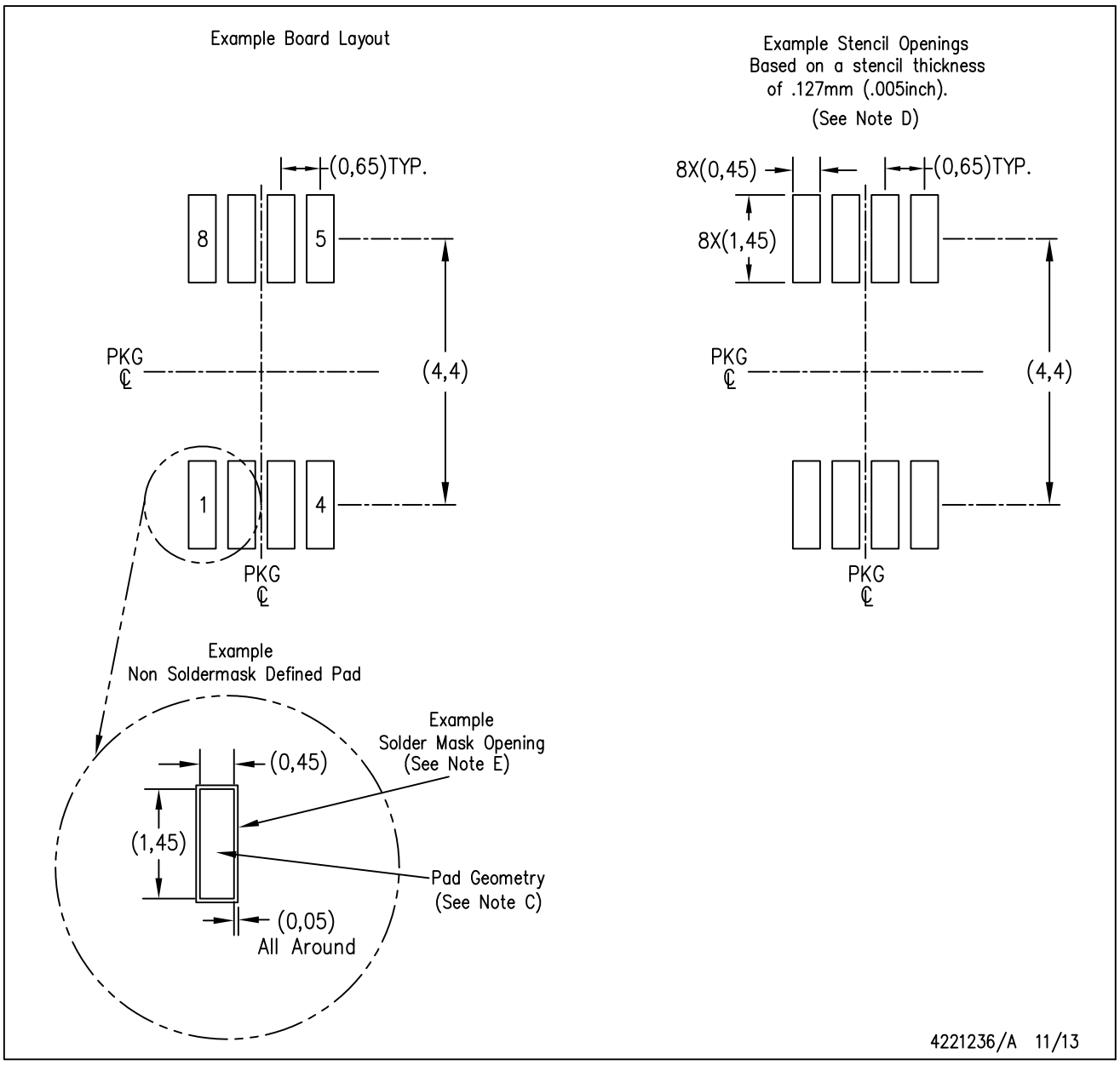
## DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE




4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

# DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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