# TLV702-Q1 300-mA, Low-$I_Q$, Low-Dropout Regulator

## 1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified with the Following Results:
  - Device Temperature Grade 1: –40°C to 125°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level H2
  - Device CDM ESD Classification Level C4B
- Very Low Dropout:
  - 37 mV at $I_{OUT}$ = 50 mA, $V_{OUT}$ = 2.8 V
  - 75 mV at $I_{OUT}$ = 100 mA, $V_{OUT}$ = 2.8 V
  - 220 mV at $I_{OUT}$ = 300 mA, $V_{OUT}$ = 2.8 V
- 2% Accuracy Over Temperature
- Low $I_Q$: 35 µA
- Fixed-Output Voltage Combinations Possible from 1.2 V to 4.8 V
- High PSRR: 68 dB at 1 kHz
- Stable with Effective Capacitance of 0.1 µF(1)
- Thermal Shutdown and Overcurrent Protection
- Packages: 5-Pin SOT and 1.5-mm × 1.5-mm, 6-Pin WSON

(1) See the *Input and Output Capacitor Requirements* in the Application Information section.

## 2 Applications

- Automotive Camera Modules
- Image Sensor Power
- Microprocessor Rails
- Automotive Infotainment Head Units
- Automotive Body Electronics

## 3 Description

The TLV702-Q1 series of low-dropout (LDO) linear regulators are low quiescent current devices with excellent line and load transient performance. These LDOs are designed for power-sensitive applications.

A precision bandgap and an error amplifier provide overall 2% accuracy. Low output noise, very high power-supply rejection ratio (PSRR), and low-dropout voltage make this series of devices ideal for a wide selection of battery-operated equipment. All device versions have thermal shutdown and current limit protections for safety.

Furthermore, these devices are stable with an effective output capacitance of only 0.1 µF. This feature enables the use of cost-effective capacitors that have higher bias voltages and temperature derating. The devices regulate to specified accuracy with no output load.

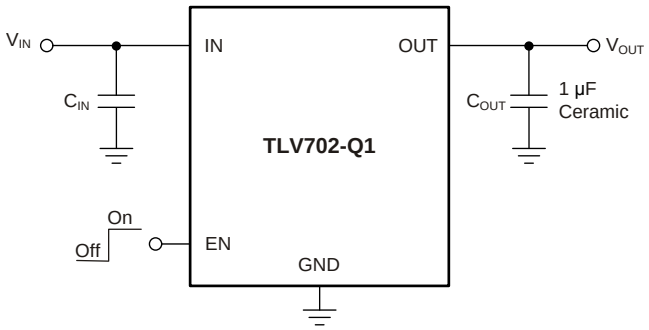
The TLV702-Q1 series of LDO linear regulators is available in SOT and WSON packages.

**Device Information(1)**

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| TLV702-Q1 | SOT (5) | 2.90 mm × 1.60 mm |
| | WSON (6) | 1.50 mm × 1.50 mm |

(1) For all available packages, see the package option addendum at the end of the data sheet.

**Typical Application**



# Table of Contents



## 4 Revision History

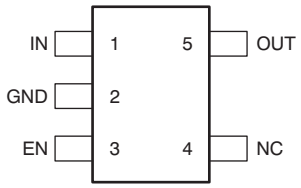
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

**Changes from Revision A (August 2013) to Revision B** **Page**

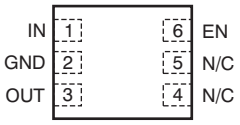
- Added DSE (6-Pin WSON) package to data sheet ... 1
- Added *Device Information*, *ESD Ratings*, and *Recommended Operating Conditions* tables, and *Detailed Description*, *Application and Implementation*, *Power Supply Recommendations*, *Layout*, *Device and Documentation Support*, and *Mechanical, Packaging, and Orderable Information* sections to data sheet ... 1
- Deleted all references to P version of device throughout data sheet ... 1
- Added "Over Temperature" to 2% accuracy *Features* bullet ... 1
- Changed DDC package name from TSOT23 to SOT throughout data sheet ... 1
- Changed *Applications* bullets ... 1
- Changed *Description* section text ... 1
- Changed ceramic capacitor units on *Typical Application* circuit from mF to µF (typo) ... 1
- Changed "free-air temperature" to "junction temperature" in *Absolute Maximum Ratings* condition statement ... 4
- Added $T_J$ to $T_A$ condition in *Electrical Characteristics* condition statement ... 5
- Changed $T_A$ to $T_J$ for typical values in *Electrcial Characteristics* condition statement ... 5

# 5 Pin Configuration and Functions

**DDC Package**
**5-pin SOT**
**Top View**




**DSE Package**
**6-Pin WSON**
**Top View**




**Pin Functions**

| PIN | | | I/O | DESCRIPTION |
|---|---|---|---|---|
| NAME | DDC (SOT) | DSE (WSON) | | |
| IN | 1 | 1 | I | Input pin. A small, 1-µF ceramic capacitor is recommended from this pin to ground to assure stability and good transient performance. See *Input and Output Capacitor Requirements* in the *Application Information* section for more details. |
| GND | 2 | 2 | — | Ground pin |
| EN | 3 | 6 | I | Enable pin. Driving EN over 0.9 V turns on the regulator. Driving EN below 0.4 V puts the regulator into shutdown mode and reduces operating current to 1 µA, nominal. |
| NC | 4 | 4, 5 | — | No connection. Tie this pin to ground to improve thermal dissipation. |
| OUT | 5 | 5 | O | Regulated output voltage pin. A small, 1-µF ceramic capacitor is needed from this pin to ground for stability. See *Input and Output Capacitor Requirements* in the *Application Information* section for more details. |

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted)(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Voltage(2) | IN | –0.3 | 6 | V |
| | EN | –0.3 | 6 | V |
| | OUT | –0.3 | 6 | V |
| Current (source) | OUT | Internally limited | | A |
| Output short-circuit duration | | Indefinite | | |
| Temperature | Operating virtual junction, $T_J$ | –55 | 150 | °C |
| | Storage, $T_{stg}$ | –55 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to network ground terminal.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per AEC Q100-002(1) | ±2000 | V |
| | | Charged-device model (CDM), per AEC Q100-011 | ±750 | |

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|
| $V_{IN}$ | 2 | | 5.5 | V |
| $V_{OUT}$ | 1.2 | | 4.8 | V |
| $I_{OUT}$ | 0 | | 300 | mA |
| Ambient temperature, $T_A$ | –40 | | 125 | °C |
| Operating virtual junction temperature, $T_J$ | –40 | | 125 | °C |

## 6.4 Thermal Information

| THERMAL METRIC(1) | | TLV702-Q1 | | UNIT |
|---|---|---|---|---|
| | | DDC (SOT) | DSE (WSON) | |
| | | 5 PINS | 6 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 262.8 | 321.3 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 68.2 | 207.9 | |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 81.6 | 281.5 | |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 1.1 | 42.4 | |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 80.9 | 284.8 | |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | N/A | 142.3 | |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

## 6.5 Electrical Characteristics

At $V_{IN}$ = $V_{OUT(nom)}$ + 0.5 V or 2 V (whichever is greater); $I_{OUT}$ = 10 mA, $V_{EN}$ = 0.9 V, $C_{OUT}$ = 1 µF, and $T_J$, $T_A$ = –40°C to +125°C, unless otherwise noted. Typical values are at $T_J$ = 25°C.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| | DC output accuracy | | –2% | 0.5% | 2% | |
| $\Delta V_{O(\Delta VI)}$ | Line regulation | $V_{OUT(nom)}$ + 0.5 V ≤ $V_{IN}$ ≤ 5.5 V, $I_{OUT}$ = 10 mA | | 1 | 5 | mV |
| $\Delta V_{O(\Delta IO)}$ | Load regulation | 0 mA ≤ $I_{OUT}$ ≤ 300 mA | | 1 | 15 | mV |
| $V_{DO}$ | Dropout voltage(1) | $V_{IN}$ = 0.98 × $V_{OUT(nom)}$, $I_{OUT}$ = 300 mA | | 260 | 375 | mV |
| $I_{CL}$ | Output current limit | $V_{OUT}$ = 0.9 × $V_{OUT(nom)}$ | 320 | 500 | 860 | mA |
| $I_{GND}$ | Ground pin current | $I_{OUT}$ = 0 mA | | 35 | 55 | µA |
| | | $I_{OUT}$ = 300 mA, $V_{IN}$ = $V_{OUT}$ + 0.5 V | | 370 | | µA |
| $I_{SHDN}$ | Ground pin current (shutdown) | $V_{EN}$ ≤ 0.4 V, $V_{IN}$ = 2 V | | 400 | | nA |
| | | $V_{EN}$ ≤ 0.4 V, 2 V ≤ $V_{IN}$ ≤ 4.5 V | | 1 | 2.5 | µA |
| PSRR | Power-supply rejection ratio | $V_{IN}$ = 2.3 V, $V_{OUT}$ = 1.8 V, $I_{OUT}$ = 10 mA, f = 1 kHz | | 68 | | dB |
| $V_n$ | Output noise voltage | BW = 100 Hz to 100 kHz, $V_{IN}$ = 2.3 V, $V_{OUT}$ = 1.8 V, $I_{OUT}$ = 10 mA | | 48 | | $\mu V_{RMS}$ |
| $t_{STR}$ | Start-up time(2) | $C_{OUT}$ = 1 µF, $I_{OUT}$ = 300 mA | | 100 | | µs |
| $V_{EN(high)}$ | Enable pin high (enabled) | | 0.9 | | $V_{IN}$ | V |
| $V_{EN(low)}$ | Enable pin low (disabled) | | 0 | | 0.4 | V |
| $I_{EN}$ | Enable pin current | $V_{IN}$ = $V_{EN}$ = 5.5 V | | 0.04 | | µA |
| UVLO | Undervoltage lockout | $V_{IN}$ rising | | 1.9 | | V |
| $T_{sd}$ | Thermal shutdown temperature | Shutdown, temperature increasing | | 165 | | °C |
| | | Reset, temperature decreasing | | 145 | | °C |

(1) $V_{DO}$ is measured for devices with $V_{OUT(nom)}$ ≥ 2.35 V.
(2) Start-up time = time from EN assertion to 0.98 × $V_{OUT(nom)}$.

## 6.6 Typical Characteristics

Over operating temperature range ($T_J$ = –40°C to +125°C), $V_{IN}$ = $V_{OUT(nom)}$ + 0.5 V or 2 V, whichever is greater; $I_{OUT}$ = 10 mA, $V_{EN}$ = $V_{IN}$, $C_{OUT}$ = 1 µF, unless otherwise noted. Typical values are at $T_J$ = 25°C.

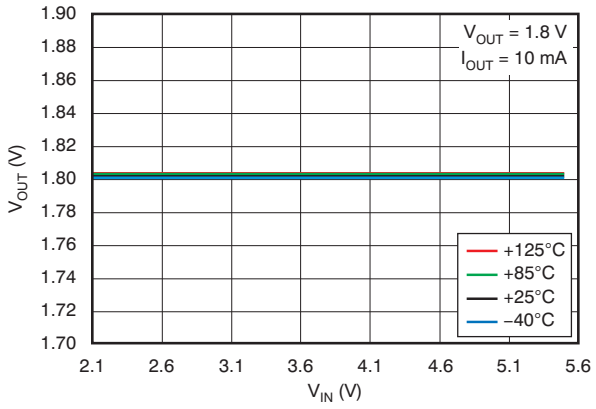



**Figure 1. Line Regulation**

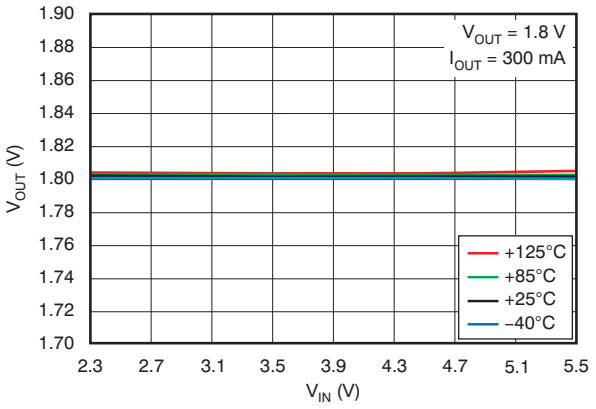



**Figure 2. Line Regulation**

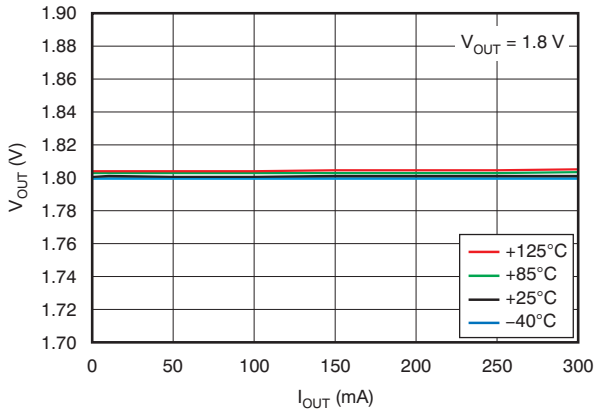



**Figure 3. Load Regulation**

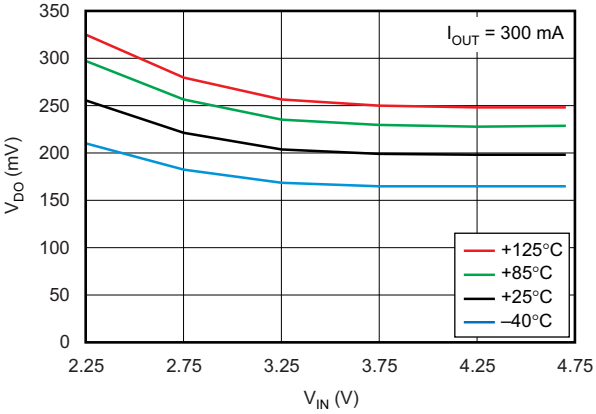



**Figure 4. Dropout Voltage vs Input Voltage**

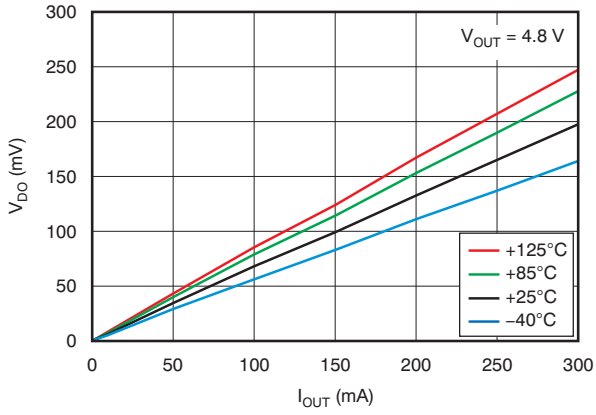



**Figure 5. Dropout Voltage vs Output Current**

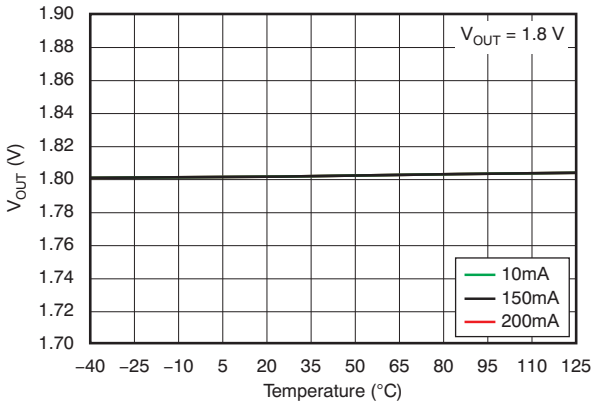



**Figure 6. Output Voltage vs Temperature**

## Typical Characteristics (continued)

Over operating temperature range ($T_J$ = –40°C to +125°C), $V_{IN}$ = $V_{OUT(nom)}$ + 0.5 V or 2 V, whichever is greater; $I_{OUT}$ = 10 mA, $V_{EN}$ = $V_{IN}$, $C_{OUT}$ = 1 µF, unless otherwise noted. Typical values are at $T_J$ = 25°C.

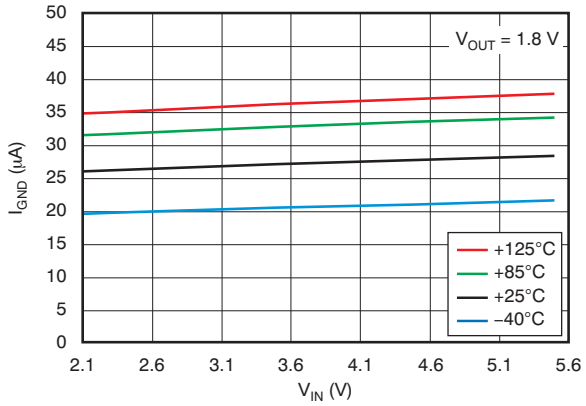



**Figure 7. Ground Pin Current vs Input Voltage**

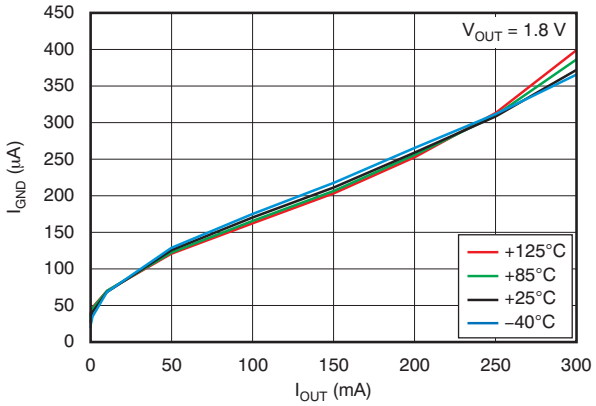



**Figure 8. Ground Pin Current vs Load**

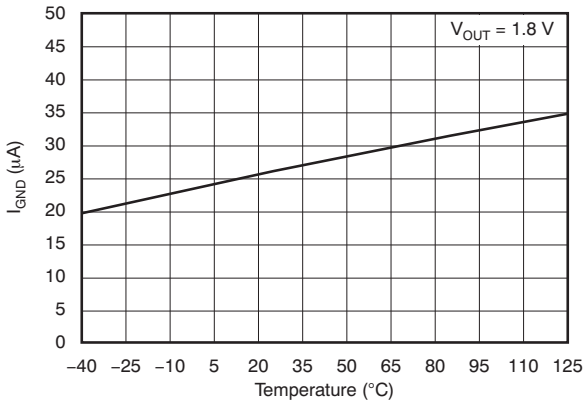



**Figure 9. Ground Pin Current vs Temperature**

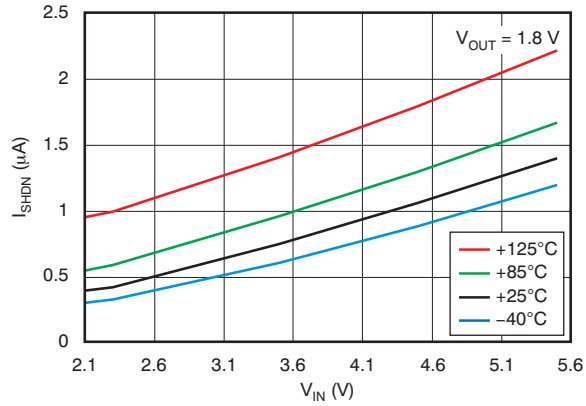



**Figure 10. Shutdown Current vs Input Voltage**

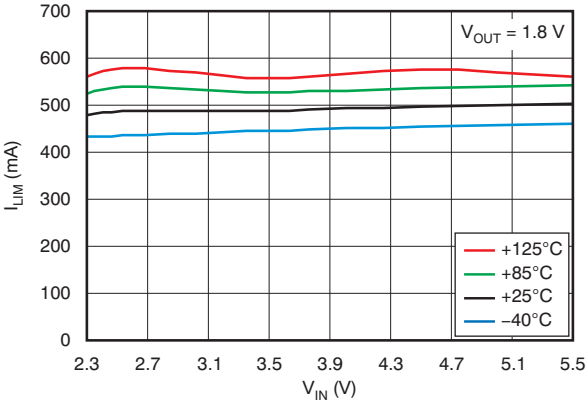



**Figure 11. Current Limit vs Input Voltage**

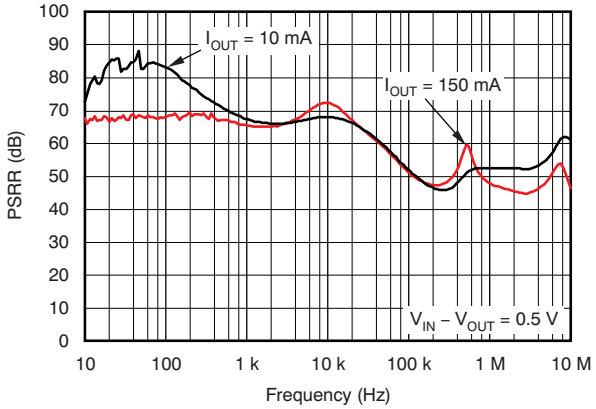



**Figure 12. Power-Supply Ripple Rejection vs Frequency**

## Typical Characteristics (continued)

Over operating temperature range ($T_J$ = –40°C to +125°C), $V_{IN}$ = $V_{OUT(nom)}$ + 0.5 V or 2 V, whichever is greater; $I_{OUT}$ = 10 mA, $V_{EN}$ = $V_{IN}$, $C_{OUT}$ = 1 µF, unless otherwise noted. Typical values are at $T_J$ = 25°C.

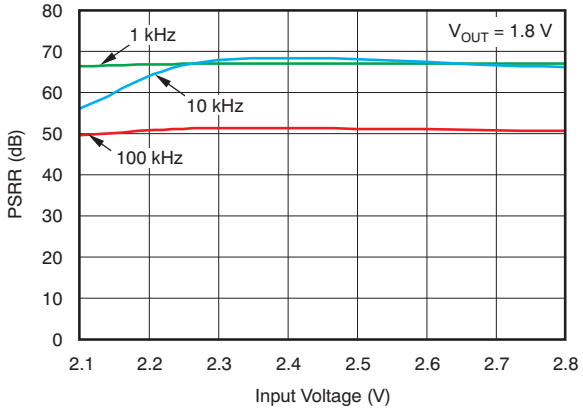



**Figure 13. Power-Supply Ripple Rejection vs Input Voltage**

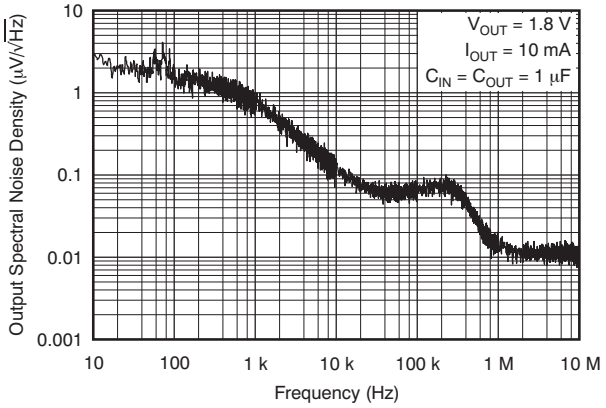



**Figure 14. Output Spectral Noise Density vs Frequency**

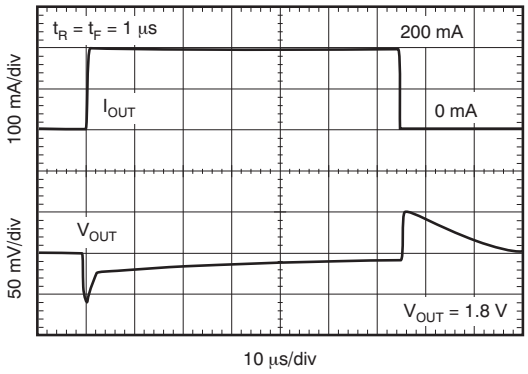



**Figure 15. Load Transient Response**

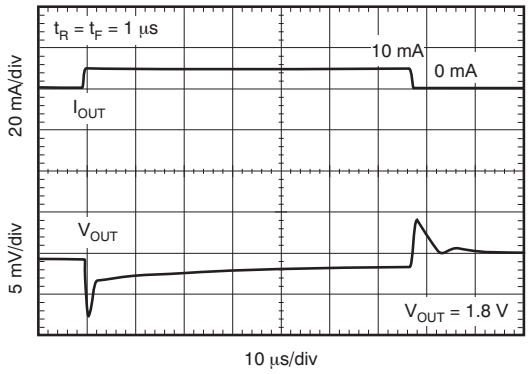



**Figure 16. Load Transient Response**

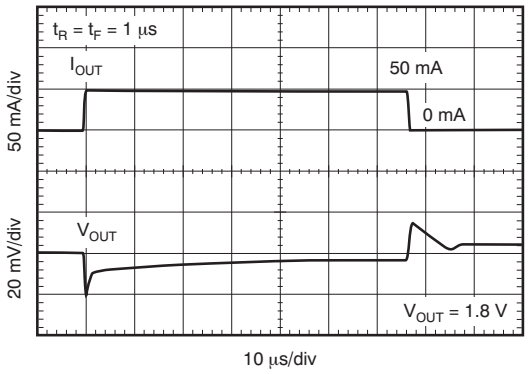



**Figure 17. Load Transient Response**

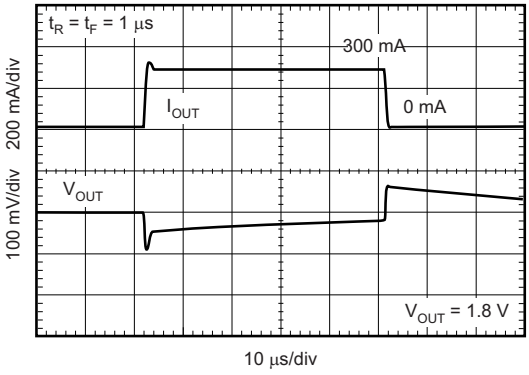



**Figure 18. Load Transient Response**

## Typical Characteristics (continued)

Over operating temperature range ($T_J$ = –40°C to +125°C), $V_{IN}$ = $V_{OUT(nom)}$ + 0.5 V or 2 V, whichever is greater; $I_{OUT}$ = 10 mA, $V_{EN}$ = $V_{IN}$, $C_{OUT}$ = 1 µF, unless otherwise noted. Typical values are at $T_J$ = 25°C.

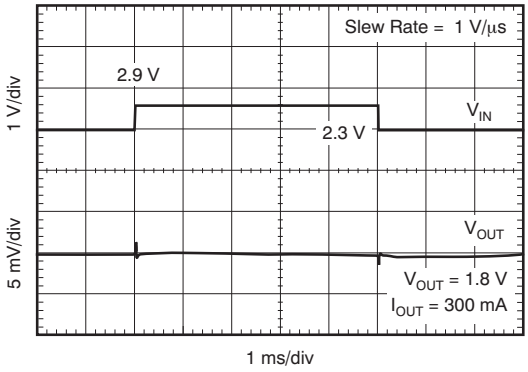



**Figure 19. Line Transient Response**

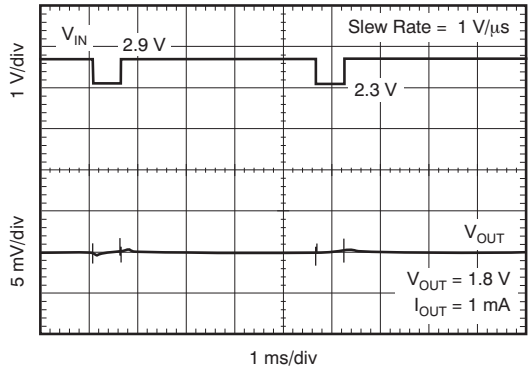



**Figure 20. Line Transient Response**

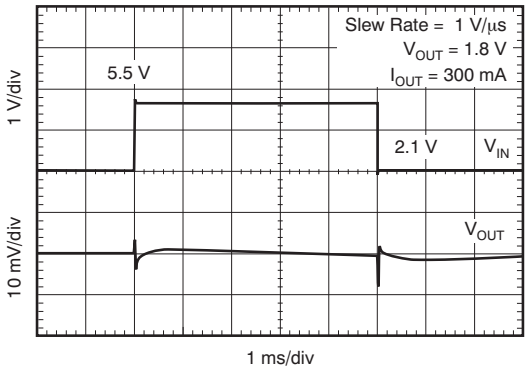



**Figure 21. Line Transient Response**

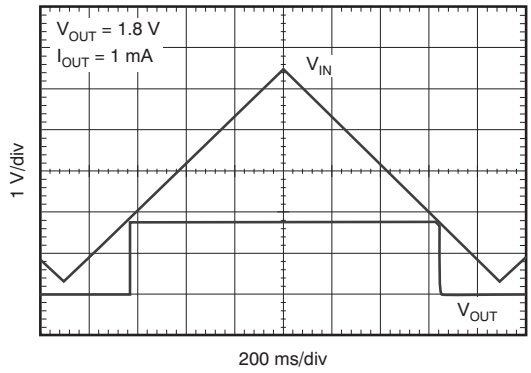



**Figure 22. $V_{IN}$ Ramp Up, Ramp Down Response**

# 7 Detailed Description

## 7.1 Overview

The TLV702-Q1 series of low-dropout (LDO) linear regulators are low quiescent current devices with excellent line and load transient performance. These LDOs are designed for power-sensitive applications. A precision bandgap and error amplifier provides overall 2% accuracy. Low output noise, very high power-supply rejection ratio (PSRR), and low dropout voltage make this series of devices ideal for most battery-operated handheld equipment. All device versions have integrated thermal shutdown, current limit, and undervoltage lockout (UVLO) protections.

## 7.2 Functional Block Diagrams

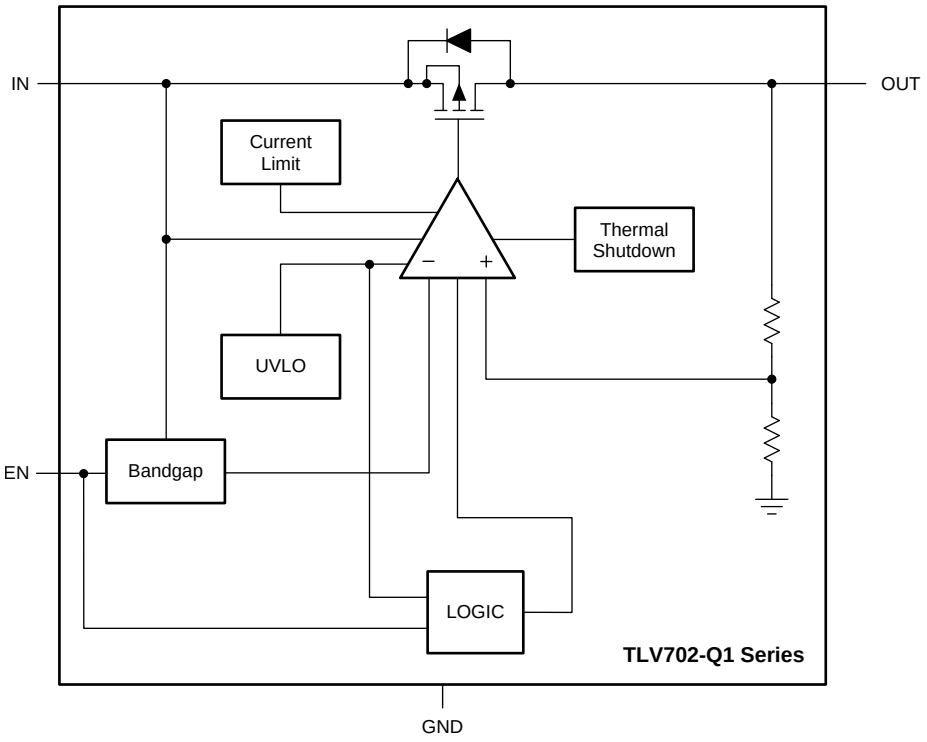



**Figure 23. TLV702-Q1 Block Diagram**

## 7.3 Feature Description

### 7.3.1 Internal Current Limit

The TLV702-Q1 internal current limit protection helps to protect the regulator during fault conditions. During current limit operation, the output sources a fixed amount of current that is largely independent of the output voltage. In such a case, the output voltage is not regulated, and is $V_{OUT} = I_{CL} \times R_{LOAD}$. The PMOS pass transistor dissipates $(V_{IN} – V_{OUT}) \times I_{CL}$ until thermal shutdown is triggered and the device turns off. As the device cools, the device is turned on by the internal thermal shutdown circuit. If the fault condition continues, the device cycles between current limit operation and thermal shutdown. See *Thermal Consideration* for more details.

The PMOS pass element in the TLV702-Q1 has a built-in body diode that conducts current when the voltage at the OUT pin exceeds the voltage at IN. This current is not limited; if extended reverse-voltage operation is anticipated, externally limit the output current to 5% of the rated $I_{OUT}$ specification.

## Feature Description (continued)

### 7.3.2 Shutdown

The enable pin (EN) is active high. The device is enabled when voltage at EN pin exceeds 0.9 V. The device is turned off when the EN pin is held at less than 0.4 V. When shutdown capability is not required, connect the EN pin to the IN pin.

### 7.3.3 Dropout Voltage

The TLV702-Q1 uses a PMOS pass transistor to achieve low dropout. When ($V_{IN}$ – $V_{OUT}$) is less than the dropout voltage ($V_{DO}$), the PMOS pass device is in the linear (triode) region of operation. The input-to-output resistance is equal to the drain-source on-state resistance ($R_{DS(on)}$) of the PMOS pass element. $V_{DO}$ scales approximately with output current because the PMOS device behaves as a resistor in dropout.

As with any linear regulator, PSRR and transient response are degraded as ($V_{IN}$ – $V_{OUT}$) approaches dropout. This effect is shown in Figure 13.

### 7.3.4 Undervoltage Lockout

The TLV702-Q1 uses a UVLO circuit to keep the output shut off until internal circuitry is operating properly.

## 7.4 Device Functional Modes

### 7.4.1 Normal Operation

The device regulates to the nominal output voltage under the following conditions:

- The input voltage is greater than the nominal output voltage added to the dropout voltage.
- The output current is less than the current limit.
- The input voltage is greater than the UVLO voltage.

### 7.4.2 Dropout Operation

If the input voltage is less than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this condition, the output voltage is the same as the input voltage minus the dropout voltage. The transient performance of the device is significantly degraded because the pass device is in a triode state and no longer regulates the output voltage of the LDO. Line or load transients in dropout may result in large output voltage deviations.

Table 1 lists the conditions that lead to the different modes of operation.

**Table 1. Device Functional Mode Comparison**

| OPERATING MODE | PARAMETER | |
|---|---|---|
| | $V_{IN}$ | $I_{OUT}$ |
| Normal mode | $V_{IN} > V_{OUT(nom)} + V_{DO}$ | $I_{OUT} < I_{CL}$ |
| Dropout mode | $V_{IN} < V_{OUT(nom)} + V_{DO}$ | $I_{OUT} < I_{CL}$ |
| Current limit | $V_{IN} >$ UVLO | $I_{OUT} > I_{CL}$ |

# 8 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 8.1 Application Information

The TLV702-Q1 belongs to a new family of next-generation value LDO regulators. These devices consume low quiescent current and deliver excellent line and load transient performance. These characteristics, combined with low noise and very good PSRR with little ($V_{IN}$ – $V_{OUT}$) headroom, make this family of devices ideal for portable RF applications. This family of regulators offers current limit and thermal protection, and is specified from –40°C to +125°C.

## 8.2 Typical Application

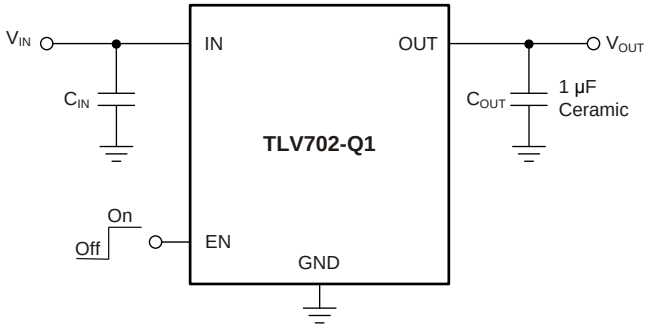



**Figure 24. Typical Application Circuit**

### 8.2.1 Design Requirements

Table 2 lists the design parameters.

**Table 2. Design Parameters**

| PARAMETER | DESIGN REQUIREMENT |
|---|---|
| Input voltage | 2.5 V to 3.3 V |
| Output voltage | 1.8 V |
| Output current | 100 mA |

### 8.2.2 Detailed Design Procedure

#### *8.2.2.1 Input and Output Capacitor Requirements*

1-µF X5R- and X7R-type ceramic capacitors are recommended because these capacitors have minimal variation in value and equivalent series resistance (ESR) over temperature.

However, the TLV702-Q1 is designed to be stable with an *effective capacitance* of 0.1 µF or larger at the output. Thus, the device is stable with capacitors of other dielectric types as well, as long as the effective capacitance under operating bias voltage and temperature is greater than 0.1 µF. This effective capacitance refers to the capacitance that the LDO sees under operating bias voltage and temperature conditions; that is, the capacitance after taking both bias voltage and temperature derating into consideration. In addition to allowing the use of lower-cost dielectrics, this capability of being stable with 0.1-µF effective capacitance also enables the use of smaller footprint capacitors that have higher derating in size- and space-constrained applications.

Using a 0.1-µF rated capacitor at the output of the LDO does not ensure stability because the effective capacitance under the specified operating conditions must not be less than 0.1 µF. Maximum ESR should be less than 200 mΩ.

Although an input capacitor is not required for stability, it is good analog design practice to connect a 0.1-µF to 1-µF, low ESR capacitor across the IN pin and GND pin of the regulator. This capacitor counteracts reactive input sources and improves transient response, noise rejection, and ripple rejection. A higher-value capacitor may be necessary if large, fast rise-time load transients are anticipated, or if the device is not located close to the power source. If source impedance is more than 2 Ω, a 0.1-µF input capacitor may be necessary for stability.

#### *8.2.2.2 Transient Response*

As with any regulator, increasing the size of the output capacitor reduces overshoot and undershoot magnitude, but increases the duration of the transient response.

### 8.2.3 Application Curves

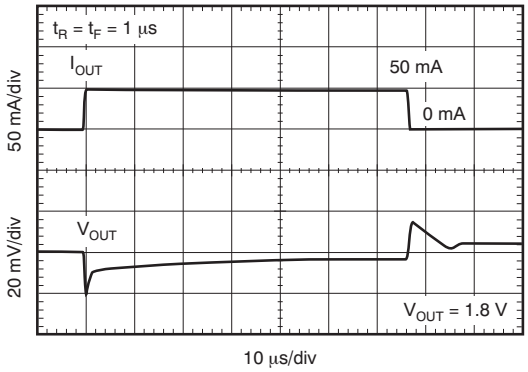



**Figure 25. Load Transient Response**

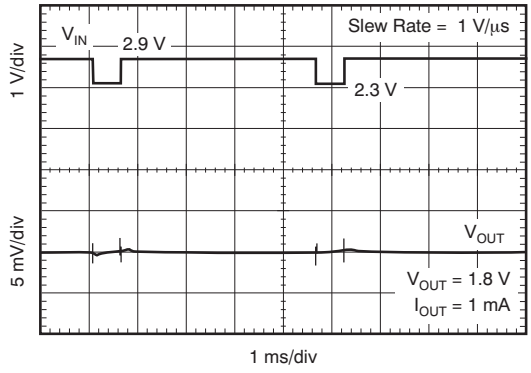



**Figure 26. Line Transient Response**

# 9 Power Supply Recommendations

Connect a low output impedance power supply directly to the IN pin of the TLV702-Q1. Inductive impedances between the input supply and the IN pin can create significant voltage excursions at the IN pin during start-up or load transient events.

## 9.1 Power Dissipation

The ability to remove heat from the die is different for each package type, presenting different considerations in the printed-circuit-board (PCB) layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air.

Refer to *Thermal Information* for thermal performance on the TLV702-Q1 evaluation module (EVM). The EVM is a two-layer board with two ounces of copper per side.

Power dissipation depends on input voltage and load conditions. Power dissipation ($P_D$) is equal to the product of the output current and the voltage drop across the output pass element, as shown in Equation 1.

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (1)$$

# 10 Layout

## 10.1 Layout Guidelines

Place the input and output capacitors as close to the device pins as possible. To improve ac performance such as PSRR, output noise, and transient response, design the board with separate ground planes for $V_{IN}$ and $V_{OUT}$, with the ground plane connected only at the GND pin of the device. In addition, connect the ground connection for the output capacitor directly to the GND pin of the device. High-ESR capacitors may degrade PSRR performance.

### 10.1.1 Thermal Consideration

Thermal protection disables the output when the junction temperature rises to approximately 165°C, allowing the device to cool. When the junction temperature cools to approximately 145°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, limit junction temperature to 125°C maximum.

To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions.

The internal protection circuitry of the TLV702-Q1 is designed to protect against overload conditions but is not intended to replace proper heatsinking. Continuously running the TLV702-Q1 into thermal shutdown degrades device reliability.

## Layout Guidelines (continued)

### 10.1.2 Package Mounting

Solder pad footprint recommendations for the TLV702-Q1 are available from the TI website at www.ti.com. The recommended layout examples for the DDC and DSE packages are shown in Figure 27 and Figure 28, respectively.

## 10.2 Layout Examples

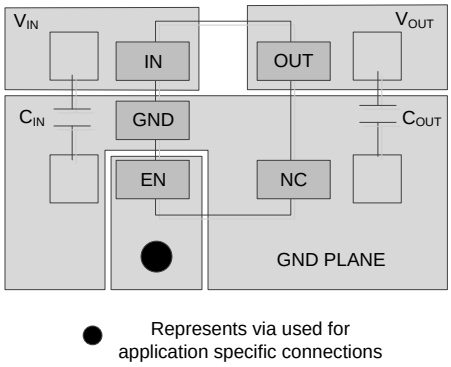



**Figure 27. Layout Example for the DDC Package**

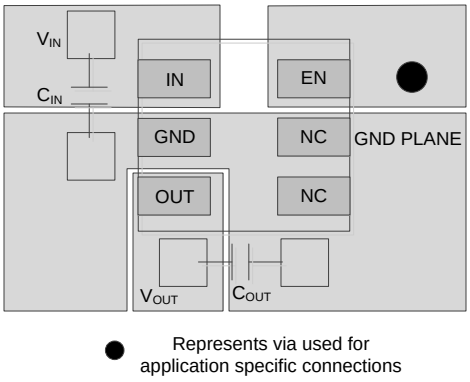



**Figure 28. Layout Example for the DSE Package**

# 11 Device and Documentation Support

## 11.1 Device Support

### 11.1.1 Development Support

#### *11.1.1.1 Spice Models*

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. A SPICE model for the TLV702 is available through the product folders under *Tools & Software*.

### 11.1.2 Device Nomenclature

**Table 3. Ordering Information(1)**

| PRODUCT | $V_{OUT}$ (2) |
|---|---|
| TLV702**xx** ***yyyz*** | **XX** is nominal output voltage (for example, 28 = 2.8 V).<br>**YYY** is the package designator.<br>**Z** is tape and reel quantity (R = 3000, T = 250). |

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.
(2) Output voltages from 1.2 V to 4.8 V in 50-mV increments are available. Contact factory for details and availability.

## 11.2 Documentation Support

### 11.2.1 Related Documentation

- *Using the TLV700xxEVM-503 Evaluation Module*, SLUU391.

## 11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

## 11.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

## 11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TLV70225QDSERQ1 | ACTIVE | WSON | DSE | 6 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | G7 | Samples |
| TLV70228QDDCRQ1 | ACTIVE | SOT-23-THIN | DDC | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | SJV | Samples |
| TLV70228QDSERQ1 | ACTIVE | WSON | DSE | 6 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HD | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF TLV702-Q1 :**

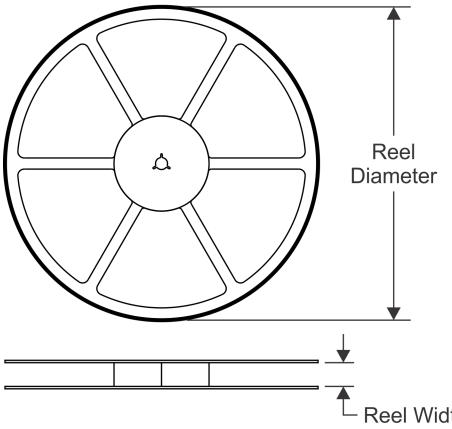
- Catalog: TLV702

NOTE: Qualified Version Definitions:

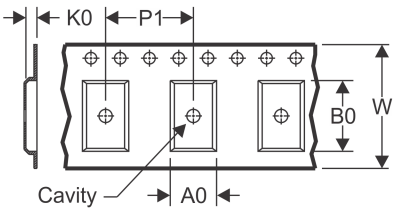
- Catalog - TI's standard catalog product

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

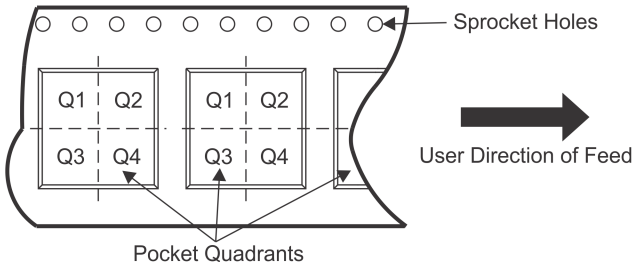



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

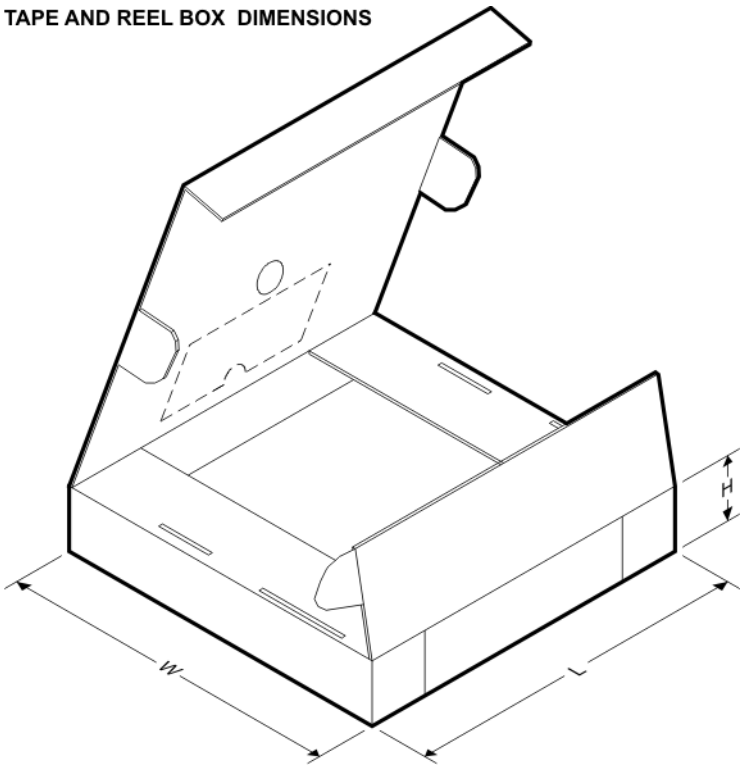
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TLV70225QDSERQ1 | WSON | DSE | 6 | 3000 | 179.0 | 8.4 | 1.8 | 1.8 | 1.0 | 4.0 | 8.0 | Q2 |
| TLV70228QDDCRQ1 | SOT-23-THIN | DDC | 5 | 3000 | 179.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV70228QDSERQ1 | WSON | DSE | 6 | 3000 | 179.0 | 8.4 | 1.8 | 1.8 | 1.0 | 4.0 | 8.0 | Q2 |

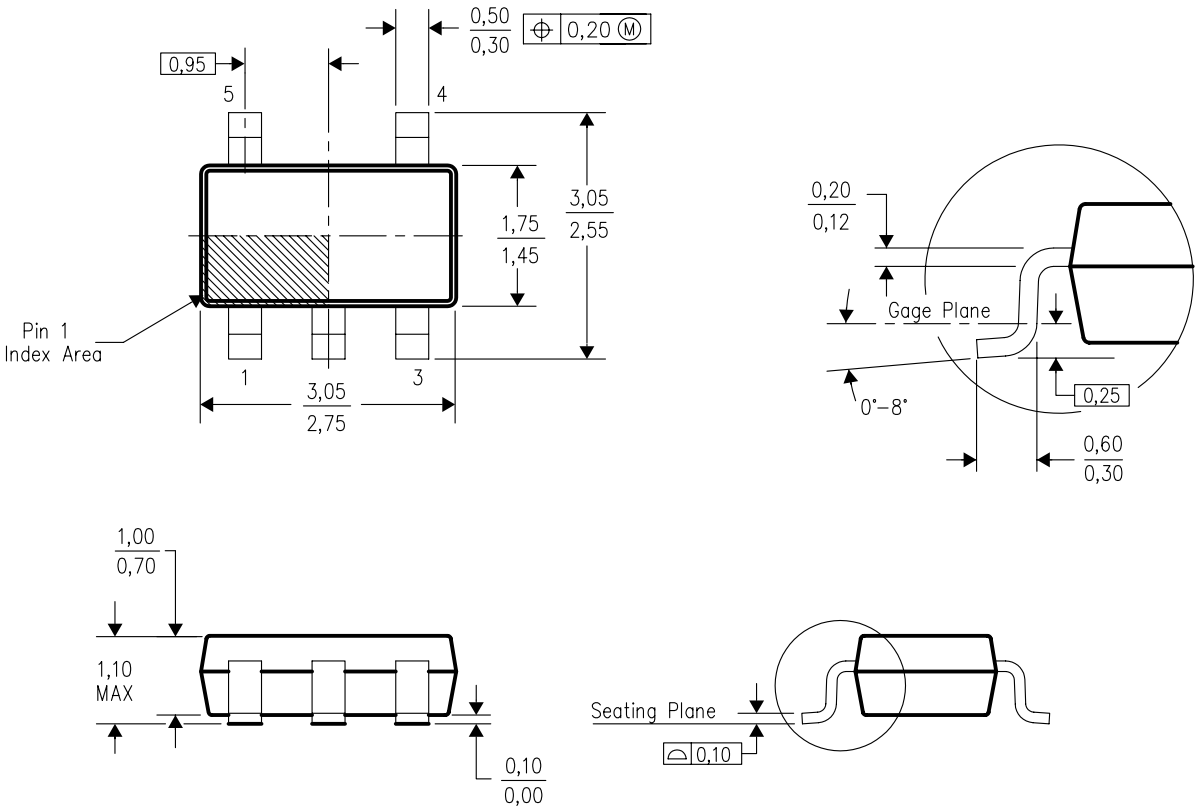
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TLV70225QDSERQ1 | WSON | DSE | 6 | 3000 | 203.0 | 203.0 | 35.0 |
| TLV70228QDDCRQ1 | SOT-23-THIN | DDC | 5 | 3000 | 195.0 | 200.0 | 45.0 |
| TLV70228QDSERQ1 | WSON | DSE | 6 | 3000 | 203.0 | 203.0 | 35.0 |

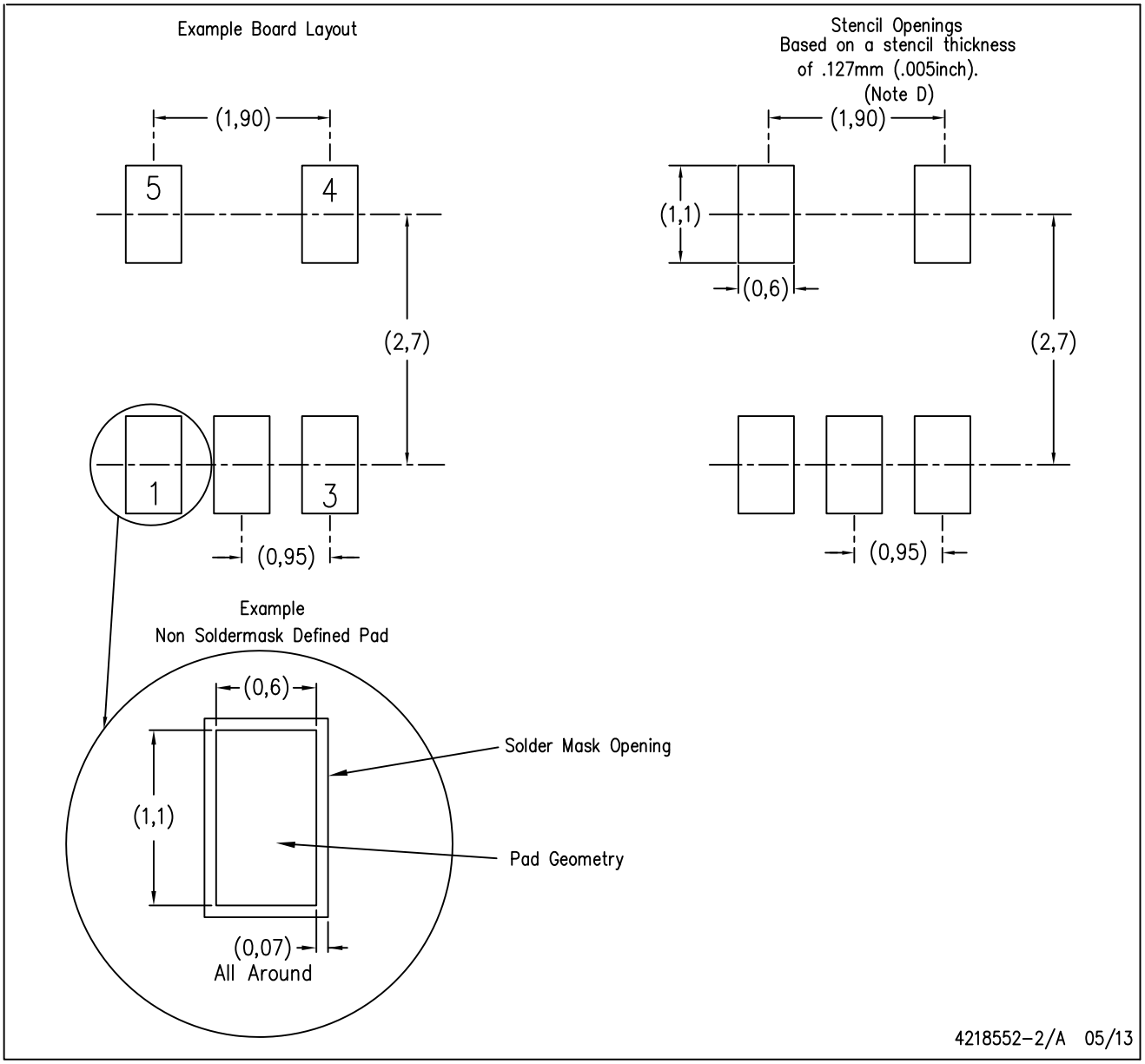
## DDC (R–PDSO–G5) PLASTIC SMALL–OUTLINE




4204403–2/E 06/05

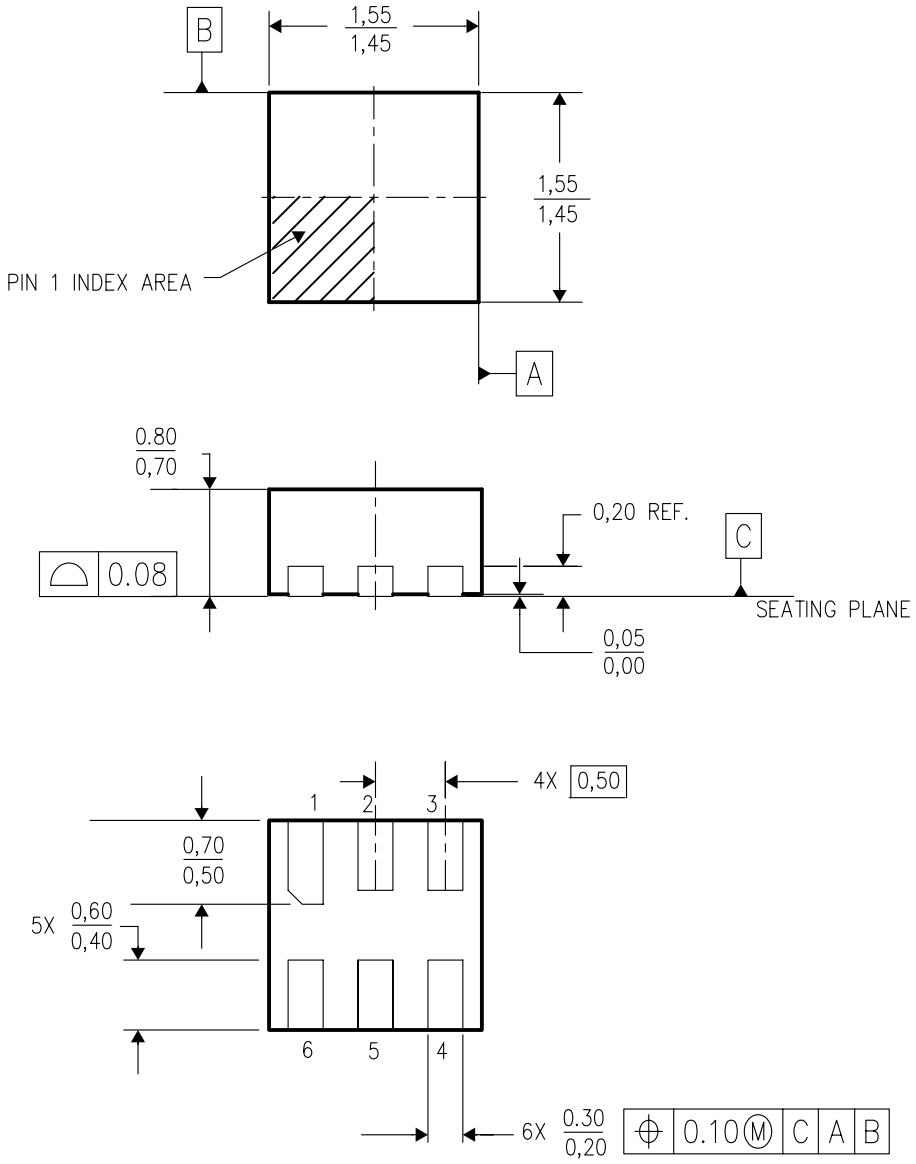
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–193 variation AB (5 pin).

DDC (R–PDSO–G5) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

DSE (S–PDSO–N6) PLASTIC SMALL OUTLINE




4207810/A 03/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. This package is lead–free.

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