TLV713 Capacitor-Free, 150-mA, Low-Dropout Regulator With Foldback Current Limit for Portable Devices

1 Features

- Stable Operation With or Without Capacitors
- Foldback Overcurrent Protection
- Packages:
  - 1-mm × 1-mm 4-Pin X2SON
  - 5-Pin SOT-23
- Very Low Dropout: 230 mV at 150 mA
- Accuracy: 1%
- Low I_Q: 50 µA
- Input Voltage Range: 1.4 V to 5.5 V
- Available in Fixed-Output Voltages: 1 V to 3.3 V
- High PSRR: 65 dB at 1 kHz
- Active Output Discharge (P Version Only)

2 Applications

- PDAs and Battery-Powered Portable Devices
- MP3 Players and Other Hand-Held Products
- WLAN and Other PC Add-On Cards

3 Description

The TLV713 series of low-dropout (LDO) linear regulators are low quiescent current LDOs with excellent line and load transient performance and are designed for power-sensitive applications. These devices provide a typical accuracy of 1%.

The TLV713 series of devices is designed to be stable without an output capacitor. The removal of the output capacitor allows for a very small solution size. However, the TLV713 series is also stable with any output capacitor if an output capacitor is used.

The TLV713 also provides inrush current control during device power up and enabling. The TLV713 limits the input current to the defined current limit to avoid large currents from flowing from the input power source. This functionality is especially important in battery-operated devices.

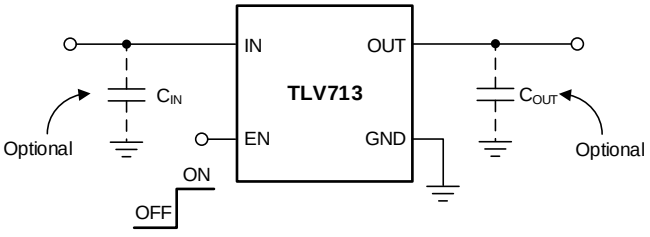
The TLV713 series is available in standard DQN and DBV packages. The TLV713P provides an active pulldown circuit to quickly discharge output loads.

Device Information(1)

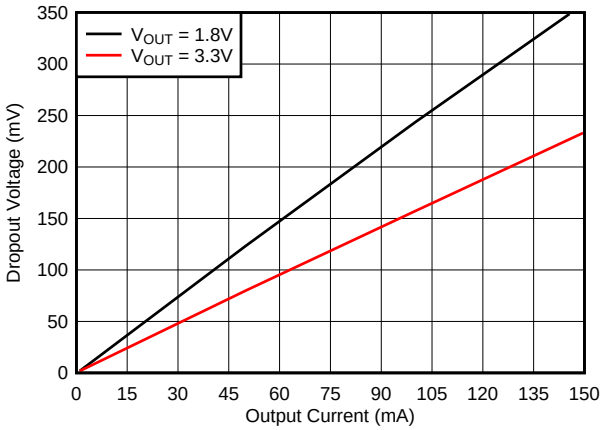
DEVICE NAME	PACKAGE	BODY SIZE
TLV713	X2SON (4)	1.00 mm × 1.00 mm
	SOT-23 (5)	2.90 mm × 1.60 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Circuit



Dropout Voltage vs Output Current



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (July 2013) to Revision E **Page**

- Changed format to meet latest data sheet standards; added new sections, and moved existing sections ... 1
- Changed Features bullet about device package options ... 1
- Changed front-page figure ... 1
- Changed Pin Configuration and Functions section; updated table format ... 5
- Changed Absolute Maximum Ratings table conditions ... 6
- Changed *Output voltage range* and *Junction temperature range* parameter maximum specifications in Absolute Maximum Ratings table ... 6
- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 6
- Corrected DBV data in Thermal Information table ... 6
- Changed conditions of Electrical Characteristics table: changed V_{IN} to $V_{IN(nom)}$; changed T_A to T_J; corrected operating temperature range ... 7
- Changed T_A to T_J and *85°C* to *125°C* throughout Electrical Characteristics table ... 7
- Added test conditions for line regulation parameter ... 7
- Changed V_{DO} parameter in Electrical Characteristics table: all rows changed ... 7
- Changed V_n parameter typical specification in Electrical Characteristics table ... 7
- Deleted T_J parameter from Electrical Characteristics table ... 7
- Added T_J condiiton to I_{LIM} parameter in Electrical Characteristics table for clarification ... 7
- Changed Typical Characteristics conditions ... 8
- Changed Figure 1 through Figure 11 in Typical Characteristics to show improved performance definition ... 8
- Added new Figure 3 ... 8
- Changed Figure 4 ... 8
- Changed Figure 5 ... 8
- Changed Figure 9 graph and figure title ... 8
- Added new Figure 10 ... 8

Revision History (continued)

- Changed Figure 12; corrected notation on axis titles to show units per graph division (units/div) 8
- Changed Figure 13; corrected notation on axis titles to show units per graph division (units/div) 9
- Changed Figure 14; corrected notation on axis titles to show units per graph division (units/div) 9
- Changed Figure 15; corrected notation on axis titles to show units per graph division (units/div) 9
- Changed Figure 17; corrected notation on axis titles to show units per graph division (units/div) 9
- Changed Figure 19; corrected notation on axis titles to show units per graph division (units/div) 10
- Changed Figure 21; corrected notation on axis titles to show units per graph division (units/div) 10
- Changed Figure 22; corrected notation on axis titles to show units per graph division (units/div) 10
- Changed Figure 23; corrected notation on axis titles to show units per graph division (units/div) 10
- Changed *Shutdown* section: clarified description 13
- Changed *Foldback Current Limit* section: adjusted flow and clarified description 14
- Changed paragraph 1 of *Thermal Protection* 14
- Changed Table 2 17
- Moved *Ordering Information* to *Device Nomenclature* section 21

Changes from Revision C (July 2013) to Revision D **Page**

- Changed document status from Mixed Status to Production Data 1
- Deleted DPW package from document 1
- Deleted reference to DPW package from last sentence of *Description* section 1
- Deleted DPW pin out drawing from front-page graphic 1
- Deleted footnote for page 1 graphic 1
- Deleted DPW pinout drawing from Pin Configurations section 5
- Deleted reference to DPW package from Pin Descriptions table 5
- Deleted DPW data from Thermal Information table 6
- Deleted footnote 3 of Ordering Information table 21

Changes from Revision B (December 2012) to Revision C **Page**

- Changed last Features bullet 1
- Added Typical Application Circuit 1
- Changed last two rows of the V_{DO} parameter in the Electrical Characteristics table 7

Changes from Revision A (October 2012) to Revision B **Page**

- Changed footnote for page 1 graphic 1
- Added DBV data to Thermal Information table 6
- Changed footnote 3 of Ordering Information table 21

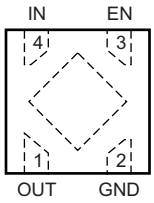
Changes from Original (September 2012) to Revision A **Page**

- Reordered Features bullets 1
- Changed dropout range in fourth Features bullet 1
- Changed *Package* and *Fixed-Output Voltage* Features bullets 1
- Added second and third paragraphs to *Description* section 1
- Updated DQN pin out drawing 1
- Changed DQN pinout caption in Pin Configurations section 5

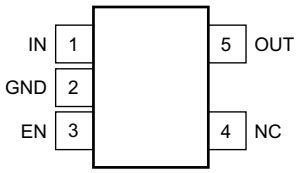
- Changed 1.2 V to 0.9 V in description of EN pin in Pin Descriptions table 5
- Changed DQN header row in Thermal Information table 6
- Changed V_{OUT} maximum specification in Electrical Characteristics table 7
- Combined all V_{DO} rows together in Electrical Characteristics table 7
- Changed V_{DO} specifications in Electrical Characteristics table 7
- Changed I_{SHDN} test conditions in Electrical Characteristics table 7
- Changed Typical Characteristics conditions 8
- Added curves 8
- Changed junction temperature range in second paragraph of *Overview* section 12
- Updated Figure 24 12
- Deleted third paragraph from *Thermal Information* section 14
- Changed second paragraph of *Input and Output Capacitor Considerations* section 16
- Deleted curve reference from *Dropout Voltage* section 16

5 Pin Configurations and Functions

DQN Package
4-Pin X2SON
Top View



DBV Package
5-Pin SOT-23
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	NO.			
	X2SON	SOT-23		
EN	3	3	I	Enable pin. Driving EN over 0.9 V turns on the regulator. Driving EN below 0.4 V puts the regulator into shutdown mode.
GND	2	2	—	Ground pin
IN	4	1	I	Input pin. A small capacitor is recommended from this pin to ground. See the *Input and Output Capacitor Considerations* section in the *Feature Description* for more details.
NC	—	4	—	No internal connection
OUT	1	5	O	Regulated output voltage pin. For best transient response, a small 1-µF ceramic capacitor is recommended from this pin to ground. See the *Input and Output Capacitor Considerations* section in the *Feature Description* for more details.
Thermal pad		—	—	The thermal pad is electrically connected to the GND node. Connect to the GND plane for improved thermal performance.

6 Specifications

6.1 Absolute Maximum Ratings

Over operating junction temperature range (T_J = 25°C), unless otherwise noted. All voltages are with respect to GND.(1)

		MIN	MAX	UNIT
Voltage	Input, V_{IN}	–0.3	6	V
	Enable, V_{EN}	–0.3	V_{IN} + 0.3	
	Output, V_{OUT}	–0.3	3.6	
Current	Maximum output, $I_{OUT(max)}$	Internally limited		
Output short-circuit duration		Indefinite		
Total power dissipation	Continuous, $P_{D(tot)}$	See *Thermal Information*		
Temperature	Storage, T_{stg}	–55	150	°C
	Junction, T_J	–55	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted).

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	1.4		5.5	V
V_{EN}	Enable range	0		V_{IN}	V
I_{OUT}	Output current	0		150	mA
C_{IN}	Input capacitor	0	1		µF
C_{OUT}	Output capacitor	0	0.1	100	µF
T_J	Operating junction temperature range	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		TLV713, TLV713P		UNIT
		DQN (X2SON)	DBV (SOT23)	
		4 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	255.8	249	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	159.3	172.7	
$R_{\theta JB}$	Junction-to-board thermal resistance	208.2	76.7	
ψ_{JT}	Junction-to-top characterization parameter	16.2	49.7	
ψ_{JB}	Junction-to-board characterization parameter	208.1	75.8	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	148.6	n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

Over operating temperature range (T_J = –40°C to 125°C), $V_{IN(nom)} = V_{OUT(nom)}$ + 0.5 V or $V_{IN(nom)}$ = 2 V (whichever is greater), I_{OUT} = 1 mA, $V_{EN} = V_{IN}$, and C_{OUT} = 0.47 µF, unless otherwise noted. Typical values are at T_J = 25°C.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range			1.4		5.5	V
V_{OUT}	Output voltage range			1		3.3	V
	DC output accuracy	$V_{OUT} \geq 1.8$ V, T_J = 25°C		–1%		1%	
		$V_{OUT} < 1.8$ V, T_J = 25°C		–20		20	mV
		$V_{OUT} \geq 1.2$ V, –40°C ≤ T_J ≤ 125°C		–1.5%		1.5%	
		$V_{OUT} < 1.2$ V, –40°C ≤ T_J ≤ 125°C		–50		50	mV
$\Delta V_{OUT(\Delta VIN)}$	Line regulation	Max {$V_{OUT(nom)}$ + 0.5 V, V_{IN} = 2.0 V} ≤ V_{IN} ≤ 5.5 V			1	5	mV
$\Delta V_{OUT(\Delta IOUT)}$	Load regulation	0 mA ≤ I_{OUT} ≤ 150 mA			10	30	mV
V_{DO}	Dropout voltage	V_{OUT} = 0.98 × $V_{OUT(nom)}$, T_J = –40°C to 85°C	1 V ≤ V_{OUT} < 1.8 V, I_{OUT} = 150 mA		600	900	mV
			V_{OUT} = 1.1 V, I_{OUT} = 100 mA		470	600	
			1.8 V ≤ V_{OUT} < 2.1 V, I_{OUT} = 30 mA		70		
			1.8 V ≤ V_{OUT} < 2.1 V, I_{OUT} = 150 mA		350	575	
			2.1 V ≤ V_{OUT} < 2.5 V, I_{OUT} = 30 mA		90		
			2.1 V ≤ V_{OUT} < 2.5 V, I_{OUT} = 150 mA		290	481	
			2.5 V ≤ V_{OUT} < 3 V, I_{OUT} = 30 mA		50		
			2.5 V ≤ V_{OUT} < 3 V, I_{OUT} = 150 mA		246	445	
			3 V ≤ V_{OUT} < 3.6 V, I_{OUT} = 30 mA		46		
			3 V ≤ V_{OUT} < 3.6 V, I_{OUT} = 150 mA		230	420	
		V_{OUT} = 0.98 × $V_{OUT(nom)}$, T_J = –40°C to 125°C	1 V ≤ V_{OUT} < 1.8 V, I_{OUT} = 150 mA		600	1020	
			V_{OUT} = 1.1 V, I_{OUT} = 100 mA		470	720	
			1.8 V ≤ V_{OUT} < 2.1 V, I_{OUT} = 150 mA		350	695	
			2.1 V ≤ V_{OUT} < 2.5 V, I_{OUT} = 150 mA		290	601	
			2.5 V ≤ V_{OUT} < 3 V, I_{OUT} = 150 mA		246	565	
			3 V ≤ V_{OUT} < 3.6 V, I_{OUT} = 150 mA		230	540	
I_{GND}	Ground pin current	I_{OUT} = 0 mA			50	75	µA
$I_{SHUTDOWN}$	Shutdown current	V_{EN} ≤ 0.4 V, 2.0 V ≤ V_{IN} ≤ 5.5 V, T_J = 25°C			0.1	1	µA
PSRR	Power-supply rejection ratio	V_{IN} = 3.3 V, V_{OUT} = 2.8 V, I_{OUT} = 30 mA	f = 100 Hz		70		dB
			f = 10 kHz		55		
			f = 1 MHz		55		
V_n	Output noise voltage	BW = 100 Hz to 100 kHz, V_{IN} = 2.3 V, V_{OUT} = 1.8 V, I_{OUT} = 10 mA			73		μV_{RMS}
t_{STR}	Start-up time(1)	C_{OUT} = 1.0 µF, I_{OUT} = 150 mA			100		µs
V_{HI}	Enable high (enabled)			0.9		V_{IN}	V
V_{LO}	Enable low (disabled)			0		0.4	V
I_{EN}	EN pin current	EN = 5.5 V			0.01		µA
$R_{PULLDOWN}$	Pulldown resistor (TLV713P only)	V_{IN} = 4 V			120		Ω
I_{LIM}	Output current limit	V_{IN} = 3.8 V, V_{OUT} = 3.3 V, T_J = –40 to 85°C		180			mA
		V_{IN} = 2.25 V, V_{OUT} = 1.8 V, T_J = –40 to 85°C		180			
		V_{IN} = 2.0 V, V_{OUT} = 1.2 V, T_J = –40 to 85°C		180			
I_{SC}	Short-circuit current	V_{OUT} = 0 V			40		mA
T_{SD}	Thermal shutdown	Shutdown, temperature increasing			158		°C
		Reset, temperature decreasing			140		

(1) Start-up time is the time from EN assertion to (0.98 × $V_{OUT(nom)}$).

6.6 Typical Characteristics

Over operating temperature range (T_J = –40°C to 125°C), V_{IN} = $V_{OUT(nom)}$ + 0.5 V or 2.0 V (whichever is greater), I_{OUT} = 10 mA, V_{EN} = V_{IN}, C_{OUT} = 1 µF, and $V_{OUT(nom)}$ = 1.8 V, unless otherwise noted. Typical values are at T_J = 25°C.

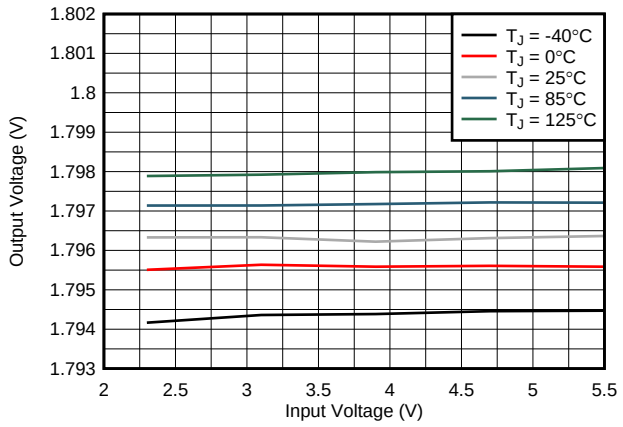


Figure 1. 1.8-V Line Regulation vs V_{IN} and Temperature

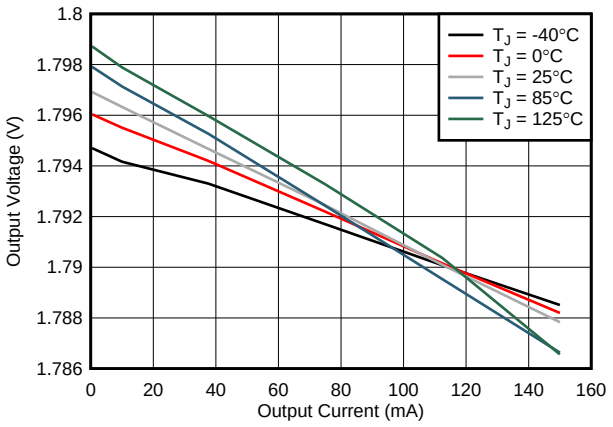


Figure 2. 1.8-V Load Regulation vs I_{OUT} and Temperature

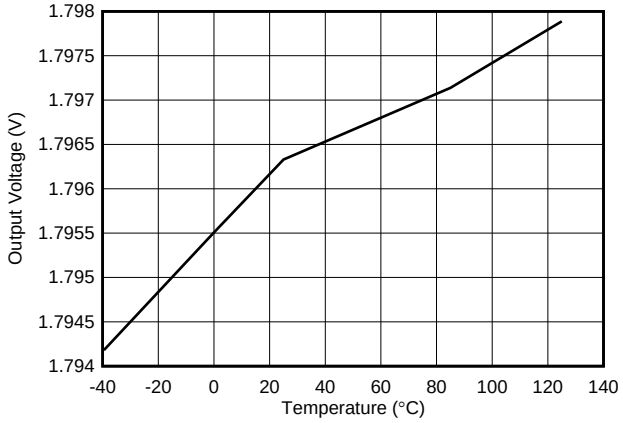


Figure 3. 1.8-V Output Voltage Over Temperature

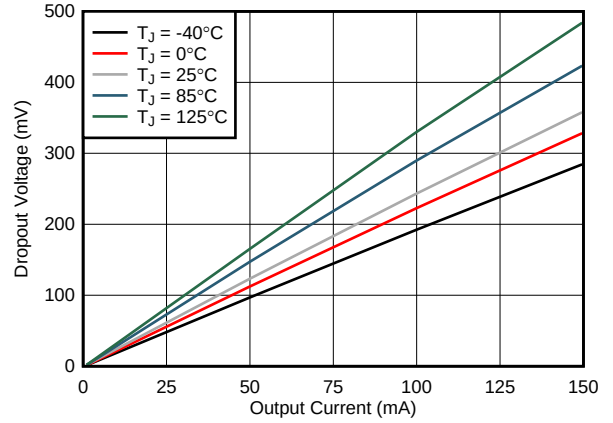


Figure 4. 1.8-V Dropout Voltage vs I_{OUT} and Temperature

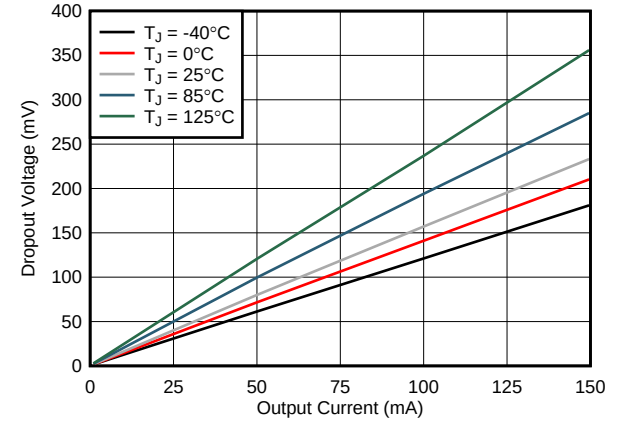


Figure 5. 3.3-V Dropout Voltage vs I_{OUT} and Temperature

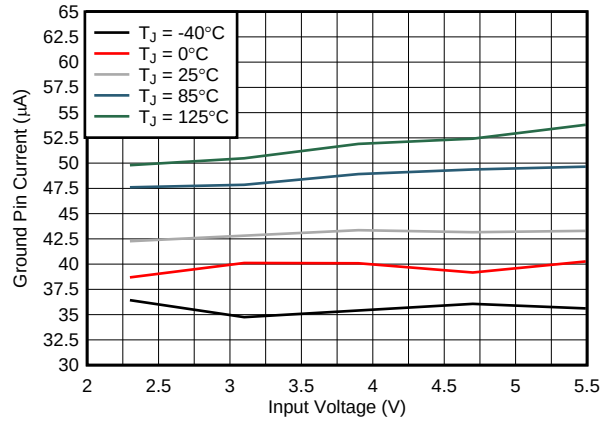


Figure 6. Ground Pin Current vs V_{IN} and Temperature

Typical Characteristics (continued)

Over operating temperature range (T_J = –40°C to 125°C), V_{IN} = $V_{OUT(nom)}$ + 0.5 V or 2.0 V (whichever is greater), I_{OUT} = 10 mA, V_{EN} = V_{IN}, C_{OUT} = 1 µF, and $V_{OUT(nom)}$ = 1.8 V, unless otherwise noted. Typical values are at T_J = 25°C.

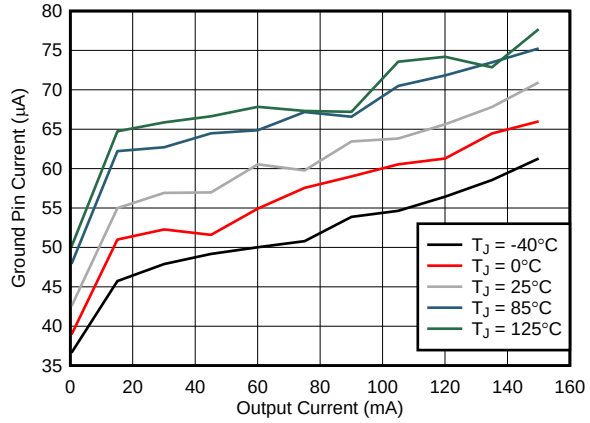


Figure 7. Ground Pin Current vs I_{OUT} and Temperature

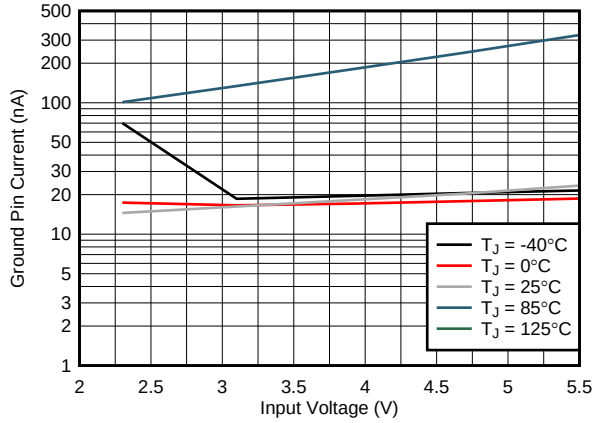


Figure 8. Shutdown Current vs V_{IN} and Temperature

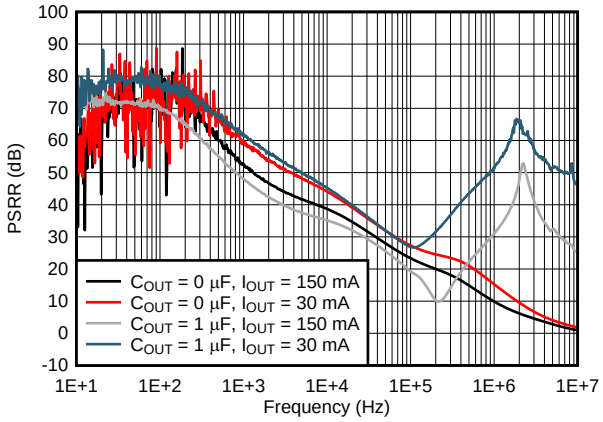


Figure 9. Power-Supply Rejection Ratio Over C_{OUT}

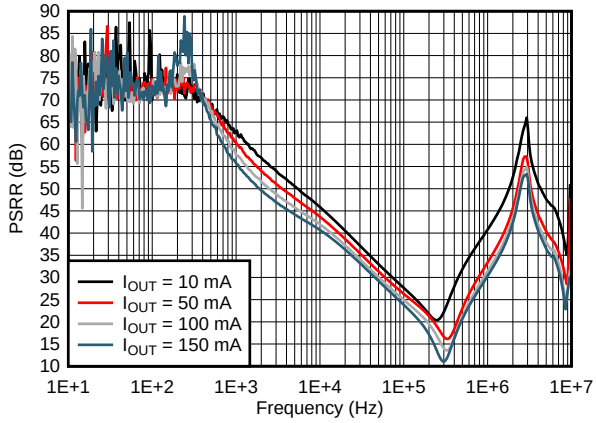


Figure 10. Power-Supply Rejection Ratio Over I_{OUT}

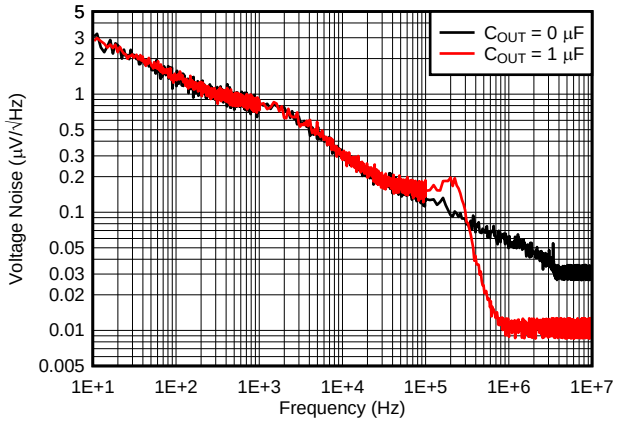


Figure 11. Output Spectral Noise Density

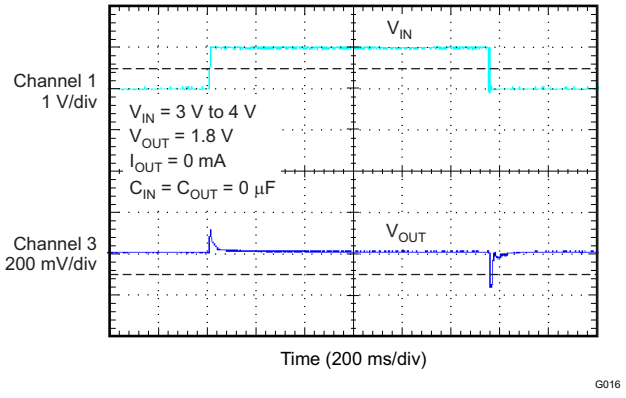


Figure 12. Line Transient

Typical Characteristics (continued)

Over operating temperature range (T_J = –40°C to 125°C), V_{IN} = $V_{OUT(nom)}$ + 0.5 V or 2.0 V (whichever is greater), I_{OUT} = 10 mA, V_{EN} = V_{IN}, C_{OUT} = 1 µF, and $V_{OUT(nom)}$ = 1.8 V, unless otherwise noted. Typical values are at T_J = 25°C.

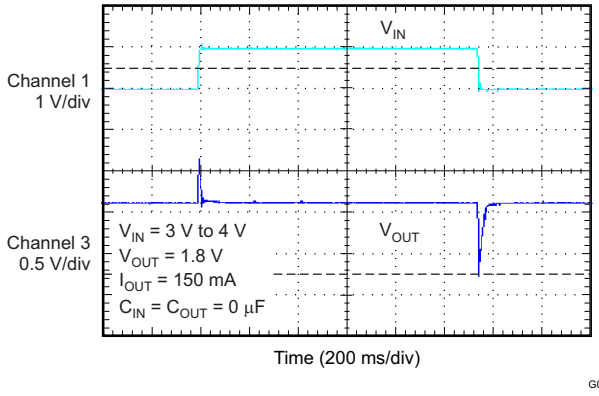


Figure 13. Line Transient

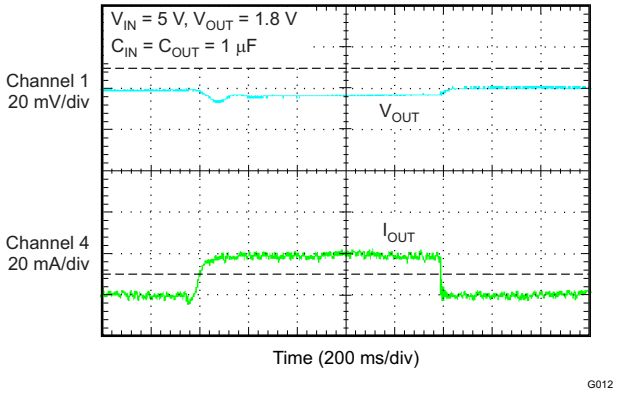


Figure 14. 0-mA to 20-mA Load Transient

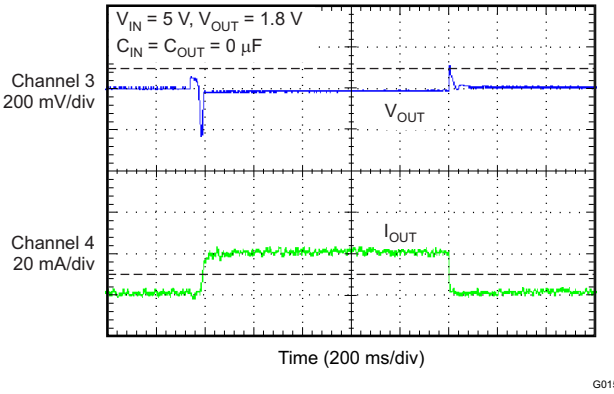


Figure 15. 0-mA to 20-mA Load Transient

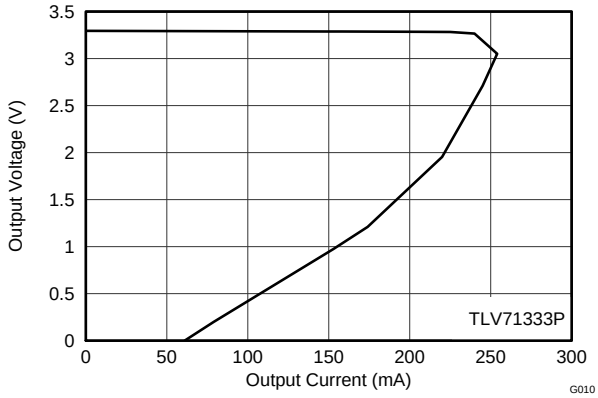


Figure 16. 3.3-V Output Voltage vs Output Current (Foldback Current Limit)

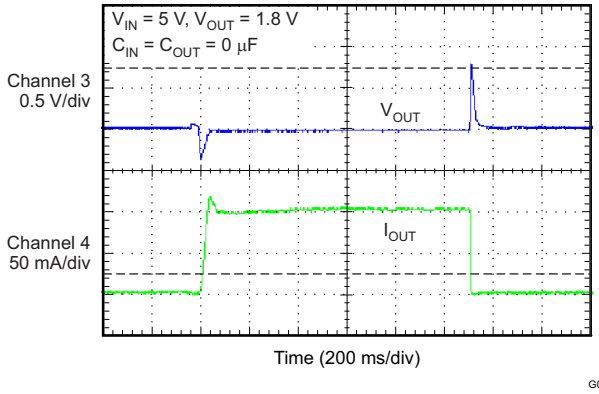


Figure 17. 0-mA to 100-mA Load Transient

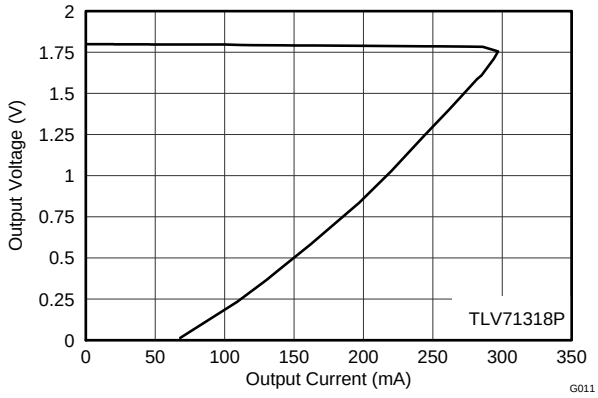


Figure 18. 1.8-V Output Voltage vs Output Current (Foldback Current Limit)

Typical Characteristics (continued)

Over operating temperature range (T_J = –40°C to 125°C), V_{IN} = $V_{OUT(nom)}$ + 0.5 V or 2.0 V (whichever is greater), I_{OUT} = 10 mA, V_{EN} = V_{IN}, C_{OUT} = 1 µF, and $V_{OUT(nom)}$ = 1.8 V, unless otherwise noted. Typical values are at T_J = 25°C.

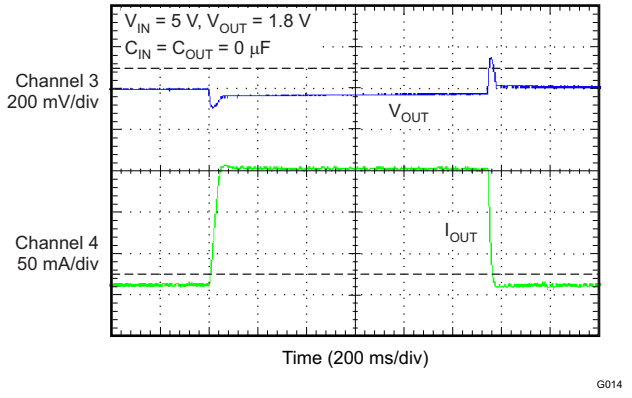


Figure 19. 10-mA to 150-mA Load Transient

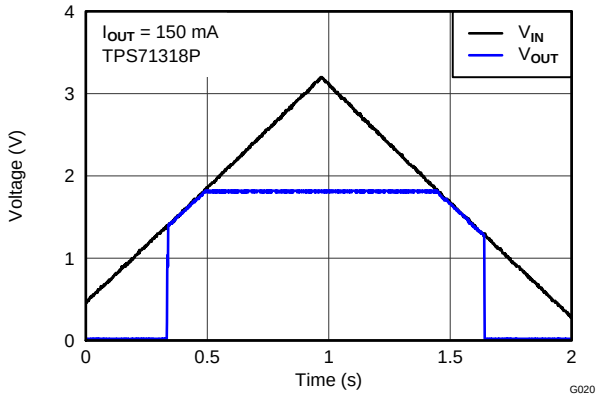


Figure 20. V_{IN} Power-Up and Power-Down

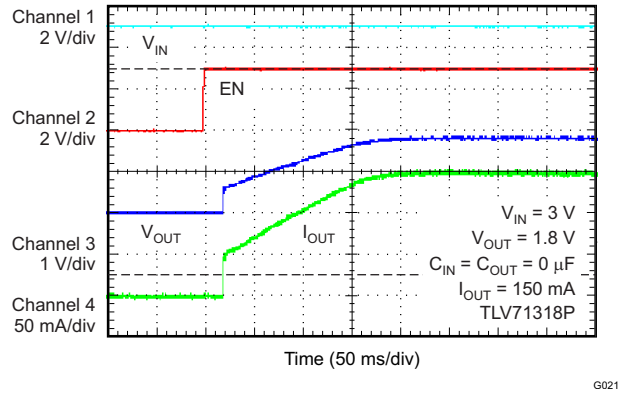


Figure 21. Start-up With EN

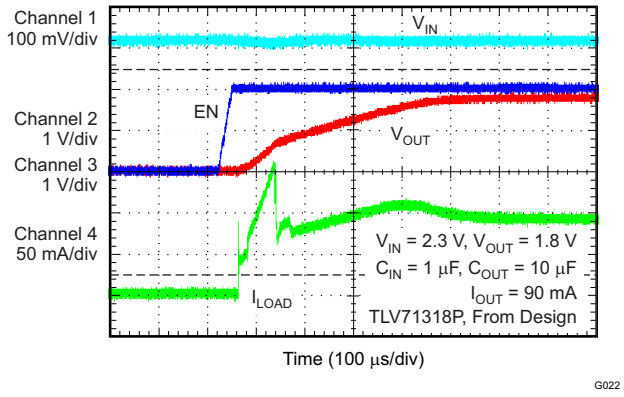


Figure 22. Start-up With EN

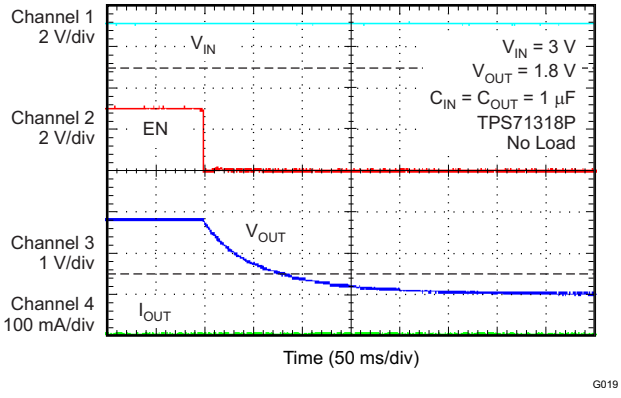


Figure 23. Shutdown Response With Enable

7 Detailed Description

7.1 Overview

These devices belong to a new family of next-generation value low-dropout (LDO) regulators. These devices consume low quiescent current and deliver excellent line and load transient performance. These characteristics, combined with low noise, very good PSRR with little (V_{IN} – V_{OUT}) headroom, make this family of devices ideal for RF portable applications.

This family of regulators offers current limit and thermal protection. Device operating junction temperature is –40°C to 125°C.

7.2 Functional Block Diagrams

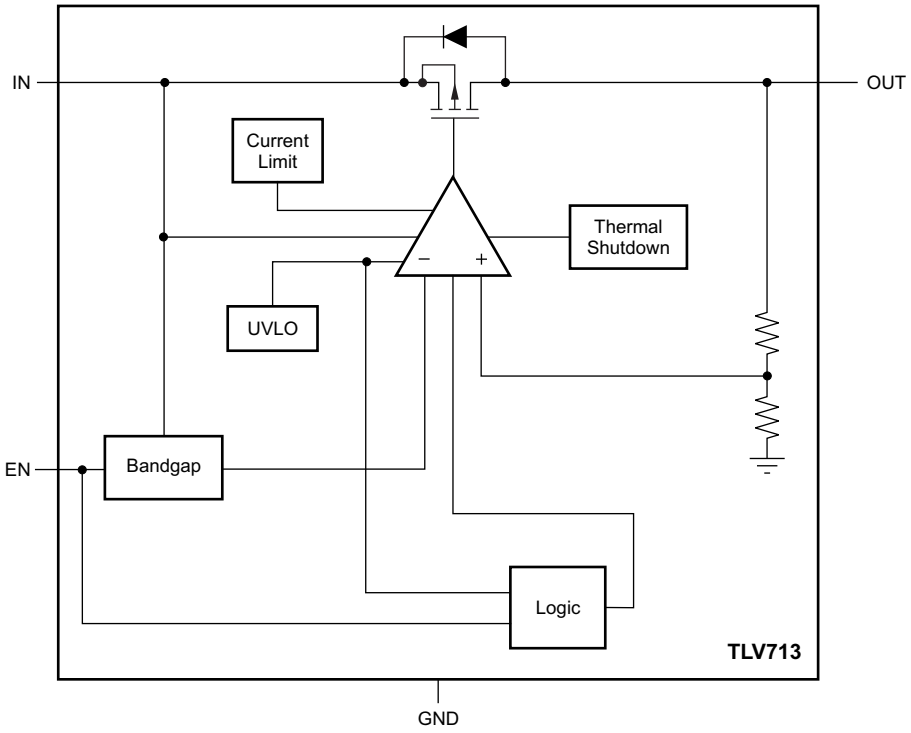


Figure 24. TLV713 Block Diagram

Functional Block Diagrams (continued)

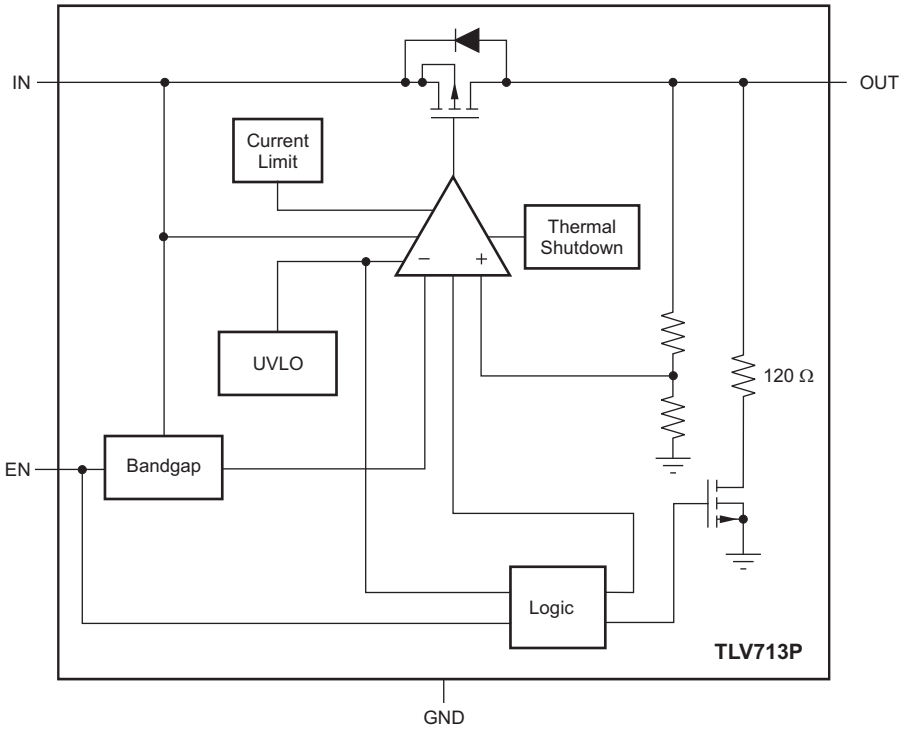


Figure 25. TLV713P Block Diagram

7.3 Feature Description

7.3.1 Undervoltage Lockout (UVLO)

The TLV713 uses a UVLO circuit that disables the output until the input voltage is greater than the rising UVLO voltage. This circuit ensures that the device does not exhibit any unpredictable behavior when the supply voltage is lower than the operational range of the internal circuitry, $V_{IN(min)}$. During UVLO disable, the output of the TLV713P version is connected to ground with a 120-Ω pulldown resistor.

7.3.2 Shutdown

The enable pin (EN) is active high. Enable the device by forcing the EN pin to exceed $V_{EN(high)}$ (0.9 V, minimum). Turn off the device by forcing the EN pin to drop below 0.4 V. If shutdown capability is not required, connect EN to IN.

The TLV713P has an internal pulldown MOSFET that connects a 120-Ω resistor to ground when the device is disabled. The discharge time after disabling depends on the output capacitance (C_{OUT}) and the load resistance (R_L) in parallel with the 120-Ω pulldown resistor. The time constant is calculated in Equation 1.

$$\tau = \frac{120 \cdot R_L}{120 + R_L} \cdot C_{OUT} \quad (1)$$

Feature Description (continued)

7.3.3 Foldback Current Limit

The TLV713 has an internal foldback current limit that helps protect the regulator during fault conditions. The current supplied by the device is gradually reducedwhile the output voltage decreases. When the output is shorted, the LDO supplies a typical current of 40 mA. Output voltage is not regulated when the device is in current limit, and is calculated by Equation 2:

$$V_{OUT} = I_{LIMIT} \times R_{LOAD} \quad (2)$$

The PMOS pass transistor dissipates $[(V_{IN} – V_{OUT}) \times I_{LIMIT}]$ until thermal shutdown is triggered and the device turns off. The device is turned on by the internal thermal shutdown circuit during cool down. If the fault condition continues, the device cycles between current limit and thermal shutdown. See the *Thermal Information* section for more details.

The TLV713 PMOS pass element has a built-in body diode that conducts current when the voltage at OUT exceeds the voltage at IN. This current is not limited, so if extended reverse voltage operation is anticipated, external limiting to 5% of the rated output current is recommended.

7.3.4 Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately 158°C, allowing the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits regulator dissipation, protecting the device from damage as a result of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, junction temperature must be limited to 125°C maximum. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions.

The TLV713 internal protection circuitry is designed to protect against overload conditions. This circuitry is not intended to replace proper heatsinking. Continuously running the TLV713 into thermal shutdown degrades device reliability.

7.4 Device Functional Modes

7.4.1 Normal Operation

The device regulates to the nominal output voltage under the following conditions:

- The input voltage is at least as high as $V_{IN(min)}$.
- The input voltage is greater than the nominal output voltage added to the dropout voltage.
- The enable voltage has previously exceeded the enable rising threshold voltage and has not decreased below the enable falling threshold.
- The output current is less than the current limit.
- The device junction temperature is less than the maximum specified junction temperature.

7.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode of operation, the output voltage is the same as the input voltage minus the dropout voltage. The transient performance of the device is significantly degraded because the pass device is in the linear region and no longer controls the current through the LDO. Line or load transients in dropout can result in large output voltage deviations.

7.4.3 Disabled

The device is disabled under the following conditions:

- The enable voltage is less than the enable falling threshold voltage or has not yet exceeded the enable rising threshold.
- The device junction temperature is greater than the thermal shutdown temperature.

Table 1 shows the conditions that lead to the different modes of operation.

Table 1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	V_{EN}	I_{OUT}	T_J
Normal mode	$V_{IN} > V_{OUT(nom)} + V_{DO}$ and $V_{IN} > V_{IN(min)}$	$V_{EN} > V_{EN(high)}$	$I_{OUT} < I_{LIM}$	$T_J < 125°C$
Dropout mode	$V_{IN(min)} < V_{IN} < V_{OUT(nom)} + V_{DO}$	$V_{EN} > V_{EN(high)}$	—	$T_J < 125°C$
Disabled mode (any true condition disables the device)	—	$V_{EN} < V_{EN(low)}$	—	$T_J > 158°C$

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Input and Output Capacitor Considerations

The TLV713 uses an advanced internal control loop to obtain stable operation both with and without the use of input or output capacitors. The TLV713 dynamic performance is improved with the use of an output capacitor. An output capacitance of 0.1 µF or larger generally provides good dynamic response. X5R- and X7R-type ceramic capacitors are recommended because these capacitors have minimal variation in value and equivalent series resistance (ESR) over temperature.

Although an input capacitor is not required for stability, it is good analog design practice to connect a 0.1-µF to 1-µF capacitor from IN to GND. This capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR. An input capacitor is recommended if the source impedance is more than 0.5 Ω. A higher-value capacitor may be necessary if large, fast, rise-time load transients are anticipated or if the device is located several inches from the input power source.

8.1.2 Dropout Voltage

The TLV713 uses a PMOS pass transistor to achieve low dropout. When (V_{IN} – V_{OUT}) is less than the dropout voltage (V_{DO}), the PMOS pass device is in the linear region of operation and the input-to-output resistance is the $R_{DS(on)}$ of the PMOS pass element. V_{DO} scales approximately with output current because the PMOS device behaves like a resistor in dropout. As with any linear regulator, PSRR and transient response are degraded as (V_{IN} – V_{OUT}) approaches dropout.

8.1.3 Transient Response

As with any regulator, increasing the size of the output capacitor reduces over- and undershoot magnitude but increases the duration of the transient response.

8.2 Typical Application

Several versions of the TPS713 are ideal for powering the MSP430 microcontroller.

Figure 26 shows a diagram of the TLV713 powering an MSP430 microcontroller. Table 2 shows potential applications of some voltage versions.

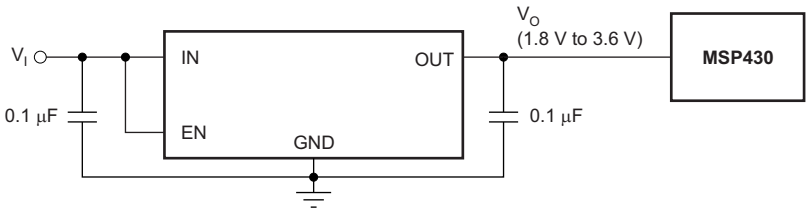


Figure 26. TLV713 Powering a Microcontroller

Table 2. Typical MSP430 Applications

DEVICE	V_{OUT} (Typ)	APPLICATION
TLV71318P	1.8 V	Allows for lowest power consumption with many MSP430s
TLV71325P	2.5 V	2.2-V supply required by many MSP430s for flash programming and erasing

8.2.1 Design Requirements

Table 3 lists the design requirements.

Table 3. Design Parameters

PARAMETER	DESIGN REQUIREMENT
Input voltage	4.2 V to 3 V (Lithium Ion battery)
Output voltage	1.8 V, ±1%
DC output current	10 mA
Peak output current	75 mA
Maximum ambient temperature	65°C

8.2.2 Detailed Design Procedure

An input capacitor is not required for this design because of the low impedance connection directly to the battery.

No output capacitor allows for the minimal possible inrush current during start-up, ensuring the 180-mA maximum input current limit is not exceeded.

Verify that the maximum junction temperature is not exceeded by referring to Figure 32.

8.2.3 Application Curves

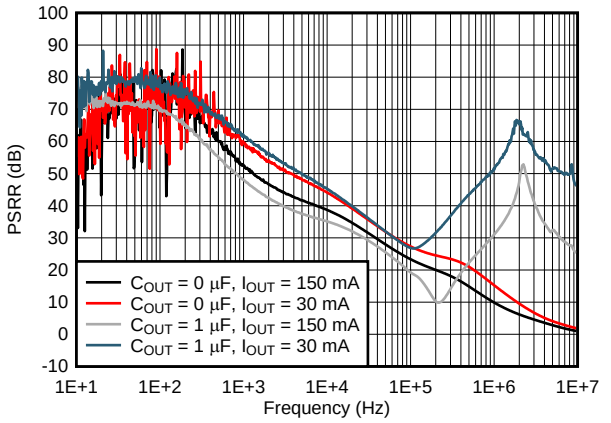


Figure 27. Power-Supply Rejection Ratio vs Frequency

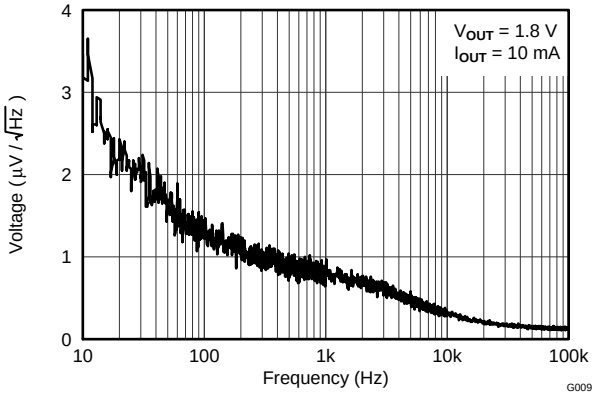


Figure 28. Output Spectral Noise Density

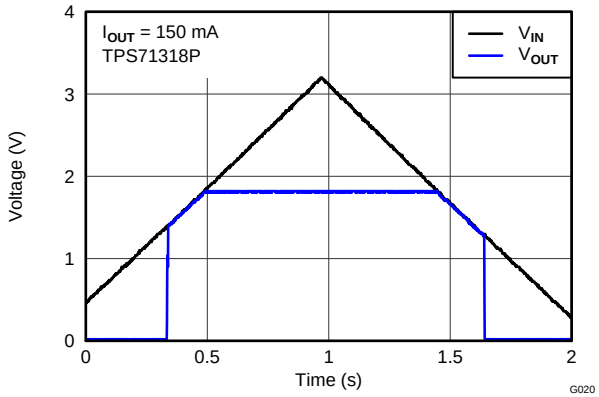


Figure 29. V_{IN} Power Up and Power Down

8.3 Do's and Don'ts

Place at least one 0.1-µF ceramic capacitor as close as possible to the OUT pin of the regulator for best transient performance.

Place at least one 1-µF capacitor as close as possible to the IN pin for best transient performance.

Do not place the output capacitor more than 10 mm away from the regulator.

Do not exceed the absolute maximum ratings.

Do not continuously operate the device in current limit or near thermal shutdown.

9 Power-Supply Recommendations

These devices are designed to operate from an input voltage supply range from 1.4 V to 5.5 V. The input voltage range must provide adequate headroom for the device to have a regulated output. This input supply must be well-regulated and stable. If the input supply is noisy, additional input capacitors with low ESR can help improve the output noise performance.

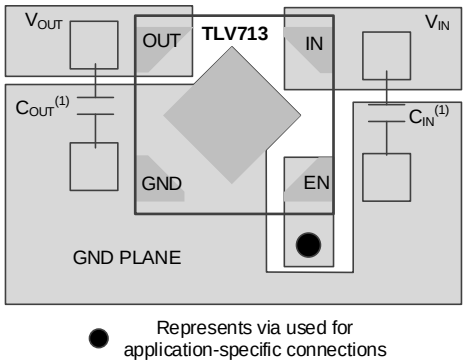
10 Layout

10.1 Layout Guidelines

10.1.1 Board Layout Recommendations to Improve PSRR and Noise Performance

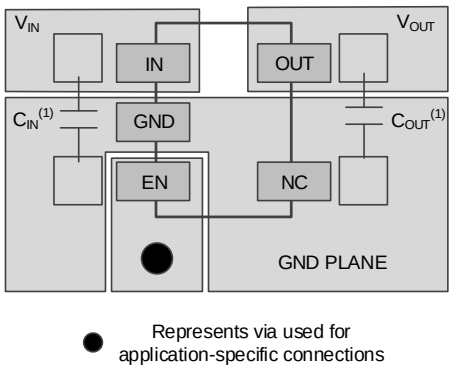
Input and output capacitors must be placed as close to the device pins as possible. To improve AC performance (such as PSRR, output noise, and transient response), TI recommends that the board be designed with separate ground planes for V_{IN} and V_{OUT}, with the ground plane connected only at the device GND pin. In addition, the output capacitor ground connection must be connected directly to the device GND pin. High-ESR capacitors may degrade PSRR performance.

10.2 Layout Examples



(1) Not required.

Figure 30. X2SON Layout Example



(1) Not required.

Figure 31. SOT-23 Layout Example

10.3 Power Dissipation

The ability to remove heat from the die is different for each package type, presenting different considerations in the printed-circuit-board (PCB) layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Performance data for JEDEC low- and high-K boards are given in *Thermal Information*. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers also improves the heatsink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation (P_D) can be approximated by the product of the output current times the voltage drop across the output pass element (V_{IN} to V_{OUT}), as shown in Equation 3.

Power Dissipation (continued)

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (3)$$

Figure 32 shows the maximum ambient temperature versus the power dissipation of the TLV713. This figure assumes the device is soldered on a JEDEC standard, high-K layout with no airflow over the board. Actual board thermal impedances vary widely. If the application requires high power dissipation, having a thorough understanding of the board temperature and thermal impedances is helpful to ensure the TLV713 does not operate above a junction temperature of 125°C.

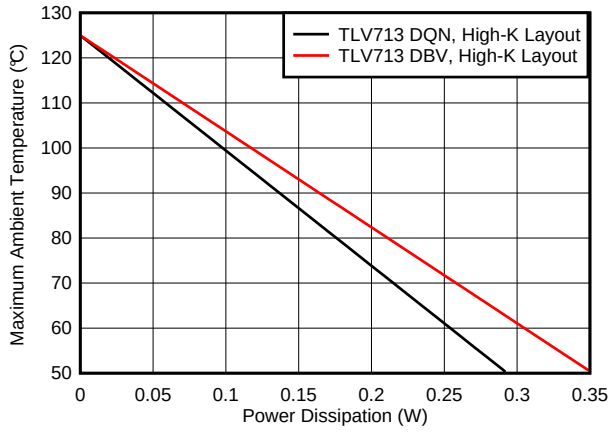


Figure 32. Maximum Ambient Temperature vs Device Power Dissipation

Estimating the junction temperature can be done by using the thermal metrics Ψ_{JT} and Ψ_{JB}, shown in the *Thermal Information* table. These metrics are a more accurate representation of the heat transfer characteristics of the die and the package than $R_{\theta JA}$. The junction temperature can be estimated with Equation 4.

$$\Psi_{JT}: \quad T_J = T_T + \Psi_{JT} \bullet P_D$$
$$\Psi_{JB}: \quad T_J = T_B + \Psi_{JB} \bullet P_D$$

where

- P_D is the power dissipation shown by Equation 3,
- T_T is the temperature at the center-top of the IC package,
- T_B is the PCB temperature measured 1 mm away from the IC package *on the PCB surface*. (4)

NOTE

Both T_T and T_B can be measured on actual application boards using a thermo-gun (an infrared thermometer).

For more information about measuring T_T and T_B, see the application note *Using New Thermal Metrics* (SBVA025), available for download at www.ti.com.

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 Evaluation Modules

Three evaluation modules (EVMs) are available to assist in the initial circuit performance evaluation using the TLV713:

- TLV71312PEVM-171
- TLV71318PEVM-171
- TLV71333PEVM-171

These EVMs can be requested at the Texas Instruments website through the device product folders or purchased directly from the TI eStore.

11.1.1.2 Spice Models

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. A SPICE model for the TLV713 is available through the product folders under *Tools & Software*.

11.1.2 Device Nomenclature

Table 4. Ordering Information(1)(2)

PRODUCT	V_O
TLV713**xx(x)Pyyyz**	**XX(X)** is the nominal output voltage. For output voltages with a resolution of 100 mV, two digits are used in the ordering number; otherwise, three digits are used (for example, 28 = 2.8 V; 475 = 4.75 V). **P** is optional; devices with P have an LDO regulator with an active output discharge. **YYY** is the package designator. **Z** is the package quantity. R is for reel (3000 pieces), T is for tape (250 pieces).

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder on www.ti.com.
(2) Output voltages from 1.0 V to 3.3 V in 50-mV increments are available. Contact the factory for details and availability.

11.2 Documentation Support

11.2.1 Related Documentation

- *Using New Thermal Metrics*, SBVA025
- *TLV713xxEVM-171 User's Guide*, SLVU771

11.3 Trademarks

All trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV71310PDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	VUQI	Samples
TLV71310PDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	VUQI	Samples
TLV71310PDQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	ET	Samples
TLV71310PDQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	ET	Samples
TLV71311PDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	VUPI	Samples
TLV71311PDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	VUPI	Samples
TLV71312PDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	VUEI	Samples
TLV71312PDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	VUEI	Samples
TLV71312PDQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AF	Samples
TLV71312PDQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AF	Samples
TLV71315PDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	VUGI	Samples
TLV71315PDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	VUGI	Samples
TLV71315PDQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AY	Samples
TLV71315PDQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AY	Samples
TLV713185PDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	VUII	Samples
TLV713185PDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	VUII	Samples
TLV713185PDQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	A1	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV713185PDQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	A1	Samples
TLV71318PDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	VUDI	Samples
TLV71318PDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	VUDI	Samples
TLV71318PDQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AW	Samples
TLV71318PDQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AW	Samples
TLV71320DQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	B2	Samples
TLV71320DQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	B2	Samples
TLV71325PDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	VUJI	Samples
TLV71325PDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	VUJI	Samples
TLV71325PDQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AZ	Samples
TLV71325PDQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AZ	Samples
TLV713285PDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	VULI	Samples
TLV713285PDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	VULI	Samples
TLV713285PDQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	A2	Samples
TLV713285PDQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	A2	Samples
TLV71328PDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	VUKI	Samples
TLV71328PDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	VUKI	Samples
TLV71328PDQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AK	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV71328PDQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AK	Samples
TLV71330PDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	VUMI	Samples
TLV71330PDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	VUMI	Samples
TLV71330PDQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AL	Samples
TLV71330PDQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AL	Samples
TLV71333PDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	VUFI	Samples
TLV71333PDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	VUFI	Samples
TLV71333PDQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AH	Samples
TLV71333PDQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AH	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TLV713P :

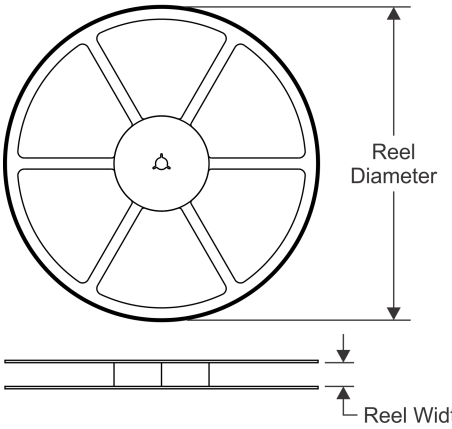
- Automotive: TLV713P-Q1

NOTE: Qualified Version Definitions:

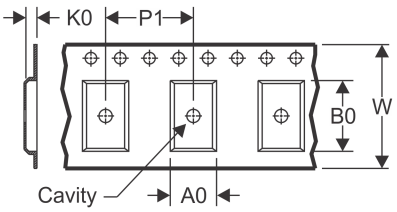
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

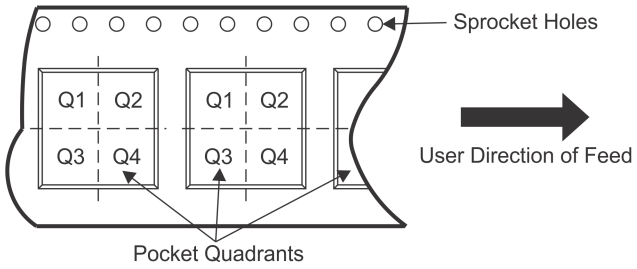


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

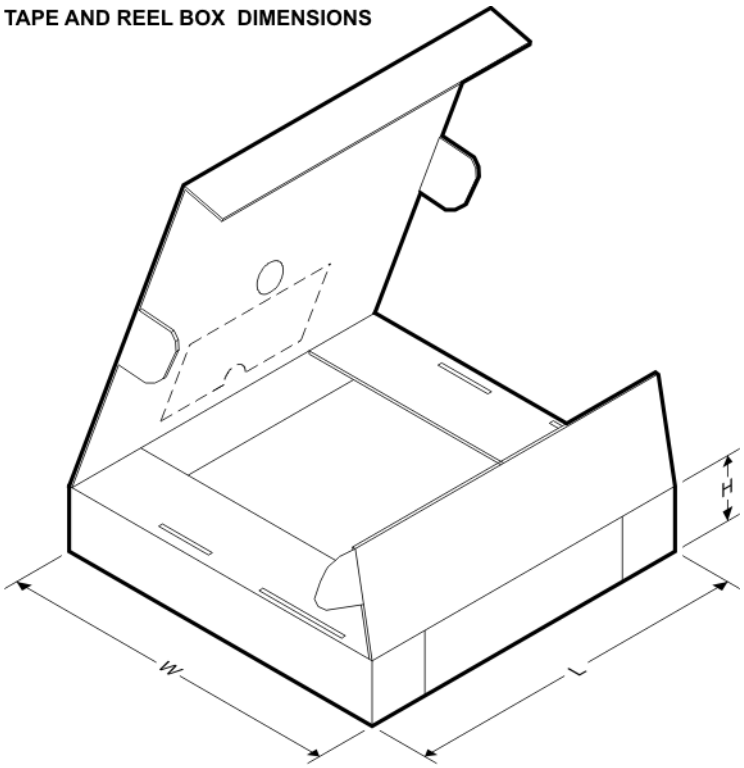


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV71310PDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV71310PDBVT	SOT-23	DBV	5	250	178.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TLV71310PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV71310PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV71311PDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV71311PDBVT	SOT-23	DBV	5	250	178.0	8.4	3.3	3.2	1.4	4.0	8.0	Q3
TLV71312PDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV71312PDBVT	SOT-23	DBV	5	250	178.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TLV71312PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV71312PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV71315PDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV71315PDBVT	SOT-23	DBV	5	250	178.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TLV71315PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV71315PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV713185PDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV713185PDBVT	SOT-23	DBV	5	250	178.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TLV713185PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV713185PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV71318PDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV71318PDBVT	SOT-23	DBV	5	250	178.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TLV71318PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV71318PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV71320DQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV71320DQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV71325PDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV71325PDBVT	SOT-23	DBV	5	250	178.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TLV71325PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV71325PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV713285PDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV713285PDBVT	SOT-23	DBV	5	250	178.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TLV713285PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV713285PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV71328PDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV71328PDBVT	SOT-23	DBV	5	250	178.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TLV71328PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV71328PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV71330PDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV71330PDBVT	SOT-23	DBV	5	250	178.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TLV71330PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV71330PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV71333PDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TLV71333PDBVT	SOT-23	DBV	5	250	178.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TLV71333PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV71333PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS

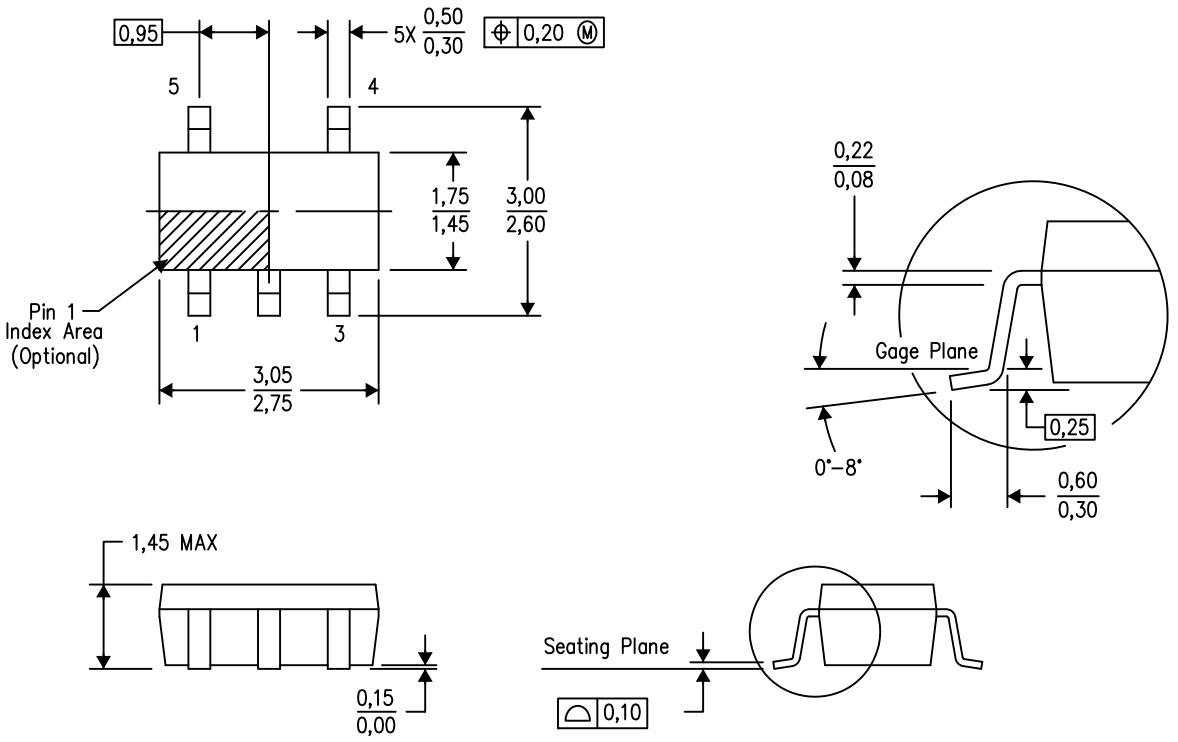


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV71310PDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV71310PDBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TLV71310PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV71310PDQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV71311PDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV71311PDBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TLV71312PDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV71312PDBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TLV71312PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV71312PDQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV71315PDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV71315PDBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TLV71315PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV71315PDQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV713185PDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV713185PDBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TLV713185PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV713185PDQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV71318PDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV71318PDBVT	SOT-23	DBV	5	250	180.0	180.0	18.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV71318PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV71318PDQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV71320DQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV71320DQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV71325PDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV71325PDBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TLV71325PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV71325PDQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV713285PDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV713285PDBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TLV713285PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV713285PDQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV71328PDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV71328PDBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TLV71328PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV71328PDQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV71330PDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV71330PDBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TLV71330PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV71330PDQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV71333PDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV71333PDBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TLV71333PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV71333PDQNT	X2SON	DQN	4	250	184.0	184.0	19.0

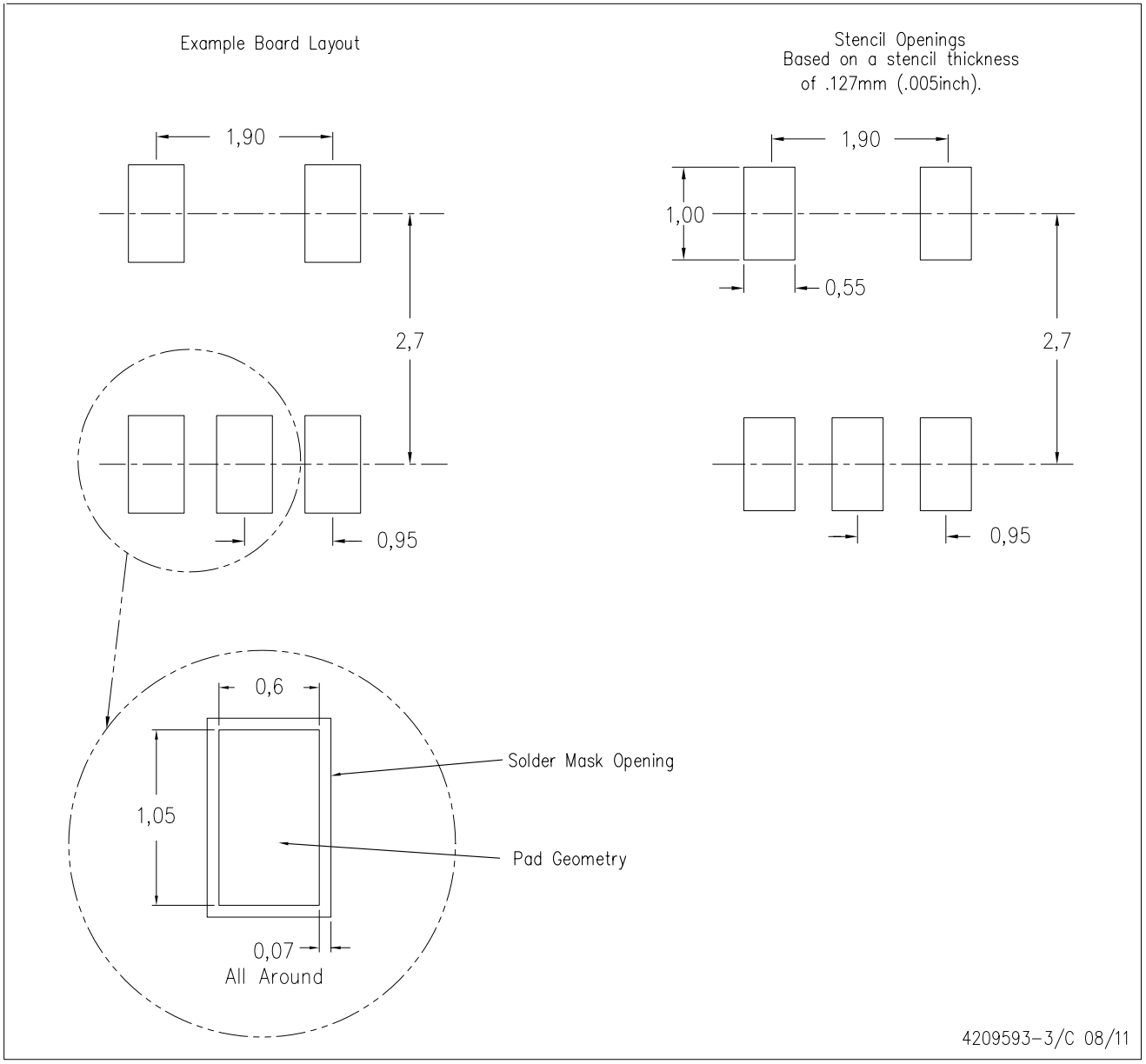
DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4073253–4/N 12/14

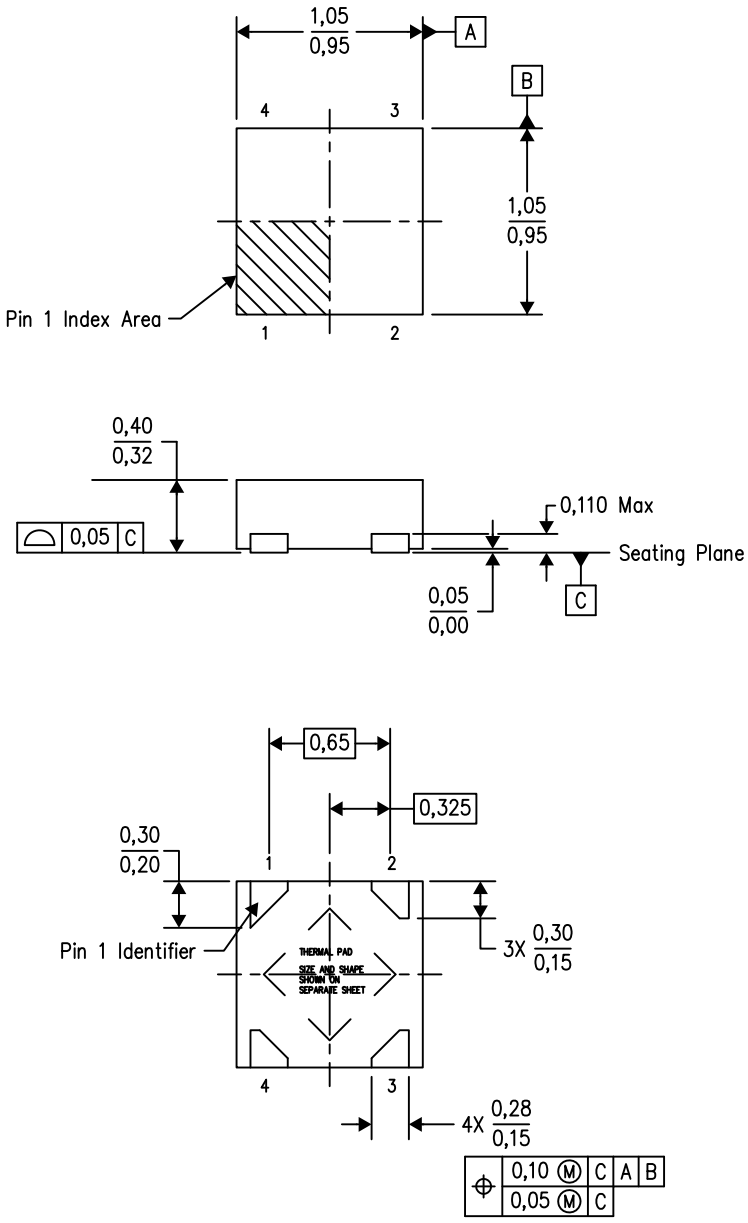
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–178 Variation AA.

DBV (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

DQN (S–PX2SON–N4) PLASTIC SMALL OUTLINE NO–LEAD



4210367/D 09/2012

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

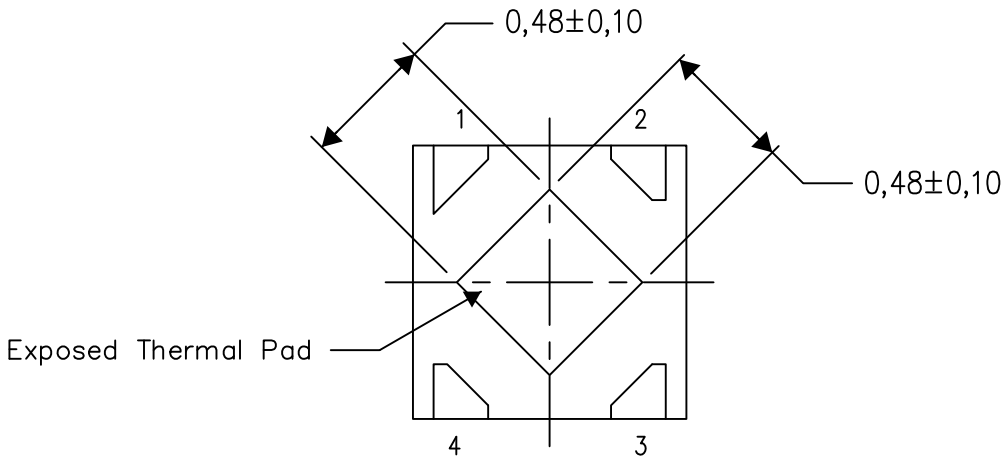
DQN (S–PX2SON–N4) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



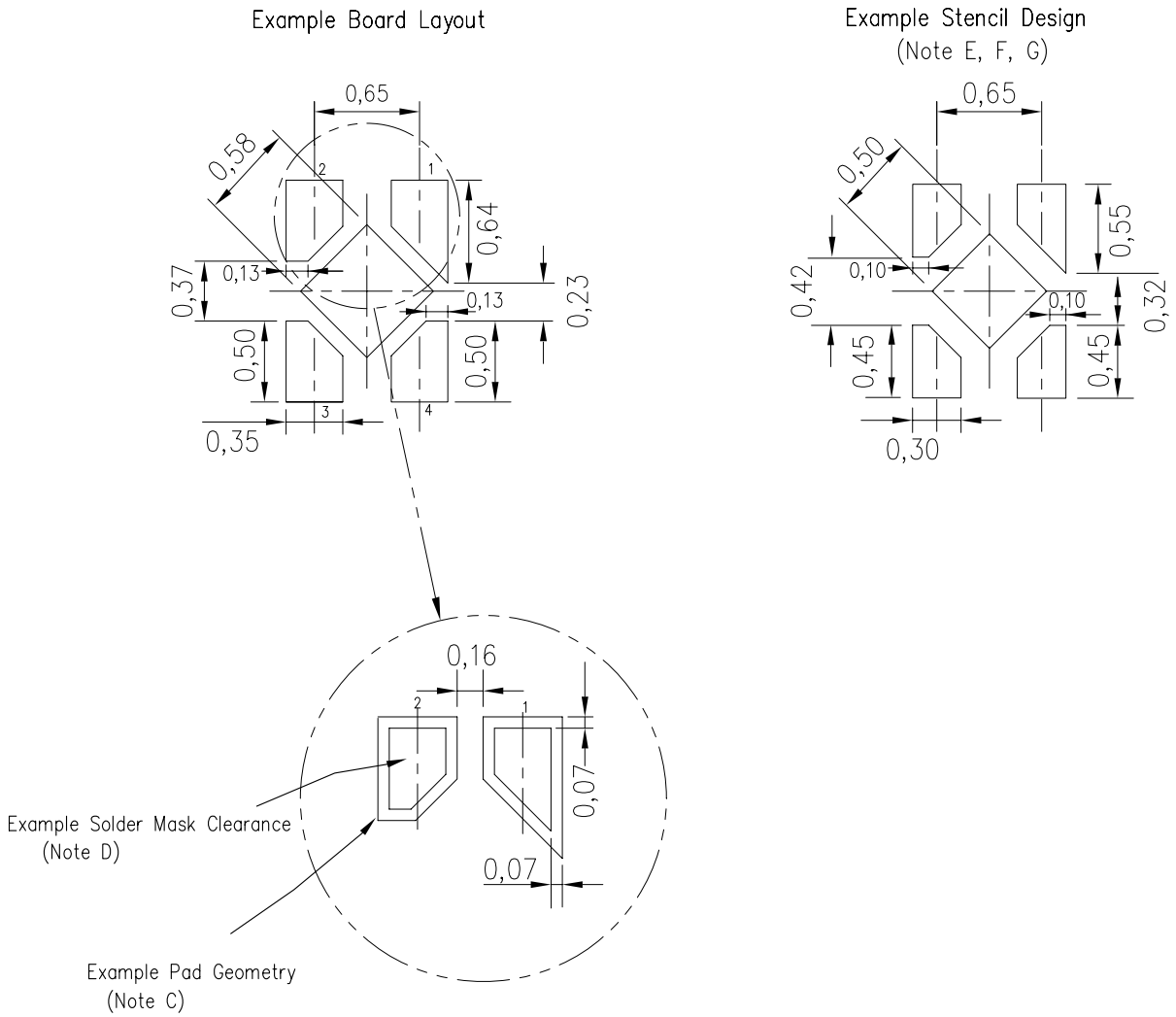
Bottom View

Exposed Thermal Pad Dimensions

4210393–3/F 05/15

NOTE: All linear dimensions are in millimeters

DQN (S–PX2SON–N4) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

IMPORTANT NOTICE

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