TPA2011D1 3.2-W Mono Filter-Free Class-D Audio Power Amplifier With Auto-Recovering Short-Circuit Protection

1 Features

- Powerful Mono Class-D Amplifier
  - 3.24 W (4 Ω, 5 V, 10% THDN)
  - 2.57 W (4 Ω, 5 V, 1% THDN)
  - 1.80 W (8 Ω, 5 V, 10% THDN)
  - 1.46 W (8 Ω, 5 V, 1% THDN)
- Integrated Feedback Resistor of 300 kΩ
- Integrated Image Reject Filter for DAC Noise Reduction
- Low Output Noise of 20 µV
- Low Quiescent Current of 1.5 mA
- Auto Recovering Short-Circuit Protection
- Thermal Overload Protection
- 9-Ball, 1.21mm x 1.16 mm 0.4 mm Pitch DSBGA

2 Applications

- Wireless or Cellular Handsets and PDAs
- Portable Navigation Devices
- General Portable Audio Devices

3 Description

The TPA2011D1 is a 3.2-W high efficiency filter-free class-D audio power amplifier (class-D amp) in a 1.21 mm × 1.16 mm wafer chip scale package (DSBGA) that requires only three external components.

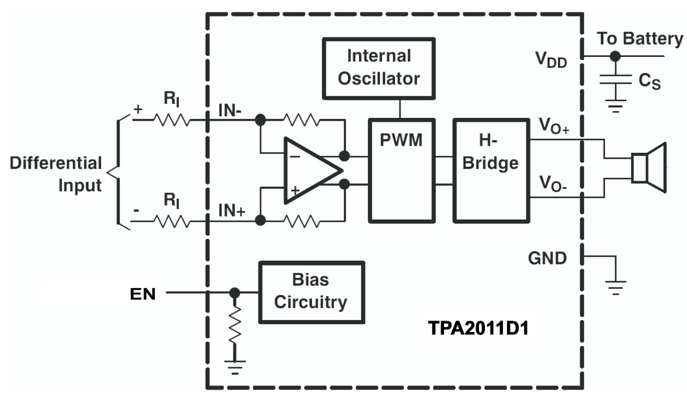
Features like 95% efficiency, 86-dB PSRR, 1.5 mA quiescent current and improved RF immunity make the TPA2011D1 class-D amp ideal for cellular handsets. A fast start-up time of 4 ms with no audible turn-on pop makes the TPA2011D1 ideal for PDA and smart-phone applications. The TPA2011D1 allows independent gain while summing signals from separate sources, and has a low 20 µV noise floor.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPA2011D1	DSBGA (9)	1.60 mm x 1.21 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Diagram



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (May 2010) to Revision B **Page**

- Added *Pin Configuration and Functions* section, *Handling Rating* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section 1

Changes from Original (December 2009) to Revision A **Page**

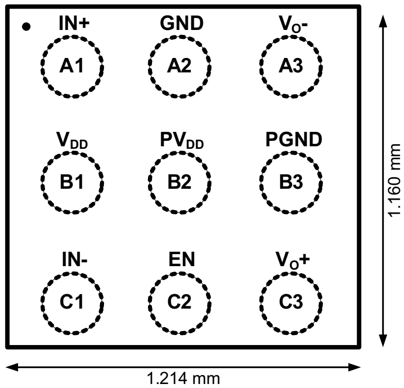
- Changed the Package Dimensions table. D was Max = 1244μm, Min = 1184μm. E was Max = 1190μm, Min = 1130μm 1

5 Device Comparison Table

DEVICE NUMBER	SPEAKER CHANNELS	SPEAKER AMP TYPE	OUTPUT POWER (W)	PSRR (dB)
TPA2011D1	Mono	Class D	3.2	86
TPA2005D1	Mono	Class D	1.4	75
TPA2010D1	Mono	Class D	2.5	75

6 Pin Configuration and Functions

YFF Package
9-Pin DSBGA
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
EN	C2	I	Shutdown terminal. When terminal is low the device is put into Shutdown mode.
GND	A2	I	Analog ground terminal. Must be connected to same potential as PGND using a direct connection to a single point ground.
IN–	C1	I	Negative differential audio input
IN+	A1	I	Positive differential audio input
PGND	B3	I	High-current Analog ground terminal. Must be connected to same potential as GND using a direct connection to a single point ground.
PV_{DD}	B2	I	High-current Power supply terminal. Must be connected to same power supply as V_{DD} using a direct connection. Voltage must be within values listed in Recommended Operating Conditions table.
V_{DD}	B1	I	Power supply terminal. Must be connected to same power supply as PV_{DD} using a direct connection. Voltage must be within values listed in Recommended Operating Conditions table.
V_{O-}	A3	O	Negative BTL audio output
V_{O+}	C3	O	Positive BTL audio output

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range, T_A = 25°C (unless otherwise noted)[(1)]

			MIN	MAX	UNIT
V_{DD}, PV_{DD}	Supply voltage	In active mode	–0.3	6	V
		In shutdown mode	–0.3	6	V
V_I	Input voltage	EN, IN+, IN–	–0.3	V_{DD} + 0.3	V
R_L	Minimum load resistance		3.2		Ω
	Output continuous total power dissipation		See *Dissipation Ratings*		
T_A	Operating free-air temperature		–40	85	°C
T_J	Operating junction temperature		–40	150	°C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds			260	°C
T_{stg}	Storage temperature		–65	85	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

			MIN	MAX	UNIT
V_{DD}	Class-D supply voltage		2.5	5.5	V
V_{IH}	High-level input voltage	EN	1.3		V
V_{IL}	Low-level input voltage	EN		0.35	V
R_I	Input resistor	Gain ≤ 20 V/V (26 dB)	15		kΩ
V_{IC}	Common mode input voltage range	V_{DD} = 2.5V, 5.5V, CMRR ≥ 49 dB	0.75	V_{DD}-1.1	V
T_A	Operating free-air temperature		–40	85	°C

7.4 Thermal Information

THERMAL METRIC[1]		TPA2011D1 YFF (DSBGA) 9 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	107	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	18.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	18	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\lvert V_{OS}\rvert$	Output offset voltage (measured differentially)	V_I = 0 V, A_V = 2 V/V, V_{DD} = 2.5 V to 5.5 V		1	5	mV
$\lvert I_{IH}\rvert$	High-level input current	V_{DD} = 5.5 V, V_{EN} = 5.5 V			50	μA
$\lvert I_{IL}\rvert$	Low-level input current	V_{DD} = 5.5 V, V_{EN} = 0 V			1	μA
$I_{(Q)}$	Quiescent current	V_{DD} = 5.5 V, no load		1.8	2.5	mA
		V_{DD} = 3.6 V, no load		1.5	2.3	
		V_{DD} = 2.5 V, no load		1.3	2.1	
$I_{(SD)}$	Shutdown current	V_{EN} = 0.35 V, V_{DD} = 2.5 V to 5.5 V		0.1	2	μA
$R_{O, SD}$	Output impedance in shutdown mode	V_{EN} = 0.35 V		2		kΩ
$f_{(SW)}$	Switching frequency	V_{DD} = 2.5 V to 5.5 V	250	300	350	kHz
A_V	Gain	V_{DD} = 2.5 V to 5.5 V, R_I in kΩ	$285/R_I$	$300/R_I$	$315/R_I$	V/V
R_{EN}	Resistance from EN to GND			300		kΩ

7.6 Operating Characteristics

V_{DD} = 3.6 V, T_A = 25°C, A_V = 2 V/V, R_L = 8 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
P_O	Output power	THD + N = 10%, f = 1 kHz, R_L = 4 Ω	V_{DD} = 5 V		3.24		W
			V_{DD} = 3.6 V		1.62		
			V_{DD} = 2.5 V		0.70		
		THD + N = 1%, f = 1 kHz, R_L = 4 Ω	V_{DD} = 5 V		2.57		W
			V_{DD} = 3.6 V		1.32		
			V_{DD} = 2.5 V		0.57		
		THD + N = 10%, f = 1 kHz, R_L = 8 Ω	V_{DD} = 5 V		1.80		W
			V_{DD} = 3.6 V		0.91		
			V_{DD} = 2.5 V		0.42		
		THD + N = 1%, f = 1 kHz, R_L = 8 Ω	V_{DD} = 5 V		1.46		W
			V_{DD} = 3.6 V		0.74		
			V_{DD} = 2.5 V		0.33		
V_n	Noise output voltage	V_{DD} = 3.6 V, Inputs AC grounded with C_I = 2μF, f = 20 Hz to 20 kHz	A-weighting		20		μV_{RMS}
			No weighting		25		
THD+N	Total harmonic distortion plus noise	V_{DD} = 5.0 V, P_O = 1.0 W, f = 1 kHz, R_L = 8 Ω			0.11%		
		V_{DD} = 3.6 V, P_O = 0.5 W, f = 1 kHz, R_L = 8 Ω			0.05%		
		V_{DD} = 2.5 V, P_O = 0.2 W, f = 1 kHz, R_L = 8 Ω			0.05%		
		V_{DD} = 5.0 V, P_O = 2.0 W, f = 1 kHz, R_L = 4 Ω			0.23%		
		V_{DD} = 3.6 V, P_O = 1.0 W, f = 1 kHz, R_L = 4 Ω			0.07%		
		V_{DD} = 2.5 V, P_O = 0.4 W, f = 1 kHz, R_L = 4 Ω			0.06%		
PSRR	AC power supply rejection ratio	V_{DD} = 3.6 V, Inputs AC grounded with C_I = 2 μF, 200 mV_{pp} ripple, f = 217 Hz			86		dB
CMRR	Common mode rejection ratio	V_{DD} = 3.6 V, V_{IC} = 1 V_{PP}, f = 217 Hz			79		dB
T_{SU}	Startup time from shutdown	V_{DD} = 3.6 V			4		ms
I_{OC}	Overcurrent protection threshold	V_{DD} = 3.6 V, V_{O+} shorted to VDD			2		A
		V_{DD} = 3.6 V, V_{O-} shorted to VDD			2		
		V_{DD} = 3.6 V, V_{O+} shorted to GND			2		
		V_{DD} = 3.6 V, V_{O-} shorted to GND			2		
		V_{DD} = 3.6 V, V_{O+} shorted to V_{O-}			2		
T_{SD}	Time for which output is disabled after a short-circuit event, after which auto-recovery trials are continuously made	V_{DD} = 2.5 V to 5.5 V			100		ms

7.7 Dissipation Ratings

PACKAGE	DERATING FACTOR(1)	T_A < 25°C	T_A = 70°C	T_A = 85°C
YFF (DSBGA)	4.2 mW/°C	525 mW	336 mW	273 mW

(1) Derating factor measure with high K board.

7.8 Typical Characteristics

V_{DD} = 3.6 V, C_I = 0.1 µF, C_{S1} = 0.1 µF, C_{S2} = 10 µF, T_A = 25°C, R_L = 8 Ω (unless otherwise noted)

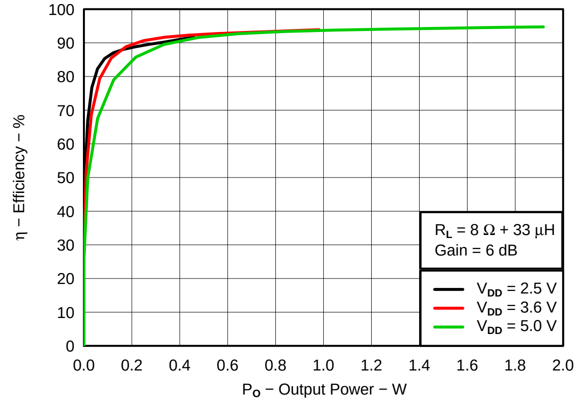


Figure 1. Efficiency vs Output Power

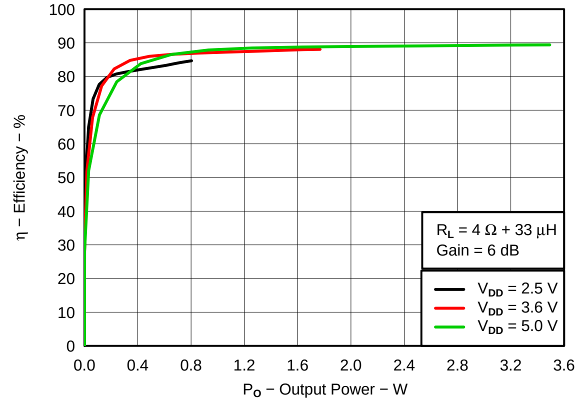


Figure 2. Efficiency vs Output Power

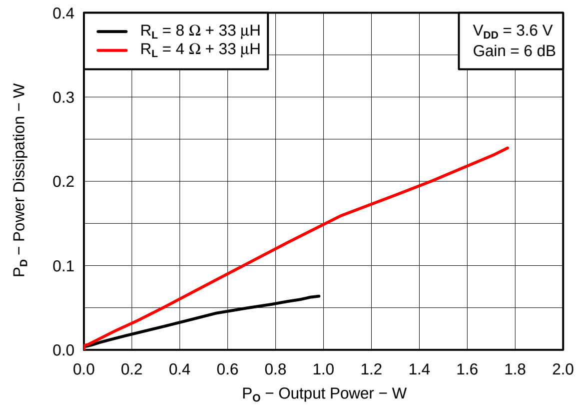


Figure 3. Power Dissipation vs Output Power

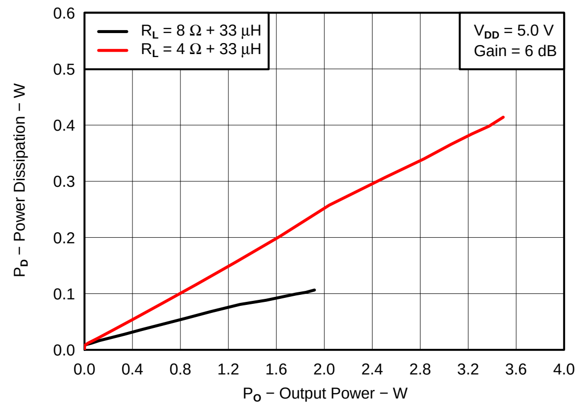


Figure 4. Power Dissipation vs Output Power

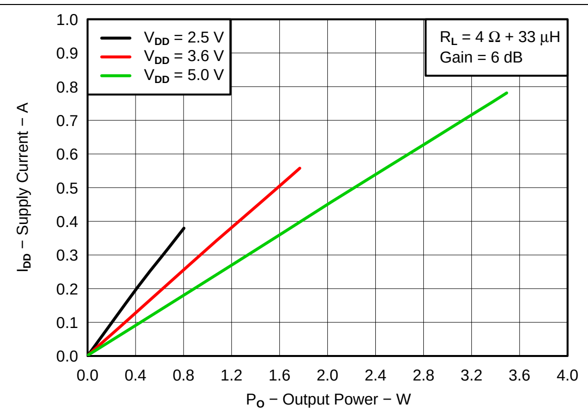


Figure 5. Supply Current vs Output Power

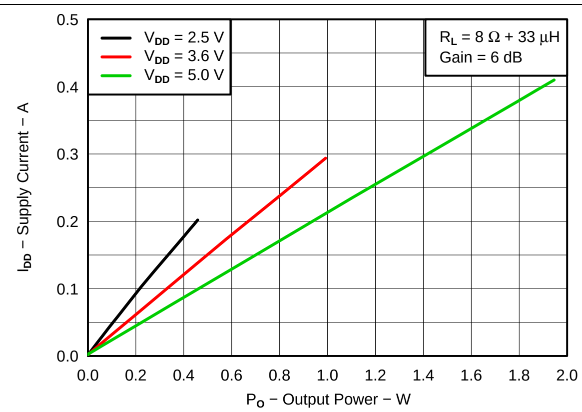


Figure 6. Supply Current vs Output Power

Typical Characteristics (continued)

V_{DD} = 3.6 V, C_I = 0.1 µF, C_{S1} = 0.1 µF, C_{S2} = 10 µF, T_A = 25°C, R_L = 8 Ω (unless otherwise noted)

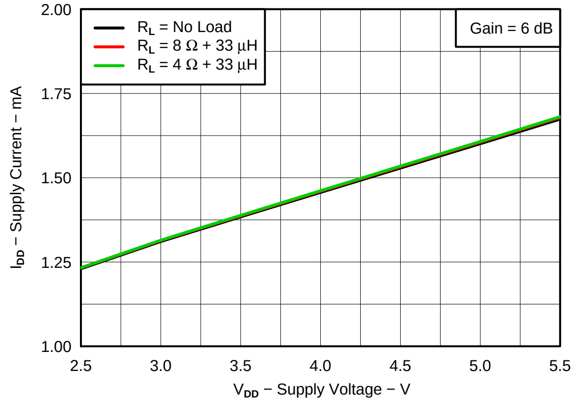


Figure 7. Supply Current vs Supply Voltage

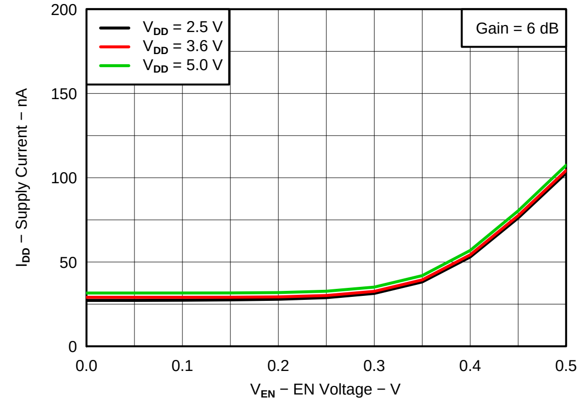


Figure 8. Supply Current vs EN Voltage

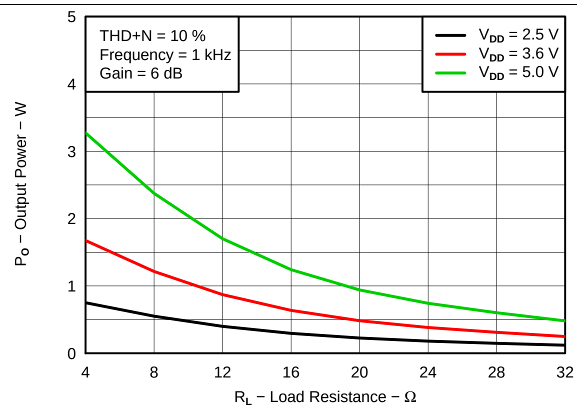


Figure 9. Output Power vs Load Resistance

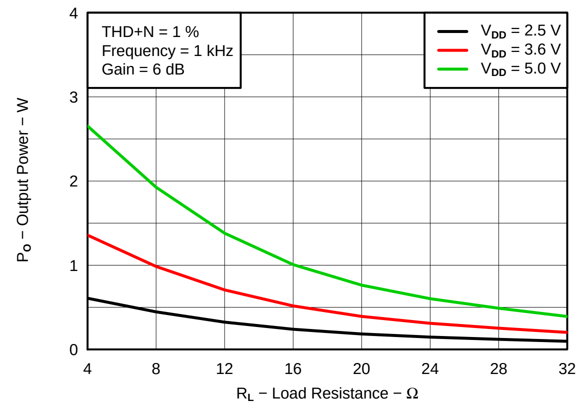


Figure 10. Output Power vs Load Resistance

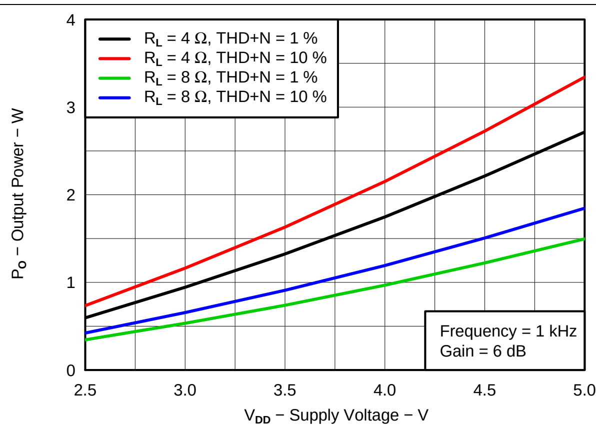


Figure 11. Output Power vs Supply Resistance

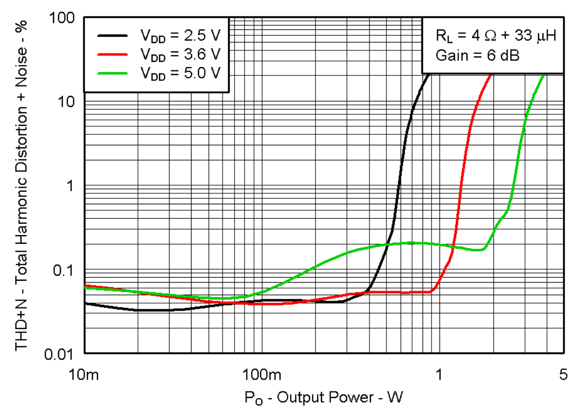


Figure 12. THD + Noise vs Output Power

Typical Characteristics (continued)

V_{DD} = 3.6 V, C_I = 0.1 μF, C_{S1} = 0.1 μF, C_{S2} = 10 μF, T_A = 25°C, R_L = 8 Ω (unless otherwise noted)

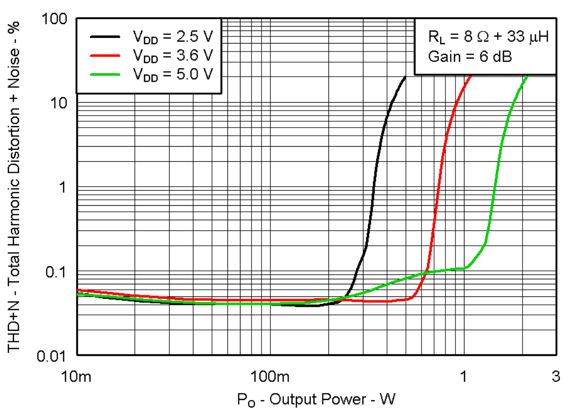


Figure 13. THD + Noise vs Output Power

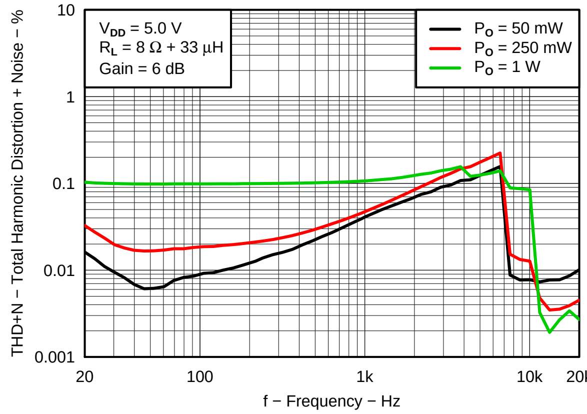


Figure 14. THD + Noise vs Frequency

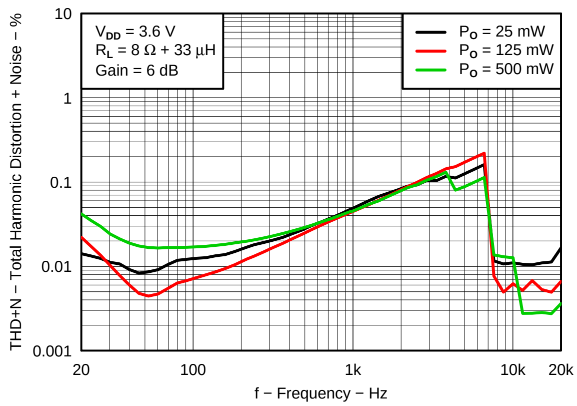


Figure 15. THD + Noise vs Frequency

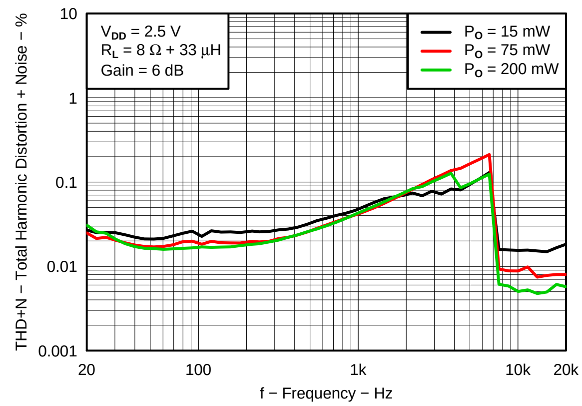


Figure 16. THD + Noise vs Frequency

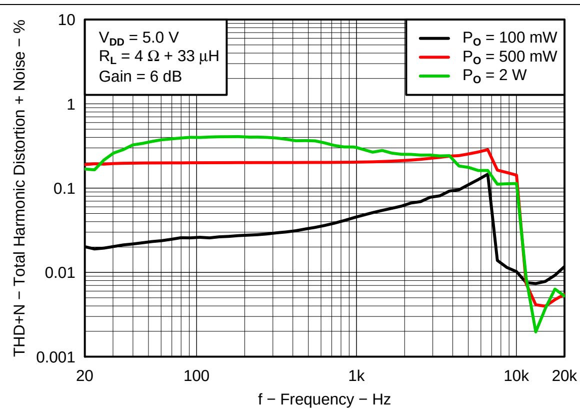


Figure 17. THD + Noise vs Frequency

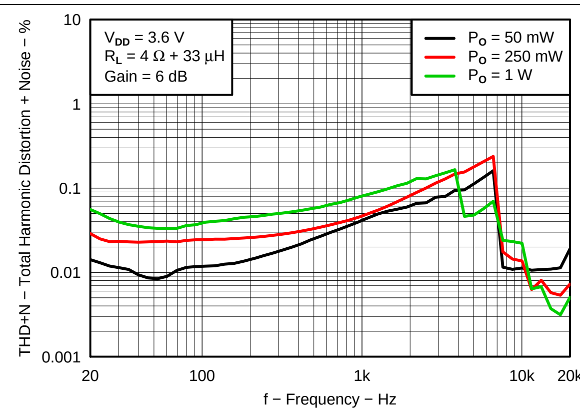


Figure 18. THD + Noise vs Frequency

Typical Characteristics (continued)

V_{DD} = 3.6 V, C_I = 0.1 µF, C_{S1} = 0.1 µF, C_{S2} = 10 µF, T_A = 25°C, R_L = 8 Ω (unless otherwise noted)

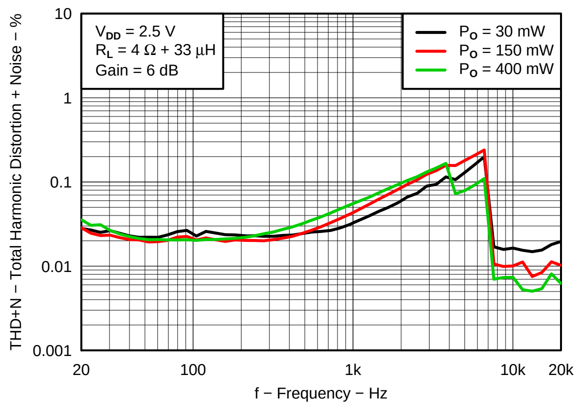


Figure 19. THD + Noise vs Frequency

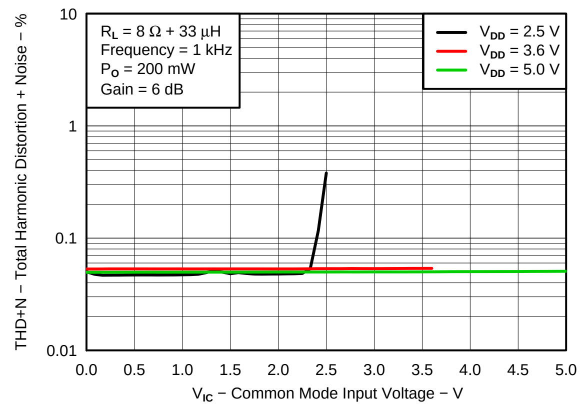


Figure 20. THD + Noise vs Common Mode Input Voltage

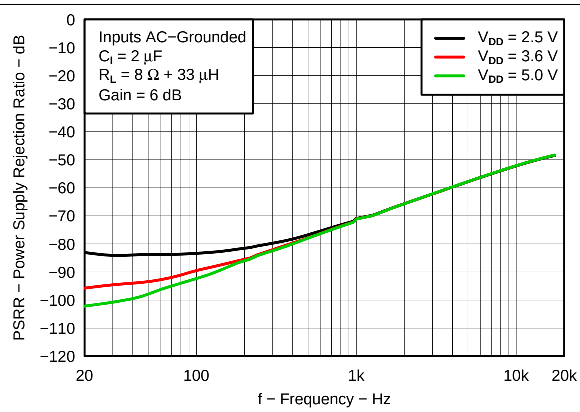


Figure 21. Power Supply Rejection Ratio vs Frequency

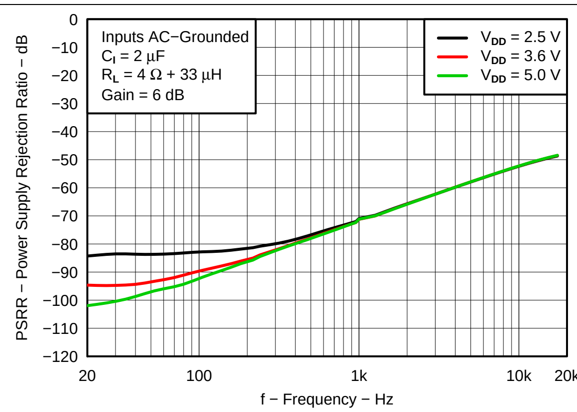


Figure 22. Power Supply Rejection Ratio vs Frequency

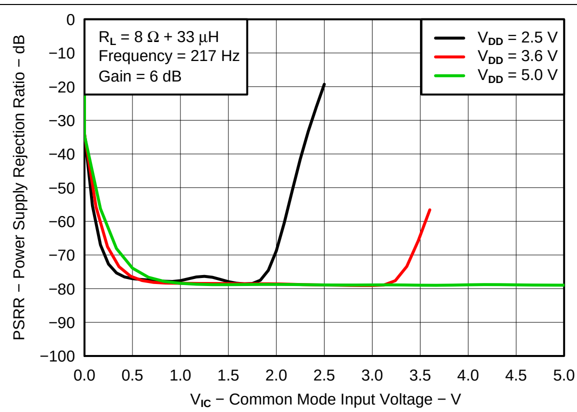


Figure 23. Power Supply Rejection Ratio vs Common Mode Input Voltage

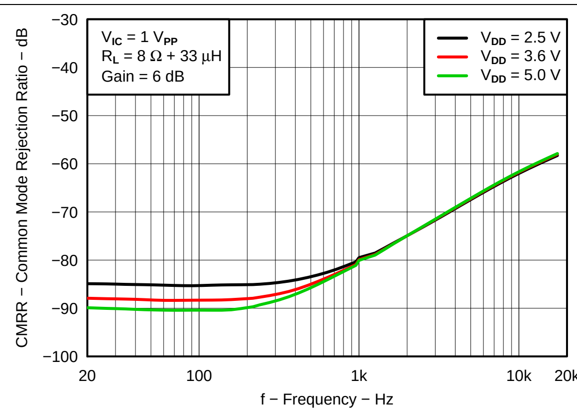


Figure 24. Common Mode Rejection Ratio vs Frequency

Typical Characteristics (continued)

V_{DD} = 3.6 V, C_I = 0.1 µF, C_{S1} = 0.1 µF, C_{S2} = 10 µF, T_A = 25°C, R_L = 8 Ω (unless otherwise noted)

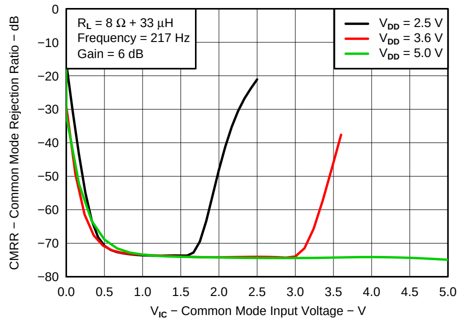


Figure 25. Common Mode Rejection Ratio vs Common Mode Input Voltage

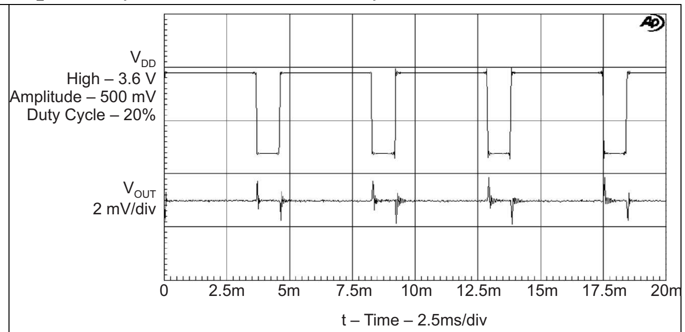


Figure 26. GSM Power Supply Rejection vs Time

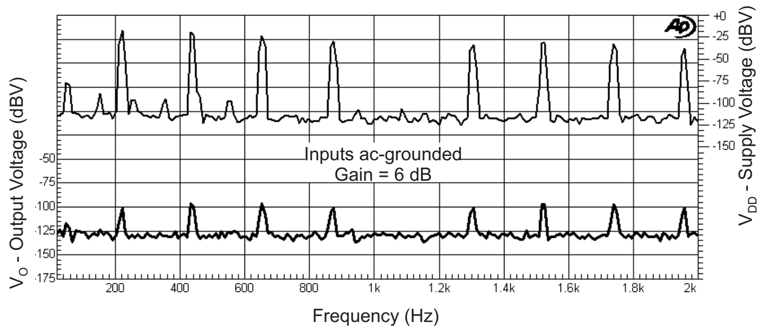
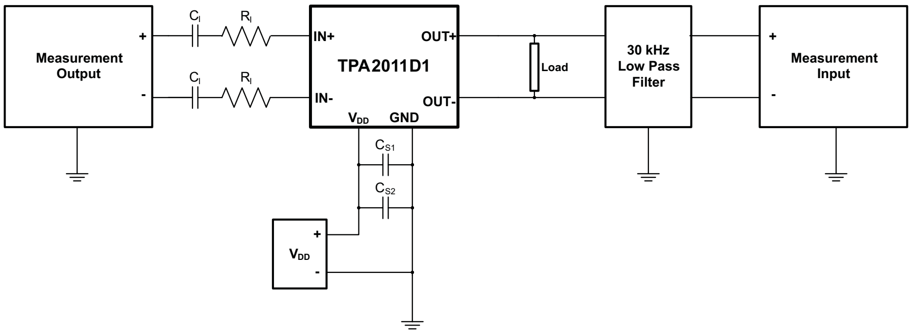


Figure 27. GSM Power Supply Rejection vs Frequency

8 Parameter Measurement Information

All parameters are measured according to the conditions described in the *Specifications* section.



(1) Input resistor R_I = 150kΩ gives a gain of 6 dB which is used for all the graphs

(2) C_I was shorted for any common-mode input voltage measurement. All other measurements were taken with C_I = 0.1-μF (unless otherwise noted).

(3) C_{S1} = 0.1μF is placed very close to the device. The optional C_{S2} = 10μF is used for datasheet graphs.

(4) The 30-kHz low-pass filter is required even if the analyzer has an internal low-pass filter. An RC low-pass filter (1kΩ, 4700pF) is used on each output for the data sheet graphs.

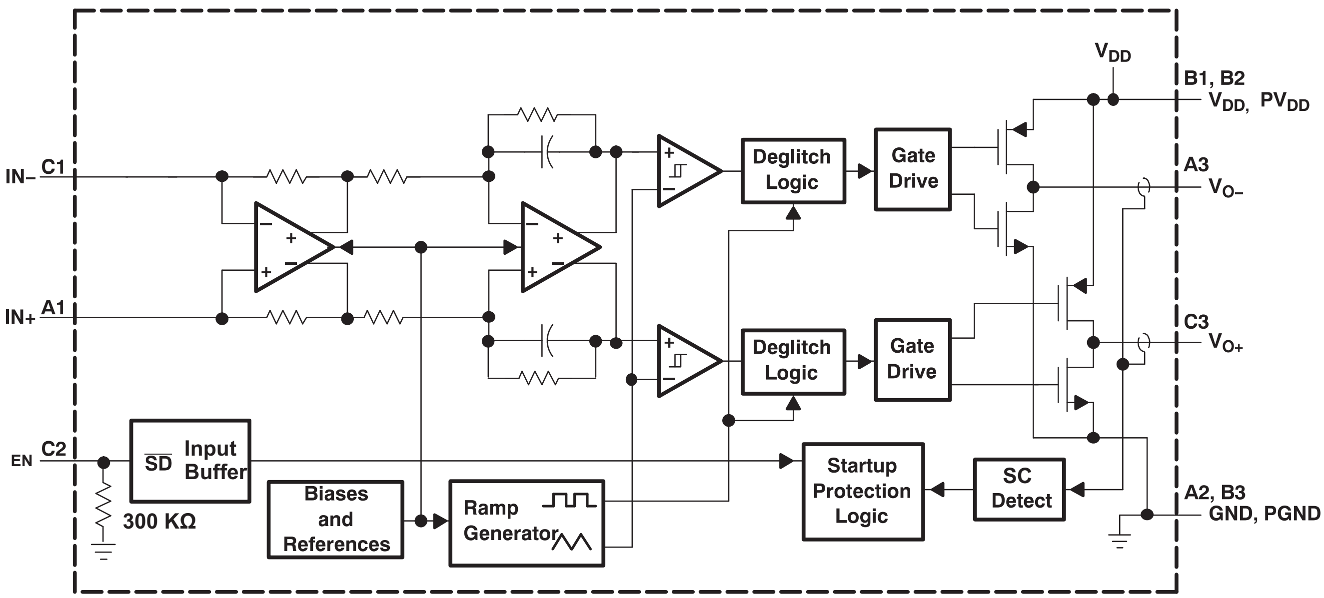
Figure 28. Test Setup for Typical Application Graphs

9 Detailed Description

9.1 Overview

The TPA2011D1 is a high-efficiency filter-free Class-D audio amplifier capable of delivering up to 3.2W into 4-Ω load with 5-V power supply. The fully-differential design of this amplifier avoids the usage of bypass capacitors and the improved CMRR eliminates the usage of input-coupling capacitors. This makes the device size a perfect choice for small, portable applications as only three external components are required. The advanced modulation used in the TPA2011D1 PWM output stage eliminates the need for an output filter.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Fully Differential Amplifier

The TPA2011D1 is a fully differential amplifier with differential inputs and outputs. The fully differential amplifier consists of a differential amplifier and a common-mode amplifier. The differential amplifier ensures that the amplifier outputs a differential voltage on the output that is equal to the differential input times the gain. The common-mode feedback ensures that the common-mode voltage at the output is biased around VDD/2 regardless of the common-mode voltage at the input. The fully differential TPA2011D1 can still be used with a single-ended input; however, the TPA2011D1 should be used with differential inputs when in a noisy environment, like a wireless handset, to ensure maximum noise rejection.

9.3.1.1 Advantages of Fully Differential Amplifiers

- Input-coupling Capacitors Not Required
  – The fully differential amplifier allows the inputs to be biased at voltage other than mid-supply. For example, if a codec has a midsupply lower than the midsupply of the TPA2011D1, the common-mode feedback circuit will adjust, and the TPA2011D1 outputs will still be biased at midsupply of the TPA2011D1. The inputs of the TPA2011D1 can be biased from 0.5 V to VDD –0.8 V. If the inputs are biased outside of that range, input-coupling capacitors are required.
- Midsupply Bypass Capacitor, C(BYPASS), Not Required
  – The fully differential amplifier does not require a bypass capacitor. This is because any shift in the midsupply affects both positive and negative channels equally and cancels at the differential output.
- Better RF-Immunity
  – GSM handsets save power by turning on and shutting off the RF transmitter at a rate of 217 Hz. The

Feature Description (continued)

transmitted signal is picked-up on input and output traces. The fully differential amplifier cancels the signal much better than the typical audio amplifier.

9.3.2 Eliminating the Output Filter With the TPA2011D1

This section focuses on why the user can eliminate the output filter with the TPA2011D1.

9.3.2.1 Effect on Audio

The class-D amplifier outputs a pulse-width modulated (PWM) square wave, which is the sum of the switching waveform and the amplified input audio signal. The human ear acts as a band-pass filter such that only the frequencies between approximately 20 Hz and 20 kHz are passed. The switching frequency components are much greater than 20 kHz, so the only signal heard is the amplified input audio signal.

9.3.2.2 When to Use an Output Filter

Design the TPA2011D1 without an Inductor / Capacitor (LC) output filter if the traces from the amplifier to the speaker are short. Wireless handsets and PDAs are great applications for this class-D amplifier to be used without an output filter.

The TPA2011D1 does not require an LC output filter for short speaker connections (approximately 100 mm long or less). A ferrite bead can often be used in the design if failing radiated emissions testing without an LC filter; and, the frequency-sensitive circuit is greater than 1 MHz. If choosing a ferrite bead, choose one with high impedance at high frequencies, but very low impedance at low frequencies. The selection must also take into account the currents flowing through the ferrite bead. Ferrites can begin to loose effectiveness at much lower than rated current values. See the TPA2011D1 EVM User's Guide for components used successfully by TI.

Figure 29 shows a typical ferrite-bead output filter.

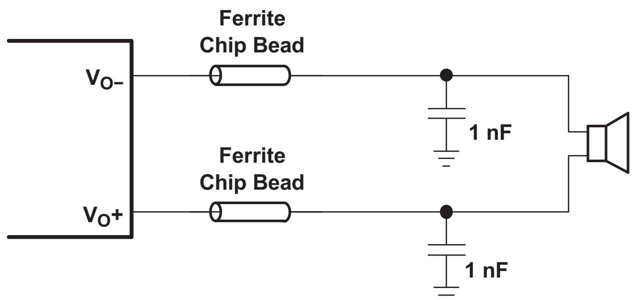


Figure 29. Typical Ferrite Chip Bead Filter

9.3.3 Short Circuit Auto-Recovery

When a short-circuit event occurs, the TPA2011D1 goes to shutdown mode and activates the integrated auto-recovery process whose aim is to return the device to normal operation once the short-circuit is removed. This process repeatedly examines (once every 100ms) whether the short-circuit condition persists, and returns the device to normal operation immediately after the short-circuit condition is removed. This feature helps protect the device from large currents and maintain a good long-term reliability.

9.3.4 Integrated Image Reject Filter for DAC Noise Rejection

In applications which use a DAC to drive Class-D amplifiers, out-of-band noise energy present at the DAC's image frequencies fold back into the audio-band at the output of the Class-D amplifier. An external low-pass filter is often placed between the DAC and the Class-D amplifier in order to attenuate this noise.

The TPA2011D1 has an integrated Image Reject Filter with a low-pass cutoff frequency of 130 kHz, which significantly attenuates this noise. Depending on the system noise specification, the integrated Image Reject Filter may help eliminate external filtering, thereby saving board space and component cost.

9.4 Device Functional Modes

9.4.1 Summing Input Signals With the TPA2011D1

Most wireless phones or PDAs need to sum signals at the audio power amplifier or just have two signal sources that need separate gain. The TPA2011D1 makes it easy to sum signals or use separate signal sources with different gains. Many phones now use the same speaker for the earpiece and ringer, where the wireless phone would require a much lower gain for the phone earpiece than for the ringer. PDAs and phones that have stereo headphones require summing of the right and left channels to output the stereo signal to the mono speaker.

9.4.1.1 Summing Two Differential Input Signals

Two extra resistors are needed for summing differential signals (a total of 5 components). The gain for each input source can be set independently (see Equation 1 and Equation 2, and Figure 30).

$$\text{Gain 1} = \frac{V_O}{V_{I1}} = \frac{2 \text{ x } 150 \text{ k}\Omega}{R_{I1}} \left(\frac{V}{V}\right) \quad (1)$$

$$\text{Gain 2} = \frac{V_O}{V_{I2}} = \frac{2 \text{ x } 150 \text{ k}\Omega}{R_{I2}} \left(\frac{V}{V}\right) \quad (2)$$

If summing left and right inputs with a gain of 1 V/V, use $R_{I1} = R_{I2} = 300\ k\Omega$.

If summing a ring tone and a phone signal, set the ring-tone gain to Gain 2 = 2 V/V, and the phone gain to gain 1 = 0.1 V/V. The resistor values would be:

$R_{I1} = 3\ M\Omega$, and = $R_{I2} = 150\ k\Omega$.

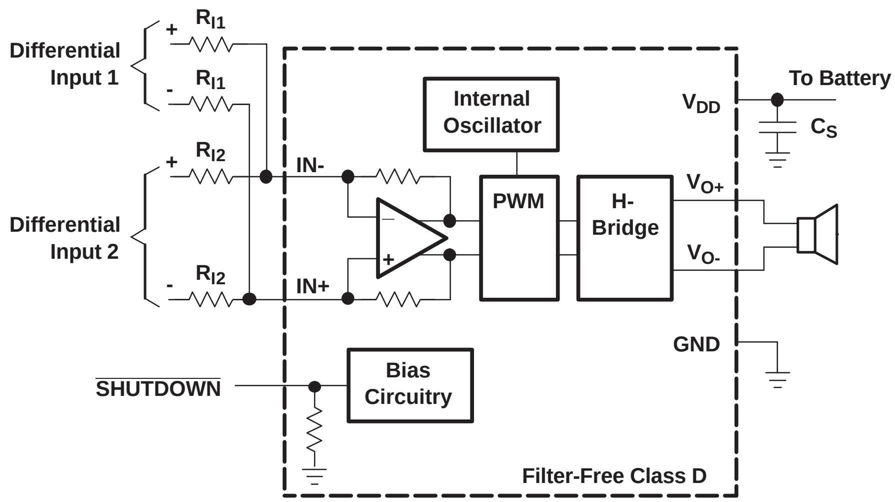


Figure 30. Application Schematic With TPA2011D1 Summing Two Differential Inputs

9.4.1.2 Summing a Differential Input Signal and a Single-Ended Input Signal

Figure 31 shows how to sum a differential input signal and a single-ended input signal. Ground noise can couple in through IN+ with this method. It is better to use differential inputs. The corner frequency of the single-ended input is set by C_{I2}, shown in Equation 5. To assure that each input is balanced, the single-ended input must be driven by a low-impedance source even if the input is not in use

$$\text{Gain 1} = \frac{V_O}{V_{I1}} = \frac{2 \text{ x } 150 \text{ k}\Omega}{R_{I1}} \left(\frac{V}{V}\right) \quad (3)$$

$$\text{Gain 2} = \frac{V_O}{V_{I2}} = \frac{2 \text{ x } 150 \text{ k}\Omega}{R_{I2}} \left(\frac{V}{V}\right) \quad (4)$$

Device Functional Modes (continued)

$$C_{I2} = \frac{1}{\left(2\pi\ R_{I2}\ f_{c2}\right)} \quad (5)$$

If summing a ring tone and a phone signal, the phone signal should use a differential input signal while the ring tone might be limited to a single-ended signal. Phone gain is set at gain 1 = 0.1 V/V, and the ring-tone gain is set to gain 2 = 2 V/V, the resistor values would be…

R_{I1} = 3 MΩ, and = R_{I2} = 150 kΩ.

The high pass corner frequency of the single-ended input is set by C_{I2}. If the desired corner frequency is less than 20 Hz...

$$C_{I2} > \frac{1}{\left(2\pi\ 150\,k\Omega\ 20\,Hz\right)} \quad (6)$$

$$C_{I2} > 53\ nF \quad (7)$$

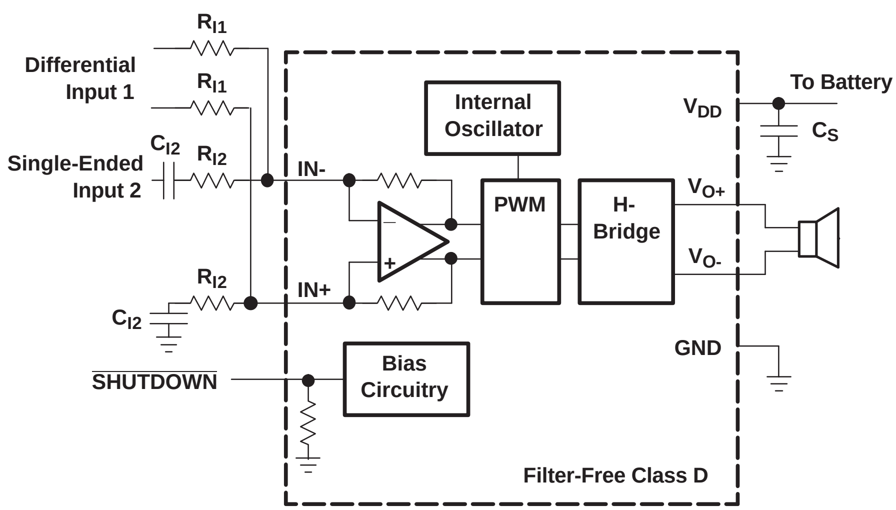


Figure 31. Application Schematic With TPA2011D1 Summing Differential Input and Single-Ended Input Signals

9.4.1.3 Summing Two Single-Ended Input Signals

Four resistors and three capacitors are needed for summing single-ended input signals. The gain and corner frequencies (f_{c1} and f_{c2}) for each input source can be set independently (see Equation 8 through Equation 11, and Figure 32). Resistor, R_P, and capacitor, C_P, are needed on the IN+ terminal to match the impedance on the IN– terminal. The single-ended inputs must be driven by low impedance sources even if one of the inputs is not outputting an ac signal.

$$\text{Gain 1} = \frac{V_O}{V_{I1}} = \frac{2 \times 150\ k\Omega}{R_{I1}} \quad \left(\frac{V}{V}\right) \quad (8)$$

$$\text{Gain 2} = \frac{V_O}{V_{I2}} = \frac{2 \times 150\ k\Omega}{R_{I2}} \quad \left(\frac{V}{V}\right) \quad (9)$$

$$C_{I1} = \frac{1}{\left(2\pi\ R_{I1}\ f_{c1}\right)} \quad (10)$$

$$C_{I2} = \frac{1}{\left(2\pi\ R_{I2}\ f_{c2}\right)} \quad (11)$$

$$C_P = C_{I1} + C_{I2} \quad (12)$$

Device Functional Modes (continued)

$$R_P = \frac{R_{I1} \times R_{I2}}{\left(R_{I1} + R_{I2}\right)} \quad (13)$$

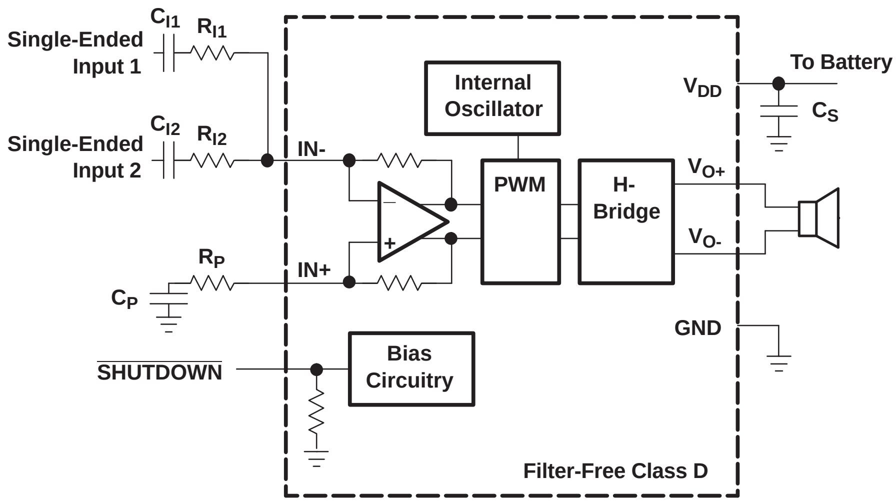


Figure 32. Application Schematic With TPA2011D1 Summing Two Single-Ended Inputs

9.4.2 Shutdown Mode

The TPA2011D1 can be put in shutdown mode when asserting SHUTDOWN pin to a logic LOW. While in shutdown mode, the device output stage is turned off and set into high impedance, making the current consumption very low. The device exits shutdown mode when a HIGH logic level is applied to SHUTDOWN pin.

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

These typical connection diagrams highlight the required external components and system level connections for proper operation of the device in several popular use cases. Each of these configurations can be realized using the Evaluation Modules (EVMs) for the device. These flexible modules allow full evaluation of the device in the most common modes of operation. Any design variation can be supported by TI through schematic and layout reviews. Visit e2e.ti.com for design assistance and join the audio amplifier discussion forum for additional information.

10.2 Typical Applications

10.2.1 TPA2011D1 with Differential Input

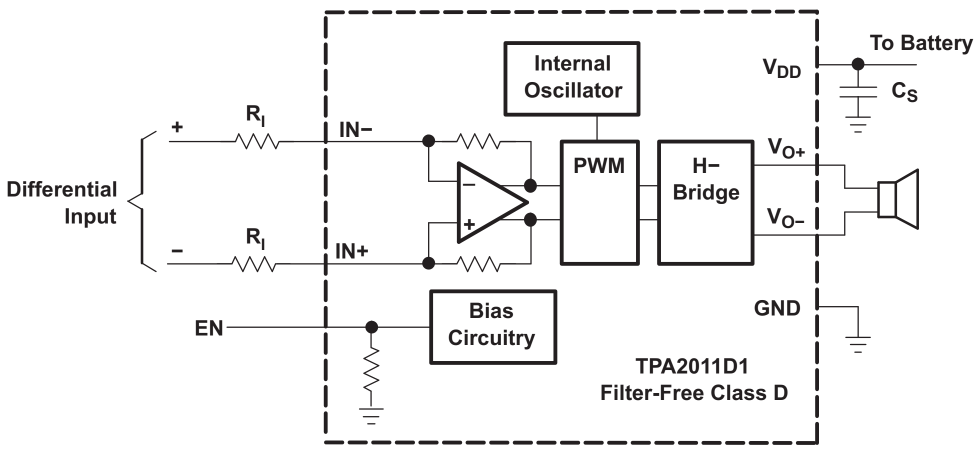


Figure 33. Typical TPA2011D1 Application Schematic with Differential Input

10.2.1.1 Design Requirements

For this design example, use the parameters listed in Table 1.

Table 1. Design Parameters

DESIGN PARAMETER	EXMAPLE VALUE
Power supply	5 V
Enable input	High > 2 V
	Low < 0.8 V
Speaker	8 Ω

10.2.1.2 Detailed Design Procedure

10.2.1.2.1 Input Resistors (R_I)

The input resistors (RI) set the gain of the amplifier according to the following equation.

$$\text{Gain} = \frac{2 \times 150\text{k}\Omega}{R_I} \left(\frac{V}{V} \right) \tag{14}$$

Resistor matching is very important in fully differential amplifiers. The balance of the output on the reference voltage depends on matched ratios of the resistors. CMRR, PSRR, and cancellation of the second harmonic distortion diminish if resistor mismatch occurs. Therefore, it is recommended to use 1% tolerance resistors or better to keep the performance optimized. Matching is more important than overall tolerance. Resistor arrays with 1% matching can be used with a tolerance greater than 1%.

Place the input resistors very close to the TPA2011D1 to limit noise injection on the high-impedance nodes.

For optimal performance, the gain should be set to 2 V/V or lower. Lower gain allows the TPA2011D1 to operate at its best, and keeps a high voltage at the input making the inputs less susceptible to noise.

10.2.1.2.2 Decoupling Capacitor (C_S)

The TPA2011D1 is a high-performance class-D audio amplifier that requires adequate power supply decoupling to ensure the efficiency is high and total harmonic distortion (THD) is low. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 1 µF, placed as close as possible to the device VDD lead works best. Placing this decoupling capacitor close to the TPA2011D1 is very important for the efficiency of the class-D amplifier, because any resistance or inductance in the trace between the device and the capacitor can cause a loss in efficiency. For filtering lower-frequency noise signals, a 10 µF or greater capacitor placed near the audio power amplifier would also help, but it is not required in most applications because of the high PSRR of this device.

10.2.1.3 Application Curves

For application curves, see the figures listed in Table 2.

Table 2. Table of Graphs

DESCRIPTION	FIGURE NUMBER
Output Power vs Supply Resistance	Figure 11
GSM Power Supply Rejection vs Time	Figure 26
GSM Power Supply Rejection vs Frequency	Figure 27

10.2.2 TPA2011D1 with Differential Input and Input Capacitors

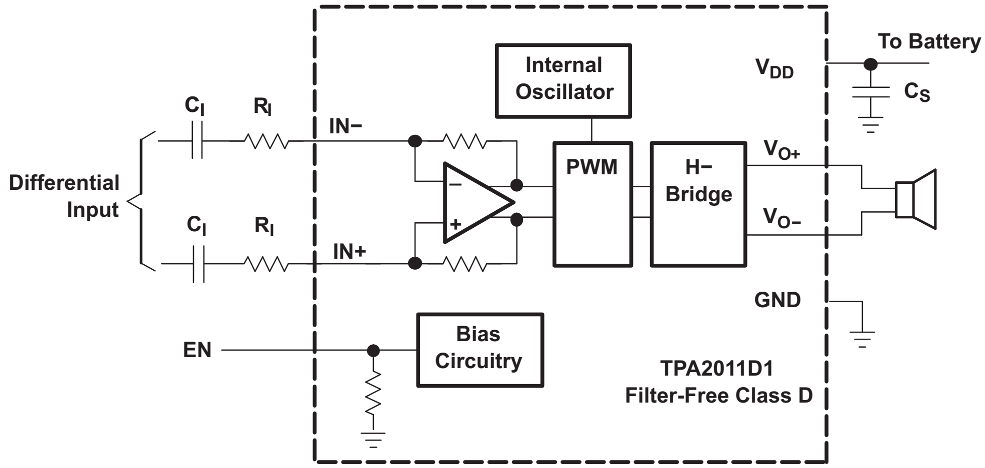


Figure 34. TPA2011D1 Application Schematic with Differential Input and Input Capacitors

10.2.2.1 Design Requirements

For this design example, use the parameters listed in Table 1.

10.2.2.2 Detailed Design Procedure

For the design procedure see *Input Resistors (R_I)* and *Decoupling Capacitor (C_S)*.

10.2.2.2.1 Input Capacitors (C_I)

The TPA2011D1 does not require input coupling capacitors if the design uses a differential source that is biased from 0.5 V to VDD –0.8 V. If the input signal is not biased within the recommended common mode input range, if needing to use the input as a high pass filter, or if using a single-ended source, input coupling capacitors are required.

The input capacitors and input resistors form a high-pass filter with the corner frequency, fC, determined in the following equation.

$$f_C = \frac{1}{2\pi R_I C_I} \tag{15}$$

The value of the input capacitor is important to consider as it directly affects the bass (low frequency) performance of the circuit. Speakers in wireless phones cannot usually respond well to low frequencies, so the corner frequency can be set to block low frequencies in this application.

The equation below is reconfigured to solve for the input coupling capacitance.

$$C_I = \frac{1}{2\pi R_I f_C} \tag{16}$$

If the corner frequency is within the audio band, the capacitors should have a tolerance of ±10% or better, because any mismatch in capacitance causes an impedance mismatch at the corner frequency and below.

For a flat low-frequency response, use large input coupling capacitors (1 μF). However, in a GSM phone the ground signal is fluctuating at 217 Hz, but the signal from the codec does not have the same 217 Hz fluctuation. The difference between the two signals is amplified, sent to the speaker, and heard as a 217 Hz hum.

10.2.2.3 Application Curves

For application curves, see the figures listed in Table 2.

10.2.3 TPA2011D1 with Single-Ended Input

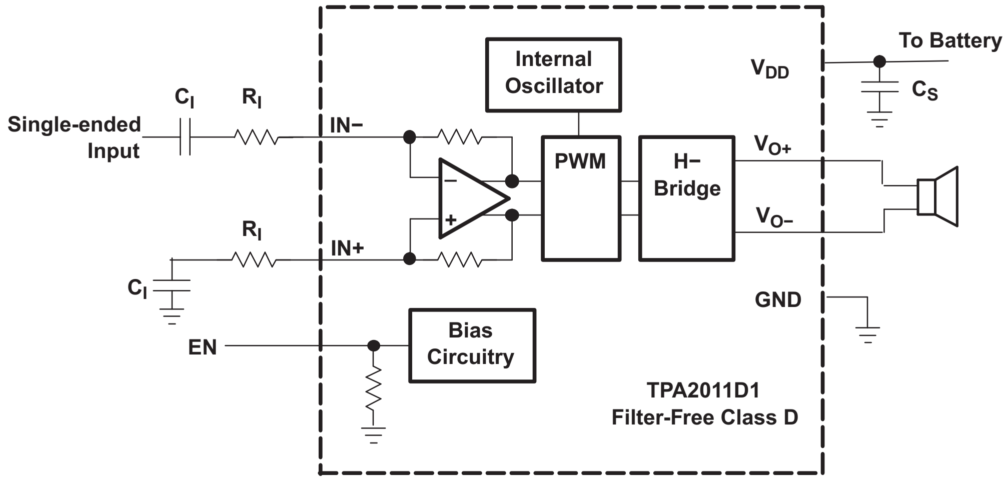


Figure 35. TPA2011D1 Application Schematic with Single-Ended Input

10.2.3.1 *Design Requirements*

For this design example, use the parameters listed in Table 1.

10.2.3.2 *Detailed Design Procedure*

For the design procedure see *Input Resistors (R_I)*, *Decoupling Capacitor (C_S)*, and *Input Capacitors (C_I)*.

10.2.3.3 *Application Curves*

For application curves, see the figures listed in Table 2.

11 Power Supply Recommendations

The TPA2011D1 is designed to operate from an input voltage supply range between 2.5-V and 5.5-V. Therefore, the output voltage range of power supply should be within this range and well regulated. The current capability of upper power should not exceed the maximum current limit of the power switch.

11.1 Power Supply Decoupling Capacitors

The TPA2011D1 requires adequate power supply decoupling to ensure a high efficiency operation with low total harmonic distortion (THD). Place a low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1 μF, within 2 mm of the VDD pin. This choice of capacitor and placement helps with higher frequency transients, spikes, or digital hash on the line. In addition to the 0.1 μF ceramic capacitor, is recommended to place a 2.2 μF to 10 μF capacitor on the VDD supply trace. This larger capacitor acts as a charge reservoir, providing energy faster than the board supply, thus helping to prevent any drop in the supply voltage.

12 Layout

12.1 Layout Guidelines

In making the pad size for the DSBGA balls, TI recommends that the layout use nonsolder mask defined (NSMD) land. With this method, the solder mask opening is made larger than the desired land area, and the opening size is defined by the copper pad width. Figure 36 shows the appropriate diameters for a DSBGA layout.

Place all the external components close to the TPA2011D1 device. Placing the decoupling capacitors as close as possible to the device is important for the efficiency of the class-D amplifier. Any resistance or inductance in the trace between the device and the capacitor can cause a loss in efficiency.

An on-pad via is not required to route the middle ball B2 (PV_{DD}) of the TPA2011D1. Just short ball B2 (PV_{DD}) to ball B1 (V_{DD}) and connect both to the supply trace as shown in Figure 37. This simplifies board routing and saves manufacturing cost.

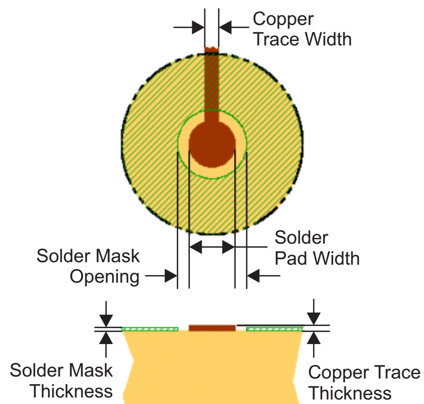


Figure 36. Land Pattern Dimensions

Table 3. Land Pattern Dimensions(1)(2)(3)(4)

SOLDER PAD DEFINITIONS	COPPER PAD	SOLDER MASK OPENING(5)	COPPER THICKNESS	STENCIL OPENING(6)(7)	STENCIL THICKNESS
Nonsolder mask defined (NSMD)	0.23 mm	0.310 mm	1 oz max (0.032 mm)	0.275 mm x 0.275 mm Sq. (rounded corners)	0.1 mm thick

(1) Circuit traces from NSMD defined PWB lands should be 75 μm to 100 μm wide in the exposed area inside the solder mask opening. Wider trace widths reduce device stand off and impact reliability.
(2) Best reliability results are achieved when the PWB laminate glass transition temperature is above the operating the range of the intended application.
(3) Recommend solder paste is Type 3 or Type 4.
(4) For a PWB using a Ni/Au surface finish, the gold thickness should be less 0.5 mm to avoid a reduction in thermal fatigue performance.
(5) Solder mask thickness should be less than 20 μm on top of the copper circuit pattern.
(6) Best solder stencil performance is achieved using laser cut stencils with electro polishing. Use of chemically etched stencils give inferior solder paste volume control.
(7) Trace routing away from DSBGA device should be balanced in X and Y directions to avoid unintentional component movement due to solder wetting forces.

12.2 Layout Example

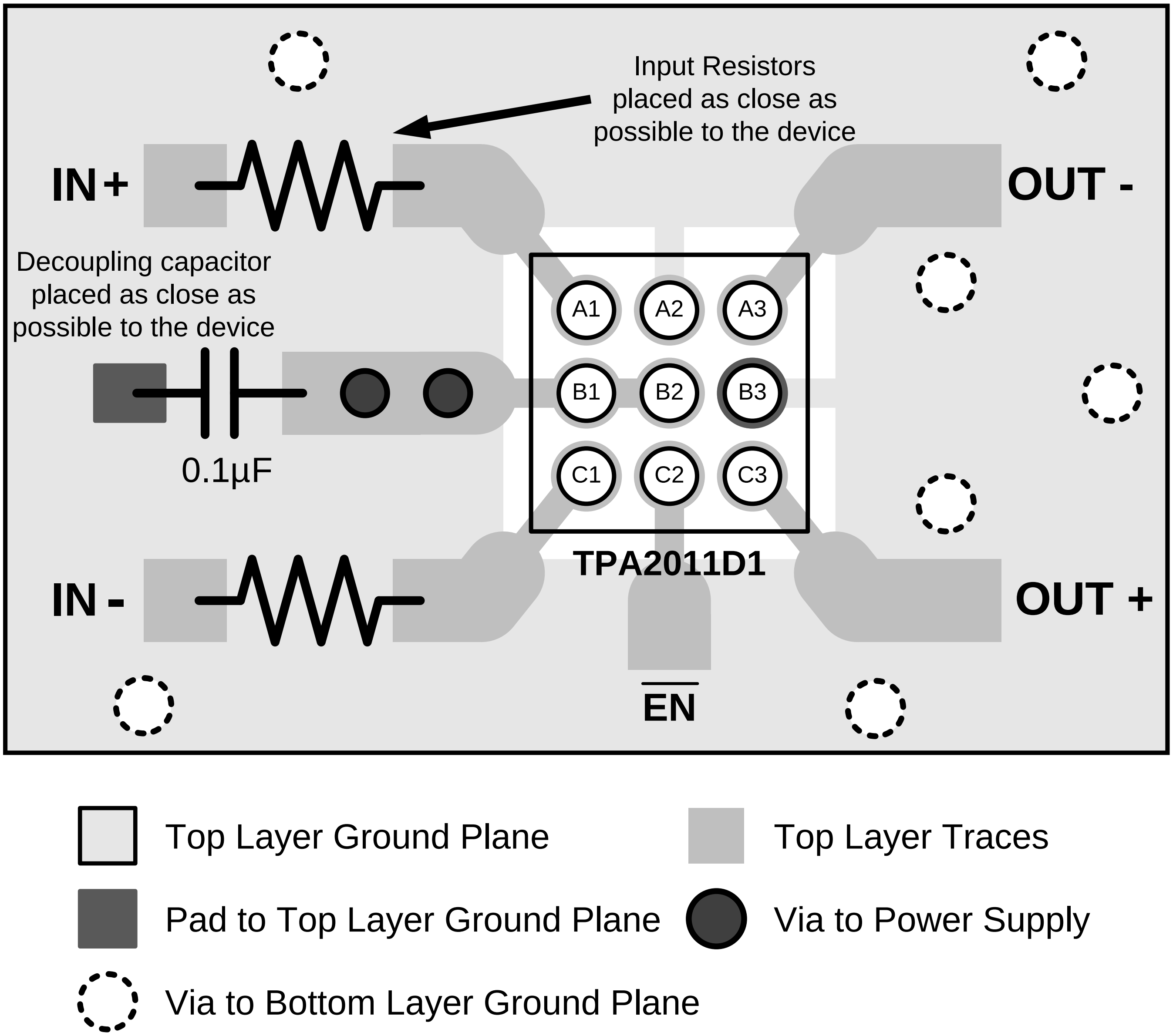


Figure 37. TPA2011D1 Layout Example

13 Device and Documentation Support

13.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

13.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPA2011D1YFFR	ACTIVE	DSBGA	YFF	9	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	OEW	Samples
TPA2011D1YFFT	ACTIVE	DSBGA	YFF	9	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	OEW	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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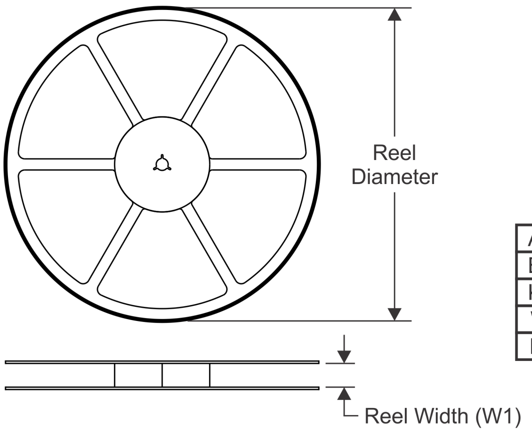
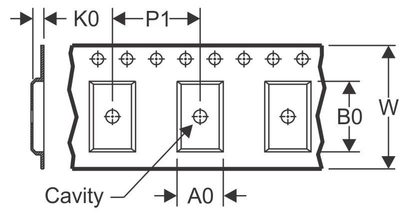
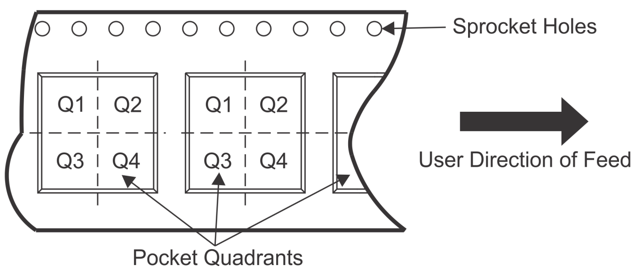
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION





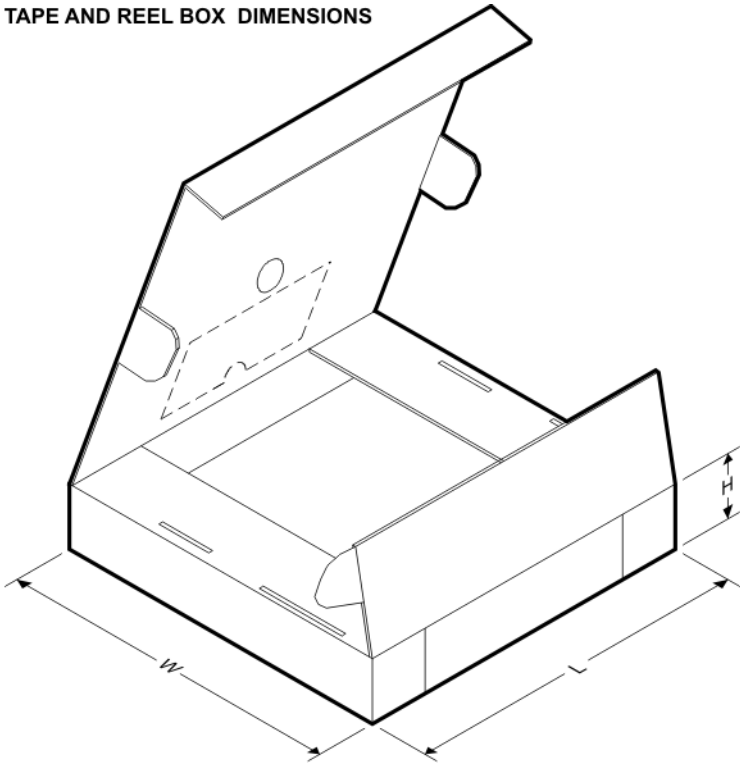
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

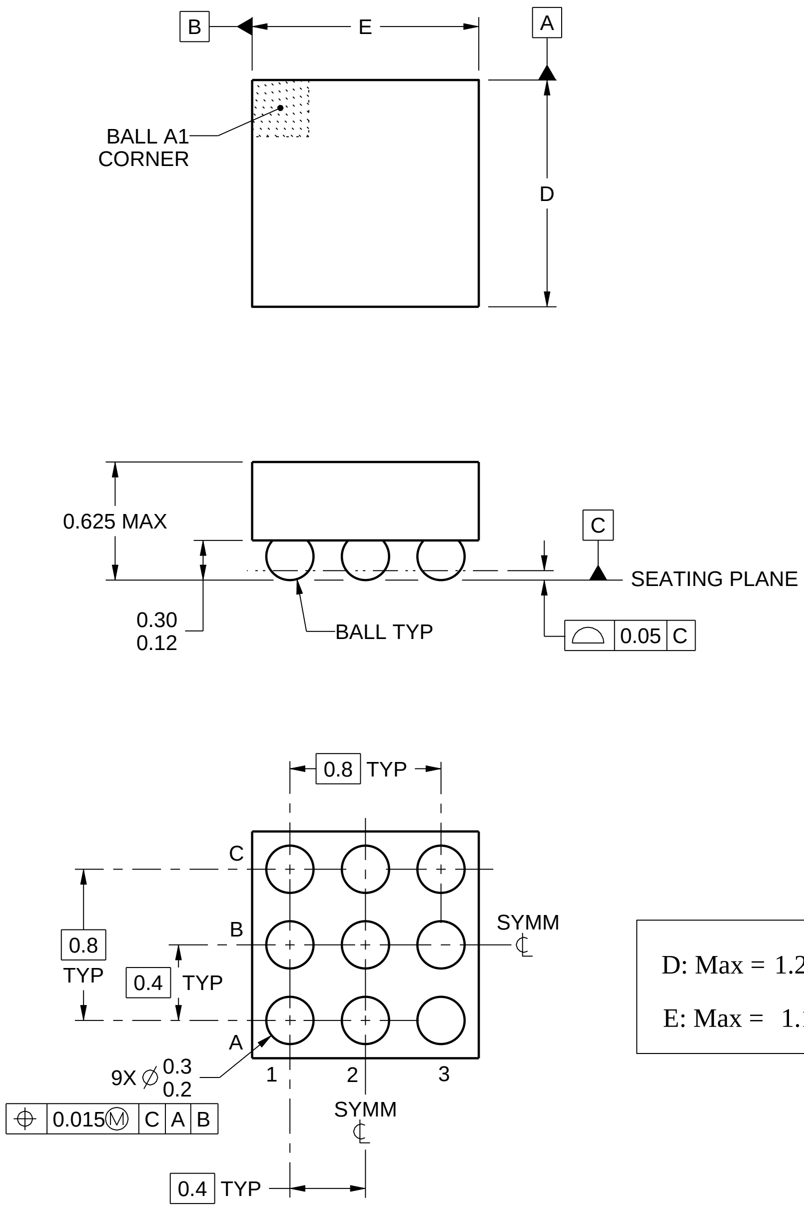
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPA2011D1YFFR	DSBGA	YFF	9	3000	180.0	8.4	1.34	1.34	0.81	4.0	8.0	Q1
TPA2011D1YFFT	DSBGA	YFF	9	250	180.0	8.4	1.34	1.34	0.81	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPA2011D1YFFR	DSBGA	YFF	9	3000	210.0	185.0	35.0
TPA2011D1YFFT	DSBGA	YFF	9	250	210.0	185.0	35.0



D: Max = 1.244 mm, Min =1.184 mm

E: Max = 1.19 mm, Min = 1.13 mm

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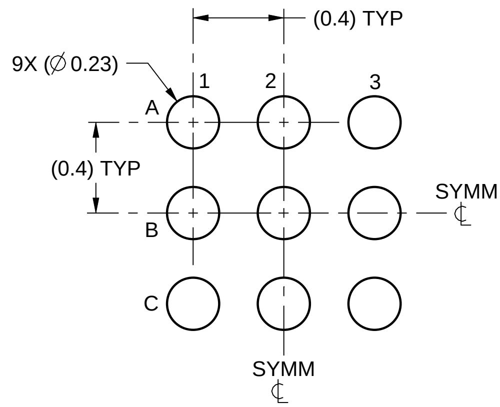
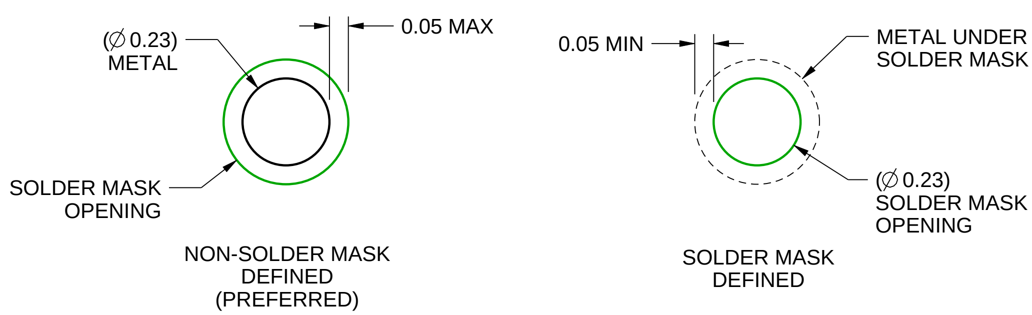
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:30X



SOLDER MASK DETAILS
NOT TO SCALE

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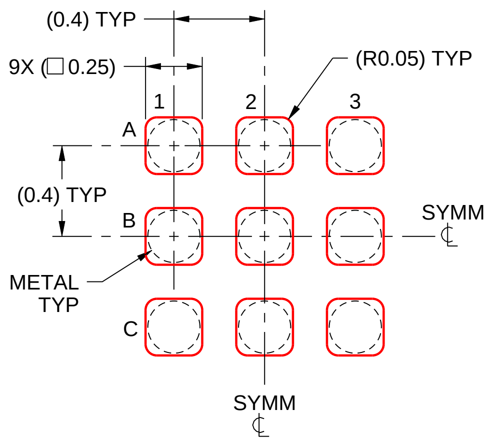
NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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