

TPD5S115 HDMI Companion Chip With Step-Up DC-DC Converter, Level-Shifter, and ESD Clamp

1 Features

- Conforms to HDMI Compliance Tests Without Any External Components
- Supports HDMI 2.0, HDMI 1.4, and HDMI 1.3 Standards
- Matches HDMI Connector Pin Mapping
- Internal DC-DC Converter to Generate 5 V From a Battery Voltage as Low as 2.3 V
- Auto-Direction Sensing, Level Shifting, and Buffering in the CEC, SDA, and SCL Paths
- IEC 61000-4-2 (Level 4) System Level ESD Compliance
- Reverse Current Blocking and Short-Circuit Protection to Protect Against Fault Conditions
- Industrial Temperature Range: -40°C to 85°C

2 Applications

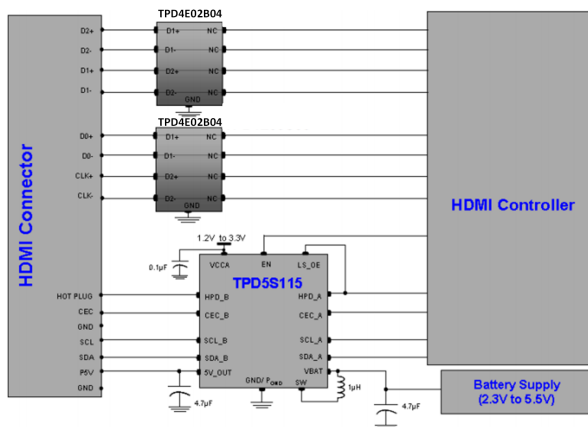
- Set-Top Boxes
- TVs
- Smart Phones
- Digital Camcorders
- Portable Game Consoles
- Digital Still Cameras

3 Description

The TPD5S115 device is an integrated HDMI companion chip solution. The device provides a regulated 5-V output (5VOUT) for sourcing the HDMI power line. The regulated 5-V output supplies up to 55 mA to the HDMI receiver with a current limiting function. The TPD5S115 features two control signals: EN and LS_OE. The control of 5VOUT and the hot plug detect (HPD) circuitry is independent of the LS_OE control signal and is controlled by the EN pin. The EN pin allows the detection scheme (5VOUT + HPD) to be active before turning on the whole HDMI link. The LS_OE activates the internal LDO, CEC, SCL, and SDA buffers only when EN is also activated. This dual stage enable scheme ensures optimized power saving for portable applications.

There are three noninverting, bidirectional, voltage level translation circuits for the SDA, SCL, and CEC lines. Each have a common power rail (VCCA) on the A side from 1.1 V to 3.6 V. On the B side, the SCL_B and SDA_B each have an internal 1.75-k Ω pullup connected to the regulated 5-V rail (5VOUT). The DDC (SCL_B and SDA_B) pins meet the I²C specification and drive up to 750-pF loads with the buffers. The CEC_B pin has an internal 27-k Ω pullup to an internal 3.3-V supply. The TPD5S115 exceeds the IEC61000-4-2 (Level 4) ESD protection level. This device features a space saving, 1.72-mm \times 1.72-mm, YFF package with 0.4-mm pitch.

Typical System Diagram



Copyright © 2016, Texas Instruments Incorporated

Device Information⁽¹⁾

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|-------------|------------|--------------------------|
| TPD5S115 | DSBGA (16) | 1.72 mm \times 1.72 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Table of Contents

| | | | |
|---|-----------|--|-----------|
| 1 Features | 1 | 7.1 Overview | 13 |
| 2 Applications | 1 | 7.2 Functional Block Diagram | 13 |
| 3 Description | 1 | 7.3 Feature Description | 13 |
| 4 Revision History | 2 | 7.4 Device Functional Modes | 15 |
| 5 Pin Configuration and Functions | 3 | 8 Application and Implementation | 16 |
| 6 Specifications | 4 | 8.1 Application Information | 16 |
| 6.1 Absolute Maximum Ratings | 4 | 8.2 Typical Applications | 16 |
| 6.2 ESD Ratings | 4 | 9 Power Supply Recommendations | 20 |
| 6.3 Recommended Operating Conditions | 4 | 10 Layout | 21 |
| 6.4 Thermal Information | 5 | 10.1 Layout Guidelines | 21 |
| 6.5 Electrical Characteristics | 5 | 10.2 Layout Example | 21 |
| 6.6 Electrical Characteristics – I/O Capacitances | 7 | 11 Device and Documentation Support | 22 |
| 6.7 Switching Characteristics – $V_{CCA} = 1.2\text{ V}$ | 7 | 11.1 Receiving Notification of Documentation Updates | 22 |
| 6.8 Switching Characteristics – $V_{CCA} = 1.5\text{ V}$ | 8 | 11.2 Community Resources | 22 |
| 6.9 Switching Characteristics – $V_{CCA} = 1.8\text{ V}$ | 8 | 11.3 Trademarks | 22 |
| 6.10 Switching Characteristics – $V_{CCA} = 2.5\text{ V}$ | 9 | 11.4 Electrostatic Discharge Caution | 22 |
| 6.11 Switching Characteristics – $V_{CCA} = 3.3\text{ V}$ | 10 | 11.5 Glossary | 22 |
| 6.12 Typical Characteristics | 11 | 12 Mechanical, Packaging, and Orderable Information | 22 |
| 7 Detailed Description | 13 | | |

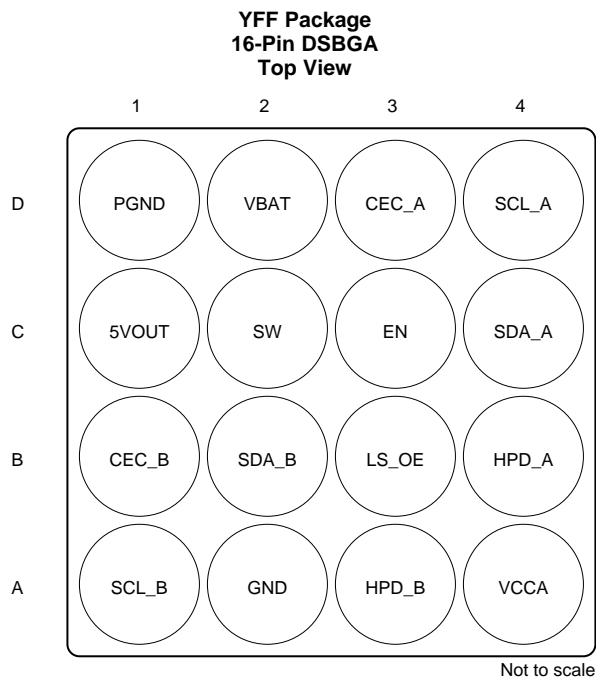
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision B (March 2013) to Revision C | Page |
|--|-------------|
| • Added <i>Device Information</i> table, <i>Pin Configuration and Functions</i> section, <i>Specifications</i> section, <i>ESD Ratings</i> table, <i>Detailed Description</i> section, <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section | 1 |
| • Deleted <i>Ordering Information</i> table; see POA at the end of the data sheet | 1 |
| • Added <i>Thermal Information</i> table | 5 |
| • Moved the passive components parameters from <i>Recommended Operating Conditions</i> table to the <i>Output Capacitor</i> section | 18 |

| Changes from Revision A (February 2013) to Revision B | Page |
|--|-------------|
| • Changed Board Layout section | 21 |

5 Pin Configuration and Functions



Pin Functions

| PIN | | TYPE ⁽¹⁾ | DESCRIPTION |
|-----------------|--------|---------------------|---|
| NAME | NO. | | |
| 5VOUT | C1 | O | DC-DC output. The 5-V power pin can supply a 55-mA regulated current to the HDMI receiver. A separate DC-DC converter control pin (EN) disables the DC-DC converter when operating at low-power mode. |
| CEC_A | D3 | I/O | LS system side CEC bus I/O. This pin is bidirectional and referenced to VCCA. |
| CEC_B | B1 | I/O | LS HDMI connector side CEC bus I/O. This pin is bidirectional and referenced to the 3.3-V internal supply. |
| EN | C3 | C | DC-DC enable. Enables the DC-DC converter and HPD circuitry when EN is HIGH. The EN is referenced based off VCCA. |
| GND | A2 | G | Device ground. |
| HPD_A | B4 | O | System side output for the hot plug detect. This pin is unidirectional and is referenced to VCCA. |
| HPD_B | A3 | I | HDMI side input for the hot plug detect. This pin is unidirectional and is referenced to 5VOUT. |
| LS_OE | B3 | C | Level shifter enable. This pin is referenced to VCCA. Enables level shifters and LDO when EN is HIGH and LS_OE is HIGH. |
| PGND | D1 | G | DC-DC converter ground. These pins are isolated from the GND pins. This pin should be tied to system GND. |
| SCL_A, SDA_A | D4, C4 | I/O | LS system side input and output for I ² C Bus. These pins are bidirectional and referenced to VCCA. |
| SCL_B, SDA_B | A1, B2 | I/O | LS HDMI side connector side input and output for I ² C Bus. These pins are bidirectional and referenced to 5VOUT. |
| SW | C2 | I | Switch input. This pin is the inductor input for the DC-DC converter. |
| VBAT | D2 | P | Battery supply. This voltage is typically 2.3 V to 5.5 V. |
| VCCA | A4 | P | System side supply. This voltage is typically 1.2 V to 3.3 V from the core microcontroller. |

(1) C = Control, G = Ground, I = Input, O = Output, P = Power

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | MIN | MAX | UNIT |
|--|----------------------------|------|-------------|------|
| Supply voltage | VCCA | | 4 | V |
| | VBAT | -0.3 | 6 | V |
| Input voltage, V_I ⁽²⁾ | SCL_A, SDA_A, CEC_A | -0.3 | 4 | V |
| | SCL_B, SDA_B, CEC_B, HPD_B | -0.3 | 6 | |
| | EN, LS_OE | -0.3 | 4 | |
| Voltage applied to any output in the high-impedance or power-off state, V_O ⁽²⁾ | SCL_A, SDA_A, CEC_A | -0.3 | 4 | V |
| | SCL_B, SDA_B, CEC_B | -0.3 | 6 | |
| Voltage applied to any output in the high or low state, V_O ⁽²⁾ | SCL_A, SDA_A, CEC_A | -0.3 | VCCA + 0.3 | V |
| | SCL_B, SDA_B, CEC_B | -0.3 | 5VOUT + 0.3 | |
| Input clamp current ($I_V < 0$) | | | -50 | mA |
| Output clamp current ($V_O < 0$) | | | -50 | mA |
| Continuous current through 5VOUT, or GND | | | ±100 | mA |
| Storage temperature, T_{stg} | | -65 | 150 | °C |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

6.2 ESD Ratings

| | | | VALUE | UNIT |
|-------------------------------------|--|---|--------|------|
| $V_{(ESD)}$ Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾ | All pins except pins 4A, B3, C3, C4, D3, and D4 | 500 | V |
| | | Pins 4A, B3, C3, C4, D3, and D4 | 2000 | |
| | Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾ | | 1000 | |
| | IEC 61000-4-2 Contact Discharge | Pins A1, A3, B1, B2, and C1 | ±14000 | |
| | IEC 61000-4-2 Air-gap Discharge | Pins A1, A3, B1, B2, and C1 | ±16000 | |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|-----------------------------------|--|--------------|--|---------------------------------|------|
| V_{CCA} | Supply voltage, VCCA | 1.2 | | 3.6 | V |
| V_{BAT} | Supply voltage, VBAT | 2.3 | | 5.5 | V |
| V_{IH} High-level input voltage | $V_{CCA} = 1.2\text{ V to }3.6\text{ V}$ | SCL_A, SDA_A | $0.7 \times V_{CCA}$ | V_{CCA} | V |
| | | CEC_A | $0.7 \times V_{CCA}$ | V_{CCA} | |
| | | EN, LS_OE | 1 | V_{CCA} | |
| | $5VOUT = 5\text{ V}$ | SCL_B, SDA_B | $0.7 \times 5VOUT$ | 5VOUT | |
| | | CEC_B | $0.7 \times 3.3\text{ V (internal)}^{(1)}$ | 3.3 V (internal) ⁽¹⁾ | |
| | | HPD_B | 2 | | |

- (1) 3.3 V (internal) is an internally generated voltage node for the CEC_B output buffer supply reference. An LDO generates this 3.3 V from 5VOUT when LS_OE and EN are HIGH.

Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | NOM | MAX | UNIT |
|------------------------------------|--|-----------------------------------|------------------------|--|--------------------------|------|
| V _{IL} | Low-Level input voltage | V _{CCA} = 1.2 V to 3.6 V | SCL_A, SDA_A | –0.5 | 0.082 × V _{CCA} | V |
| | | | CEC_A | –0.5 | 0.082 × V _{CCA} | |
| | | | EN, LS_OE | –0.5 | 0.4 | |
| | 5VOUT = 5 V | SCL_B, SDA_B | –0.5 | 0.3 × 5VOUT | | |
| | | CEC_B | –0.5 | 0.3 × 3.3 (internal) ⁽¹⁾ | | |
| | | HPD_B | 0 | 0.8 | | |
| V _{ILC} | Low-level input voltage | | –0.5 | 0.065 × V _{CCA} | V | |
| V _{OL} – V _{ILC} | Delta between V _{OL} and V _{ILC} (V _{IO} = 2.5 V) | | 0.1 × V _{CCA} | | V | |
| T _A | Operating free-air temperature | | –40 | | 85 | °C |

6.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | TPD5S115 | UNIT |
|-------------------------------|--|-------------|------|
| | | YFF (DSBGA) | |
| | | 16 PINS | |
| R _{θJA} | Junction-to-ambient thermal resistance | 78.2 | °C/W |
| R _{θJC(top)} | Junction-to-case (top) thermal resistance | 0.6 | °C/W |
| R _{θJB} | Junction-to-board thermal resistance | 13.2 | °C/W |
| ψ _{JT} | Junction-to-top characterization parameter | 2.5 | °C/W |
| ψ _{JB} | Junction-to-board characterization parameter | 13 | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics

T_A = –40°C to 85°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT | |
|-----------------------|--|--|---|-------------------------|-----|-----|------|----|
| V _{OHA} | | I _{OH} = –10 μA, V _I = V _{IH} , V _{CCA} = 1.2 V to 3.6 V | | V _{CCA} × 0.8 | | | V | |
| V _{OLA} | | I _{OL} = 10 μA, V _I = V _{IL} , V _{CCA} = 1.2 V to 3.6 V | | V _{CCA} × 0.16 | | | V | |
| V _{OHB} | | I _{OH} = –10 μA, V _I = V _{IH} | | | | | V | |
| V _{OLB} | | I _{OL} = 3 mA, V _I = V _{IL} | | | | 0.4 | V | |
| R _{PU} | Internal pullup | SCL_A, SDA_A | Pullup connected to V _{CCA} rail | 10 | | | kΩ | |
| | | SCL_B, SDA_B | Pullup connected to 5-V rail | 1.75 | | | | |
| I _{PULLUPAC} | Transient boosted pullup current (rise-time accelerator) | SCL_B, SDA_B | Pullup connected to 5-V rail | 15 | | | mA | |
| I _{OFF} | Leakage current | A port | V _{CCA} = 0 V, V _I or V _O = 0 to 3.6 V, V _{CCA} = 0 V | | | ±5 | μA | |
| | | B port | 5VOUT = 0 V, V _I or V _O = 0 to 5.5 V, V _{CCA} = 0 V to 3.6 V | | | ±5 | | |
| I _{OZ} | | A port | V _O = V _{CCO} or GND, V _{CCA} = 1.2 V to 3.6 V | | | ±5 | | |
| | | B port | V _I = V _{CCI} or GND, V _{CCA} = 1.2 V to 3.6 V | | | ±5 | | |
| C _L | Bus load capacitance | A port | | | | 15 | pF | |
| | | B port | | | | 750 | | |
| SUPPLY CURRENT | | | | | | | | |
| I _{CCA} | V _{CCA} supply current | Standby | I/Os = HIGH | | | 2 | μA | |
| | | Active | I/Os = HIGH | | | 15 | μA | |
| I _{CCB} | V _{BAT} supply current | Standby | EN = LOW, LS_OE = LOW | | | 0.5 | μA | |
| | | DC-DC and HPD active | EN = HIGH, LS_OE = LOW | | | 30 | 50 | μA |
| | | DC-DC, HPD, DDC, CEC Active | EN = HIGH, LS_OE = LOW, I/Os = HIGH | | | 225 | 300 | μA |

Electrical Characteristics (continued)
 $T_A = -40^{\circ}\text{C}$ to 85°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|--|--|--|-----------------------|-----------|------------------|
| DC-DC CONVERTER | | | | | | |
| V_{BAT} | Input voltage | | 2.3 | | 5.5 | V |
| V_{OUT} | Total DC output voltage ⁽¹⁾ | | 4.9 | 5 | 5.13 | V |
| T_{OVA} | Total output voltage accuracy ⁽²⁾ | | 4.8 | 5 | 5.3 | V |
| V_{IO_Ripple} | Output voltage ripple, loaded | $I_O = 65\text{ mA}$ | | 50.6 | | mV _{PP} |
| | | $I_O = 150\text{ mA}$ | | 16 | | |
| f_{CLK} | Internal operating frequency | $V_{BAT} = 2.3\text{ V to }5.5\text{ V}$ | | 3.5 | | MHz |
| t_{START} | Start-up time | From EN input to 5-V power output 90% point | | 187 | | μs |
| I_O | Output current | $V_{BAT} = 2.3\text{ V to }5.5\text{ V}$ | 55 | | | mA |
| | Reverse leakage current, V_O | EN = LOW, $V_O = 5.5\text{ V}$ | | | 2.5 | μA |
| | Leakage current from battery to V_O | EN = LOW | | | 5 | μA |
| V_{BATUV} | Undervoltage lockout threshold | Falling | | 2 | | V |
| | | Rising | | 2.1 | | V |
| | Line transient response | $V_{BAT} = 3.4\text{ V}$, $I_O = 20\text{ mA to }65\text{ mA}$, A 217 Hz, 600 mV _{PP} square wave pulse | | 17.1 | | mV _{pk} |
| | Load transient response | $V_{BAT} = 3.4\text{ V}$, $I_O = 5\text{ mA to }65\text{ mA}$, 10- μs pulse, $t_{RISE} = t_{FALL} = 0.1\text{ }\mu\text{s}$ | | 63.5 | | mV _{pk} |
| I_{INRUSH} | Inrush current, average over t_{START} | $V_{BAT} = 2.3\text{ V to }5.5\text{ V}$, $I_{OUT} = 65\text{ mA}$ | | 168 | | mA |
| I_{SC} | Short-circuit current limit from output | | | 90 | | mA |
| VOLTAGE LEVEL SHIFTER CEC LINE (x_A & x_B PORTS) | | | | | | |
| V_{OHA} | | $I_{OH} = -10\text{ }\mu\text{A}$, $V_I = V_{IH}$, $V_{CCA} = 1.2\text{ V to }3.6\text{ V}$ | $V_{CCA} \times 0.8$ | | | V |
| V_{OLA} | | $I_{OL} = 10\text{ }\mu\text{A}$, $V_I = V_{IL}$, $V_{CCA} = 1.2\text{ V to }3.6\text{ V}$ | | $V_{CCA} \times 0.16$ | | V |
| V_{OHB} | | $I_{OH} = -20\text{ }\mu\text{A}$, $V_I = V_{IH}$ | $V_{CCA} \times 0.8$ | | | V |
| V_{OLB} | | $I_{OL} = 3\text{ mA}$, $V_I = V_{IL}$ | | | 0.4 | V |
| R_{PU} | Internal pullup | CEC_A | Pullup connected to V_{CCA} rail | | 10 | k Ω |
| | | CEC_B | Pullup connected to 3.3 V rail | 22 | 26 | |
| R_{PD} | Internal pulldown | CEC_B | Pullup connected to GND | | 14 | M Ω |
| I_{OFF} | A port | $V_{CCA} = 0\text{ V}$, V_I or $V_O = 0$ to 3.6 V, $V_{CCA} = 0\text{ V}$ | | | ± 5 | μA |
| | B port | $5V_{OUT} = 0\text{ V}$, V_I or $V_O = 0$ to 5.5 V, $V_{CCA} = 0\text{ V to }3.6\text{ V}$ | | | ± 1.8 | |
| I_{OZ} | A port | $V_O = V_{CCO}$ or GND, $V_{CCA} = 1.2\text{ V to }3.6\text{ V}$ | | | ± 5 | μA |
| | B port | $V_I = V_{CCI}$ or GND, $V_{CCA} = 1.2\text{ V to }3.6\text{ V}$ | | | ± 5 | |
| VOLTAGE LEVEL SHIFTER - HPD LINE (X_A & X_B) | | | | | | |
| V_{OHA} | | $I_{OH} = -3\text{ mA}$, $V_I = V_{IH}$, $V_{CCA} = 1.2\text{ V to }3.6\text{ V}$ | $V_{CCA} \times 0.7$ | | | V |
| V_{OLA} | | $I_{OL} = 3\text{ mA}$, $V_I = V_{IL}$, $V_{CCA} = 1.2\text{ V to }3.6\text{ V}$ | | | 0.4 | V |
| R_{PD} | Internal pulldown | HPD_B | Pullup connected to GND | | 100 | k Ω |
| I_{OZ} | | A port | $V_I = V_{CCI}$ or GND, $V_{CCA} = 3.6\text{ V}$ | | ± 5 | μA |
| LS_OE, EN | | | | | | |
| I_i | | $V_I = V_{CCA}$ or GND, $V_{CCA} = 1.2\text{ V to }3.6\text{ V}$ | | | ± 12 | |

(1) Includes voltage references, DC load and line regulations, process and temperature.

(2) Includes voltage references, DC load and line regulations, transient load and line regulations, ripple, process, and temperature.

6.6 Electrical Characteristics – I/O Capacitances

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|-------------|---------------------|--|---|-----|-----|-----|------|
| Capacitance | EN, LS_OE | $V_{BIAS} = 1.8\text{ V}$, $f = 1\text{ MHz}$, 30-mV _{pp} AC signal | $V_{CCA} = 3.6\text{ V}$, $V_{BAT} = 5\text{ V}$ | | 7.1 | 9.5 | pF |
| | SCL_A, SDA_A, CEC_A | | $V_{CCA} = 3.6\text{ V}$, $V_{BAT} = 5\text{ V}$, EN = LOW | | 7 | | pF |
| | HPD_A, HPD_B | | $V_{CCA} = 3.6\text{ V}$, $V_{BAT} = 5\text{ V}$, EN = LOW | | 4 | | pF |
| | SCL_B, SDA_B | $V_{BIAS} = 2.5\text{ V}$, $f = 100\text{ kHz}$, 3.5-V _{pp} AC signal | $V_{CCA} = 3.6\text{ V}$, $V_{BAT} = 5\text{ V}$, EN = LOW, LS_OE = HIGH | | 10 | | pF |
| | CEC_B | $V_{BIAS} = 1.65\text{ V}$, $f = 100\text{ kHz}$, 2.5-V _{pp} AC signal | $V_{CCA} = 3.6\text{ V}$, $V_{BAT} = 5\text{ V}$, EN = LOW, LS_OE = HIGH | | 7 | | pF |
| | CEC_B | | $V_{CCA} = 0\text{ V}$, $5V_{IN} = 0\text{ V}$ | | 7 | | pF |

6.7 Switching Characteristics – $V_{CCA} = 1.2\text{ V}$

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|--|-------------------------------|-----------------|----------------------|-----|------|-----|------|
| SCL and SDA LINES (x_A & x_B PORTS) | | | | | | | |
| t_{PHL} | High-to-low propagation delay | A to B | DDC channels enabled | | 394 | | ns |
| | | B to A | DDC channels enabled | | 347 | | |
| t_{PLH} | Low-to-high propagation delay | A to B | DDC channels enabled | | 504 | | ns |
| | | B to A | DDC channels enabled | | 171 | | |
| t_{FALL} | Fall time | A port | DDC channels enabled | | 146 | | ns |
| | | B port | DCC channels enabled | | 135 | | |
| t_{RISE} | Rise time | A port | DCC channels enabled | | 190 | | ns |
| | | B port | DCC channels enabled | | 93 | | |
| f_{MAX} | Maximum switching frequency | | DCC channels enabled | | 400 | | kHz |
| CEC LINE (x_A & x_B PORTS) | | | | | | | |
| t_{PHL} | High-to-low propagation delay | A to B | CEC channels enabled | | 550 | | ns |
| | | B to A | CEC channels enabled | | 350 | | |
| t_{PLH} | Low-to-high propagation delay | A to B | CEC channels enabled | | 13 | | μs |
| | | B to A | CEC channels enabled | | 290 | | |
| t_{FALL} | Fall time | A port | CEC channels enabled | | 146 | | ns |
| | | B port | CEC channels enabled | | 200 | | |
| t_{RISE} | Rise time | A port | CEC channels enabled | | 190 | | ns |
| | | B port | CEC channels enabled | | 16.4 | | |
| HPD LINE (x_A & x_B PORTS) | | | | | | | |
| t_{PHL} | Propagation delay | B to A | CEC channels enabled | | 10.4 | | ns |
| t_{PLH} | Low-to-high propagation delay | B to A | CEC channels enabled | | 9.9 | | ns |
| t_{FALL} | Fall time | A port | CEC channels enabled | | 0.7 | | ns |
| t_{RISE} | Rise time | A port | CEC channels enabled | | 0.8 | | ns |

6.8 Switching Characteristics – $V_{CCA} = 1.5 V$

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|-------------------------------|-----------------|----------------------|-----|------|-----|------|
| SCL, SDA LINES (x_A & x_B PORTS) | | | | | | | |
| t _{PHL} | High-to-low propagation delay | A to B | DDC channels enabled | | 375 | | ns |
| | | B to A | DDC channels enabled | | 272 | | |
| t _{PLH} | Low-to-high propagation delay | A to B | DDC channels enabled | | 488 | | ns |
| | | B to A | DDC channels enabled | | 166 | | |
| t _{FALL} | Fall time | A port | DDC channels enabled | | 114 | | ns |
| | | B port | DCC channels enabled | | 135 | | |
| t _{RISE} | Rise time | A port | DCC channels enabled | | 186 | | ns |
| | | B port | DCC channels enabled | | 93 | | |
| f _{MAX} | Maximum switching frequency | | DCC channels enabled | 400 | | | kHz |
| CEC Line (x_A & x_B Ports) | | | | | | | |
| t _{PHL} | High-to-low propagation delay | A to B | CEC channels enabled | | 536 | | ns |
| | | B to A | CEC channels enabled | | 272 | | |
| t _{PLH} | Low-to-high propagation delay | A to B | CEC channels enabled | | 13 | | μs |
| | | B to A | CEC channels enabled | | 285 | | |
| t _{FALL} | Fall time | A port | CEC channels enabled | | 113 | | ns |
| | | B port | CEC channels enabled | | 201 | | |
| t _{RISE} | Rise time | A port | CEC channels enabled | | 187 | | ns |
| | | B port | CEC channels enabled | | 16 | | |
| HPD LINE (x_A & x_B PORTS) | | | | | | | |
| t _{PHL} | High-to-low propagation delay | B to A | CEC channels enabled | | 10 | | ns |
| t _{PLH} | Low-to-high propagation delay | B to A | CEC channels enabled | | 10 | | ns |
| t _{FALL} | Fall time | A port | CEC channels enabled | | 0.46 | | ns |
| t _{RISE} | Rise time | A port | CEC channels enabled | | 0.5 | | ns |

6.9 Switching Characteristics – $V_{CCA} = 1.8 V$

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|-------------------------------|-----------------|----------------------|-----|-----|-----|------|
| SCL, SDA LINES (x_A & x_B PORTS) | | | | | | | |
| t _{PHL} | High-to-low propagation delay | A to B | DDC channels enabled | | 370 | | ns |
| | | B to A | DDC channels enabled | | 230 | | |
| t _{PLH} | Low-to-high propagation delay | A to B | DDC channels enabled | | 480 | | ns |
| | | B to A | DDC channels enabled | | 163 | | |
| t _{FALL} | Fall time | A port | DDC channels enabled | | 100 | | ns |
| | | B port | DCC channels enabled | | 135 | | |
| t _{RISE} | Rise time | A port | DCC channels enabled | | 180 | | ns |
| | | B port | DCC channels enabled | | 93 | | |
| f _{MAX} | Maximum switching frequency | | DCC channels enabled | 400 | | | kHz |
| CEC LINE (x_A & x_B PORTS) | | | | | | | |
| t _{PHL} | High-to-low propagation delay | A to B | CEC channels enabled | | 530 | | ns |
| | | B to A | CEC channels enabled | | 230 | | |
| t _{PLH} | Low-to-high propagation delay | A to B | CEC channels enabled | | 13 | | μs |
| | | B to A | CEC channels enabled | | 280 | | |
| t _{FALL} | Fall time | A port | CEC channels enabled | | 98 | | ns |
| | | B port | CEC channels enabled | | 200 | | |

Switching Characteristics – $V_{CCA} = 1.8\text{ V}$ (continued)

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---------------------------------------|-------------------------------|-----------------|----------------------|-----|------|-----|---------------|
| t_{RISE} | Rise time | A port | CEC channels enabled | | 180 | | ns |
| | | B port | CEC channels enabled | | 16 | | μs |
| HPD LINE (x_A & x_B PORTS) | | | | | | | |
| t_{PHL} | High-to-low propagation delay | B to A | CEC channels enabled | | 10 | | ns |
| t_{PLH} | Low-to-high propagation delay | B to A | CEC channels enabled | | 10 | | ns |
| t_{FALL} | Fall time | A port | CEC channels enabled | | 0.41 | | ns |
| t_{RISE} | Rise time | A port | CEC channels enabled | | 0.41 | | ns |

6.10 Switching Characteristics – $V_{CCA} = 2.5\text{ V}$

over operating free-air temperature range (unless otherwise noted)

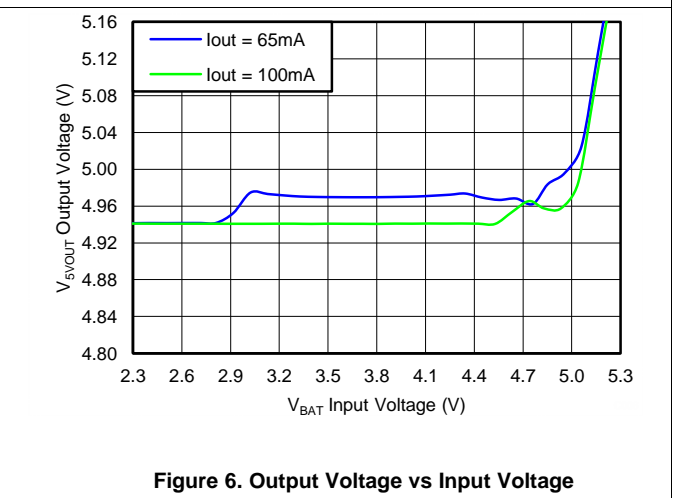
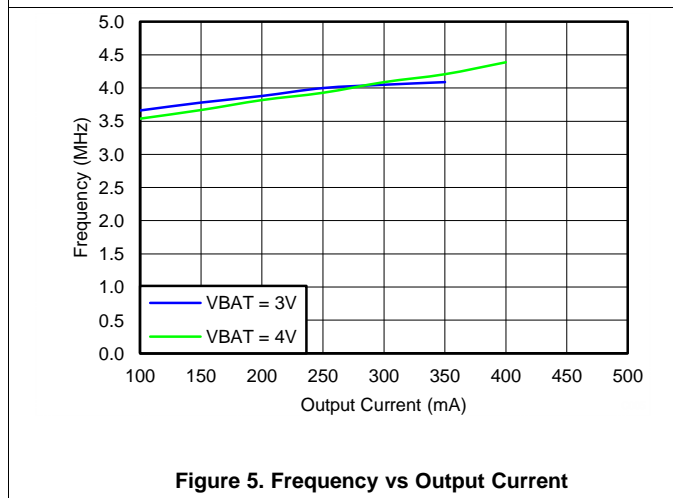
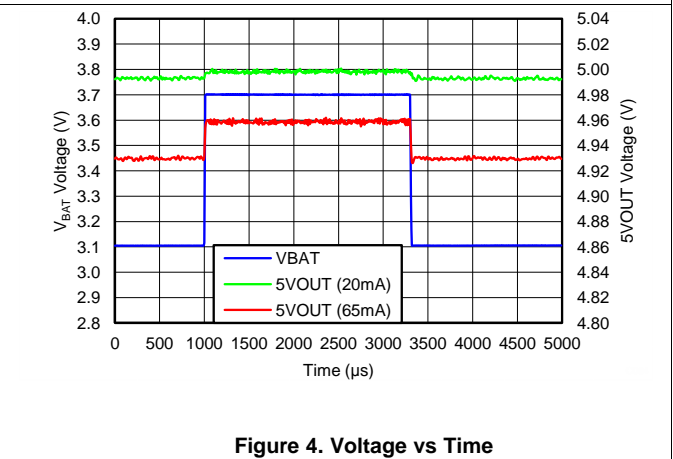
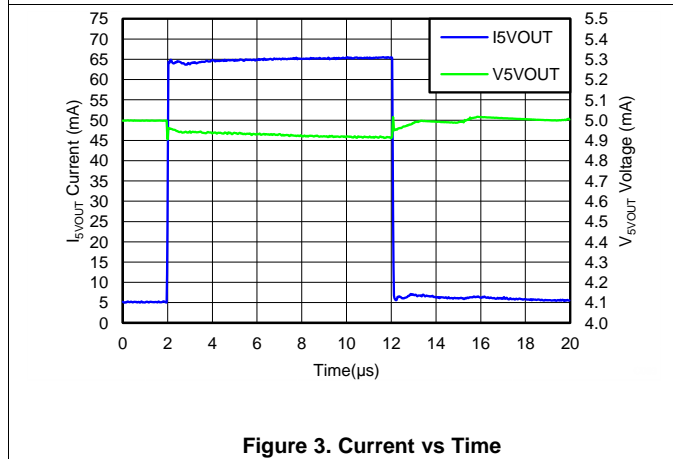
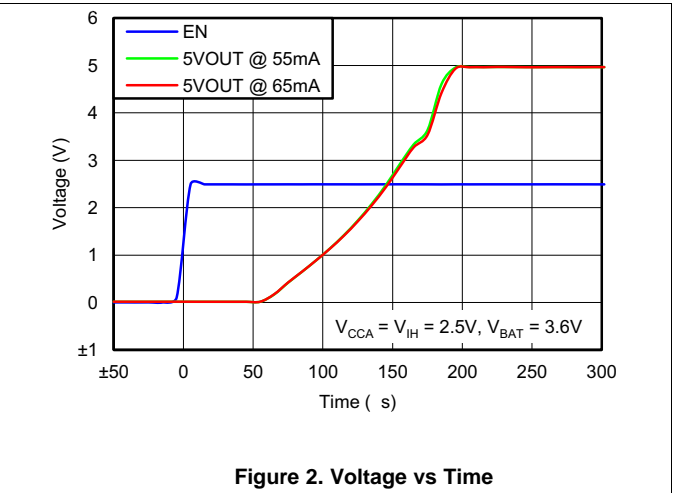
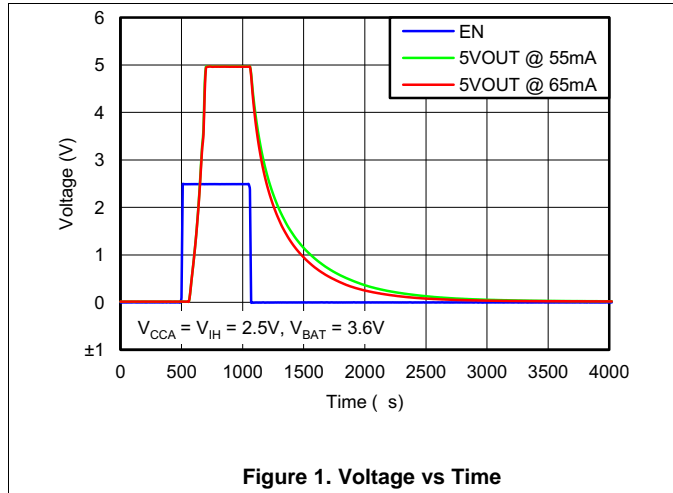
| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|-------------------------------|-----------------|----------------------|-----|------|-----|---------------|
| SCL, SDA LINES (x_A & x_B PORTS) | | | | | | | |
| t_{PHL} | High-to-low propagation delay | A to B | DDC channels enabled | | 370 | | ns |
| | | B to A | DDC channels enabled | | 185 | | |
| t_{PLH} | Low-to-high propagation delay | A to B | DDC channels enabled | | 467 | | ns |
| | | B to A | DDC channels enabled | | 160 | | |
| t_{FALL} | Fall time | A port | DDC channels enabled | | 80 | | ns |
| | | B port | DCC channels enabled | | 135 | | |
| t_{RISE} | Rise time | A port | DCC channels enabled | | 179 | | ns |
| | | B port | DCC channels enabled | | 93 | | |
| f_{MAX} | Maximum switching frequency | | DCC channels enabled | 400 | | | kHz |
| CEC LINE (x_A & x_B PORTS) | | | | | | | |
| t_{PHL} | High-to-low propagation delay | A to B | CEC channels enabled | | 530 | | ns |
| | | B to A | CEC channels enabled | | 185 | | |
| t_{PLH} | Low-to-high propagation delay | A to B | CEC channels enabled | | 13 | | μs |
| | | B to A | CEC channels enabled | | 275 | | ns |
| t_{FALL} | Fall time | A port | CEC channels enabled | | 80 | | ns |
| | | B port | CEC channels enabled | | 200 | | |
| t_{RISE} | Rise time | A port | CEC channels enabled | | 180 | | ns |
| | | B port | CEC channels enabled | | 16 | | μs |
| HPD LINE (x_A & x_B PORTS) | | | | | | | |
| t_{PHL} | High-to-low propagation delay | B to A | CEC channels enabled | | 10 | | ns |
| t_{PLH} | Low-to-high propagation delay | B to A | CEC channels enabled | | 10 | | ns |
| t_{FALL} | Fall time | A port | CEC channels enabled | | 0.35 | | ns |
| t_{RISE} | Rise time | A port | CEC channels enabled | | 0.35 | | ns |

6.11 Switching Characteristics – $V_{CCA} = 3.3\text{ V}$

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|-------------------------------|-----------------|----------------------|-----|------|-----|------|
| SCL, SDA LINES (x_A & x_B PORTS) | | | | | | | |
| t _{PHL} | High-to-low propagation delay | A to B | DDC channels enabled | | 370 | | ns |
| | | B to A | DDC channels enabled | | 160 | | |
| t _{PLH} | Low-to-high propagation delay | A to B | DDC channels enabled | | 460 | | ns |
| | | B to A | DDC channels enabled | | 155 | | |
| t _{FALL} | Fall time | A port | DDC channels enabled | | 75 | | ns |
| | | B port | DCC channels enabled | | 135 | | |
| t _{RISE} | Rise time | A port | DCC channels enabled | | 180 | | ns |
| | | B port | DCC channels enabled | | 93 | | |
| f _{MAX} | Maximum switching frequency | | DCC channels enabled | 400 | | | kHz |
| CEC LINE (x_A & x_B PORTS) | | | | | | | |
| t _{PHL} | High-to-low propagation delay | A to B | CEC channels enabled | | 530 | | ns |
| | | B to A | CEC channels enabled | | 160 | | |
| t _{PLH} | Low-to-high propagation delay | A to B | CEC channels enabled | | 13 | | μs |
| | | B to A | CEC channels enabled | | 275 | | ns |
| t _{FALL} | Fall time | A port | CEC channels enabled | | 73 | | ns |
| | | B port | CEC channels enabled | | 200 | | |
| t _{RISE} | Rise time | A port | CEC channels enabled | | 180 | | ns |
| | | B port | CEC channels enabled | | 16 | | μs |
| HPD LINE (x_A & x_B PORTS) | | | | | | | |
| t _{PHL} | High-to-low propagation delay | B to A | CEC channels enabled | | 10 | | ns |
| t _{PLH} | Low-to-high propagation delay | B to A | CEC channels enabled | | 10 | | ns |
| t _{FALL} | Fall time | A port | CEC channels enabled | | 0.34 | | ns |
| t _{RISE} | Rise time | A port | CEC channels enabled | | 0.36 | | ns |

6.12 Typical Characteristics



Typical Characteristics (continued)

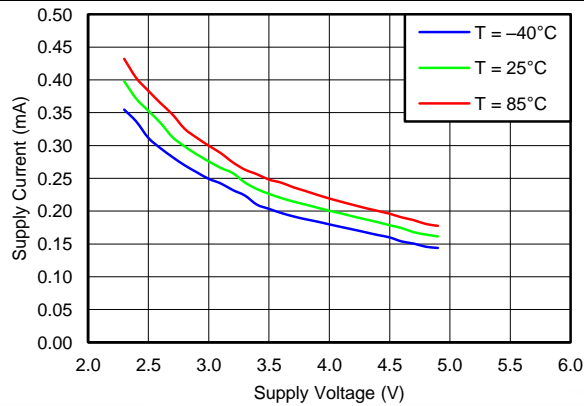


Figure 7. Supply Current vs Supply Voltage

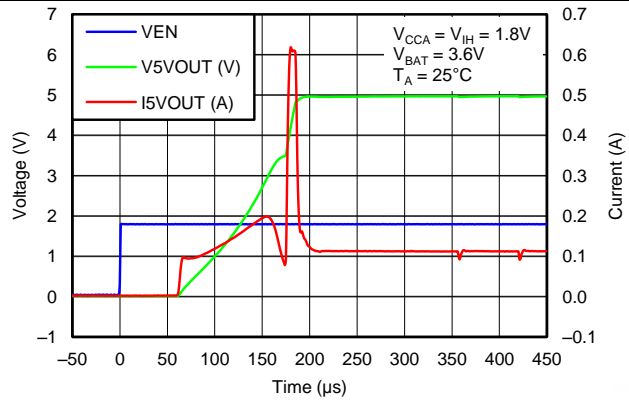


Figure 8. Voltage and Current vs Time

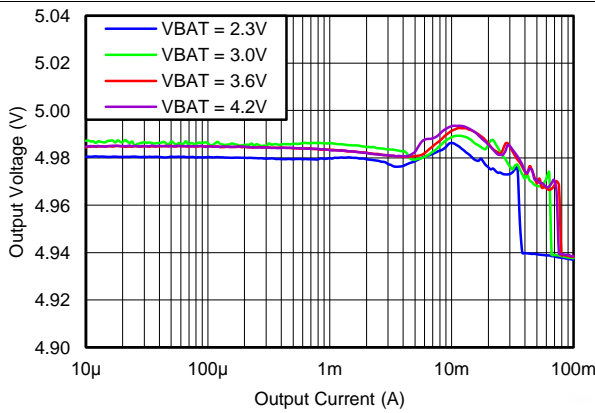


Figure 9. Output Voltage vs Output Current

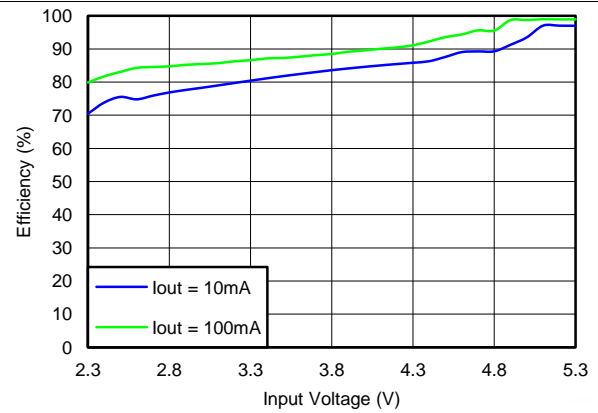


Figure 10. Efficiency vs Input Voltage

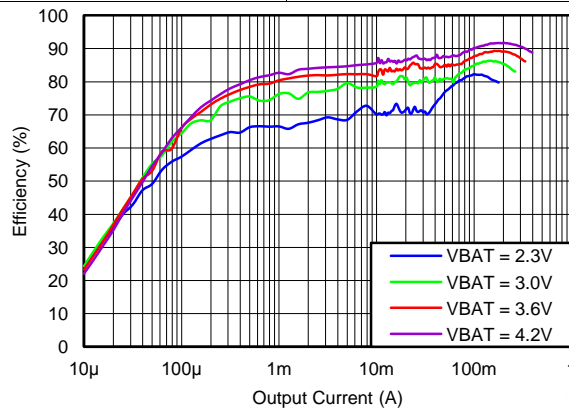


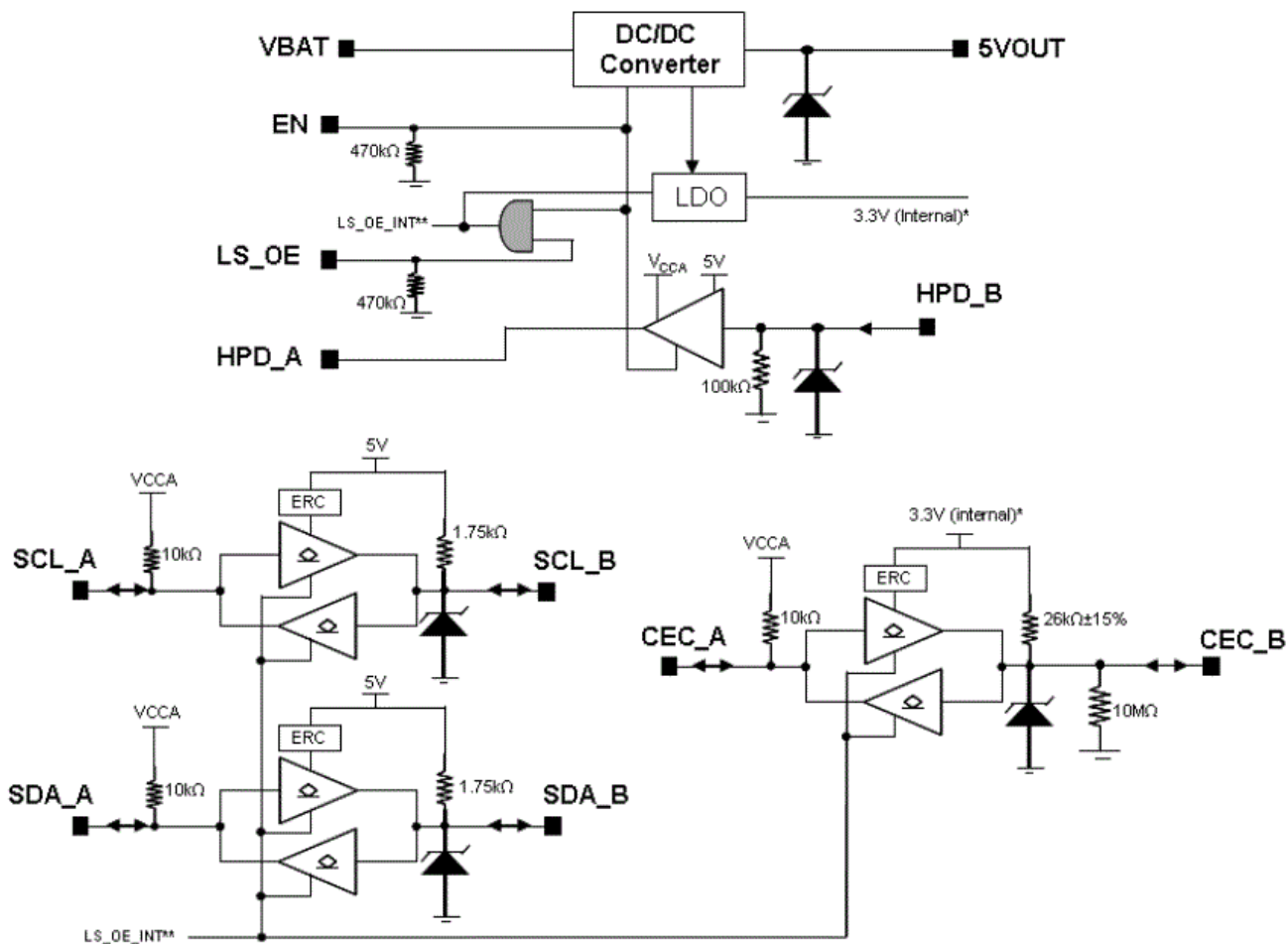
Figure 11. Efficiency vs Output Current

7 Detailed Description

7.1 Overview

The TPD5S115 is an integrated interface solution that covers HDMI versions' 2.0, 1.4, and 1.3 need for power supply voltage management and control line level translation. On the power supply line, it has a DC-DC converter that takes the internal power supply from 2.3 V to 5.5 V, and outputs a regulated and current-limited, 5-V voltage to the connector. The drivers support level translation on HPD, ECE, SCL, and SDA lines in both transmission directions. Moreover, the rise-time acceleration feature helps drive the high capacitive load on the cable side. Every channel comes with robust ESD protection with ± 14 -kV contact and ± 16 -kV air-gap IEC61000-4-2 capability.

7.2 Functional Block Diagram

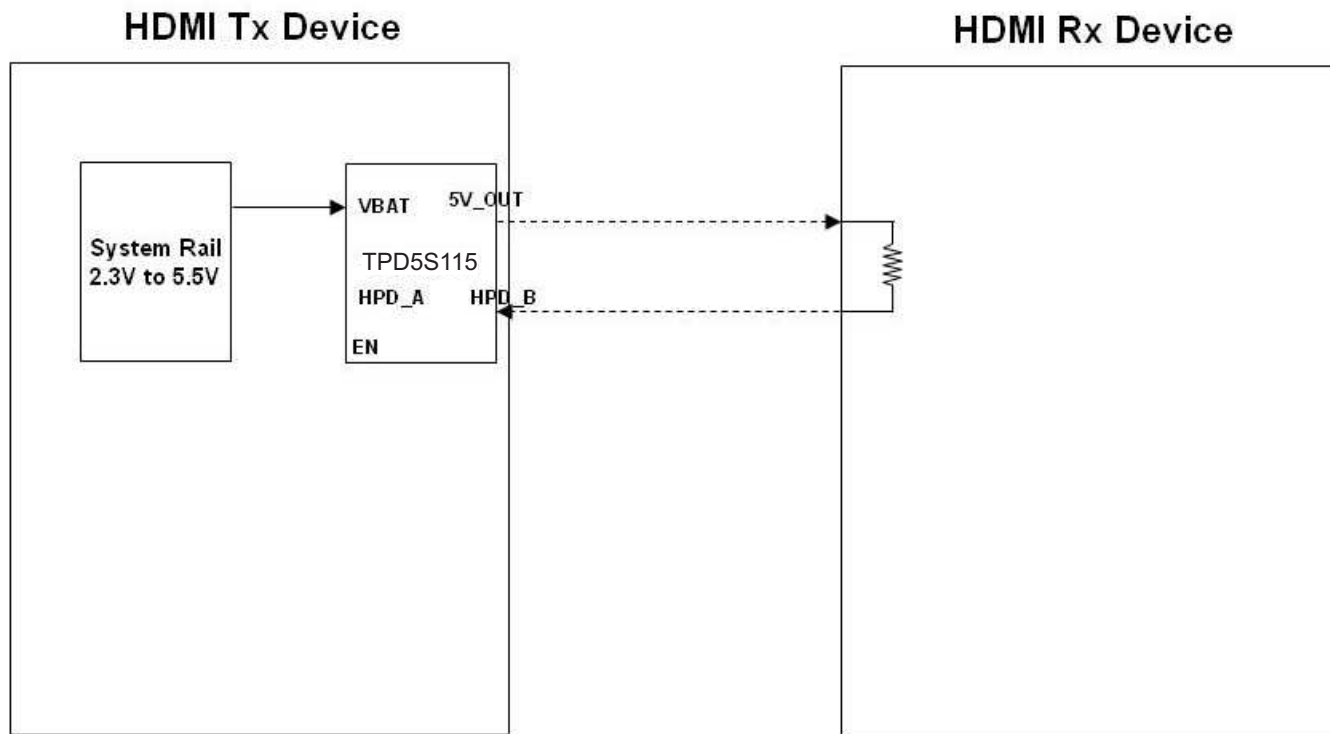


- (1) 3.3 V (internal) is an internal 3.3-V supply rail which is generated from 5VOUT when EN and LS_OE are HIGH.
- (2) LS_OE_INT* is an internal control signal generated from EN and LS_OE signals. LS_OE_INT* is active when both EN and LS_OE are HIGH.

7.3 Feature Description

7.3.1 Rise-Time Accelerators

The HDMI cable side of the DDC lines incorporates rise-time accelerators to support the high capacitive load on the HDMI cable side. The rise-time accelerator boosts the cable-side DDC signal, independent of which side of the bus is releasing the signal.

Feature Description (continued)


Copyright © 2016, Texas Instruments Incorporated

Figure 12. Receiving and Transmitting Interaction
7.3.2 Hot Plug Detect

After the TPD5S115's DC-DC converter and HPD block are enabled through the EN pin, the TPD5S115 is ready for continual HDMI receiver detection. After a HDMI cable connects a receiving and transmitting device together, the 5-V signal from the DC-DC output flows through the receiving device's internal resistor and into HPD's input. The HPD buffer's output then goes high, indicating to the transmitter that a receiving device is connected. To save power, periodic detection can be done by turning on and off the DC-DC converter before a receiving device is connected.

NOTE

Ground offset between the TPD5S115 ground and the ground of devices on port A of the TPD5S115 must be avoided. A CMOS or NMOS open-drain capable of sinking 3 mA of current at 0.4 V has an output resistance of 133 Ω or less ($R = E / I$). Such a driver shares enough current with the port A output pulldown of the TPD5S115 to be detected as a LOW while the ground offset is zero. If the ground offset is greater than 0 V, then the driver resistance must be less. Because V_{ILC} can be as low as 90 mV at cold temperatures and the low end of the current distribution, the maximum ground offset should not exceed 50 mV. Bus repeaters that use an output offset are not interoperable with the port A of the TPD5S115 as their output LOW levels are not recognized by the TPD5S115 as a LOW. If the TPD5S115 is placed in an application where the V_{IL} of port A of the TPD5S115 does not go below its V_{ILC} it will pull port B LOW initially when port A input transitions LOW but the port B will return HIGH, so it does not reproduce the port A input on port B. Such applications must be avoided. Port B is interoperable with all I²C-bus slaves, masters, and repeaters.

Feature Description (continued)

7.3.3 CEC Level Shift Operation

The CEC level shift function operates in the same manner as the DDC lines except that the CEC line does not need the rise time accelerator function.

7.3.4 Pullup Resistor

The system is designed to work properly with no external pullup resistors on the DDC, CEC, and HPD lines.

7.3.5 Undervoltage Lockout

The undervoltage-lockout circuit prevents the DC-DC converter from malfunctioning at low input voltages and from excessive discharge of the battery. It disables the output stage of the converter once the falling V_{IN} trips the undervoltage-lockout threshold (V_{BATUV}). The undervoltage-lockout threshold for falling V_{IN} is typically 2 V. The device starts operation once the rising V_{IN} trips the under-voltage-lockout threshold again at 2.1 V (typical).

7.3.6 Soft Start

The DC-DC converter has an internal soft-start circuit that controls the ramp-up of the output voltage. The output voltage reaches its nominal value within 250 μ s (typical) after EN has been pulled high. The output voltage ramps up from 5% to its nominal value within 300 μ s (typical). This limits the in-rush current in the converter during start-up and prevents possible input voltage drops when a battery or high impedance power source is used. During soft start, the switch current limit is reduced to 300 mA until the output voltage reaches V_{IN} . Once the output voltage trips this threshold, the device operates with its nominal current limit.

7.4 Device Functional Modes

7.4.1 Power-Save Mode

The TPD5S115 integrates a power-save mode to improve efficiency at light loads. In power-save mode, the converter only operates when the output voltage trips below a set threshold voltage. It ramps up the output voltage with several pulses and goes into power-save mode once the output voltage exceeds the set threshold voltage. The PFM mode is ended and PWM mode begins in case the output current can no longer be supported in PFM mode.

7.4.2 Enable

The DC-DC converter is enabled when the EN is set to high. At first, the internal reference is activated and the internal analog circuits are settled. Afterwards, the soft start is activated and the output voltage is ramped up. The output voltage reaches its nominal value in 250 μ s (typical) after the device has been enabled. The EN input can be used to control power sequencing in a system with various DC-DC converters. The EN pin can be connected to the output of another converter to drive the EN pin high and create a sequencing of supply rails. When EN = GND, the converter enters shutdown mode.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

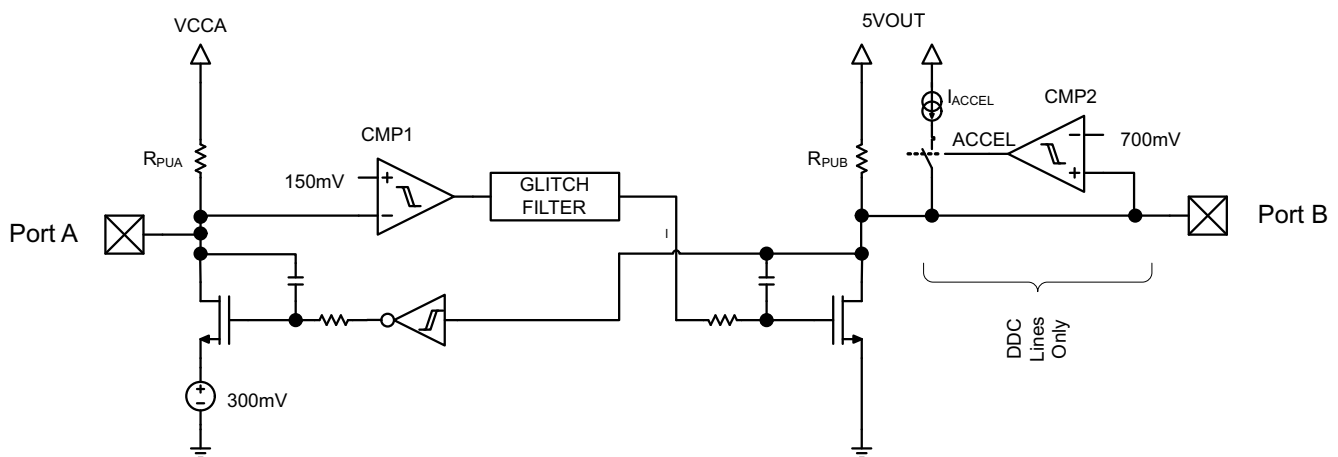
8.1 Application Information

The TPD5S115 is an integrated solution for HDMI 2.0, 1.3, and 1.4 interfaces. The device has a boost converter on the power supply, signal conditioning circuits on CEC, SCL, SDA, and HPD lines, and ESD protection on all the connector-facing lines.

8.2 Typical Applications

8.2.1 DDC or CEC Level Shifter

The TPD5S115 enables DDC translation from VCCA (system side) voltage levels to 5-V (HDMI cable side) voltage levels without degradation of system performance. The TPD5S115 contains 2 bidirectional, open-drain buffers specifically designed to support up and down-translation between the low voltage, VCCA side DDC-bus and the 5-V DDC-bus. The port B I/Os are overvoltage tolerant to 5.5 V, even when the device is shutdown. After power up and with the LS_OE and EN pins HIGH, a LOW level on port A (below $V_{ILC} = 0.08 \times V_{CCA}$) turns the corresponding port B driver (either SDA or SCL) on and drives port B down to V_{OLB} . When port A rises above approximately $0.10 \times V_{CCA}$, the port B pulldown driver is turned off and the internal pullup resistor pulls the pin HIGH. When port B falls first and goes below $0.3 \times V_{OUT}$, a CMOS hysteresis input buffer detects the falling edge, turns on the port A driver, and pulls port A down to approximately $V_{OLA} = 0.16 \times V_{CCA}$. The port B pulldown is not enabled unless the port A voltage goes below V_{ILC} . If the port A low voltage goes below V_{ILC} , the port B pulldown driver is enabled until port A rises above $(V_{ILC} + \Delta V_{T-HYSTA})$, then port B, if not externally driven LOW, continues to rise being pulled up by the internal pullup resistor.



Copyright © 2016, Texas Instruments Incorporated

Figure 13. DDC or CEC Level Shifter Block Diagram

Typical Applications (continued)

8.2.1.1 Design Requirements

For this design example, use the parameters listed in [Table 1](#) as the input parameters.

Table 1. Design Parameters

| PARAMETER | VALUE |
|--|------------------|
| 5VOUT DC current | 55 mA |
| CEC_A, HPD_A, SCL_A, SDA_A voltage level | V _{CCA} |
| HDMI 2.0 data rate per TMDS signal pair | 6 Gbps |
| Required IEC 61000-4-2 ESD Protection | ±8-kV contact |

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 DDC or CEC Level Shifter Operational Notes for V_{CCA} = 1.8 V

- The threshold of CMP1 is approximately 150 mV ± the 40 mV of total hysteresis
- The comparator trips for a falling waveform at approximately 130 mV
- The comparator trips for a rising waveform at approximately 170 mV
- To be recognized as a zero, the level at port A must first go below 130 mV (V_{ILC} in spec) and then stay below 170 mV (V_{ILA} in spec)
- To be recognized as a one, the level at A must first go above 170 mV and then stay above 130 mV
- V_{ILC} is specified as 110 mV in [Electrical Characteristics](#) to give some margin to the 130 mV
- V_{ILA} is specified as 140 mV in [Electrical Characteristics](#) to give some margin to the 170 mV
- V_{IHA} is specified as 70% of V_{CCA} to be consistent with standard CMOS levels

8.2.1.2.2 Input Capacitor

Due to the nature of the boost converter having a pulsating input current, a low-ESR input capacitor is required to prevent large voltage transients that can cause poor performance of the device or interference with other circuits in the system. TI recommends a 1.2-μF (minimum) input capacitor to improve transient behavior of the regulator and EMI behavior of the total power-supply circuit. TI recommends placing a ceramic capacitor (4.7 μF) as close as possible to the V_{IN} and GND pins to improve the input noise filtering.

8.2.1.2.3 Output Capacitor

TI recommends using a small ceramic capacitors placed as close as possible to the V_{OUT} and GND pins of the IC. If the application requires the use of large capacitors which can not be placed close to the IC, TI recommends using a smaller ceramic capacitor in parallel to the large capacitor. This small capacitor must be placed as close as possible to the V_{OUT} and GND pins of the IC. Use [Equation 1](#) to estimate the recommended minimum output capacitance.

$$C_{\min} = \frac{I_{\text{OUT}} \times (V_{\text{OUT}} - V_{\text{IN}})}{f \times \Delta V \times V_{\text{OUT}}}$$

where

- f is the switching frequency
 - ΔV is the maximum allowed ripple
- (1)

If a ripple voltage of 10 mV is chosen, a minimum effective capacitance of 2.7 μF is needed. The total ripple is larger due to the ESR of the output capacitor. This additional component of the ripple can be calculated using [Equation 2](#).

$$\Delta V_{\text{ESR}} = I_{\text{OUT}} \times R_{\text{ESR}}$$
(2)

To maintain control loop stability, a capacitor with a value in the range of the calculated minimum must be used. There are no additional requirements regarding minimum ESR. There is no upper limit for the output capacitance value. Larger capacitors cause lower output voltage ripple as well as lower output voltage drop during load transients.

Ceramic capacitors have a DC-bias effect, which has a strong influence on the final effective capacitance needed. Therefore the appropriate capacitor value must be chosen very carefully. Package size, voltage rating, and material are responsible for differences between the rated capacitor value and the effective capacitance. The minimum effective capacitance value is 1.2 μF , but the recommended value is 4.7 μF .

Table 2. Passive Components: Recommended Effective Values

| COMPONENT | MIN | TYP | MAX | UNIT |
|------------|-----|-----|-----|---------------|
| C_{IN} | 1.2 | 4.7 | 6.5 | μF |
| C_{OUT} | 1.2 | 4.7 | 10 | μF |
| L_{IN} | 0.7 | 1 | 1.3 | μH |
| C_{VCCA} | | 0.1 | | μF |

8.2.1.3 Application Curve

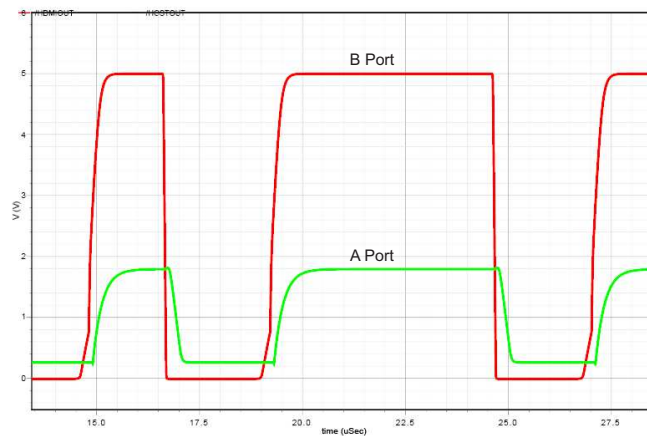
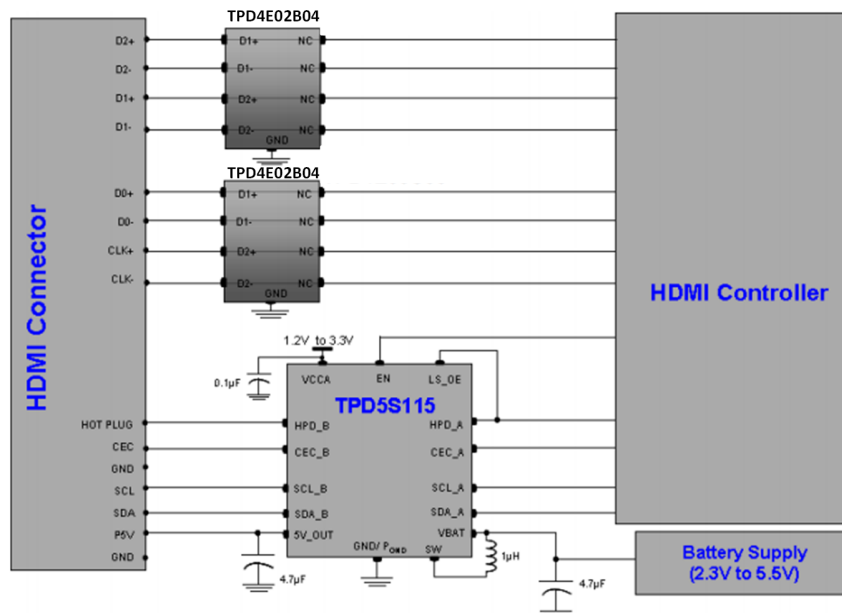


Figure 14. DDC Level Shifter Operation (B to A Direction)

8.2.2 Other Application Circuits

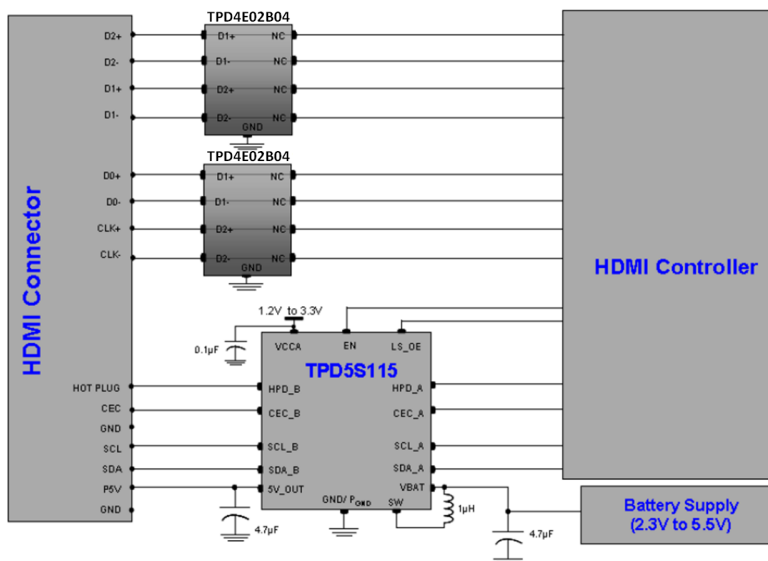
Figure 15 and Figure 16 show application examples using the TPD5S115 devices. Customers must fully validate and test any circuit before implementing a design based on an example in this section. Unless otherwise noted, the design procedures in *DDC or CEC Level Shifter* are applicable.



Copyright © 2016, Texas Instruments Incorporated

Figure 15. Application Schematic for HDMI Controllers With One GPIO for HDMI Interface Control

Some HDMI controllers may have only one GPIO to control the HDMI interface, thus, the HDMI driver chip controls the TPD5S115 through only one control line (EN). In this mode the HPD_A to LS_OE pins are connected to each other (see Figure 15).



Copyright © 2016, Texas Instruments Incorporated

Figure 16. Application Schematic for HDMI Controllers With Two GPIOs for HDMI Interface Control

Some HDMI driver chips may have two GPIOs to control the HDMI interface chip. In this case a flexible power saving mode can be implemented. The LS_OE and EN are active-high enable pins. They control the TPD5S115 power-saving options according to [Table 3](#) and [Table 4](#).

Table 3. Device Status – Part 1

| LS_OE | EN | V _{CCA} | V _{BAT} | 5VOUT | A-SIDE PULLUPS | DCC, B-SIDE PULLUPS | CEC, B-SIDE PULLUPS |
|-------|----|------------------|------------------|--------|----------------|---------------------|---------------------|
| L | L | 1.8 V | 5 V | Off | Off | Off | Off |
| L | H | 1.8 V | 5 V | On | On | On | Off |
| H | L | 1.8 V | 5 V | Off | Off | Off | Off |
| H | H | 1.8 V | 5 V | On | On | On | On |
| X | X | 0 V | 0 V | High-Z | High-Z | High-Z | High-Z |
| X | X | 1.8 V | 0 V | Low | Low | High-Z | High-Z |
| X | X | 0 V | 5 V | High-Z | High-Z | High-Z | High-Z |

Table 4. Device Status – Part 2

| LS_OE | EN | CEC LDO | DC-DC AND HPD | DDC OR CEC VLTS | I _{CCA} TYP | I _{CC} V _{BAT} TYP | COMMENT |
|-------|----|---------|---------------|-----------------|----------------------|--------------------------------------|------------------|
| L | L | Off | Off | OFF and High-Z | 1 μA | 1 μA | Fully disabled |
| L | H | Off | On | OFF and High-Z | 1 μA | 30 μA | DC-DC (30 μA) ON |
| H | L | Off | Off | OFF and High-Z | 1 μA | 1 μA | Not valid state |
| H | H | On | On | ON | 13 μA | 225 μA | Fully ON |
| X | X | Off | Off | High-Z | 0 μA | 0 μA | Power down |
| X | X | Off | Off | High-Z | 0 μA | 0 μA | Power down |
| X | X | Off | Off | High-Z | 0 μA | 0 μA | Power down |

9 Power Supply Recommendations

To keep the normal function of TPD5S115, the designer needs to make sure that both V_{BAT} and V_{CCA} are within the recommended operating range. See [Detailed Design Procedure](#) for power supply recommendations.

10 Layout

10.1 Layout Guidelines

For proper operation, follow these layout and design guidelines:

- Place the TPD5S115 as close to the connector as possible. This allows it to remove the energy associated with ESD strike before it reaches the internal circuitry of the system board.
- Place power line capacitors and inductors close to the pins with wide traces to allow enough current to flow through with less trace parasitics. Ensure that there is enough metallization for the GND pad. A sufficient current path enables safe discharge of all the energy associated with the ESD strike.

10.2 Layout Example

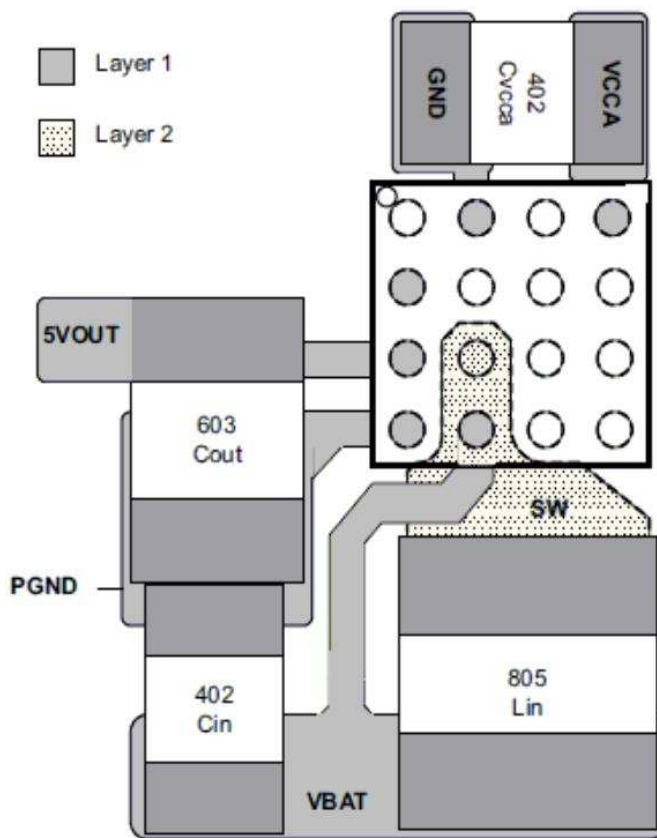


Figure 17. Board Layout With DC-DC Components (Top View)

11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary


[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|---|
| TPD5S115YFFR | ACTIVE | DSBGA | YFF | 16 | 3000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | RE115 |  |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

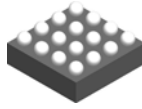
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

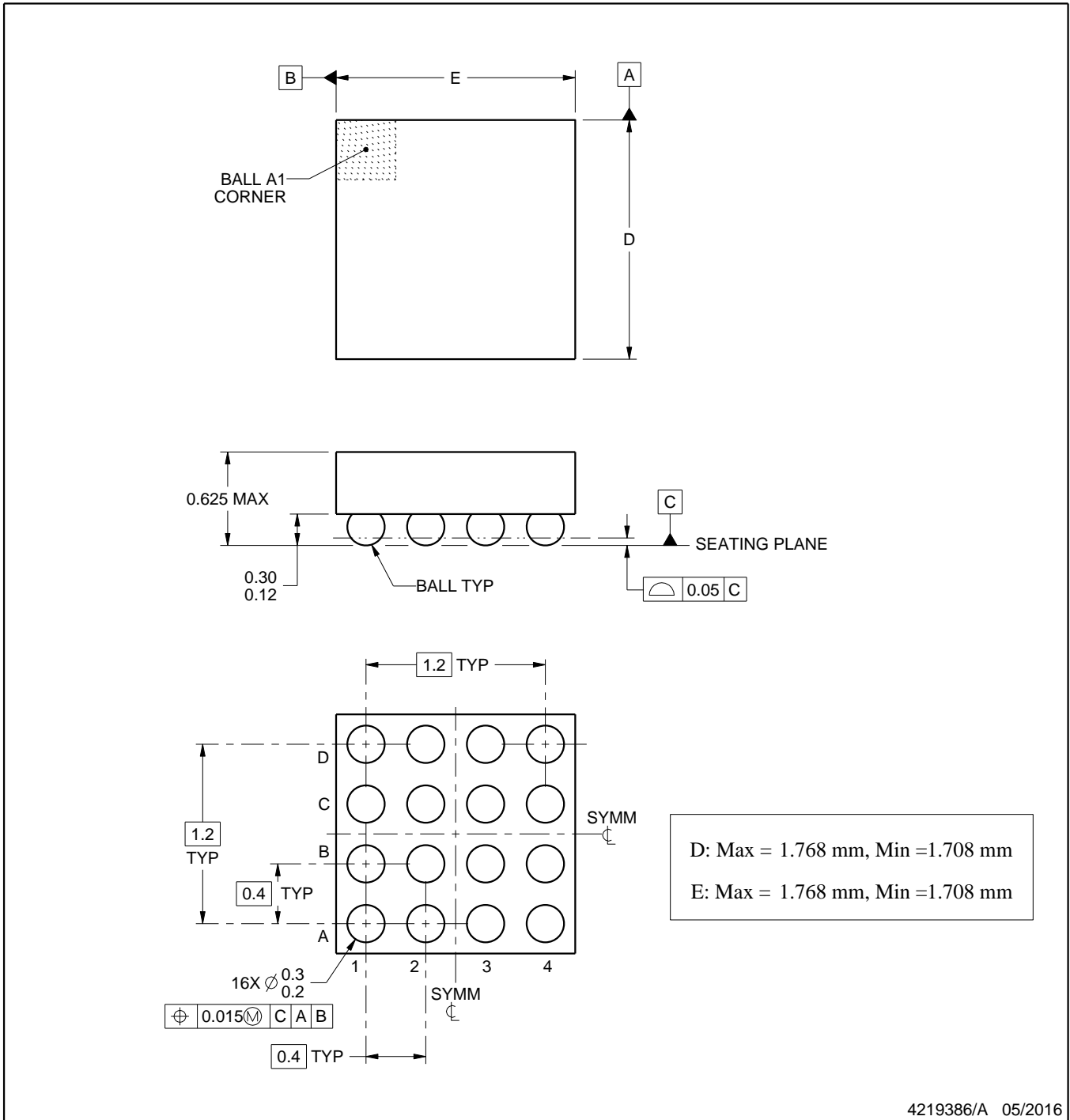
YFF0016



PACKAGE OUTLINE

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



NOTES:

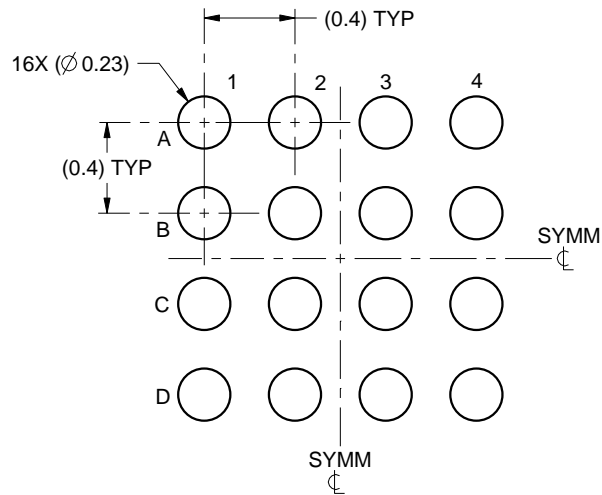
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

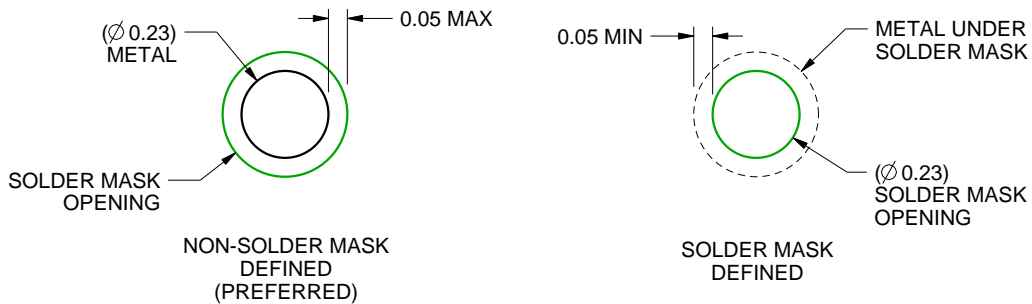
YFF0016

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
SCALE:30X



SOLDER MASK DETAILS
NOT TO SCALE

4219386/A 05/2016

NOTES: (continued)

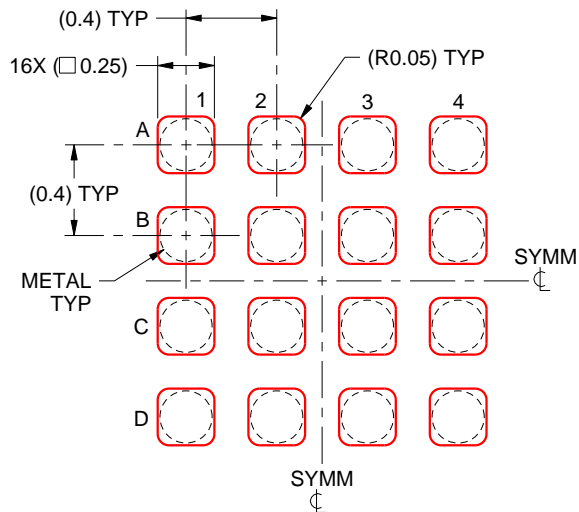
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YFF0016

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4219386/A 05/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.