TPS22975 5.7-V, 6-A, 16-mΩ On-Resistance Load Switch

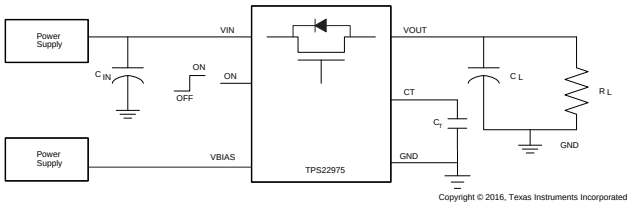
1 Features

- Integrated Single-Channel Load Switch
- Input Voltage Range: 0.6 V to V_{BIAS}
- V_{BIAS} Voltage Range: 2.5 V to 5.7 V
- On-Resistance (R_{ON})
  - R_{ON} = 16 mΩ (typical) at VIN = 0.6 V to 5.7 V, V_{BIAS} = 5.7 V
- 6-A Maximum Continuous Switch Current
- Low Quiescent Current
  - 37 µA (typical) at V_{IN} = V_{BIAS} = 5 V
- Low-Control Input-Threshold Enables Use of 1.2-, 1.8-, 2.5-, and 3.3-V Logic
- Configurable Rise Time
- Thermal Shutdown
- Quick-Output Discharge (QOD) (Optional)
- SON 8-pin Package with Thermal Pad
- ESD Performance Tested per JESD 22
  - 2000-V HBM and 1000-V CDM

2 Applications

- Ultrabook™
- Notebooks and Netbooks
- Tablet PC
- Consumer Electronics
- Set-top Boxes and Residential Gateways
- Telecom Systems
- Solid State Drives (SSDs)

Simplified Schematic



3 Description

The TPS22975 product family consists of two devices: TPS22975 and TPS22975N. Each device is a single-channel load switch that provides a configurable rise time to minimize inrush current. The device contains an N-channel MOSFET that can operate over an input voltage range of 0.6 V to 5.7 V and can support a maximum continuous current of 6 A. The switch is controlled by an on and off input (ON), which is capable of interfacing directly with low-voltage control signals. TPS22975 has an optional 230-Ω on-chip load resistor for quick output discharge when switch is turned off.

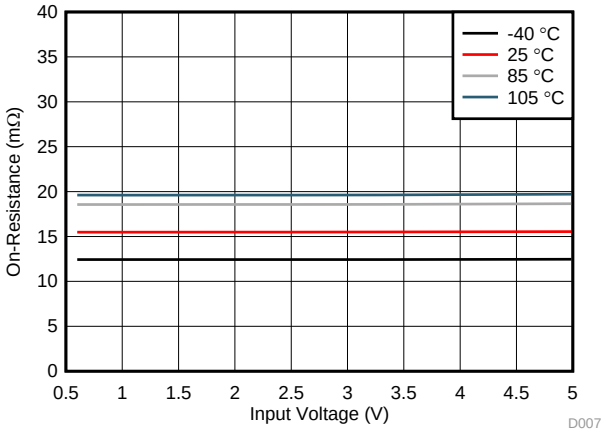
The TPS22975 is available in a small, space-saving 2-mm × 2-mm 8-pin SON package (DSG) with integrated thermal pad allowing for high power dissipation. The device is characterized for operation over the free-air temperature range of –40°C to +105°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS22975 TPS22975N	WSON (8)	2.00 mm × 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

On-Resistance vs Input Voltage



V_{BIAS} = 5 V, I_{VOUT} = –200 mA

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4 Revision History

Changes from Original (May 2016) to Revision A **Page**

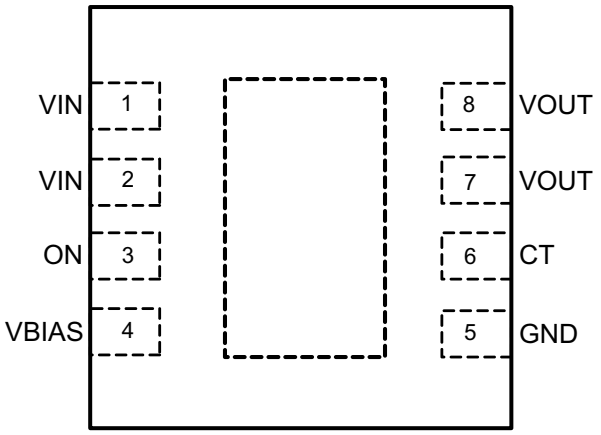
- Changed device status from *Product Preview* to *Production Data* ... 1

5 Device Comparison Table

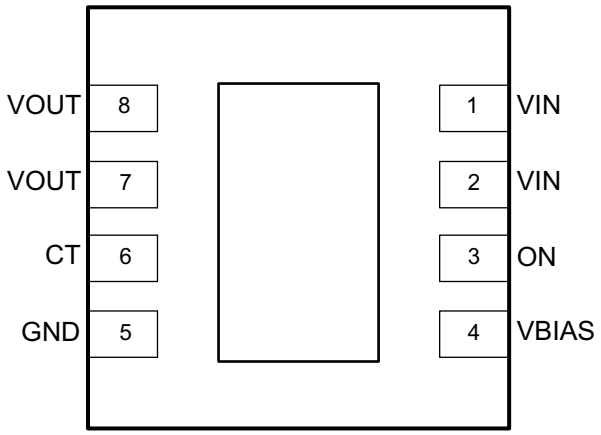
DEVICE	R_{ON} AT V_{IN} = V_{BIAS} = 5 V (TYPICAL)	QUICK-OUTPUT DISCHARGE	MAXIMUM OUTPUT CURRENT	ENABLE
TPS22975	16 mΩ	Yes	6 A	Active high
TPS22975N	16 mΩ	No	6 A	Active high

6 Pin Configuration and Functions

DSG Package
8-Pin (WSON)
Top View



DSG Package
8-Pin (WSON)
Bottom View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	VIN	I	Switch input. Input bypass capacitor recommended for minimizing V_{IN} dip. Must be connected to Pin 1 and Pin 2. See the *Application and Implementation* section for more information
2			
3	ON	I	Active high switch control input. Do not leave floating
4	VBIAS	I	Bias voltage. Power supply to the device. Recommended voltage range for this pin is 2.5 V to 5.7 V. See the *Application and Implementation* section for more information
5	GND	—	Device ground
6	CT	O	Switch slew rate control. Can be left floating. See the *Adjustable Rise Time* section under *Feature Description* for more information
7	VOUT	O	Switch output
8			
—	Thermal Pad	—	Thermal pad (exposed center pad) to alleviate thermal stress. Tie to GND. See the *Layout Example* section for layout guidelines

7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{IN}	Input voltage	–0.3	6	V
V_{OUT}	Output voltage	–0.3	6	V
V_{BIAS}	Bias voltage	–0.3	6	V
V_{ON}	On voltage	–0.3	6	V
I_{MAX}	Maximum continuous switch current		6	A
I_{PLS}	Maximum pulsed switch current, pulse < 300 µs, 2% duty cycle		8	A
T_J	Maximum junction temperature		125	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

			MIN	MAX	UNIT
V_{IN}	Input voltage		0.6	V_{BIAS}	V
V_{BIAS}	Bias voltage		2.5	5.7	V
V_{ON}	ON voltage		0	5.7	V
V_{OUT}	Output voltage			V_{IN}	V
V_{IH}	High-level input voltage, ON	V_{BIAS} = 2.5 V to 5 V	1.1	5.7	V
		V_{BIAS} = 5 V to 5.7 V	1.2	5.7	V
V_{IL}	Low-level input voltage, ON	V_{BIAS} = 2.5 V to 5.7 V	0	0.5	V
C_{IN}	Input capacitor		1(1)		µF
T_A	Operating free-air temperature(1)(2)		–40	105	°C

(1) See the *Application Information* section.
(2) In applications where high power dissipation and-or poor package thermal resistance is present, the maximum ambient temperature may have to be derated and device lifetime may be affected. Maximum ambient temperature ($T_{A(max)}$) is dependent on the maximum operating junction temperature ($T_{J(max)}$), the maximum power dissipation of the device in the application ($P_{D(max)}$), and the junction-to-ambient thermal resistance of the part-package in the application (θ_{JA}), and can be approximated by the following equation: $T_{A\ (max)} = T_{J(max)} – (\theta_{JA} \times P_{D(max)})$.

7.4 Thermal Information

THERMAL METRIC(1)		TPS22975 DSG (WSON) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	74.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	81	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	44.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	45.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	16.4	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Electrical Characteristics—V_{BIAS} = 5 V

Unless otherwise noted, the specifications in the following table applies where V_{BIAS} = 5 V. Typical values are for T_A = 25 °C.

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
POWER SUPPLIES AND CURRENTS								
$I_{Q, VBIAS}$	V_{BIAS} quiescent current	I_{OUT} = 0 A, V_{IN} = V_{ON} = 5 V		–40°C to +105°C		37	45	µA
$I_{SD, VBIAS}$	V_{BIAS} shutdown current	V_{ON} = V_{OUT} = 0 V		–40°C to +105°C			2.3	µA
$I_{SD, VIN}$	V_{IN} off-state supply current	V_{ON} = V_{OUT} = 0 V	V_{IN} = 5 V	–40°C to +85°C		0.005	5	µA
				–40°C to +105°C			10	
			V_{IN} = 3.3 V	–40°C to +85°C		0.002	1.5	
				–40°C to +105°C			3.5	
			V_{IN} = 1.8 V	–40°C to +85°C		0.002	1	
				–40°C to +105°C			2	
			V_{IN} = 0.6 V	–40°C to +85°C		0.001	0.5	
				–40°C to +105°C			1	
I_{ON}	On-pin input leakage current	V_{ON} = 5.5 V		–40°C to +105°C			0.1	µA
RESISTANCE CHARACTERISTICS								
R_{ON}	On-resistance	I_{OUT} = –200 mA	V_{IN} = 5 V	25°C		16	19	mΩ
				–40°C to +85°C			23	
				–40°C to +105°C			25	
			V_{IN} = 3.3 V	25°C		16	19	
				–40°C to +85°C			23	
				–40°C to +105°C			25	
			V_{IN} = 1.8 V	25°C		16	19	
				–40°C to +85°C			23	
				–40°C to +105°C			25	
			V_{IN} = 1.5 V	25°C		16	19	
				–40°C to +85°C			23	
				–40°C to +105°C			25	
			V_{IN} = 1.05 V	25°C		16	19	
				–40°C to +85°C			23	
				–40°C to +105°C			25	
			V_{IN} = 0.6 V	25°C		16	19	
				–40°C to +85°C			23	
				–40°C to +105°C			25	
$V_{ON, HYS}$	On-pin hysteresis	V_{IN} = 5 V		25°C		120		mV
R_{PD} (1)	Output pulldown resistance	V_{IN} = 5 V, V_{ON} = 0 V		–40°C to +105°C		230	300	Ω
T_{SD}	Thermal shutdown	Junction temperature rising				160		°C
$T_{SD, HYS}$	Thermal shutdown hysteresis	Junction temperature falling				20		°C

(1) TPS22975 only

7.6 Electrical Characteristics—V_{BIAS} = 2.5 V

Unless otherwise noted, the specifications in the following table applies where V_{BIAS} = 2.5 V. Typical values are for T_A = 25 °C.

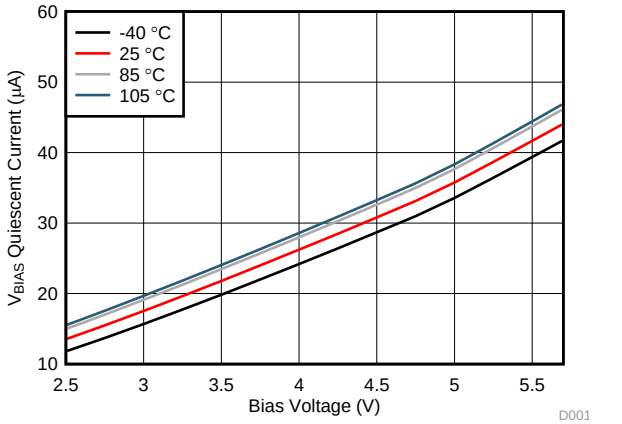
PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
POWER SUPPLIES AND CURRENTS								
$I_{Q, VBIAS}$	V_{BIAS} quiescent current	I_{OUT} = 0 mA, V_{IN} = V_{ON} = 2.5 V		–40°C to +105°C		14	20	µA
$I_{SD, VBIAS}$	V_{BIAS} shutdown current	V_{ON} = V_{OUT} = 0 V		–40°C to +105°C			1	µA
$I_{SD, VIN}$	V_{IN} off-state supply current	V_{ON} = V_{OUT} = 0 V	V_{IN} = 2.5 V	–40°C to +85°C		0.005	1.3	µA
				–40°C to +105°C			2.6	
			V_{IN} = 1.8 V	–40°C to +85°C		0.002	1	
				–40°C to +105°C			2	
			V_{IN} = 1.05 V	–40°C to +85°C		0.002	0.8	
				–40°C to +105°C			1.5	
			V_{IN} = 0.6 V	–40°C to +85°C		0.001	0.5	
				–40°C to +105°C			1	
I_{ON}	On-pin input leakage current	V_{ON} = 5.5 V		–40°C to +105°C			0.1	µA
RESISTANCE CHARACTERISTICS								
R_{ON}	On-resistance	I_{OUT} = –200 mA	V_{IN} = 2.5 V	25°C		20	26	mΩ
				–40°C to +85°C			32	
				–40°C to +105°C			34	
			V_{IN} = 1.8 V	25°C		18	23	
				–40°C to +85°C			29	
				–40°C to +105°C			31	
			V_{IN} = 1.5 V	25°C		18	22	
				–40°C to +85°C			28	
				–40°C to +105°C			30	
			V_{IN} = 1.2 V	25°C		17	22	
				–40°C to +85°C			27	
				–40°C to +105°C			29	
			V_{IN} = 0.6 V	25°C		17	21	
				–40°C to +85°C			26	
				–40°C to +105°C			27	
$V_{ON, HYS}$	On-pin hysteresis	V_{IN} = 2.5 V		25°C		85		mV
R_{PD} (1)	Output pulldown resistance	V_{IN} = 2.5 V, V_{ON} = 0 V		–40°C to +105°C		230	330	Ω
T_{SD}	Thermal shutdown	Junction temperature rising				160		°C
$T_{SD, HYS}$	Thermal shutdown hysteresis	Junction temperature falling				20		°C

(1) TPS22975 only

7.7 Switching Characteristics

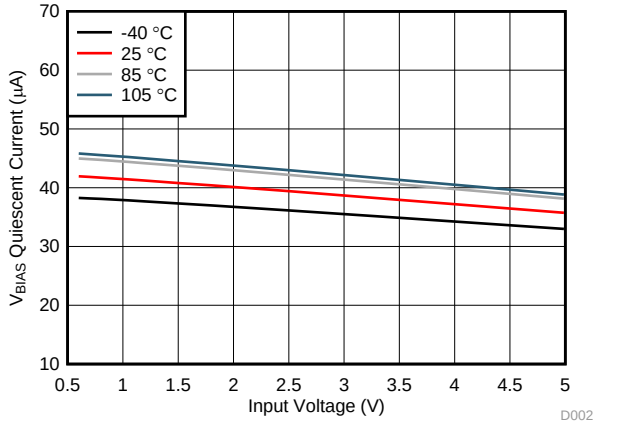
PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{IN} = V_{BIAS} = 5 V, T_A = 25ºC (unless otherwise noted)						
t_{ON}	Turnon time	R_L = 10 Ω, C_L = 0.1 µF, C_{IN} = 1 µF, C_T = 1000 pF, V_{ON} = 5 V		1450		µs
t_{OFF}	Turnoff time	R_L = 10 Ω, C_L = 0.1 µF, C_{IN} = 1 µF, C_T = 1000 pF, V_{ON} = 5 V		2		
t_R	V_{OUT} rise time	R_L = 10 Ω, C_L = 0.1 µF, C_{IN} = 1 µF, C_T = 1000 pF, V_{ON} = 5 V		1750		
t_F	V_{OUT} fall time	R_L = 10 Ω, C_L = 0.1 µF, C_{IN} = 1 µF, C_T = 1000 pF, V_{ON} = 5 V		2		
t_D	ON delay time	R_L = 10 Ω, C_L = 0.1 µF, C_{IN} = 1 µF, C_T = 1000 pF, V_{ON} = 5 V		600		
V_{IN} = 0.6 V, V_{BIAS} = 5 V, T_A = 25ºC (unless otherwise noted)						
t_{ON}	Turnon time	R_L = 10 Ω, C_L = 0.1 µF, C_{IN} = 1 µF, C_T = 1000 pF, V_{ON} = 5 V		620		µs
t_{OFF}	Turnoff time	R_L = 10 Ω, C_L = 0.1 µF, C_{IN} = 1 µF, C_T = 1000 pF, V_{ON} = 5 V		2		
t_R	V_{OUT} rise time	R_L = 10 Ω, C_L = 0.1 µF, C_{IN} = 1 µF, C_T = 1000 pF, V_{ON} = 5 V		280		
t_F	V_{OUT} fall time	R_L = 10 Ω, C_L = 0.1 µF, C_{IN} = 1 µF, C_T = 1000 pF, V_{ON} = 5 V		2		
t_D	ON delay time	R_L = 10 Ω, C_L = 0.1 µF, C_{IN} = 1 µF, C_T = 1000 pF, V_{ON} = 5 V		485		
V_{IN} = V_{BIAS} = 2.5 V, T_A = 25ºC (unless otherwise noted)						
t_{ON}	Turnon time	R_L = 10 Ω, C_L = 0.1 µF, C_{IN} = 1 µF, C_T = 1000 pF, V_{ON} = 5 V		2180		µs
t_{OFF}	Turnoff time	R_L = 10 Ω, C_L = 0.1 µF, C_{IN} = 1 µF, C_T = 1000 pF, V_{ON} = 5 V		2		
t_R	V_{OUT} rise time	R_L = 10 Ω, C_L = 0.1 µF, C_{IN} = 1 µF, C_T = 1000 pF, V_{ON} = 5 V		2150		
t_F	V_{OUT} fall time	R_L = 10 Ω, C_L = 0.1 µF, C_{IN} = 1 µF, C_T = 1000 pF, V_{ON} = 5 V		2		
t_D	ON delay time	R_L = 10 Ω, C_L = 0.1 µF, C_{IN} = 1 µF, C_T = 1000 pF, V_{ON} = 5 V		1120		
V_{IN} = 0.6 V, V_{BIAS} = 2.5 V, T_A = 25ºC (unless otherwise noted)						
t_{ON}	Turnon time	R_L = 10 Ω, C_L = 0.1 µF, C_{IN} = 1 µF, C_T = 1000 pF, V_{ON} = 5 V		1315		µs
t_{OFF}	Turnoff time	R_L = 10 Ω, C_L = 0.1 µF, C_{IN} = 1 µF, C_T = 1000 pF, V_{ON} = 5 V		3		
t_R	V_{OUT} rise time	R_L = 10 Ω, C_L = 0.1 µF, C_{IN} = 1 µF, C_T = 1000 pF, V_{ON} = 5 V		650		
t_F	V_{OUT} fall time	R_L = 10 Ω, C_L = 0.1 µF, C_{IN} = 1 µF, C_T = 1000 pF, V_{ON} = 5 V		2		
t_D	ON delay time	R_L = 10 Ω, C_L = 0.1 µF, C_{IN} = 1 µF, C_T = 1000 pF, V_{ON} = 5 V		975		

7.8 Typical DC Characteristics



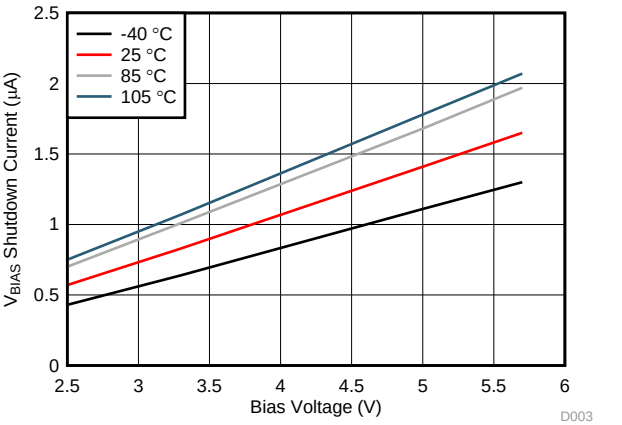
$V_{IN} = V_{BIAS}$ $V_{ON} = 5$ V $V_{OUT} = 0$ V

Figure 1. V_{BIAS} Quiescent Current vs Bias Voltage



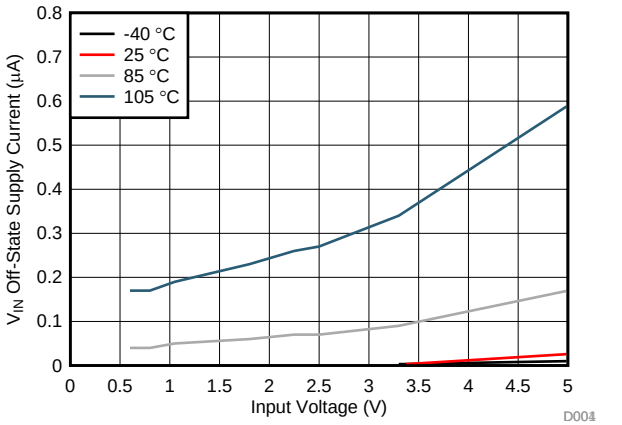
$V_{BIAS} = 5$ V $V_{ON} = 5$ V $V_{OUT} = 0$ V

Figure 2. V_{BIAS} Quiescent Current vs Input Voltage



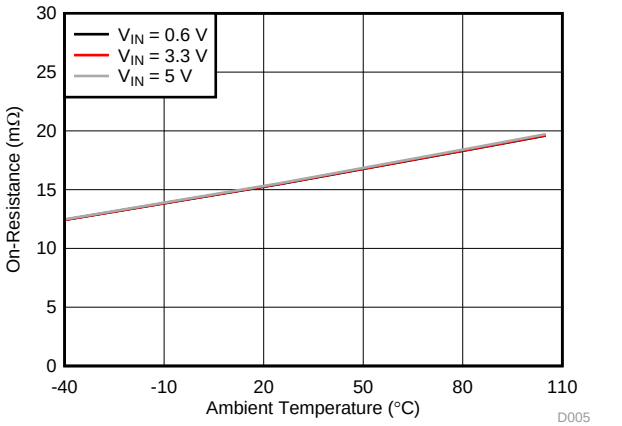
$V_{IN} = V_{BIAS}$ $V_{ON} = 0$ V $V_{OUT} = 0$ V

Figure 3. V_{BIAS} Shutdown Current vs Bias Voltage



$V_{BIAS} = 5$ V $V_{ON} = 0$ V $V_{OUT} = 0$ V

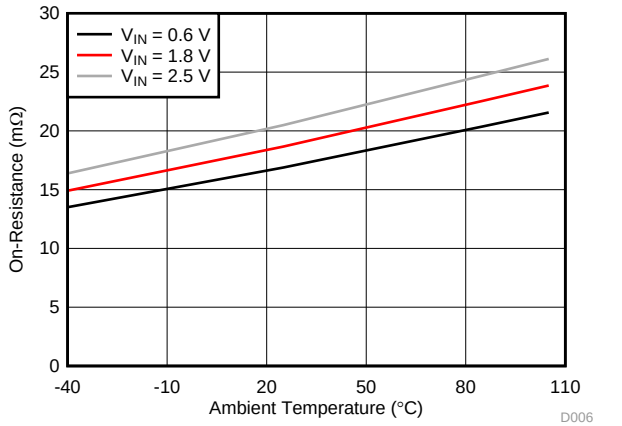
Figure 4. V_{IN} Off-State Supply Current vs Input Voltage



$V_{BIAS} = 5$ V $I_{OUT} = -200$ mA $V_{ON} = 5$ V

Note: All three R_{ON} curves have the same values; therefore, only one line is visible.

Figure 5. On-Resistance vs Ambient Temperature



$V_{BIAS} = 2.5$ V $I_{OUT} = -200$ mA $V_{ON} = 5$ V

Figure 6. On-Resistance vs Ambient Temperature

Typical DC Characteristics (continued)

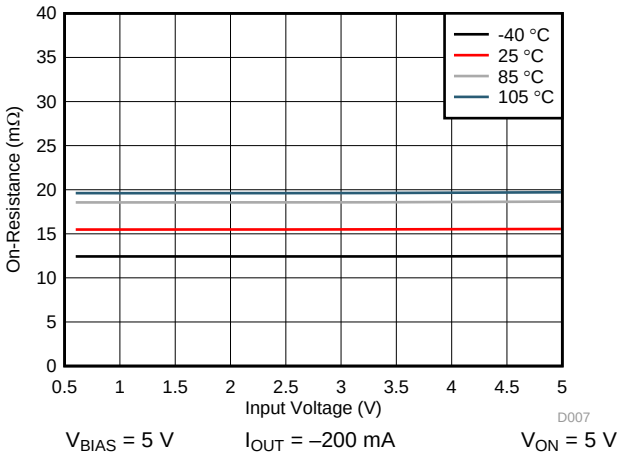


Figure 7. On-Resistance vs Input Voltage

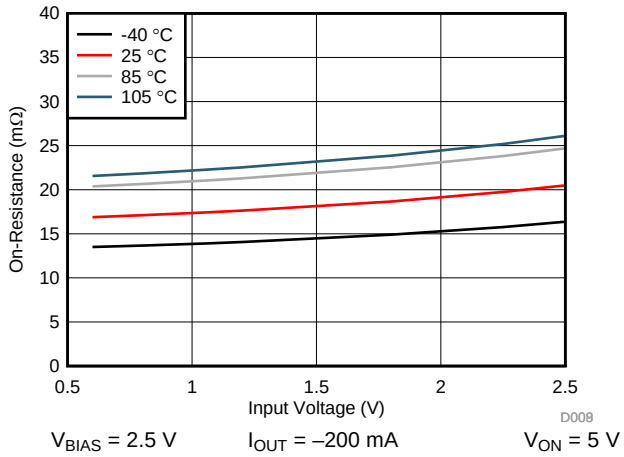


Figure 8. On-Resistance vs Input Voltage

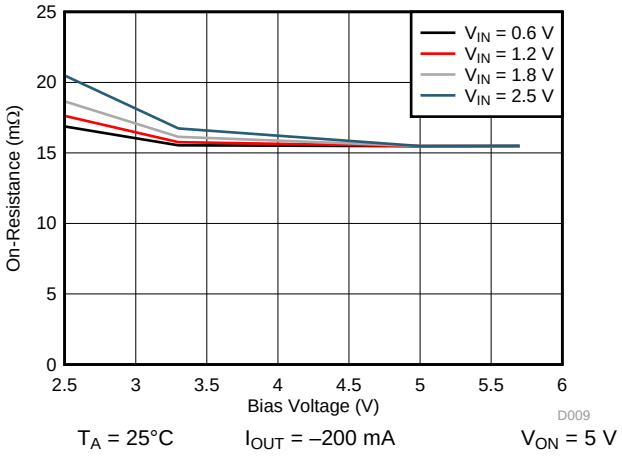


Figure 9. On-Resistance vs Bias Voltage

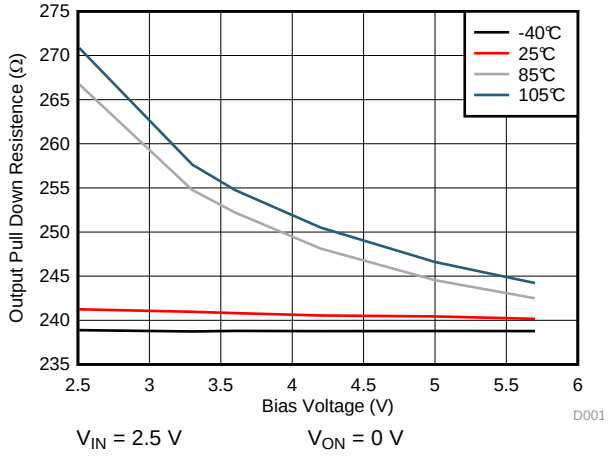


Figure 10. Output Pull Down Resistance vs Bias Voltage

7.9 Typical AC Characteristics

T_A = 25°C, C_T = 1000 pF, C_{IN} = 1 µF, C_L = 0.1 µF, R_L = 10 Ω

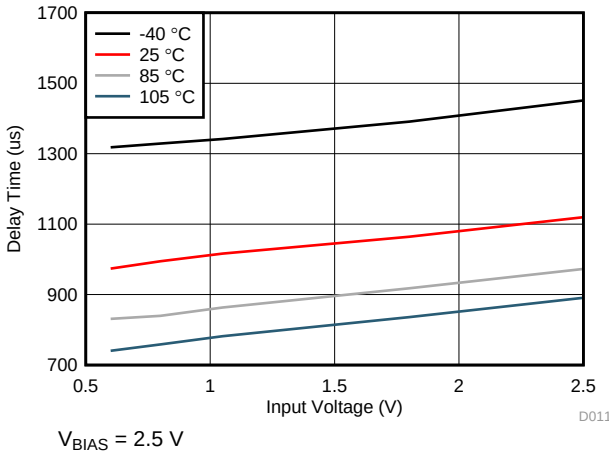


Figure 11. Delay Time vs Input Voltage

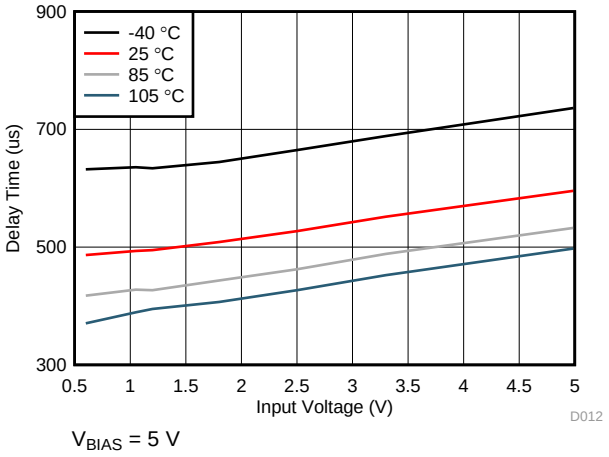


Figure 12. Delay Time vs Input Voltage

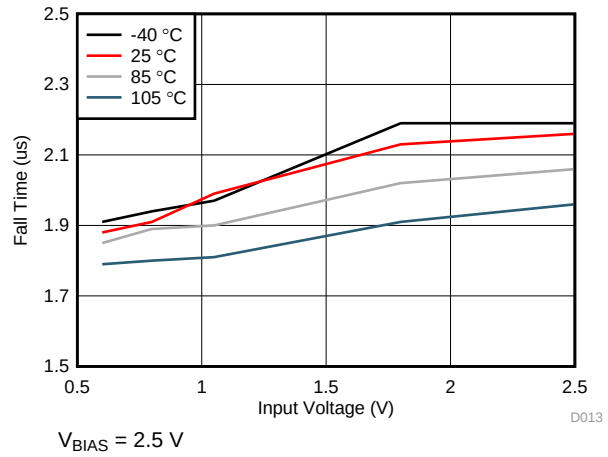


Figure 13. Fall Time vs Input Voltage

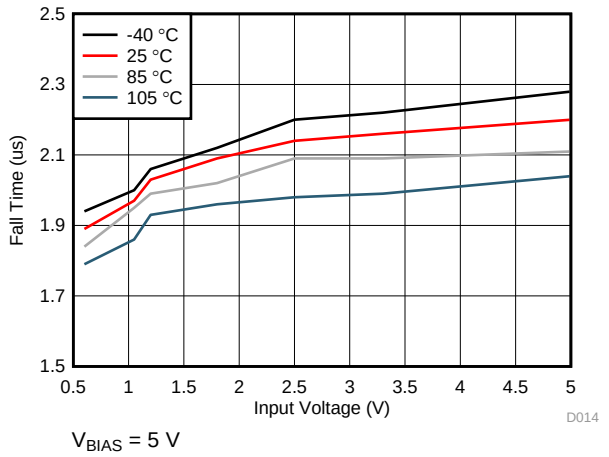


Figure 14. Fall Time vs Input Voltage

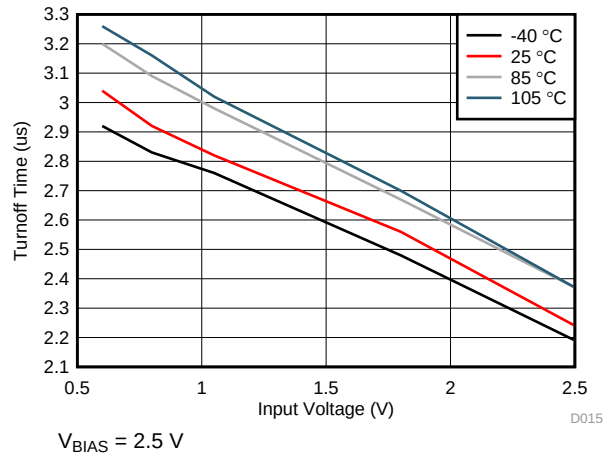


Figure 15. Turnoff Time vs Input Voltage

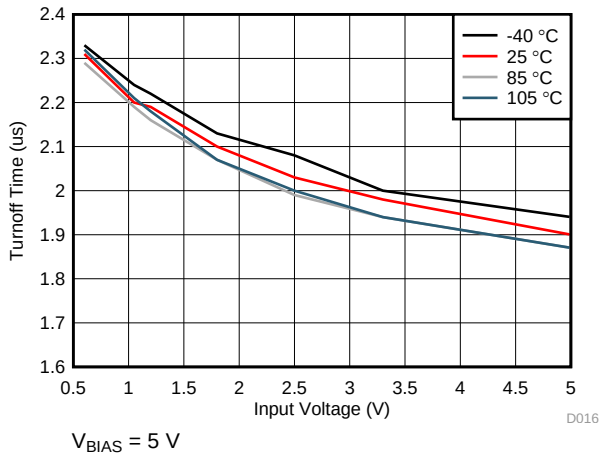
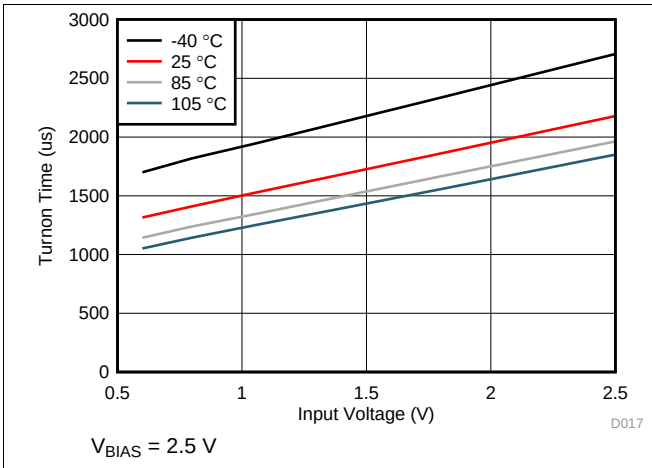


Figure 16. Turnoff Time vs Input Voltage

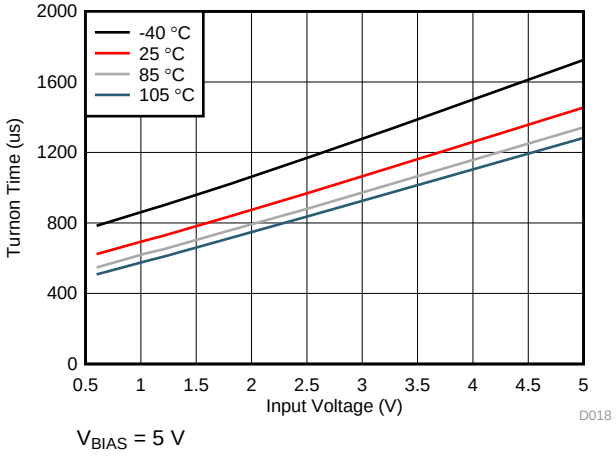
Typical AC Characteristics (continued)

T_A = 25°C, C_T = 1000 pF, C_{IN} = 1 µF, C_L = 0.1 µF, R_L = 10 Ω



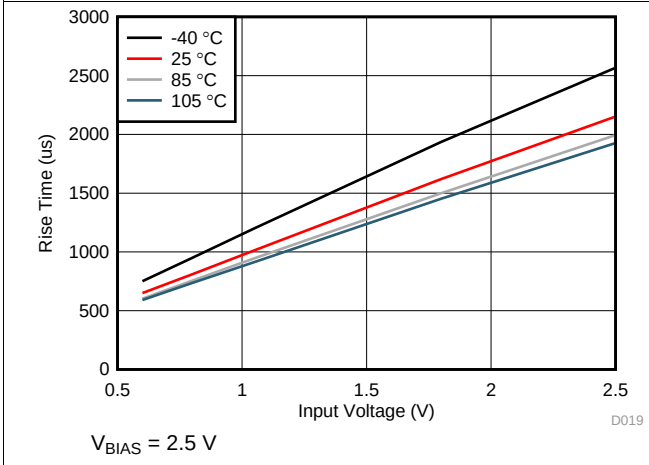
V_{BIAS} = 2.5 V

Figure 17. Turnon Time vs Input Voltage



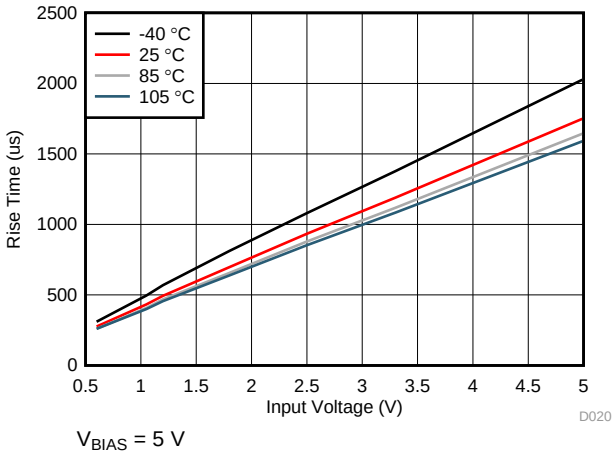
V_{BIAS} = 5 V

Figure 18. Turnon Time vs Input Voltage



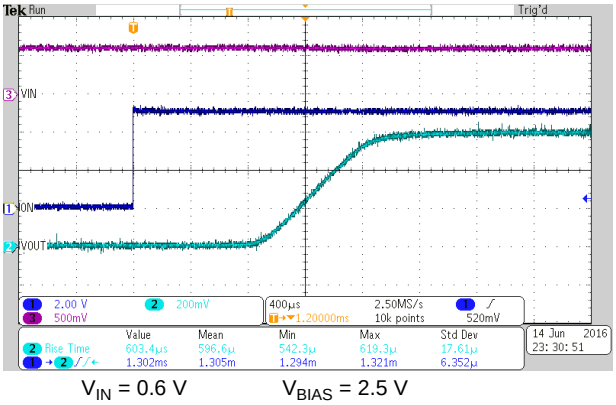
V_{BIAS} = 2.5 V

Figure 19. Rise Time vs Input Voltage



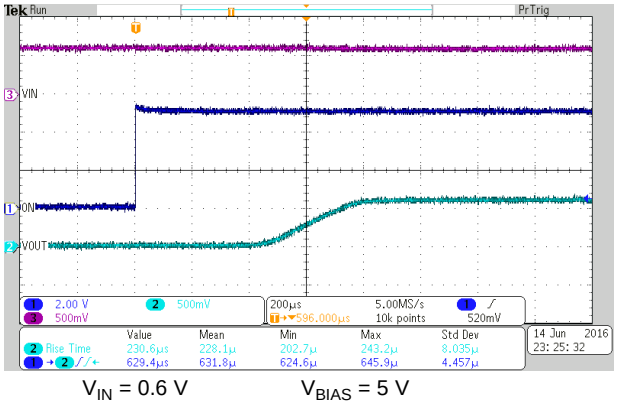
V_{BIAS} = 5 V

Figure 20. Rise Time vs Input Voltage



V_{IN} = 0.6 V V_{BIAS} = 2.5 V

Figure 21. Turnon Response Time

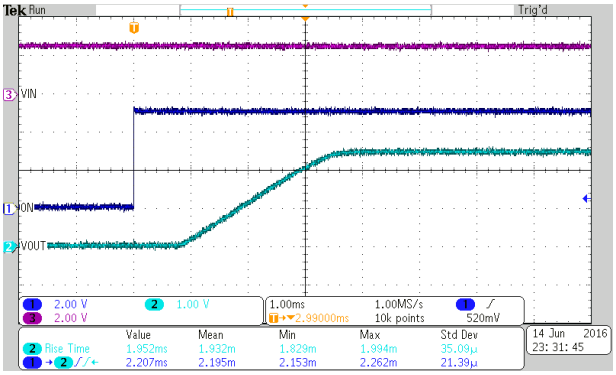


V_{IN} = 0.6 V V_{BIAS} = 5 V

Figure 22. Turnon Response Time

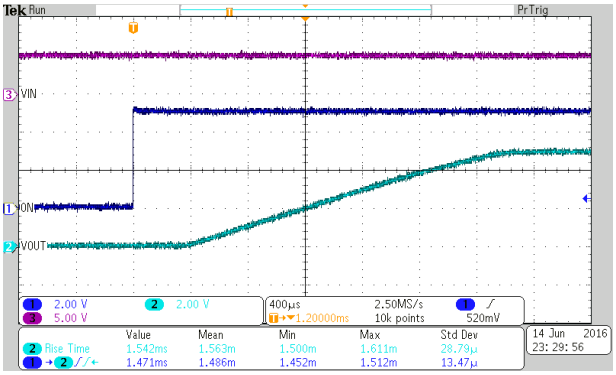
Typical AC Characteristics (continued)

T_A = 25°C, C_T = 1000 pF, C_{IN} = 1 µF, C_L = 0.1 µF, R_L = 10 Ω



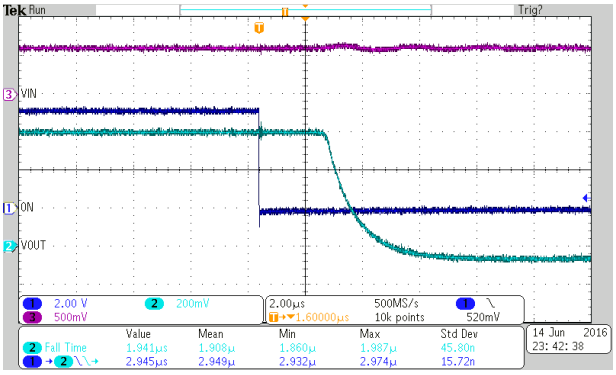
V_{IN} = 2.5 V V_{BIAS} = 2.5 V

Figure 23. Turnon Response Time



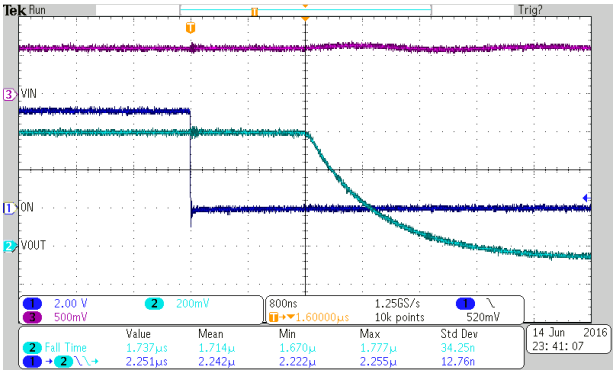
V_{IN} = 5 V V_{BIAS} = 5 V

Figure 24. Turnon Response Time



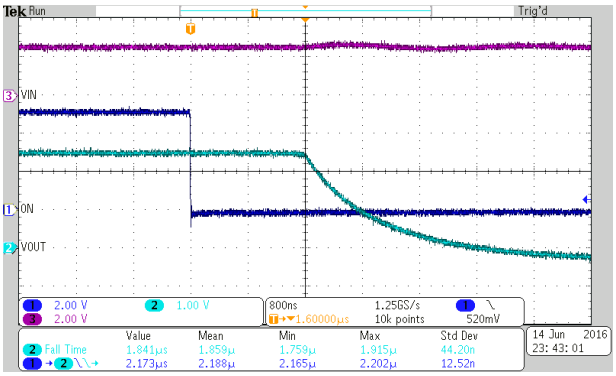
V_{IN} = 0.6 V V_{BIAS} = 2.5 V

Figure 25. Turnoff Response Time



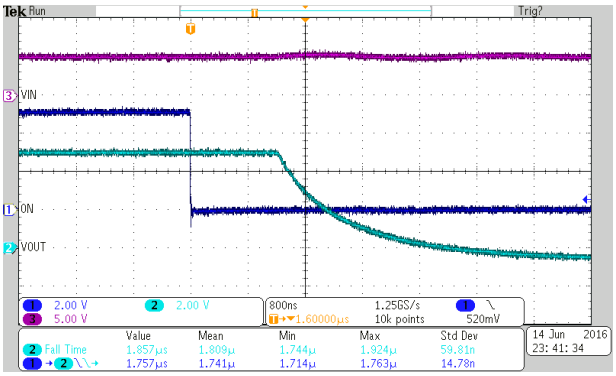
V_{IN} = 0.6 V V_{BIAS} = 5 V

Figure 26. Turnoff Response Time



V_{IN} = 2.5 V V_{BIAS} = 2.5 V

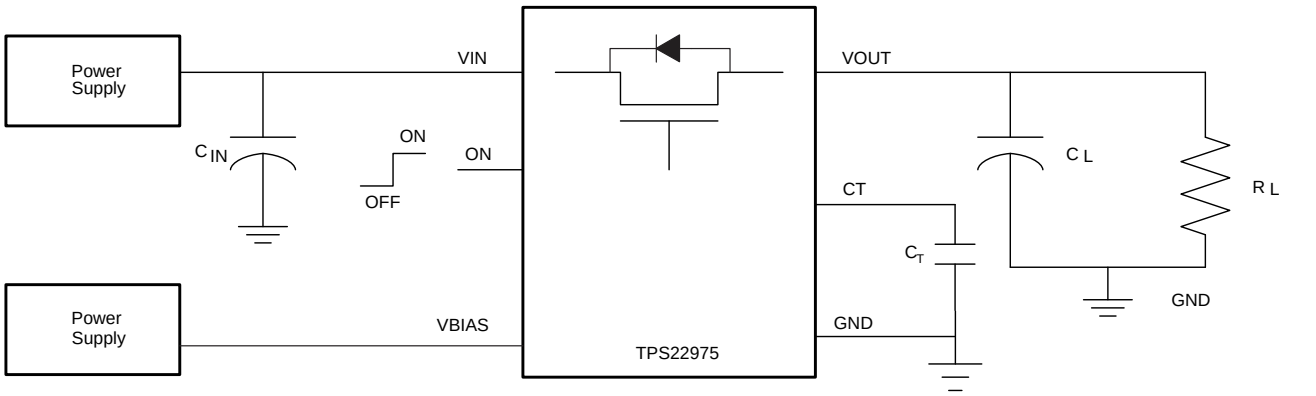
Figure 27. Turnoff Response Time



V_{IN} = 5 V V_{BIAS} = 5 V

Figure 28. Turnoff Response Time

8 Parameter Measurement Information



A. Rise and fall times of the control signal are 100 ns.

B. Turnoff times and fall times are dependent on the time constant at the load. For the TPS22975, the internal pull-down resistance R_{PD} is enabled when the switch is disabled. The time constant is (R_{PD} || R_L) × C_L.

Figure 29. Test Circuit

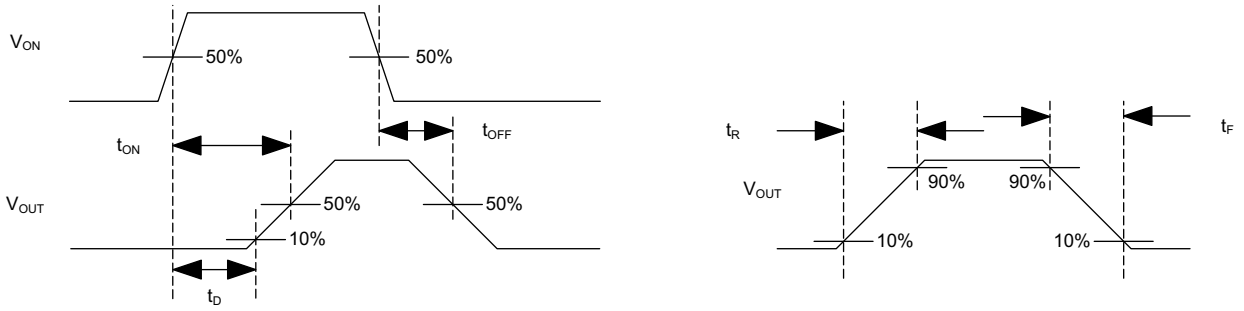


Figure 30. t_{ON} and t_{OFF} Waveforms

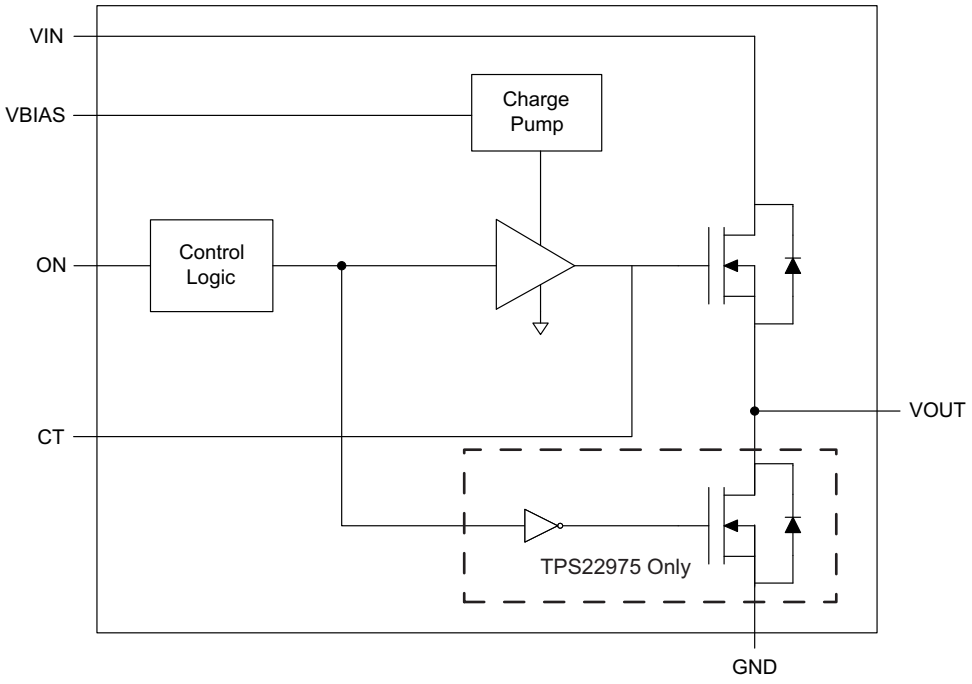
9 Detailed Description

9.1 Overview

The TPS22975 device is a single-channel, 6-A load switch in an 8-pin SON package. To reduce the voltage drop in high current rails, the device implements an N-channel MOSFET. The device has a configurable slew rate for applications that require a specific rise-time.

The device prevents downstream circuits from pulling high standby current from the supply by limiting the leakage current of the device when it is disabled. The integrated control logic, driver, power supply, and output discharge FET eliminates the need for any external components, which reduces solution size and bill of materials (BOM) count.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Adjustable Rise Time

A capacitor to GND on the CT pin sets the slew rate. The voltage on the CT pin can be as high as 15 V; therefore, the minimum voltage rating for the CT capacitor must be 30 V for optimal performance. An approximate formula for the relationship between C_T and slew rate when V_{BIAS} is set to 5 V is shown in Equation 1. This equation accounts for 10% to 90% measurement on V_{OUT} and does not apply for C_T < 100 pF. Use Table 1 to determine rise times for when C_T = 0 pF.

$$SR = 0.43 \times C_T + 26 \quad (1)$$

where

- SR is the slew rate (in µs/V)
- C_T is the capacitance value on the CT pin (in pF)
- The units for the constant 26 are µs/V. The units for the constant 0.43 are µs/(V × pF).

Rise time can be calculated by multiplying the input voltage by the slew rate. Table 1 contains rise time values measured on a typical device. Rise times shown in Table 1 are only valid for the power-up sequence where V_{IN} and V_{BIAS} are already in steady state condition before the ON pin is asserted high.

Table 1. Rise Time t_R vs CT Capacitor

C_T (pF)	RISE TIME (µs) 10% - 90%, C_L = 0.1 µF, C_{IN} = 1 µF, R_L = 10 Ω, V_{BIAS} = 5 V(1)						
	VIN = 5 V	VIN = 3.3 V	VIN = 1.8 V	VIN = 1.5 V	VIN = 1.2 V	VIN = 1.05 V	VIN = 0.6 V
0	140	105	75	65	60	55	40
220	520	360	215	185	160	140	95
470	970	660	385	330	275	240	155
1000	1750	1190	700	595	495	435	275
2200	3875	2615	1520	1290	1070	940	595
4700	7580	5110	2950	2510	2075	1830	1150
10000	16980	11485	6650	5635	4685	4110	2595

(1) Typical Values at 25°C with a 25-V X7R 10% Ceramic Capacitor on CT

9.3.2 Quick-Output Discharge (QOD) (Optional)

The TPS22975 includes an optional QOD feature. When the switch is disabled, an internal discharge resistance is connected between VOUT and GND to remove the remaining charge from the output. This resistance has a typical value of 230 Ω and prevents the output from floating while the switch is disabled. For best results, it is recommended that the device gets disabled before V_{BIAS} falls below the minimum recommended voltage.

9.3.3 Thermal Shutdown

Thermal shutdown protects the part from internally or externally generated excessive temperatures. When the device temperature triggers T_{SD} (typical 160°C), the switch is turned off. The switch automatically turns on again if the temperature of the die drops 20 degrees below the T_{SD} threshold.

9.4 Device Functional Modes

The Table 2 lists the VOUT pin states as determined by the ON pin.

Table 2. VOUT Connection

ON	TPS22975	TPS22975N
L	GND	Open
H	VIN	VIN

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

10.1.1 ON and OFF Control

The ON pin controls the state of the switch. ON is active high and has a 1.2-V ON-pin enable threshold, making it capable of interfacing with low-voltage signals. The ON pin is compatible with standard GPIO logic thresholds. It can be used with any microcontroller with 1.2 V or higher GPIO voltage. This pin cannot be left floating and must be driven either high or low for proper functionality.

10.1.2 Input Capacitor (C_{IN}) (Optional)

To limit the voltage drop on the input supply caused by transient inrush currents when the switch turns on into a discharged load capacitor or short-circuit, a capacitor needs to be placed between VIN and GND. A 1-µF ceramic capacitor, C_{IN}, placed close to the pins, is usually sufficient. Higher values of C_{IN} can be used to further reduce the voltage drop during high current applications. When switching heavy loads, it is recommended to have an input capacitor about 10 times higher than the output capacitor (C_L) to avoid excessive voltage drop.

10.1.3 Output Capacitor (C_L) (Optional)

Because of the integrated body diode in the NMOS switch, a C_{IN} greater than C_L is highly recommended. A C_L greater than C_{IN} can cause V_{OUT} to exceed V_{IN} when the system supply is removed. This could result in current flow through the body diode from V_{OUT} to V_{IN}. A C_{IN} to C_L ratio of 10 to 1 is recommended for minimizing V_{IN} dip caused by inrush currents during startup; however, a 10 to 1 ratio for capacitance is not required for proper functionality of the device. A ratio smaller than 10 to 1 (such as 1 to 1) could cause slightly more V_{IN} dip upon turn-on because of inrush currents. This can be mitigated by increasing the capacitance on the CT pin for a longer rise time (see the *Adjustable Rise Time* section).

10.2 Typical Application

For optimal R_{ON} performance, it is recommended to have $V_{IN} \leq V_{BIAS}$. The device is functional if $V_{IN} > V_{BIAS}$ but it exhibits R_{ON} greater than what is listed in the *Electrical Characteristics—V_{BIAS} = 5 V* and Electrical Characteristics—V_{BIAS} = 2.5 V tables.

Figure 31 demonstrates how the TPS22975 can be used to power downstream modules.

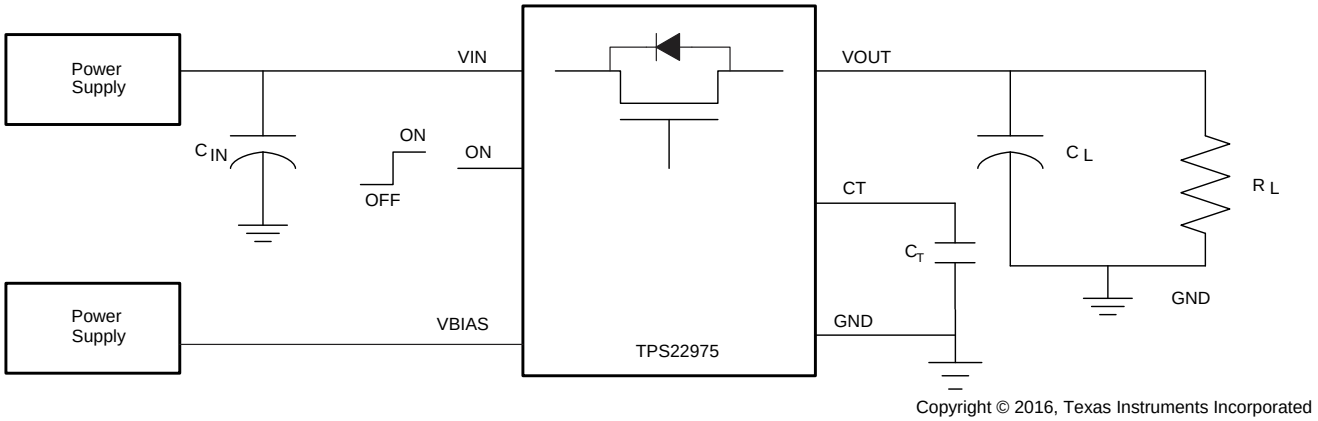


Figure 31. Powering a Downstream Module

Typical Application (continued)

10.2.1 Design Requirements

DESIGN PARAMETER	EXAMPLE VALUE
V_{IN}	3.3 V
V_{BIAS}	5 V
C_L	22 µF
Maximum Acceptable Inrush Current	400 mA

10.2.2 Detailed Design Procedure

10.2.2.1 Inrush Current

When the switch is enabled, the output capacitors must be charged up from 0 V to the set value (3.3 V in this example). This charge arrives in the form of inrush current. Inrush current can be calculated using Equation 2.

$$\text{Inrush Current} = C_L \times dV_{OUT}/dt \quad (2)$$

Where:

- C_L is the output capacitance
- dV_{OUT} is the change in V_{OUT} during the ramp up of the output voltage when device is enabled.
- dt is the rise time in V_{OUT} during the ramp up of the output voltage when the device is enabled.

The TPS22975 offers adjustable rise time for VOUT. This feature allows the user to control the inrush current during turnon. The appropriate rise time can be calculated using the design requirements and the inrush current equation as shown in Equation 3.

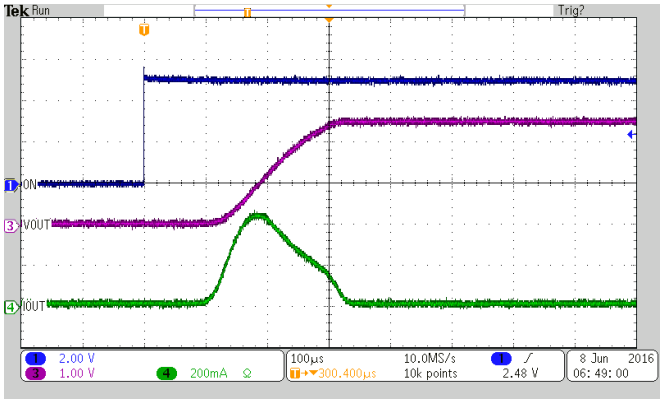
$$400\ \text{mA} = 22\ \mu\text{F} \times 3.3\ \text{V}/dt \quad (3)$$

The value of dt is given by Equation 4.

$$dt = 181.5\ \mu\text{s} \quad (4)$$

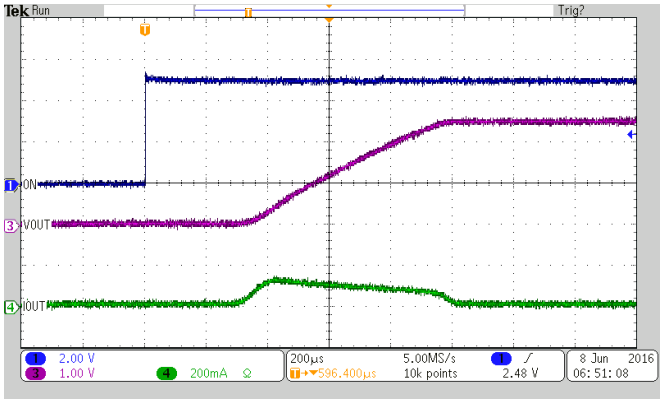
To ensure an inrush current of less than 400 mA, choose a CT value that yields a rise time of more than 181.5 µs. See the oscilloscope captures in the *Application Curves* section for an example of how the CT capacitor can be used to reduce inrush current.

10.2.3 Application Curves



V_{BIAS} = 5 V V_{IN} = 3.3 V C_L = 22 µF

Figure 32. Inrush Current with CT = 0 pF



V_{BIAS} = 5 V V_{IN} = 3.3 V C_L = 22 µF

Figure 33. Inrush Current with CT = 220 pF

11 Power Supply Recommendations

The supply to the device must be well regulated and placed as close to the device terminal as possible with the recommended 1-µF bypass capacitor. If the supply is located more than a few inches from the device terminals, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. If additional bulk capacitance is required, an electrolytic, tantalum or ceramic capacitor of 1 µF may be sufficient.

The TPS22975 operates regardless of power sequencing order. The order in which voltages are applied to V_{IN}, V_{BIAS}, and ON does not damage the device as long as the voltages do not exceed the absolute maximum operating conditions. If voltage is applied to ON before V_{IN}, the slew rate of V_{OUT} can not be controlled.

12 Layout

12.1 Layout Guidelines

For best performance, all traces must be as short as possible. To be most effective, the input and output capacitors must be placed close to the device to minimize the effects that parasitic trace inductances may have on normal operation. Using wide traces for VIN, VOUT, and GND helps minimize the parasitic electrical effects along with minimizing the case to ambient thermal impedance. The CT trace must be as short as possible to reduce parasitic capacitance.

12.2 Layout Example

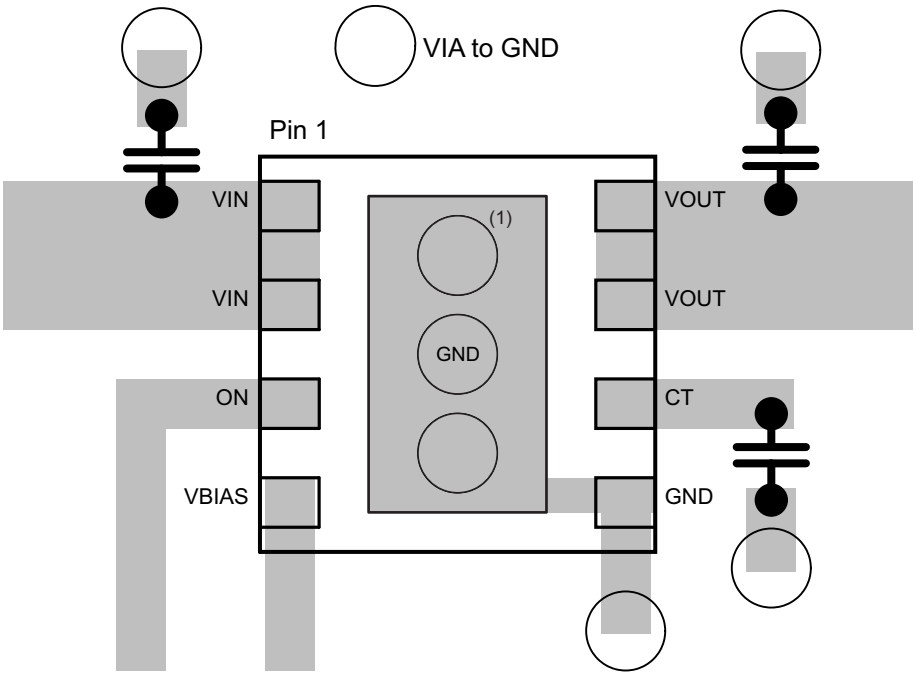


Figure 34. Layout Recommendation

12.3 Thermal Considerations

The maximum IC junction temperature must be restricted to 125°C under normal operating conditions. To calculate the maximum allowable dissipation, $P_{D(max)}$, for a given ambient temperature, use Equation 5 as a guideline.

$$P_{D(max)} = \frac{T_{J(max)} - T_A}{\theta_{JA}} \quad (5)$$

where

- $P_{D(max)}$ is the maximum allowable power dissipation
- $T_{J(max)}$ is the maximum allowable junction temperature (125°C for the TPS22975)
- T_A is the ambient temperature of the device
- Θ_{JA} is the junction to air thermal impedance. See the *Thermal Information* section. This parameter is highly dependent upon board layout.

In Figure 34, notice that the thermal vias are located under the exposed thermal pad of the device. This allows for thermal diffusion away from the device.

13 Device and Documentation Support

13.1 Device Support

13.1.1 Developmental Support

For the TPS22975 PSpice Transient Model, see SLVMBO6.

13.2 Related Documentation

For related documentation see the following:

- *Fundamentals of On-Resistance in Load Switches*, SLVA771
- *TPS22975 Load Switch Evaluation Module User's Guide*, SLVUAR3

13.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.5 Trademarks

E2E is a trademark of Texas Instruments.
Ultrabook is a trademark of Intel.
All other trademarks are the property of their respective owners.

13.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS22975DSGR	ACTIVE	WSON	DSG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 105	13XH	Samples
TPS22975DSGT	ACTIVE	WSON	DSG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 105	13XH	Samples
TPS22975NDSGR	ACTIVE	WSON	DSG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 105	14YH	Samples
TPS22975NDSGT	ACTIVE	WSON	DSG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 105	14YH	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

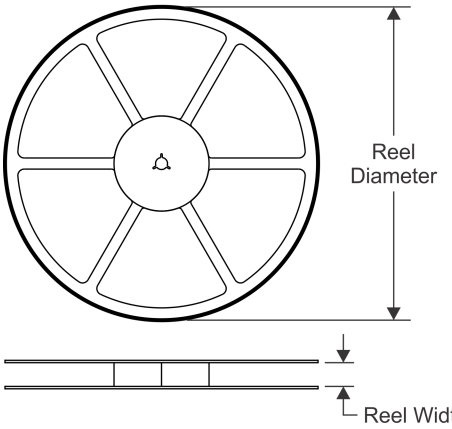
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

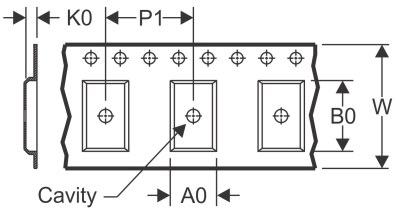
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

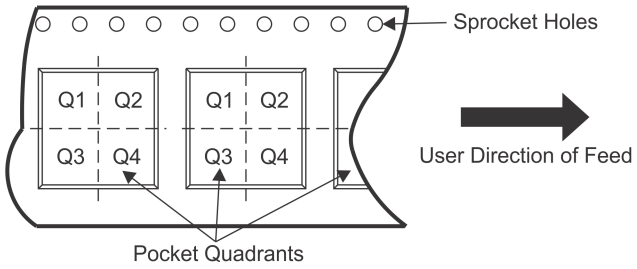


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

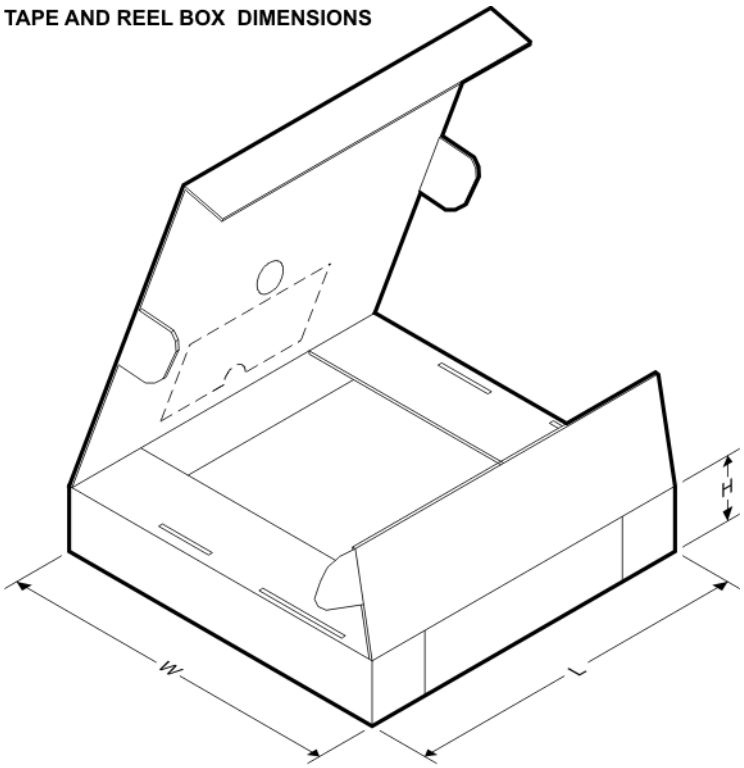
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS22975DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS22975DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS22975NDSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS22975NDSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS22975NDSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS22975NDSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

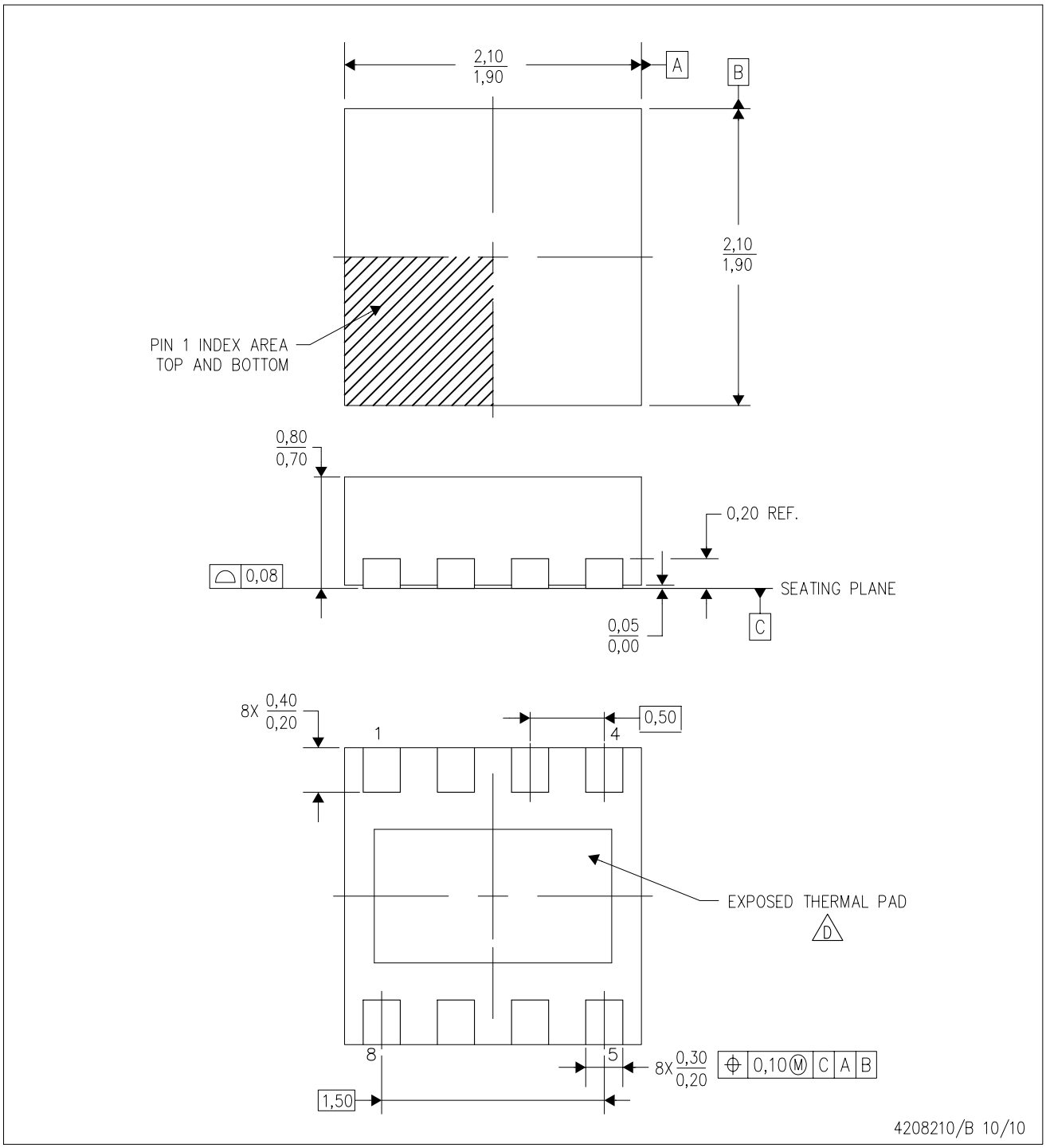
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS22975DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
TPS22975DSGT	WSON	DSG	8	250	210.0	185.0	35.0
TPS22975NDSGR	WSON	DSG	8	3000	210.0	185.0	35.0
TPS22975NDSGR	WSON	DSG	8	3000	210.0	185.0	35.0
TPS22975NDSGT	WSON	DSG	8	250	210.0	185.0	35.0
TPS22975NDSGT	WSON	DSG	8	250	210.0	185.0	35.0

DSG (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–Leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–229.

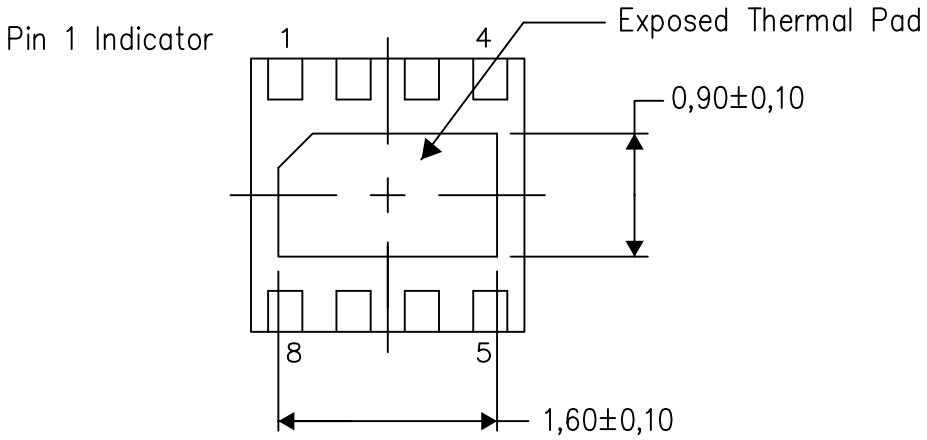
DSG (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



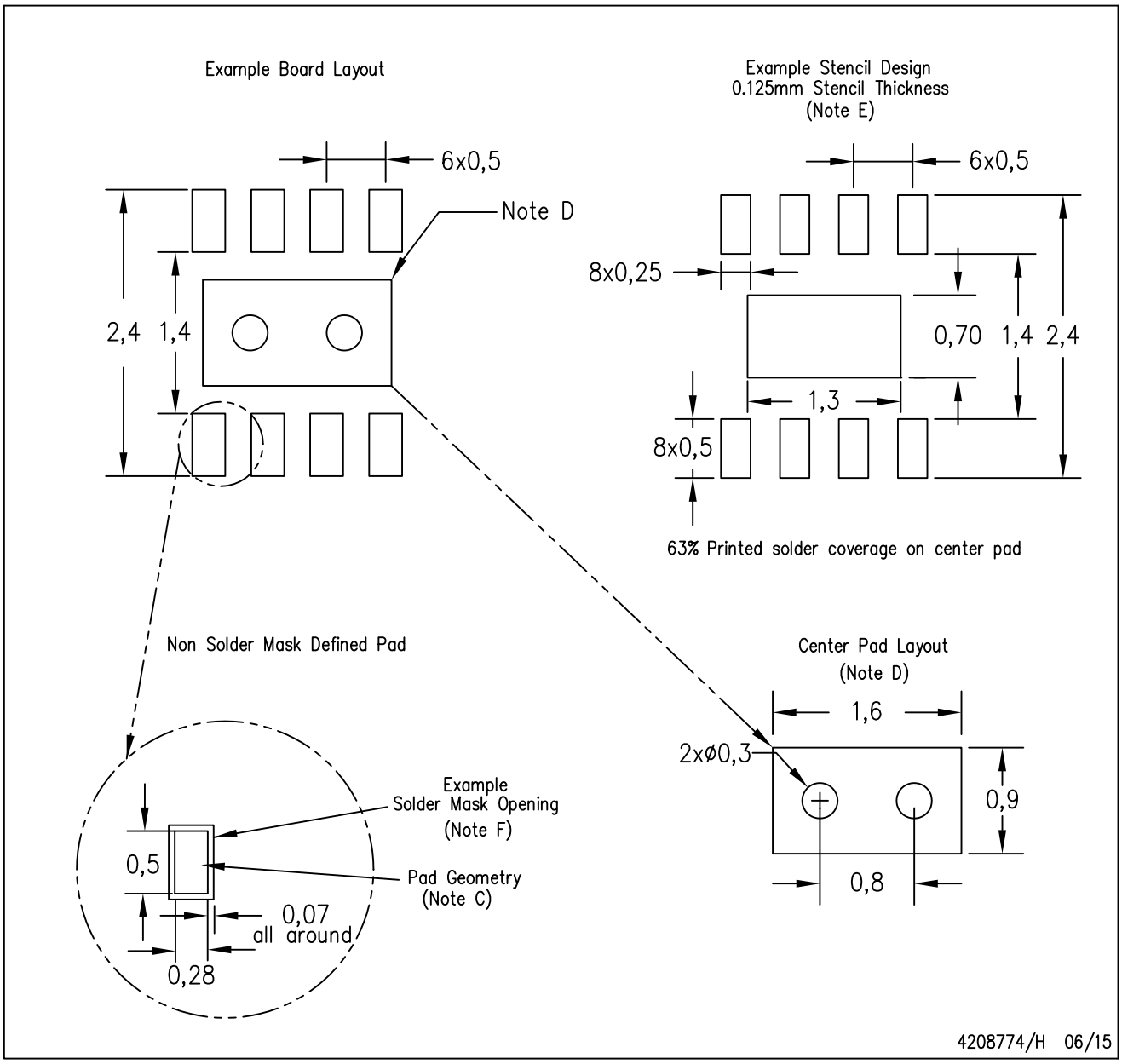
Bottom View

Exposed Thermal Pad Dimensions

4208347/I 06/15

NOTE: All linear dimensions are in millimeters

DSG (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

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