TEXAS INSTRUMENTS

TPS40192, TPS40193

SLUS719F – MARCH 2007 – REVISED NOVEMBER 2016

TPS4019x 4.5-V to 18-V Input, 10-Pin, Synchronous Buck Controller With Power Good

1 Features

- Input Operating Voltage Range: 4.5 V to 18 V
- Up to 20-A Output Currents
- Supports Pre-Biased Outputs
- 0.5%, 591-mV Reference
- Switching Frequency
  - TPS40192: 600 kHz
  - TPS40193: 300 kHz
- Three Selectable Thermally Compensated Short-Circuit Protection Levels
- Hiccup Restart from Faults
- Internal 5-V Regulator
- High-Side and Low-Side MOSFET ON-resistance ($R_{DS(on)}$) Current Sensing
- 10-Pin 3 mm × 3 mm SON Package
- Internal 4-ms Soft-Start Time
- Thermal Shutdown Protection at 145°C

2 Applications

- Cable Modem CPE
- Digital Set Top Box
- Graphics/Audio Cards
- Entry Level and Mid-Range Servers

3 Description

TPS40192 and TPS40193 are cost-optimized synchronous buck controllers that operate from 4.5 V to 18 V input. These controllers implement a voltage-mode control architecture with the switching frequency fixed at either 600 kHz (TPS40192) or 300 kHz (TPS40193). The higher switching frequency facilitates the use of smaller inductor and output capacitors, thereby providing a compact power-supply solution. An adaptive anti-cross conduction scheme is used to prevent shoot through current in the power FETs.

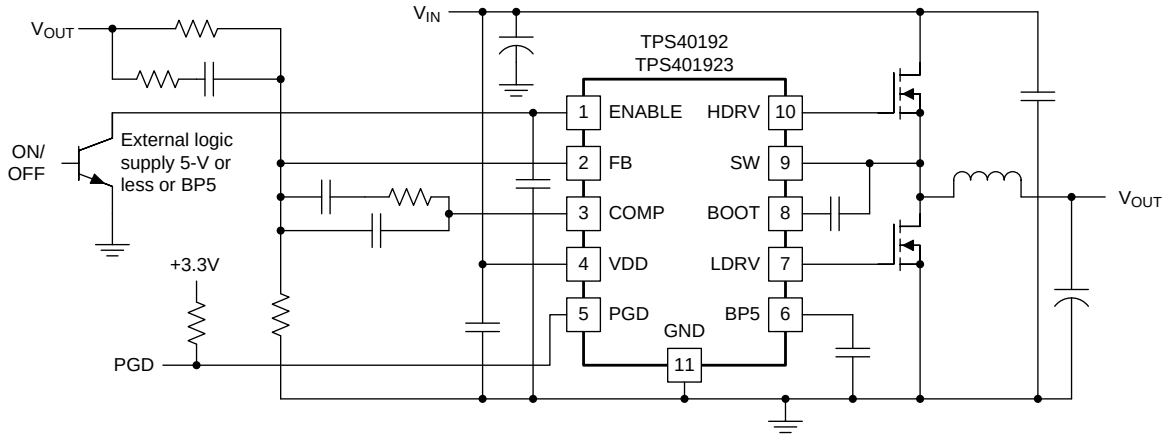
Short circuit detection is done by sensing the voltage drop across the low-side MOSFET when it is on and comparing it with a user selected threshold of 100 mV, 200 mV or 280 mV. The threshold is set with a single external resistor connected from COMP to GND. This resistor is sensed at startup and the selected threshold is latched. Pulse-by-pulse limiting (to prevent current runaway) is provided by sensing the voltage across the high-side MOSFET when it is on and terminating the cycle when the voltage drop rises above a fixed threshold of 550 mV. When the controller senses an output short circuit, both MOSFETs are turned off and a timeout period is observed before attempting to restart. This behavior provides limited power dissipation in the event of a sustained fault.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS40192	VSON (10)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Application Diagram



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (May 2013) to Revision F — **Page**

- Added *Pin Configuration and Functions* section, *ESD Rating* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

Changes from Revision D (July 2012) to Revision E — **Page**

- Added clarity to Figure 15 ... 15
- Added note regarding high-resistance resistor ... 19

Changes from Revision C (August 2010) to Revision D — **Page**

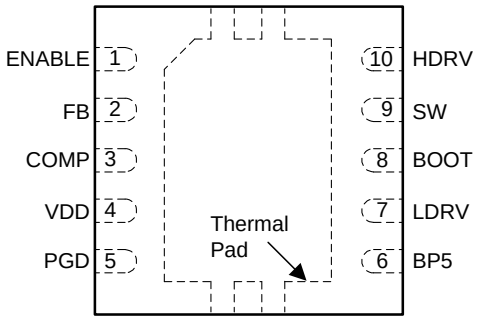
- Added text to the last paragraph in the Enable Functionality section. ... 10

Changes from Revision B (September 2007) to Revision C — **Page**

- Changed corrected label for pin 8 ... 3
- Changed corrected waveform ... 11

5 Pin Configuration and Functions

DRC Package
10-Pin VSON
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
BOOT	8	I	Gate drive voltage for the high-side N-channel MOSFET. A capacitor 100 nF typical must be connected between this pin and SW.
BP5	6	O	Output bypass for the internal regulator. Connect a capacitor with a value of at least 1-μF from this pin to GND. Larger capacitors (up to 4.7-μF) can improve noise performance when using a low-side MOSFET with a gate charge of 25 nC or greater. Low power, low noise loads may be connected here if desired. The sum of the external load and the gate drive requirements must not exceed 50 mA. This regulator is turned off when ENABLE is pulled low.
COMP	3	O	Output of the error amplifier.
ENABLE	1	I	Logic level input which starts or stops the controller from an external user command. A high-level turns the controller on. A weak internal pull-up holds this pin high so that the pin may be left floating if this function is not used.
FB	2	I	Inverting input to the error amplifier. In normal operation the voltage on this pin is equal to the internal reference voltage (591 mV typical)
HDRV	10	O	Bootstrapped output for driving the gate of the high-side N-channel FET.
LDRV	7	O	Output to the rectifier MOSFET gate
PGD	5	O	Open drain power good output
SW	9	I	Sense line for the adaptive anti-cross conduction circuitry. Serves as common connection for the flying high-side MOSFET driver
VDD	4	I	Power input to the controller
Thermal pad		G	Common reference for the device. Connect to the system GND.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range unless otherwise noted(1)

		MIN	MAX	UNIT
Input voltage	VDD, ENABLE	–0.3	20	V
	SW	–5	25	
	BOOT, HDRV	–0.3	30	
	BOOT-SW, HDRV-SW (differential from BOOT or HDRV to SW)	–0.3	6	
	COMP, FB, BP5, LDRV, PGD	–0.3	6	
Operating junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–55	150	

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	MAX	UNIT
V_{VDD}	Input voltage	4.5	18	V
T_J	Operating Junction temperature	-40	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		TPS40192 DRC (VSON) 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	46.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	51.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	21.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	22.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	6.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

T_J = –40°C to 85°C, V_{VDD}= 12 V_{dc}, all parameters at zero power dissipation (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
REFERENCE							
V_{FB}	Feedback voltage range	0°C ≤ T_J ≤ 85°C		588	591	594	mV
		-40°C ≤ T_J ≤ 85°C		585	591	594	
INPUT SUPPLY							
V_{VDD}	Input voltage range			4.5		18	V
I_{VDD}	Operating current	V_{ENABLE} = 3 V			2.5	4	mA
		V_{ENABLE} = 0.6 V			45	70	µA
ON BOARD REGULATOR							
V_{5VBP}	Output voltage	V_{VDD} > 6 V, I_{5VBP} ≤ 10 mA		5.1	5.3	5.5	V
V_{DO}	Regulator dropout voltage	V_{VDD} - V_{BP5} , V_{VDD} = 5 V, I_{BP5} ≤ 25 mA			350	550	mV
I_{SC}	Regulator current limit threshold			50			mA
I_{BP5}	Average current					50	
OSCILLATOR							
f_{SW}	Switching frequency		TPS40193	240	300	360	kHz
			TPS40192	500	600	700	
V_{RMP}	Ramp amplitude(1)				1		V
PWM							
D_{MAX}	Maximum duty cycle(1)			85%			
$t_{ON(min)}$	Minimum controlled pulse(1)					110	ns
t_{DEAD}	Output driver dead time	HDRV off to LDRV on			50		
		LDRV off to HDRV on			25		
SOFT-START							
t_{SS}	Soft-start time			3	4	6	ms
t_{SSDLY}	Soft-start delay time				2		
t_{REG}	Time to regulation				6		
ERROR AMPLIFIER							
GBWP	Gain bandwidth product(1)			7	10		MHz
A_{OL}	DC gain(1)			60			dB
I_{IB}	Input bias current (current out of FB pin)					100	nA
I_{EAOP}	Output source current	V_{FB} = 0 V		1			mA
I_{EAOM}	Output sink current	V_{FB} = 2 V		1			
SHORT CIRCUIT PROTECTION							
$t_{PSS(min)}$	Minimum pulse during short circuit(1)				250		ns
t_{BLNK}	Blanking time(1)			60	90	120	
t_{OFF}	Off-time between restart attempts			30	50		ms
V_{ILIM}	Short circuit comparator threshold voltage	$R_{COMP(GND)}$ = OPEN, T_J = 25°C		160	200	240	mV
		$R_{COMP(GND)}$ = 4 kΩ, T_J = 25°C		80	100	120	
		$R_{COMP(GND)}$ = 12 kΩ, T_J = 25°C		228	280	342	
V_{ILIMH}	Short circuit threshold voltage on high-side MOSFET	T_J = 25°C		400	550	650	

(1) Specified by design. Not production tested.

Electrical Characteristics (continued)

T_J = –40°C to 85°C, V_{VDD}= 12 V_{dc}, all parameters at zero power dissipation (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT DRIVERS						
R_{HDHI}	High-side driver pull-up resistance	V_{BOOT} - V_{SW} = 4.5 V, I_{HDRV} = -100 mA		3	6	Ω
R_{HDLO}	High-side driver pull-down resistance	V_{BOOT} - V_{SW} = 4.5 V, I_{HDRV} = 100 mA		1.5	3.0	
R_{LDHI}	Low-side driver pull-up resistance	I_{LDRV} = -100 mA		2.5	5.0	
R_{LDLO}	Low-side driver pull-down resistance	I_{LDRV} = 100 mA		0.8	1.5	
t_{HRISE}	High-side driver rise time(1)	C_{LOAD} = 1 nF		15	35	ns
t_{HFALL}	High-side driver fall time(1)			10	25	
t_{LRISE}	Low-side driver rise time(1)			15	35	
t_{LFALL}	Low-side driver fall time(1)			10	25	
UVLO						
V_{UVLO}	Turn-on voltage		3.9	4.2	4.4	V
$UVLO_{HYST}$	Hysteresis		700	800	900	mV
SHUTDOWN						
V_{IH}	High-level input voltage, ENABLE			1.9	3	V
V_{IL}	Low-level input votlage, ENABLE		0.6			
POWER GOOD						
V_{OV}	Feedback voltage limit for powergood			650		mV
V_{UV}	Feedback voltage limit for powergood			525		
V_{PG_HYST}	Powergood hysteresis voltage at FB pin			30		
R_{PGD}	Pulldown resistance of PGD pin	V_{FB} = 0 V		7	50	Ω
I_{PDGLK}	Leakage current	V_{FB} = 0 V		7	12	µA
BOOT DIODE						
V_{DFWD}	Bootstrap diode forward voltage	I_{BOOT} = 5 mA	0.5	0.8	1.2	V
THERMAL SHUTDOWN						
T_{JSD}	Junction shutdown temperature(1)			145		°C
T_{JSDH}	Hysteresis(1)			20		

6.6 Dissipation Ratings

PACKAGE	AIRFLOW (LFM)	$R_{\theta JA}$ High-K Board(1) (°C/W)	Power Rating (W) T_A = 25°C	Power Rating (W) T_A = 85°C
DRC	0 (Natural Convection)	47.9	2.08	0.835
	200	40.5	2.46	0.987
	400	38.2	2.61	1.04

(1) Ratings based on JEDEC High Thermal Conductivity (High K) Board. For more information on the test method, see TI Technical Brief SZZA017.

6.7 Typical Characteristics

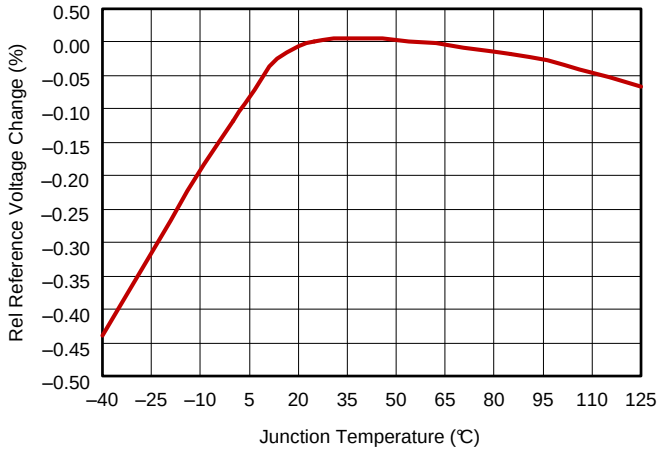


Figure 1. Relative Reference Feedback Voltage vs Junction Temperature

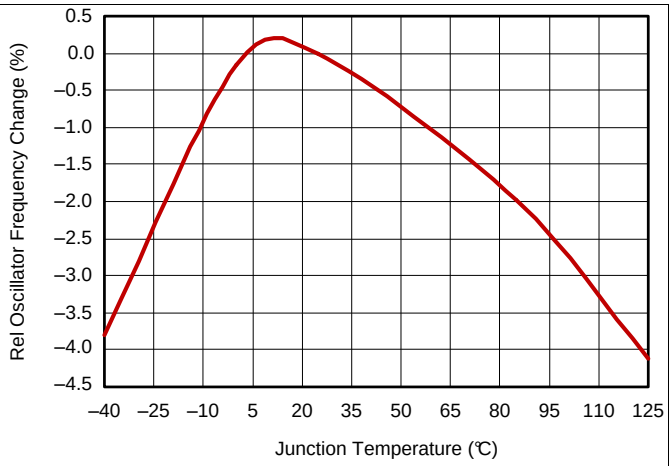


Figure 2. Relative Oscillator Frequency Change vs Junction Temperature

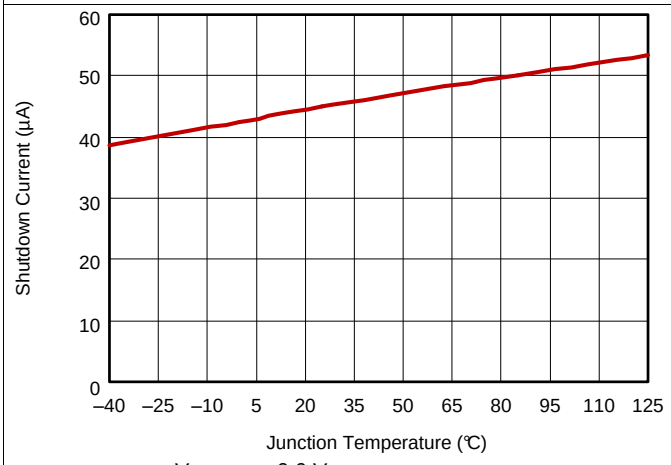


Figure 3. Shutdown Input Current vs Junction Temperature

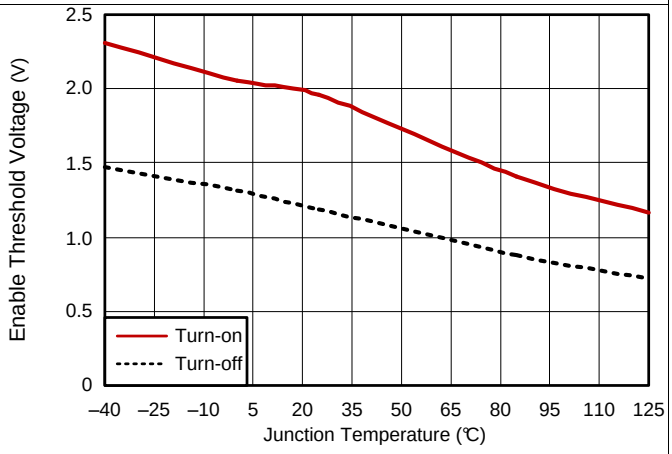


Figure 4. Enable Threshold Voltage vs Junction Temperature

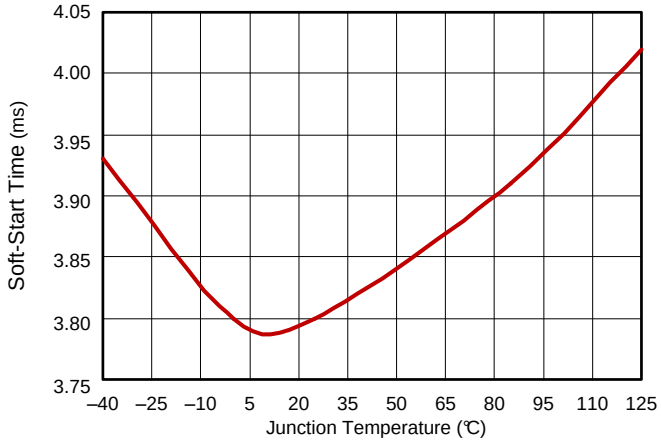


Figure 5. Soft-start Time vs Junction Temperature

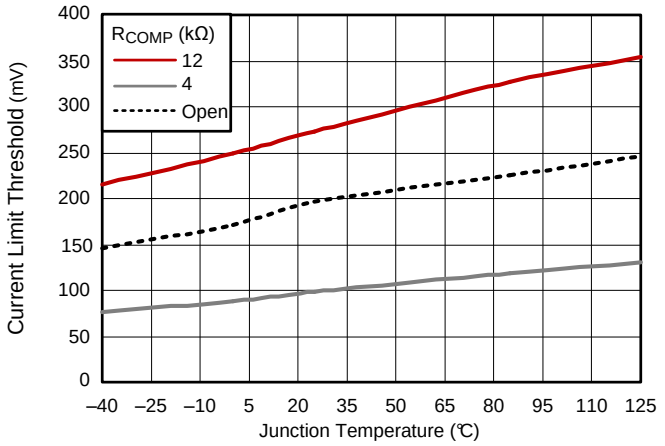


Figure 6. Low-Side MOSFET Current Limit Threshold vs Junction Temperature

Typical Characteristics (continued)

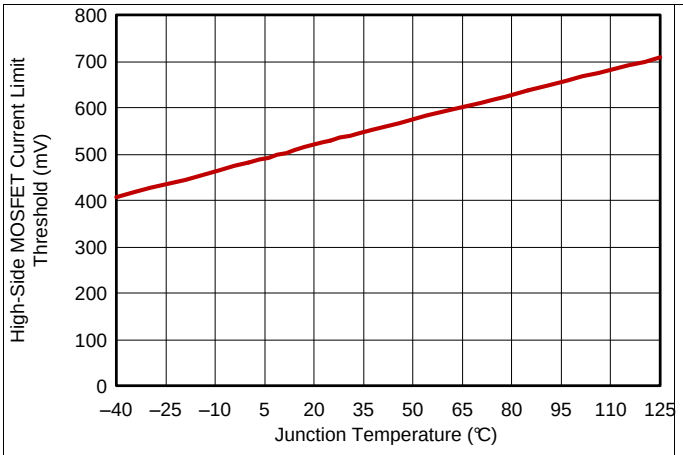


Figure 7. High-Side MOSFET Current Limit Threshold vs Junction Temperature

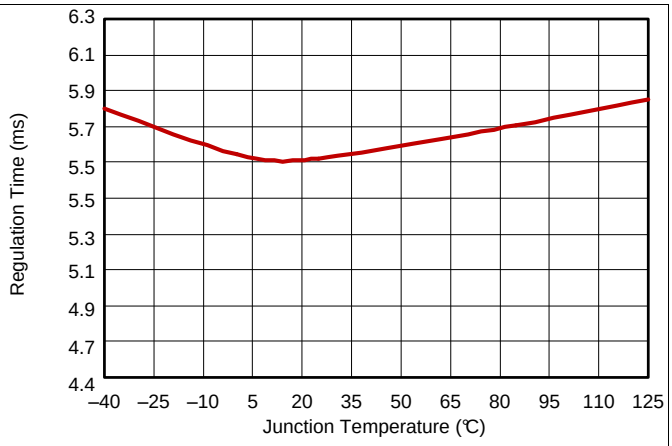


Figure 8. Total Time to Regulation vs Junction Temperature

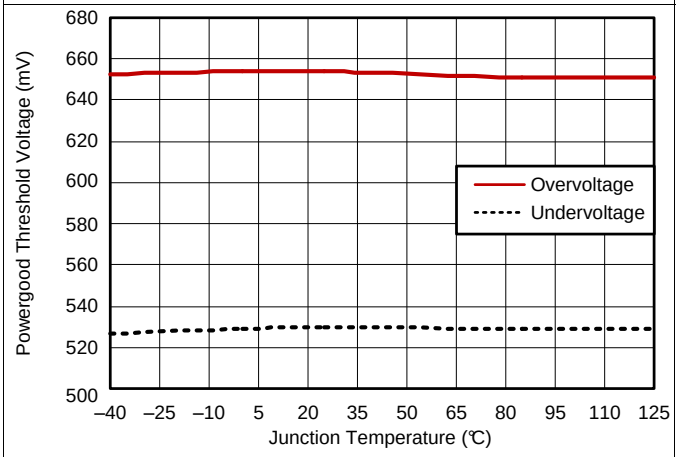


Figure 9. POWERGOOD THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

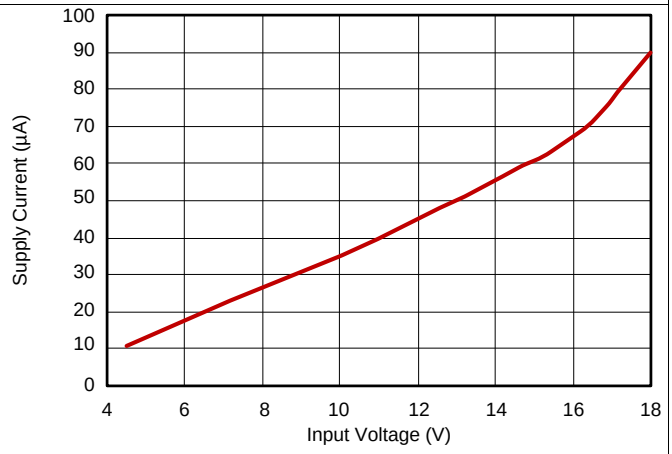


Figure 10. SHUTDOWN CURRENT vs INPUT VOLTAGE

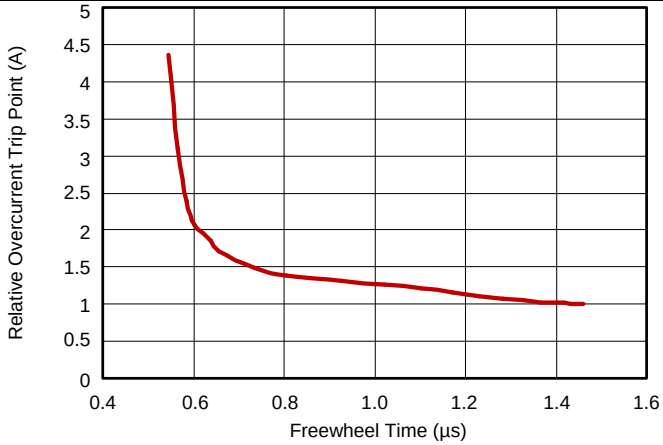


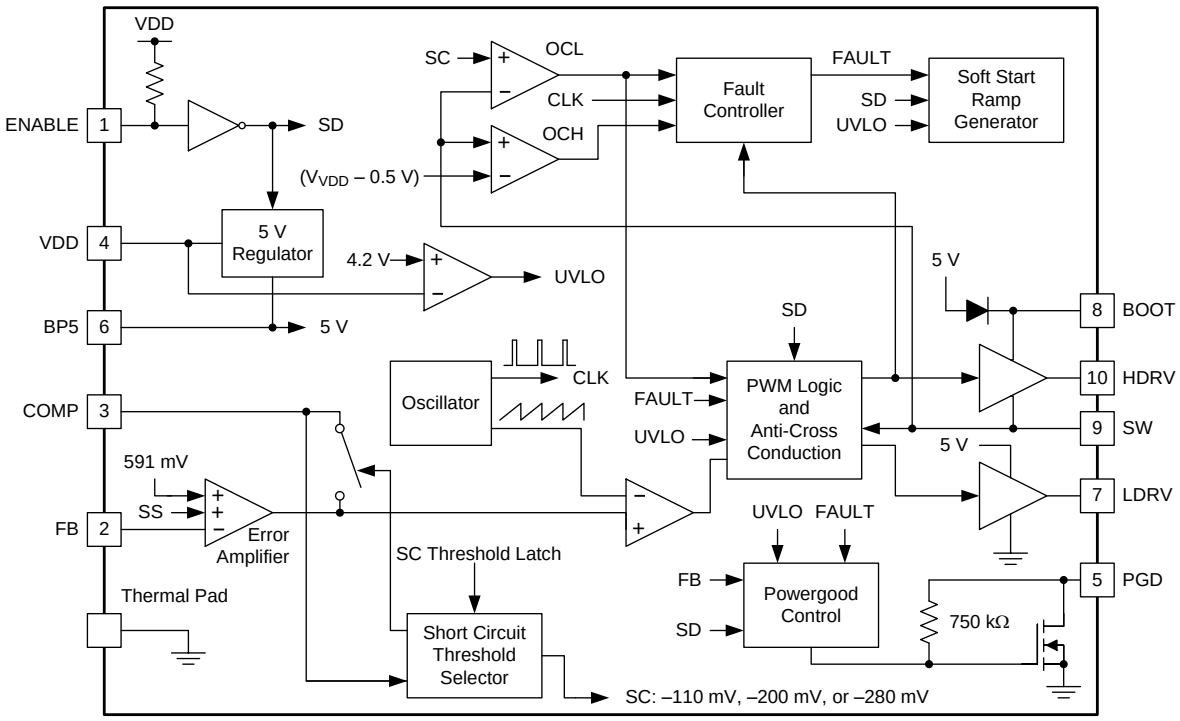
Figure 11. Relative Overcurrent Trip Point vs Freewheel Time

7 Detailed Description

7.1 Overview

The TPS40192 and TPS40193 devices are cost optimized controllers providing all the necessary features to construct a high performance DC/DC converter while keeping costs to a minimum. Support for pre-biased outputs eliminates concerns about damaging sensitive loads during startup. Strong gate drivers for the high-side and rectifier N-channel MOSFETs decrease switching losses for increased efficiency. Adaptive gate drive timing prevents shoot through and minimizes body diode conduction in the rectifier MOSFET, also increasing efficiency. Selectable short circuit protection thresholds and hiccup recovery from a short circuit increase design flexibility and minimize power dissipation in the event of a prolonged output fault. The dedicated ENABLE pin allows the converter to be placed in a very low quiescent current shutdown mode. Internally fixed switching frequency and soft-start time reduce external component count, simplifying design and layout, as well as reducing footprint and cost. The 3 mm × 3 mm package size also contributes to a reduced overall converter footprint.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Voltage Reference

The band gap cell is designed with a trimmed 591-mV output. The 0.5% tolerance on the reference voltage allows the user to design a very accurate power-supply.

7.3.2 Oscillator

The TPS40192 has a fixed internal switching frequency of 600 kHz. Tthe TPS40193 operates at a switching frequency of 300 kHz.

Feature Description (continued)

7.3.3 UVLO

When the input voltage is below the UVLO threshold, the device holds all gate drive outputs in the low (OFF) state. When the input rises above the UVLO threshold, and the ENABLE pin is above the turn ON threshold, the oscillator begins to operate and the start-up sequence is allowed to begin. The UVLO level is internally fixed at 4.2 V.

7.3.4 Enable Functionality

A dedicated ENABLE pin simplifies a user-level interface design where no multiplexed functions exist. Another benefit is a true low power shutdown mode of operation. When the ENABLE pin is pulled to GND, all unnecessary functions, including the BP5 regulator, are turned off, reducing the device supply (I_{DD}) current to 45-μA. A functionally equivalent circuit of the enable circuitry shown in Figure 12.

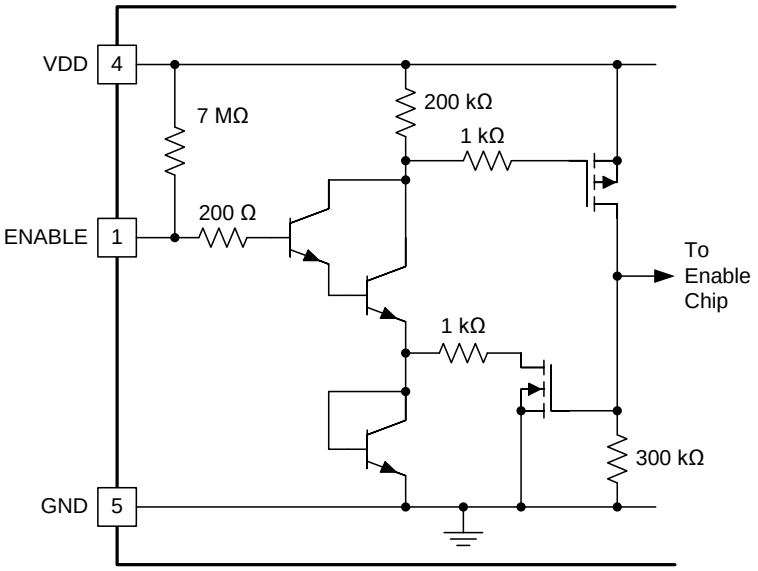


Figure 12. Enable Pin Internal Circuitry

If the ENABLE pin is left floating, the chip starts automatically. The pin must be pulled to less than 600 mV to ensure that the TPS40192 and TPS40193 devices is in shutdown mode. Note that the ENABLE pin is relatively high impedance. Some applications generate enough nearby noise to cause the ENABLE pin to swing below the 600 mV threshold and give an erroneous shutdown commands to the rest of the device. There are two solutions to solve this problem.

1. Place a capacitor from ENABLE to GND. A side effect of this is to delay the start of the converter while the capacitor charges past the enable threshold
2. Place a resistor from VDD to ENABLE. This causes more current to flow in the shutdown mode, but does not delay converter startup. If a resistor is used, the total current into the ENABLE pin should be limited to no more than 500 μA.

The ENABLE pin is self-clamping. The clamp voltage can be as low as 1 V with a 1-kΩ ground impedance. Due to this self-clamping feature, the pull-up impedance on the ENABLE pin should be selected to limit the sink current to less than 500 μA. Driving the ENABLE pin with a low-impedance source voltage can result in damage to the device. Because of the self-clamping feature, it requires care when connecting multiple ENABLE pins together. For enabling multiple TPS4019x devices (TPS40190, TPS40192, TPS40193, TPS40195, TPS40197), see the Application Report SLVA509.

Feature Description (continued)

7.3.5 Startup Sequence and Timing

After input power is applied, the 5-V onboard regulator comes up. Once this regulator comes up, the device goes through a period where it samples the impedance at the COMP pin and determines the short circuit protection threshold voltage, by placing 400 mV on the COMP pin for approximately 1 ms. During this time, the current is measured and compared against internal thresholds to select the short circuit protection threshold. After this, the COMP pin is brought low for 1 ms. This ensures that the feedback loop is preconditioned at startup and no sudden output rise occurs at the output of the converter when the converter is allowed to start switching. After these initial two milliseconds, the internal soft-start circuitry is engaged and the converter is allowed to start. See Figure 13.

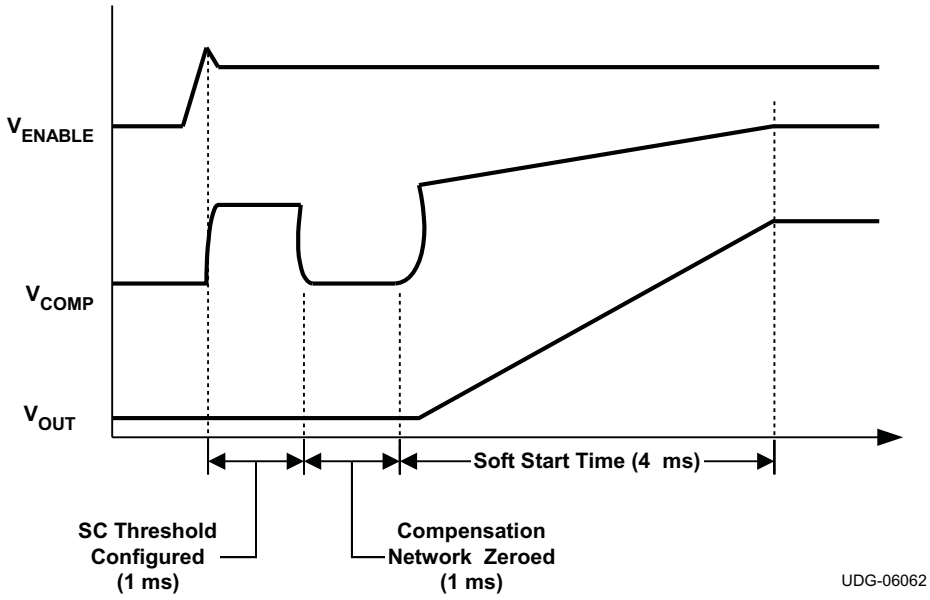


Figure 13. Startup Sequence

7.3.6 Selecting the Short Circuit Current

A short circuit in the devices is detected by sensing the voltage drop across the low-side MOSFET when it is on, and across the high-side MOSFET when it is on. If the voltage drop across either MOSFET exceeds the short circuit threshold in any given switching cycle, a counter increments one count. If the voltage across the high-side MOSFET was higher that the short circuit threshold, that MOSFET is turned off early. If the voltage drop across either MOSFET does not exceed the short circuit threshold during a cycle, the counter is decremented for that cycle. If the counter fills up (a count of 7) a fault condition is declared and the drivers turn off both MOSFETs. After a timeout of approximately 50 ms, the controller attempts to restart. If a short circuit is still present at the output, the current quickly ramps up to the short circuit threshold and another fault condition is declared and the process of waiting for the 50 ms an attempting to restart repeats. The low-side threshold increases as the low-side on time decreases due to blanking time and comparator response time. See Figure 11 for changes in the threshold as the low-side MOSFET conduction time decreases.

These devices provide three selectable short circuit protection thresholds for the low-side MOSFET: 100 mV, 200 mV and 280 mV. The particular threshold is selected by connecting a resistor from COMP to GND. Table 1 shows the short circuit thresholds for corresponding resistors from COMP to GND. When designing the compensation for the feedback loop, remember that a low impedance compensation network combined with a long network time constant can cause the short circuit threshold setting to not be as expected. The time constant and impedance of the network connected from COMP to FB should be as in Equation 1 to ensure no interaction with the short circuit threshold setting.

Feature Description (continued)

$$\frac{0.4\ \text{V}}{\text{R1}} \times e^{\left(\frac{-t}{\text{R1} \times \text{C1}}\right)} < 10\ \mu\text{A} \quad (1)$$

where

- t is 1 ms, the sampling time of the short circuit threshold setting circuit
- R1 and C1 are the values of the components in Figure 14

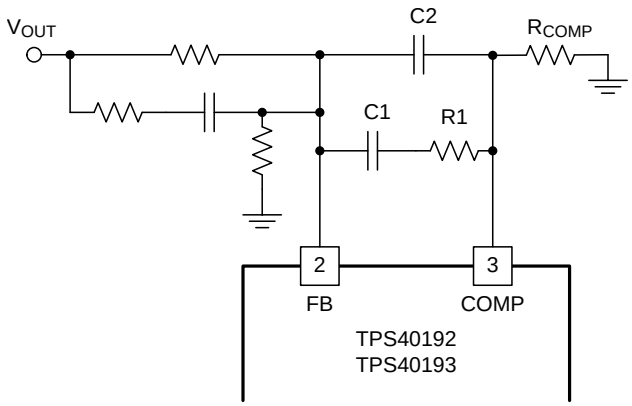


Figure 14. Short Circuit Threshold Feedback Network

Table 1. Short Circuit Threshold Voltage Selection

COMPARATOR RESISTANCE R_{COMP} (kΩ)	CURRENT LIMIT THRESHOLD VOLTAGE (mV) V_{ILIM}(V)
12 ±10%	280
Open	200
4 ±10%	100

The range of short circuit current thresholds that can be expected is shown in Equation 2 and Equation 3.

$$I_{SCP\,(max)} = \frac{V_{ILIM\,(max)}}{R_{DS\,(on)min}} \quad (2)$$

$$I_{SCP\,(min)} = \frac{V_{ILIM\,(min)}}{R_{DS\,(on)max}}$$

where

- I_{SCP} is the short circuit current
- V_{ILIM} is the short circuit threshold for the low-side MOSFET
- $R_{DS(on)}$ is the channel ON-resistance of the low-side MOSFET (3)

Due to blanking time considerations, overcurrent threshold accuracy may fall off for duty cycle greater than 75% with the TPS40192, or 88% with the TPS40193. Specifically, the overcurrent comparator has only a very short time to sample the SW pin voltage under these conditions. As a result, the comparator may not have time to respond to voltages very near the threshold.

The short circuit protection threshold for the high-side MOSFET is fixed at 550 mV typical, 400 mV minimum. This threshold is in place to provide a maximum current output using pulse by pulse current limit in the case of a fault. The pulse terminates when the voltage drop across the high-side MOSFET exceeds the short circuit threshold. The maximum amount of current that can be specified to be sourced from a converter is found by Equation 4.

$$I_{OUT\,(max)} = \frac{V_{ILIM\,(min)}}{R_{DS\,(on)max}}$$

where

- $I_{OUT(max)}$ is the maximum current that the converter is specified to source
- $V_{ILIMH(min)}$ is the short circuit threshold for the high-side MOSFET (400 mV)
- $R_{DS(on)max}$ is the maximum resistance of the high-side MOSFET (4)

If the required current from the converter is greater than the calculated $I_{OUT(max)}$, a lower resistance high-side MOSFET must be chosen. Both the high-side and low-side thresholds use temperature compensation to approximate the change in resistance for a typical power MOSFET. This helps to counteract shifts in overcurrent thresholds as temperature increases. For this feature to be effective, the MOSFETs and the device must be well coupled thermally.

7.3.7 5-V Regulator

An on board 5-V regulator that allows the parts to operate from a single voltage feed. No separate 5-V feed to the part is required. This regulator needs to have a minimum of 1-μF of capacitance on the BP5 pin for stability. A ceramic capacitor is suggested for this purpose.

This regulator can also be used to supply power to nearby circuitry, eliminating the need for a separate LDO in some cases. If this pin is used for external loads, be aware that this is the power supply for the internals of the TPS40192 and TPS40193 devices . While efforts have been made to reduce sensitivity, any noise induced on this line has an adverse effect on the overall performance of the internal circuitry and shows up as increased pulse jitter, or skewed reference voltage. Also, when the device is disabled by pulling the EN pin low, this regulator is turned off and cannot supply power.

The amount of power available from this pin varies with the size of the power MOSFETs that the drivers must operate. Larger MOSFETs require more gate drive current and reduce the amount of power available on this pin for other tasks. The total current that this pin can draw from both the gate drive and external loads cannot exceed 50 mA. The device uses up to 4 mA from the regulator and the total gate drive current can be found from Equation 5.

For regulator stability, a 1-μF capacitor is required to be connected from BP5 to GND. In some applications using higher gate charge MOSFETs, a larger capacitor is required for noise suppression. For a total gate charge of both the high and low-side MOSFETs greater than 20 nC, a 2.2-μF or larger capacitor is recommended.

$$I_G = f_{SW} \times \left(Q_{G\,(high\,)} + Q_{G\,(low\,)}\right)$$

where

- I_G is the required gate drive current
- f_{SW} is the switching frequency (600 kHz for TPS40192, and 300 kHz for TPS40193)
- $Q_{G(high)}$ is the gate charge requirement for the high-side MOSFET when V_{GS}= 5 V
- $Q_{G(low)}$ is the gate charge requirement for the low-side MOSFET when V_{GS}= 5 V (5)

7.3.8 Prebias Start-Up

The TPS40192 and TPS40193 devices contains a unique circuit to prevent current from being *pulled* from the output during startup in the condition the output is pre-biased. When the soft-start commands a voltage higher than the pre-bias level (internal soft-start becomes greater than feedback voltage [V_{FB}]), the controller slowly activates synchronous rectification by starting the first LDRV pulses with a narrow on-time. It then increments that on-time on a cycle-by-cycle basis until it coincides with the time dictated by (1-D), where D is the duty cycle of the converter. This scheme prevents the initial sinking of the pre-bias output, and ensures that the out voltage (V_{OUT}) starts and ramps up smoothly into regulation and the control loop is given time to transition from pre-biased startup to normal mode operation with minimal disturbance to the output voltage. The amount of time from the start of switching until the low-side MOSFET is turned on for the full (1-D) interval is defined by 32 clock cycles.

7.3.9 Drivers

The drivers for the external HDRV and LDRV MOSFETs are capable of driving a gate-to-source voltage of 5 V. The LDRV driver switches between VDD and GND, while HDRV driver is referenced to SW and switches between BOOT and SW. The drivers have non-overlapping timing that is governed by an adaptive delay circuit to minimize body diode conduction in the synchronous rectifier. The drivers are capable of driving MOSFETS that are appropriate for a 15-A (TPS40192) or 20-A (TPS40193) converter.

7.3.10 Power Good

The TPS40192 and TPS40193 devices provides an indication that output power is good for the converter. This is an open drain signal and pulls low when any condition exists that would indicate that the output of the supply might be out of regulation. These conditions include:

- V_{FB} is more than ±10% from nominal
- soft-start is active
- an undervoltage condition exists for the device
- a short circuit condition has been detected
- die temperature is over (145°C)

NOTE

When there is no power to the device, PGOOD is not able to pull close to GND if an auxiliary supply is used for the power good indication. In this case, a built in resistor connected from drain to gate on the PGOOD pull down device makes the PGOOD pin look approximately like a diode to GND.

7.3.11 Thermal Shutdown

If the junction temperature of the device reaches the thermal shutdown limit of 145°C, the PWM and the oscillator are turned off and the HDRV pin and the LDRV pin are driven low, turning off both FETs. When the junction cools to the required level (125°C nominal), the PWM inititates soft start as during a normal power up cycle.

7.4 Device Functional Modes

7.4.1 Continuous Conduction Mode

The TPS40192 and TPS40193 devices devices operate in continuous conduction mode, regardless of the output current. Following the first 32 cycles, during which the low-side MOSFET on-time is slowly increased to prevent current sinking due to a pre-biased output, the high-side MOSFET and low-side MOSFET on-times are fully complementary.

7.4.2 Low-Quiescent Shutdown

When the ENABLE pin of the TPS40192, and TPS40193 devices is held below 0.6 V, the device enters a low quiescent current shutdown mode, drawing only 45 µA typically from the VDD pin.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

This example illustrates the design process and component selection for a 12 V to 1.8 V point-of-load synchronous buck regulator using the TPS40192. A definition of symbols used can be found in Table 7 of this datasheet.

8.2 Typical Application

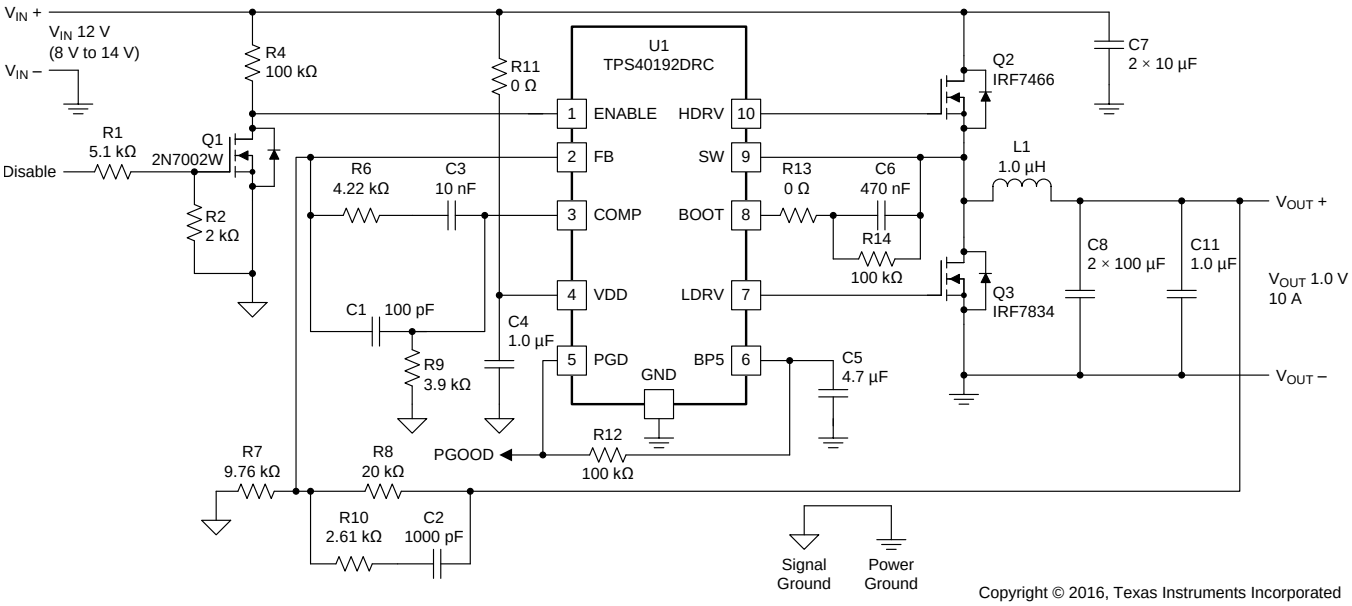


Figure 15. TPS40192 Design Example Schematic

Typical Application (continued)

8.2.1 Design Requirements

The requirements for this design are summarized in Table 2.

Table 2. Design Requirements

Parameter		Notes and Conditions	Min	Nom	Max	Units
Input Characteristics						
V_{IN}	Input voltage		8	12	14	V
I_{IN}	Input current	V_{IN} = 8 V, I_{OUT} = 10 A		2.7	2.85	A
	No load input current	V_{IN} = 8 V, I_{OUT} = 0 A		48	60	mA
VIN_UVLO	Input UVLO	0 A ≤ I_{OUT} ≤ 10 A	3.9	4.2	4.4	V
Output Characteristics						
V_{OUT}	Output voltage	V_{IN} = 12 V, I_{OUT} = 6 A		1.8		V
	Line regulation	8 V ≤ V_{IN} ≤ 14 V, I_{OUT} = 6 A			0.5%	
	Load regulation	V_{IN} = 12 V, 0 A ≤ I_{OUT} ≤ 10 A			0.5%	
$V_{OUT(ripple)}$	Output voltage ripple	V_{IN} = 12 V, I_{OUT} = 10 A			40	mVpp
I_{OUT}	Output current	8 V ≤ V_{IN} ≤ 14	0	6	10	A
I_{OCP}	Output overcurrent inception point	V_{IN} = 12 V, VOUT = VOUT-5%		19		A
Transient Response						
ΔI	Load step	0.75 x $I_{OUT(max)}$ to 0.25 × $I_{OUT(max)}$		5		A
	Load slew rate			5		A/µsec
	Overshoot				50	mV
Systems Characteristics						
f_{SW}	Switching frequency		480	600	720	kHz
ηpk	Peak efficiency	V_{IN} = 8 V, 0 A ≤ I_{OUT} ≤ 10 A		89%		
η	Full-load efficiency	V_{IN} = 8 V, I_{OUT} ≤ 10 A		86%		
T_J	Operating temperature range	8 V ≤ V_{IN} ≤ 14 V, 0 A ≤ I_{OUT} ≤ 10 A	-40	25	60	°C

8.2.2 Detailed Design Procedure

8.2.2.1 Selecting the Switching Frequency

Choose a switching f_{SW} of 600 kHz to reduce the required inductor and capacitor sizes.

8.2.2.2 Inductor Selection

The inductor is typically sized for approximately 30% peak-to-peak ripple current (I_{RIPPLE}). Given this target ripple current, the required inductor size can be calculated by Equation 6.

$$L \approx \frac{V_{IN(max)} - V_{OUT}}{I_{RIPPLE}} \times \frac{V_{OUT}}{V_{IN(max)}} \times \frac{1}{f_{SW}} = \frac{14\ V - 1.8\ V}{0.3 \times 10\ A} \times \frac{1.8\ V}{14\ V} \times \frac{1}{600\ kHz} = 0.87\ \mu H \quad (6)$$

A standard value of 1.0 µH is selected. Solving for I_{RIPPLE} using an inductor value of 1.0 µH, results in 2.6-A peak-to-peak ripple.

The RMS current through the inductor is approximated by Equation 7.

$$I_{L(rms)} = \sqrt{\left(I_{L(avg)}\right)^2 + \frac{1}{12} \times (I_{RIPPLE})^2} = \sqrt{(I_{OUT})^2 + \frac{1}{12} \times (I_{RIPPLE})^2}$$

$$= \sqrt{(10\ A)^2 + \frac{1}{12} \times (2.6\ A)^2} \approx 10.03\ A \quad (7)$$

Using Equation 7, the maximum RMS current in the inductor is approximately 10.03 A

8.2.2.3 Output Capacitor Selection (C8)

The selection of the output capacitor is typically driven by the output transient response. The Equation 8 and Equation 9 overestimate the voltage deviation to account for delays in the loop bandwidth and can be used to determine the required output capacitance.

$$V_{OVER} < \frac{I_{TRAN}}{C_{OUT}} \times \Delta t = \frac{I_{TRAN}}{C_{OUT}} \times \frac{I_{TRAN} \times L}{V_{OUT}} = \frac{(I_{TRAN})^2 \times L}{V_{OUT} \times C_{OUT}}$$

$$V_{UNDER} < \frac{I_{TRAN}}{C_{OUT}} \times \Delta t = \frac{I_{TRAN}}{C_{OUT}} \times \frac{I_{TRAN} \times L}{(V_{IN} - V_{OUT})} = \frac{(I_{TRAN})^2 \times L}{(V_{IN} - V_{OUT}) \times C_{OUT}} \quad (8)$$

If

- $V_{IN(min)} > 2 \times V_{OUT}$, use overshoot to calculate minimum output capacitance.
- $V_{IN(min)} < 2 \times V_{OUT}$, use undershoot to calculate minimum output capacitance. (9)

$$C_{OUT\,(min)} = \frac{(I_{TRAN\,(max)})^2 \times L}{V_{OUT} \times V_{OVER}} = \frac{(4\text{ A})^2 \times 1.0\ \mu\text{H}}{1.8\text{ V} \times 50\text{ mV}} = 178\ \mu\text{F} \quad (10)$$

With a minimum capacitance, the maximum allowable ESR is determined by the maximum ripple voltage and is approximated by Equation 11.

$$ESR_{MAX} < \frac{V_{RIPPLE\,(tot)} - V_{RIPPLE\,(cap)}}{C_{OUT}} = \frac{V_{RIPPLE\,(tot)} - \left(\frac{I_{RIPPLE}}{C_{OUT} \times f_{SW}}\right)}{I_{RIPPLE}}$$

$$= \frac{36\text{ mV} - \left(\frac{2.6\text{ A}}{178\ \mu\text{F} \times 600\text{ kHz}}\right)}{2.6\text{ A}} = 4.4\ \text{m}\Omega \quad (11)$$

Two 1206 100-µF, 6.3-V X5R ceramic capacitors are selected to provide more than 178-µF of minimum capacitance and less than 4.4 mΩ of ESR (2.5 mΩ each).

8.2.2.4 Peak Current Rating of the Inductor

With output capacitance, it is possible to calculate the charge current during start-up and determine the minimum saturation current rating for the inductor. The start-up charging current is approximated by Equation 12.

$$I_{CHARGE} = \frac{V_{OUT} \times C_{OUT}}{t_{SS}} = \frac{1.8\text{ V} \times 200\ \mu\text{F}}{3.0\text{ ms}} = 120\text{ mA} \quad (12)$$

$$I_{L(peak)} = I_{OUT\,(max)} + \left(\frac{1}{2} \times I_{RIPPLE}\right) + I_{CHARGE} = 10\text{ A} + \left(\frac{1}{2} \times 2.6\text{ A}\right) + 120\text{ mA} = 11.4\text{ A} \quad (13)$$

Table 3. Inductor Requirements

PARAMETER	SYMBOL	VALUE	UNITS
Inductance	L	1.0	µH
RMS current (thermal rating)	$I_{L(rms)}$	10.03	A
Peak current (saturation rating)	$I_{L(peak)}$	11.4	

A PG0083.102 1.0-µH is selected for its small size, low DCR (6.6 mΩ) and high current handling capability (12 A thermal, 17 A saturation)

8.2.2.5 Input Capacitor Selection (C7)

The input voltage ripple is divided between capacitance and ESR. For this design $V_{RIPPLE(cap)}$ = 400 mV and $V_{RIPPLE(ESR)}$ = 200 mV. Use Equation 14 to estimate the minimum capacitance and maximum ESR.

$$C_{IN\,(min)} = \frac{I_{OUT} \times V_{OUT}}{V_{RIPPLE\,(cap)} \times V_{IN\,(MIN)} \times f_{SW}} = \frac{10\text{ A} \times 1.8\text{ V}}{400\text{ mV} \times 8\text{ V} \times 600\text{ kHz}} = 9.375\ \mu\text{F} \quad (14)$$

$$ESR_{MAX} = \frac{V_{RIPPLE\ (esr)}}{I_{OUT} + \left(\frac{1}{2} \times I_{RIPPLE}\right)} = \frac{200\ mV}{10\ A + \left(\frac{1}{2} \times 2.6\ A\right)} = 17.7\ m\Omega \quad (15)$$

For this design $C_{IN(min)}$> 9.375 µF and ESR < 17.7 mΩ . Use Equation 16 to estimate the RMS current in the input capacitors.

$$I_{RMS\,(cin)} = I_{IN\,(rms)} - I_{IN\,(avg)} = \left(I_{OUT} + \frac{1}{12} \times I_{RIPPLE}\right) \times \sqrt{\frac{V_{OUT}}{V_{IN}}} - \frac{V_{OUT} \times I_{OUT}}{V_{IN}}$$

$$= \left(10\ A + \frac{1}{12} \times 2.6\ A\right) \times \sqrt{\frac{1.8\ V}{14\ V}} - \frac{1.8\ V \times 10\ A}{14\ V} = 2.37\ A \quad (16)$$

The total input capacitance must support 2.37 A of RMS ripple current.

Two 1210 10-µF, 25 V, X5R ceramic capacitors with approximately 2 mΩ ESR and a 2-A_{RMS} current rating are selected. Higher voltage capacitors minimize capacitance loss at the DC bias voltage to ensure the capacitors have sufficient capacitance at the working voltage.

8.2.2.6 MOSFET Switch Selection (Q1, Q2)

The switching losses for the high-side MOSFET are estimated by Equation 17.

$$P_{G1SW} = \frac{1}{2} \times V_{IN} \times I_{OUT} \times \Delta t_{SW} \times f_{SW} = \frac{1}{2} \times V_{IN} \times I_{OUT} \times \frac{Q_{GD1}}{\frac{V_{DRV} - V_{TH}}{R_{DRV}}} \times f_{SW} \quad (17)$$

Switching losses in this design are highest at high-line. Designing for 1 W of total loss in each MOSFET and 60% of the total high-side MOSFET losses in switching losses, estimate the maximum gate-drain charge for the design by using Equation 18.

$$Q_{GD1\,(max)} = \frac{P_{G1SW}}{V_{IN} \times I_{OUT}} \times \frac{V_{DRV} - V_{TH}}{R_{DRV}} \times \frac{1}{f_{SW}} = \frac{600\ mW}{14\ V \times 10\ A} \times \frac{5\ V - 2\ V}{2.5\ \Omega} \times \frac{1}{600\ kHz} = 8.6\ nC \quad (18)$$

The switching losses of the synchronous rectifier are lower than the switching losses of the main MOSFET because the voltage across the MOSFET at the point of switching is reduced to the forward voltage drop across the body diode of the SR MOSFET and are estimated by using Equation 19. The conduction losses in the main MOSFET are estimated by the RMS current through the MOSFET times its $R_{DS(on)}$.

$$P_{G1\,(CON)} = I_{L(rms)} \times R_{DS\,(on)Q1} \times \frac{V_{OUT}}{V_{IN}} \quad (19)$$

Estimating about 40% of total MOSFET losses to be high-side conduction losses, the maximum $R_{DS(on)}$ of the high-side MOSFET can be estimated by using Equation 20.

$$R_{DS\,(on)Q1,MAX} = \frac{P_{Q1CON}}{\left(I_{L(rms)}\right)^2 \times \frac{V_{OUT}}{V_{IN}}} = \frac{400\ mW}{(10.03\ A)^2 \times \frac{1.8\ V}{14\ V}} = 30.9\ m\Omega \quad (20)$$

Estimating 80% of total low-side MOSFET losses in conduction losses, repeat the calculation for the synchronous rectifier, whose losses are dominated by the conduction losses. Calculate the maximum $R_{DS(on)}$ of the synchronous rectifier by Equation 21.

$$R_{DS\,(on)Q2\_MAX} = \frac{P_{Q2CON}}{\left(I_{L(rms)}\right)^2 \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} = \frac{800\ mW}{10.03^2 \times \left(1 - \frac{1.8\ V}{14\ V}\right)} = 9.1\ m\Omega \quad (21)$$

Table 4. Power MOSFET Requirements

PARAMETER	SYMBOL	VALUE	UNITS
High-side MOSFET on-resistance	$R_{DS(on)Q1}$	30.9	mΩ
High-side MOSFET gate-to-drain charge	Q_{GD1}	8.5	nC
Low-side MOSFET on-resistance	$R_{DS(on)Q2}$	8.8	mΩ

The IRF7466 has an $R_{DS(on)MAX}$ of 30.9 mΩ at 4.5-V gate drive and only 8.0-nC V_{GD} "Miller" charge with a 4.5-V gate drive, and is chosen as a high-side MOSFET. The IRF7834 has an $R_{DS(on)Q1,MAX}$ of 5.5 mΩ at 4.5-V gate drive and 44 nC of total gate charge. These two FETs have maximum total gate charges of 23 nC and 44 nC respectively, which draws 40.2-mA from the 5-V regulator, less than its 50-mA minimum rating.

8.2.2.7 Boot Strap Capacitor

To ensure proper charging of the high-side MOSFET gate, limit the ripple voltage on the boost capacitor to less than 50 mV.

$$C_{BOOST} = 20 \times Q_{G1} = 20 \times 23\ nC = 460\ nF \quad (22)$$

Use the next higher standard value of 470 nF for the value of the bootstrap capacitor.

NOTE

It is recommended to add a high-resistance resistor in parallel with the bootstrap capacitor. Adding a small amount of load to the bootstrap capacitor (100 kΩ for a 100-nF typical capacitor) creates a discharge time constant for the bootstrap voltage following a shutdown event. This prevents the possibility of an inadvertent turn-on of the high-side MOSFET following shutdown via the ENABLE pin, due to leakage paths within the driver stage which can slowly transfer the bootstrap voltage to the HDRV pin following the shutdown. (See Figure 15)

8.2.2.8 Input Bypass Capacitor (C6)

As suggested, select a 1.0-μF ceramic bypass capacitor for VDD.

8.2.2.9 BP5 Bypass Capacitor (C5)

The recommended minimum 1.0-μF ceramic capacitance stabilizes the 5-V regulator. To limit regulator noise to less than 10 mV, the bypass capacitor is sized by using Equation 23.

$$C_{BP5} = 100 \times MAX(Q_{G1}, Q_{G2}) = 100 \times MAX(23\ nC, 44\ nC) \cong 4.4\ \mu F \quad (23)$$

Because the Q2 gate charge is larger than Q1 and the total gate charge of Q2 is 44 nC, a BP5 capacitor of 4.4-μF is calculated, and the next larger standard value of 4.7 μF is selected to limit noise on the BP5 regulator.

8.2.2.10 Input Voltage Filter Resistor (R11)

Because the minimum input voltage ($V_{IN(min)}$) is greater than 6.0 V, place a 0-Ω resistor in the VDD resistor location. If $V_{IN(min)}$ was < 6.0 V, an optional series VDD resistor with a value between 1 Ω and 2 Ω filters switching noise from the device. Limit the voltage drop across this resistor to less than 50 mV.

$$R_{VDD} = \frac{V_{RVDD\ (max)}}{I_{DD}} = \frac{50\ mV}{3\ mA + (Q_{G1,tot} + Q_{G2,tot}) \times f_{SW}} = \frac{50\ mV}{3\ mA + (44\ nC + 23\ nC) \times 600\ kHz)}$$
$$= \frac{50\ mV}{43\ mA} \cong 1\Omega \quad (24)$$

Driving the two FETs with 23 nC and 44 nC respectively, the maximum I_{VDD} current calculation of 43 mA yields a resistor value of approximately 1 Ω.

8.2.2.11 Short Circuit Protection (R9)

The devices use the negative drop across the low-side MOSFET during the OFF time to measure the inductor current. Equation 25 approximates the voltage drop across the low-side MOSFET.

$$V_{CS\,(max)} = I_{L(peak)} \times R_{DS\,(on),Q2,MAX} = 11.4\ A \times 5.5\ m\Omega \cong 62.7\ mV \quad (25)$$

The internal temperature coefficient of the TPS40192 device helps compensate for the MOSFET on-resistance ($R_{DS(on)}$) temperature coefficient. For this design select the short circuit protection voltage threshold of 110 mV by selecting R9 = 3.9 kΩ.

8.2.2.12 Feedback Compensation (Modeling the Power Stage)

The DC gain of the modulator is given by Equation 26.

$$A_{MOD} = \frac{dV_{OUT}}{dV_{COMP}} = \frac{dD}{V_{COMP}} \times V_{IN} = \frac{dt}{dV_{RAMP}} \times \frac{1}{t_{SW}} \times V_{IN} \quad (26)$$

Because the peak-to-peak ramp voltage given in the *Electrical Characteristics* table is projected from the ramp slope over a full switching period, the modulator gain can be calculated as Equation 27. The maximum modulator gain for this design is found to be 14 (23.0 dB).

$$A_{MOD\,(max)} = \frac{V_{IN\,(max)}}{V_{RAMP\ (pp)}} = \frac{14\ V}{1\ V_{PP}} = 14 \quad (27)$$

The L-C filter applies a double pole at the resonance frequency described in Equation 28.

$$f_{RES} = \frac{1}{2\pi \times \sqrt{L \times C}} = \frac{1}{2\pi \times \sqrt{1\ \mu H \times 200\ \mu F}} \cong 11.3\ kHz \quad (28)$$

At any frequency lower than this (11.3 kHz), the power stage has a DC gain of 23 dB and at any higher frequency the power stage gain drops off at -40 dB per decade. The ESR zero is approximated in Equation 29.

$$f_{ESR} = \frac{1}{2\pi \times C_{OUT} \times R_{ESR}} = \frac{1}{2\pi \times (2 \times 100\ \mu F) \times \left(\frac{2.5\ m\Omega}{2}\right)} = 636\ kHz \quad (29)$$

Using two 100 µF, 2.5 mΩ ESR ceramic output capacitors, the calculated f_{ESR} of 636 kHz is greater than 1/5th the switching frequency, and therefore outside the scope of the error amplifier design. The gain of the power stage would change to –20 dB per decade above f_{ESR}. The straight line approximation the power stage gain is described in Figure 16.

The following compensation design procedure assumes $f_{ESR} > f_{RES}$. For designs using large high-ESR bulk capacitors on the output where $f_{ESR} < f_{RES}$. Type-II compensation can be used but is not described in this data sheet.

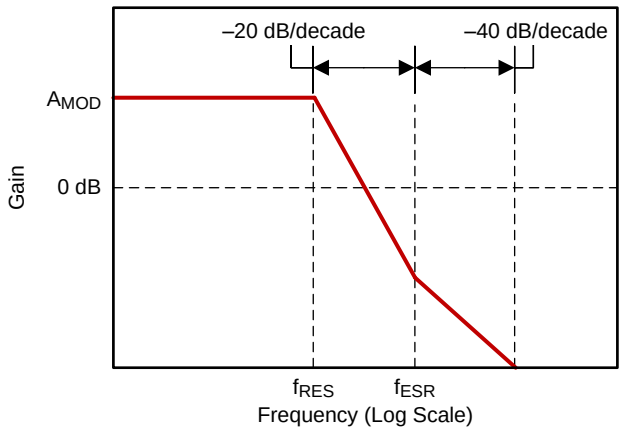


Figure 16. Approximation of Power Stage Gain

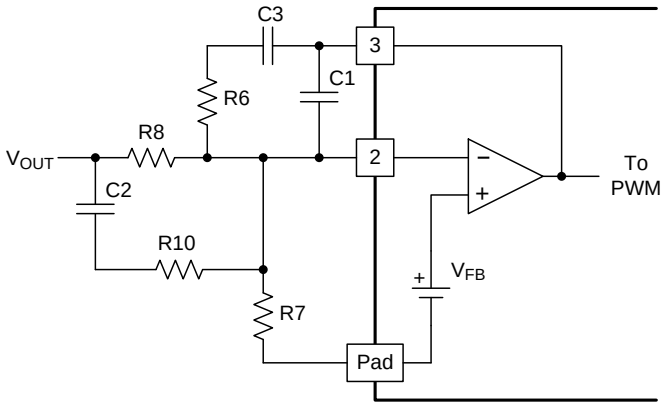


Figure 17. Type-III Compensator Used with TPS40040 or TPS40041

8.2.2.13 Feedback Divider (R7, R8)

Select a value for R8 between 10 kΩ and 100 kΩ. For this design, select 20 kΩ. R7 is then selected to produce the desired output voltage when V_{FB} = 0.591 V using Equation 30.

$$R7 = \frac{V_{FB} \times R8}{V_{OUT} - V_{FB}} = \frac{0.591\ V \times 20\ k\Omega}{1.8\ V - 0.591\ V} = 9.78\ k\Omega \quad (30)$$

Select the closest standard value of 9.76 kΩ. A slightly lower nominal value increases the nominal output voltage slightly to compensate for some trace impedance at load.

8.2.2.14 Error Amplifier Compensation (R6, R10, C1, C2, C3)

Place two zeros at 50% and 100% of the resonance frequency to boost the phase margin before resonance frequency generates –180° of phase shift. For f_{RES} = 11.7 kHz, f_{Z1} = 5.8 kHz and f_{Z2} = 11 kHz. Selecting the crossover frequency (f_{CO}) of the control loop between 3 times the LC filter resonance and 1/5th the switching frequency. For most applications 1/10th the switching frequency provides a good balance between ease of design and fast transient response.

- If $f_{ESR} < f_{CO}$; $f_{P1} = f_{ESR}$ and $f_{P2} = 4 \times f_{CO}$
- If $f_{ESR} > 2 \times f_{CO}$; $f_{P1} = f_{CO}$ and $f_{P2} = 8 \times f_{CO}$.

  For this design
- f_{SW} = 600 kHz
- f_{RES} = 11.7 kHz
- f_{ESR} = 636 kHz
- f_{CO} = 60 kHz and because
- $f_{ESR} > 2 \times f_{CO}$, $F_{P1} = f_{CO}$ = 60 kHz and $f_{P2} = 4 \times f_{CO}$ = 500 kHz.

Because $f_{CO} < f_{ESR}$ the power stage gain at the desired crossover can be approximated in Equation 31.

$$A_{PS\,(fco)} = A_{MOD\,(dc)} - 40\ \log\left(\frac{f_{CO}}{f_{RES}}\right) = 10^{APS\,(FCC)/20} = 10^{5.4\ dB/20} = 1.86 \quad (31)$$

Table 5. Error Amplifier Design Parameters

PARAMETER	SYMBOL	VALUE	UNITS
First zero frequency	f_{Z1}	5.8	kHz
Second zero frequency	f_{Z2}	11.0	
First pole frequency	f_{P1}	60	
Second pole frequency	f_{P2}	500	
Midband gain	$A_{MID(band)}$	1.86	V/V

Approximate C2 with the formula described in Equation 32.

$$C2 = \frac{1}{2\pi \times R8 \times f_{Z2}} = \frac{1}{2\pi \times 20\ k\Omega \times 11\ kHz} = 723\ pF \quad (32)$$

For a calculated value for C2 of 723 pF, the closest standard capacitor value is 1000 pF.

Approximate R10 using Equation 33.

$$R10 = \frac{1}{2\pi \times C2 \times f_{P1}} = \frac{1}{2\pi \times 1000\ pF \times 60\ kHz} = 2.65\ k\Omega \quad (33)$$

For a calculated value for R10 of 2.65 kΩ, the closest standard resistor value is 2.61 kΩ.

Calculate R6 using Equation 34.

$$R6 = \frac{A_{MID\,(band)} \times R10 \times R8}{R10 + R8} = \frac{1.86 \times 2.61\ k\Omega \times 20\ k\Omega}{2.61\ k\Omega + 20\ k\Omega} = 4.29\ k\Omega \quad (34)$$

For a calculated value for R6 of 4.29 kΩ, the closest standard resistor value is 4.22 kΩ.

Calculate C1 and C3 using Equation 35 and Equation 36.

$$C3 = \frac{1}{2\pi \times R6 \times f_{Z1}} = \frac{1}{2\pi \times 4.22\ k\Omega \times 5.8\ kHz} = 6.5\ nF \quad (35)$$

$$C1 = \frac{1}{2\pi \times R6 \times f_{P2}} = \frac{1}{2\pi \times 4.22\ k\Omega \times 500\ kHz} = 75\ pF \quad (36)$$

Using the a standard value close to 75 pF, select C1 = 100 pF. Likewise, using a standard value close to 6.5 nF, select C3 = 10 nF.

The error amplifier straight line approximation transfer function is described in Figure 18.

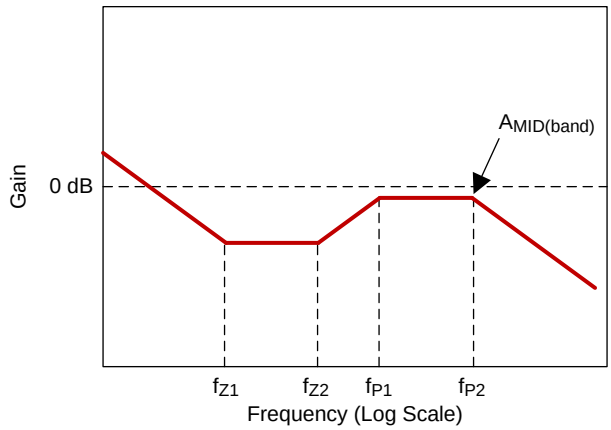


Figure 18. Error Amplifier Transfer Function Approximation

8.2.3 Application Curves

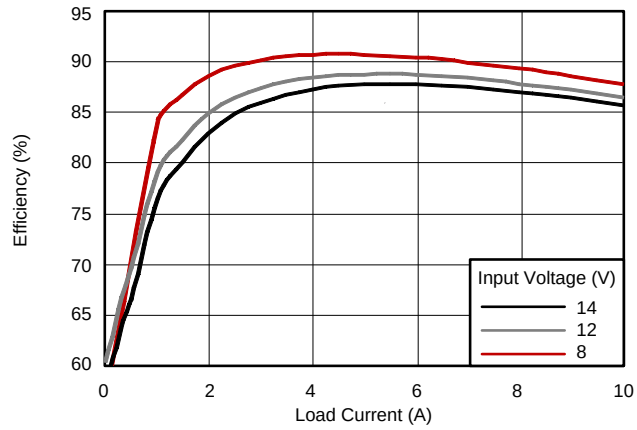


Figure 19. Efficiency vs. Output Current

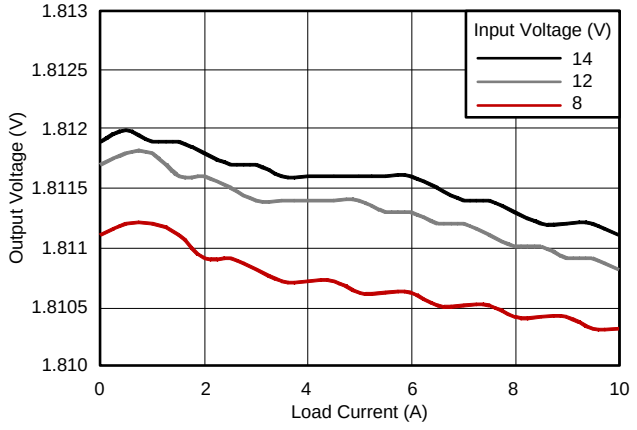


Figure 20. Output Voltage Regulation

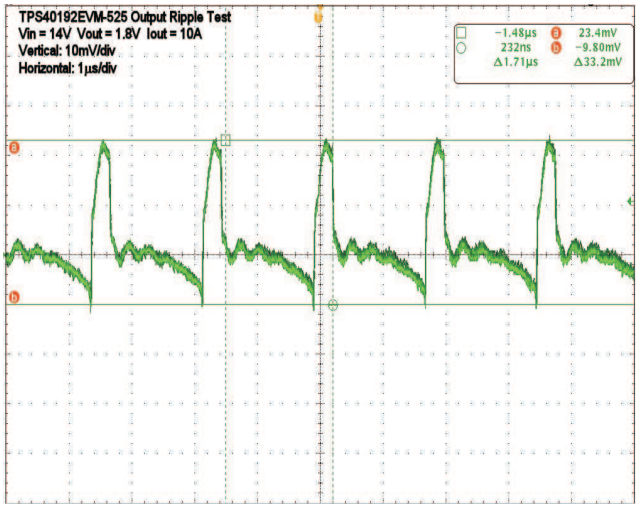


Figure 21. Output Voltage Ripple

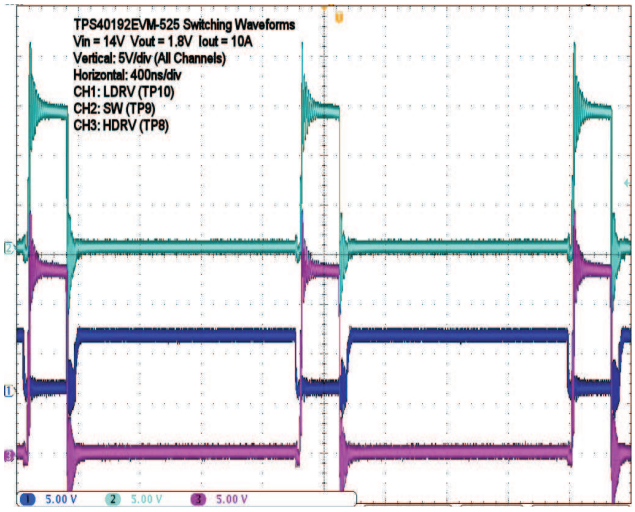


Figure 22. Switching Waveforms

9 Power Supply Recommendations

The TPS40192, and TPS40193 devices are designed to operate from a supply on the VDD pin, ranging from 4.5 V to 18 V. This supply must be well regulated and bypassed for proper operation of the devices. The VDD pin must be connected to the same supply as the power stage conversion input voltage for accurate high-side current sensing. The BP5 pin is the output of an internal low dropout regulator which is used to supply the gate drive voltages, and must also have good local bypassing for proper operation of the devices.

10 Layout

10.1 Layout Guidelines

- Optionally use R11 as a VDD filter resistor
- Locate the bypass capacitors (C7) near the power MOSFETs.
- Terminate signal components to a signal ground island separate from power ground
- Connect signal ground island to thermal pad with a single 10-mil wide trace.
- Connect power ground to the source of the synchronous rectifier.
- The thermal pad serves as the only ground for the controller.
- PowerPAD must be connected to signal ground and power ground at a single point only. Connect the PowerPad to the system ground.
- PowerPad™ should be directly connected to SYNC MOSFET (Q3) source with short, wide trace.
- Locate 3-5 vias in PowerPad™ land to remove heat from the device.
- Connect input capacitors (C7 and C9) and output capacitors (C8 andC10) grounds directly to SYNC MOSFET (Q3) source with wide copper trace or solid power ground island.
- Locate input capacitors (C7 and C9), MOSFETs (Q2 and Q3), inductor (L1) and output capacitor (C8 andC10) over power ground island.
- Use short, wide traces for LDRV and HDRV MOSFET connections.
- Route SW trace near HDRV trace.
- Route GND trace near LDRV trace.
- Use separate analog ground island under feedback components (C1, C2, C3, R5, R6, R7, R8 and R10).
- Connect ground islands at PowerPad™ with 10-mil wide trace opposite SYNC MOSFET (Q2) source connection.

10.2 Layout Examples

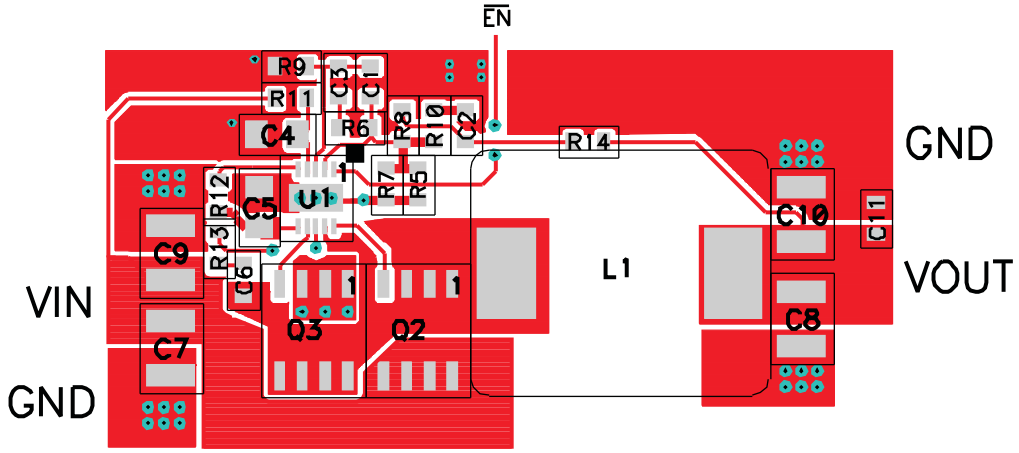


Figure 23. TPS40192 and TPS40193 devices Sample Layout - Component Placement and Top Side Copper

Layout Examples (continued)

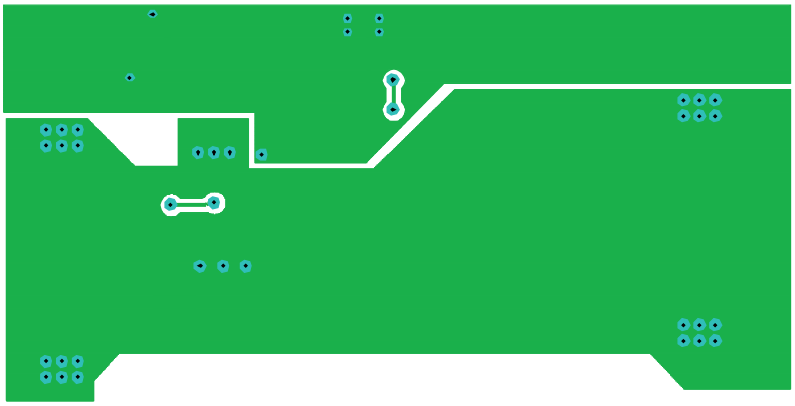


Figure 24. TPS40192 and TPS40193 devices Sample Layout - Bottom Side Copper (X-Ray view from Top)

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 Related Devices

The following devices have characteristics similar to the TPS40192 and TPS40193.

Table 6. Related Devices

DEVICE	DESCRIPTION
TPS40100	Midrange Input Synchronous Controller with Advanced Sequencing and Output Margining
TPS40075	Wide Input Synchronous Controller with Voltage Feed Forward
TPS40190	Low Pin Count Synchronous Buck Controller

11.1.2 Device Nomenclature

Table 7. Definition of Symbols

SYMBOL	DESCRIPTION
$V_{IN(max)}$	Maximum operating input voltage
$V_{IN(min)}$	Minimum operating input voltage
$V_{IN(ripple)}$	Peak- to-peak AC ripple voltage on V_{IN}
V_{OUT}	Target output voltage
$V_{OUT(ripple)}$	Peak- to-peak AC ripple voltage on V_{OUT}
$I_{OUT(max)}$	Maximum operating load current
I_{RIPPLE}	Peak-to-Peak ripple current through Inductor
$I_{L(peak)}$	Peak current through inductor
$I_{L(rms)}$	Root mean squared current through inductor
$I_{RMS(Cin)}$	Root mean squared current through input capacitor
f_{SW}	Switching frequency
f_{CO}	Desired control loop crossover frequency
A_{MOD}	Low frequency gain of the pwm modulator (V_{OUT} / $V_{CONTROL}$)
$V_{CONTROL}$	PWM control voltage (error amplifier output voltage V_{COMP})
f_{RES}	L-C filter resonant frequency
f_{ESR}	Output capacitor ESR zero frequency
f_{P1}	First pole frequency in error amplifier compensation
f_{P2}	Second pole frequency in error amplifier compensation
f_{Z1}	First zero frequency in error amplifier compensation
f_{Z2}	Second pole frequency in error amplifier compensation
Q_{G1}	Total gate charge of main MOSFET
Q_{G2}	Total gate charge of synchronous rectifier MOSFET
$R_{DS(on)Q1}$	"ON" drain-to-source resistance of main MOSFET
$R_{DS(on)Q2}$	"ON" drain-to-source resistance of synchronous rectifier MOSEFT
$P_{Q1C(on)}$	Conduction losses in main switching MOSFET
P_{Q1SW}	Switching losses in main switching MOSFET
$P_{Q2C(on)}$	Conduction losses in synchronous rectifier MOSFET
Q_{GD}	Gate-to-drain charge of synchronous rectifier MOSFET
Q_{GS}	Gate-t-source charge of synchronous rectifier MOSFET

11.2 Documentation Support

Access these reference documents as well as design tools and links to additional references, including design software at www.power.ti.com.

- *Under The Hood Of Low Voltage DC/DC Converters*, SEM1500 Topic 5, 2002 Seminar Series
- *Understanding Buck Power Stages in Switchmode Power Supplies*, March 1999
- *Design and Application Guide for High Speed MOSFET Gate Drive Circuits*, SEM 1400, 2001 Seminar Series
- *Designing Stable Control Loops*, SEM 1400, 2001 Seminar Series
- *PowerPAD™ Thermally Enhanced Package* Application Report
- *PowerPAD™ Made Easy* Application Report
- *QFN/SON PCB Attachment* Application Report

11.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 8. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS40192	Click here	Click here	Click here	Click here	Click here
TPS40193	Click here	Click here	Click here	Click here	Click here

11.4 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.5 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.6 Trademarks

E2E is a trademark of Texas Instruments.

11.7 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.8 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS40192DRCR	ACTIVE	VSON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	0192	Samples
TPS40192DRCRG4	ACTIVE	VSON	DRC	10		TBD	Call TI	Call TI	-40 to 85		Samples
TPS40192DRCT	ACTIVE	VSON	DRC	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	0192	Samples
TPS40192DRCTG4	ACTIVE	VSON	DRC	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	0192	Samples
TPS40193DRCR	ACTIVE	VSON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	0193	Samples
TPS40193DRCRG4	ACTIVE	VSON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	0193	Samples
TPS40193DRCT	ACTIVE	VSON	DRC	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	0193	Samples
TPS40193DRCTG4	ACTIVE	VSON	DRC	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	0193	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

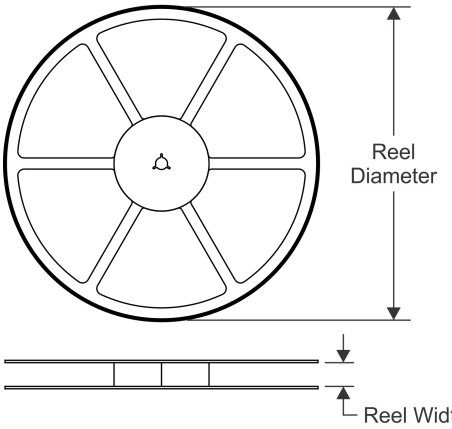
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

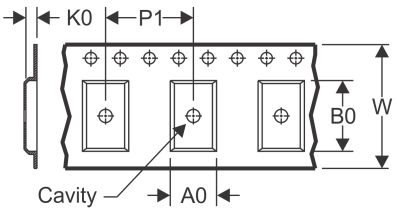
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

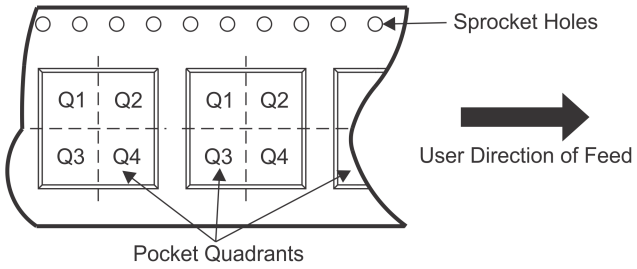


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

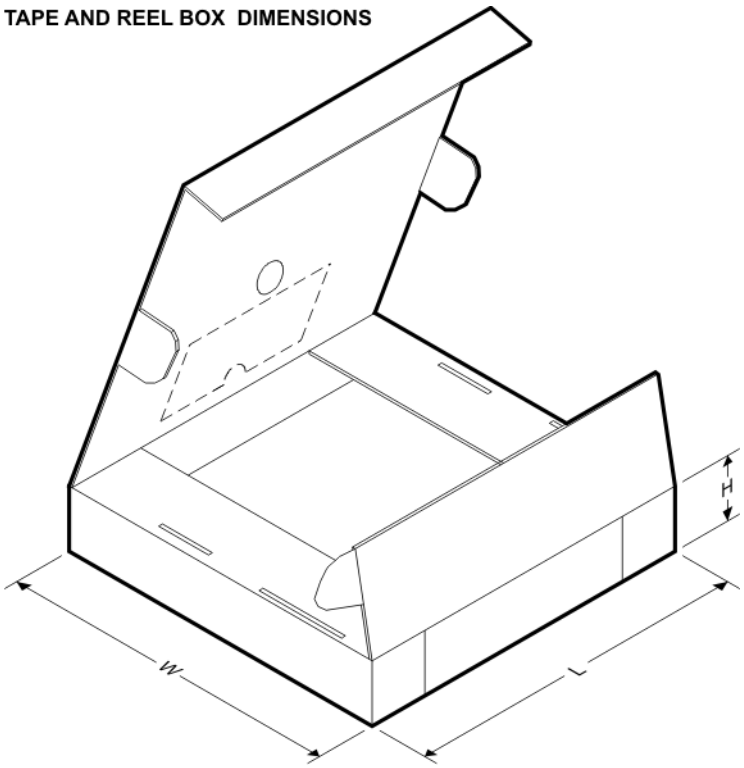
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS40192DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
TPS40192DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS40192DRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
TPS40192DRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS40193DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS40193DRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

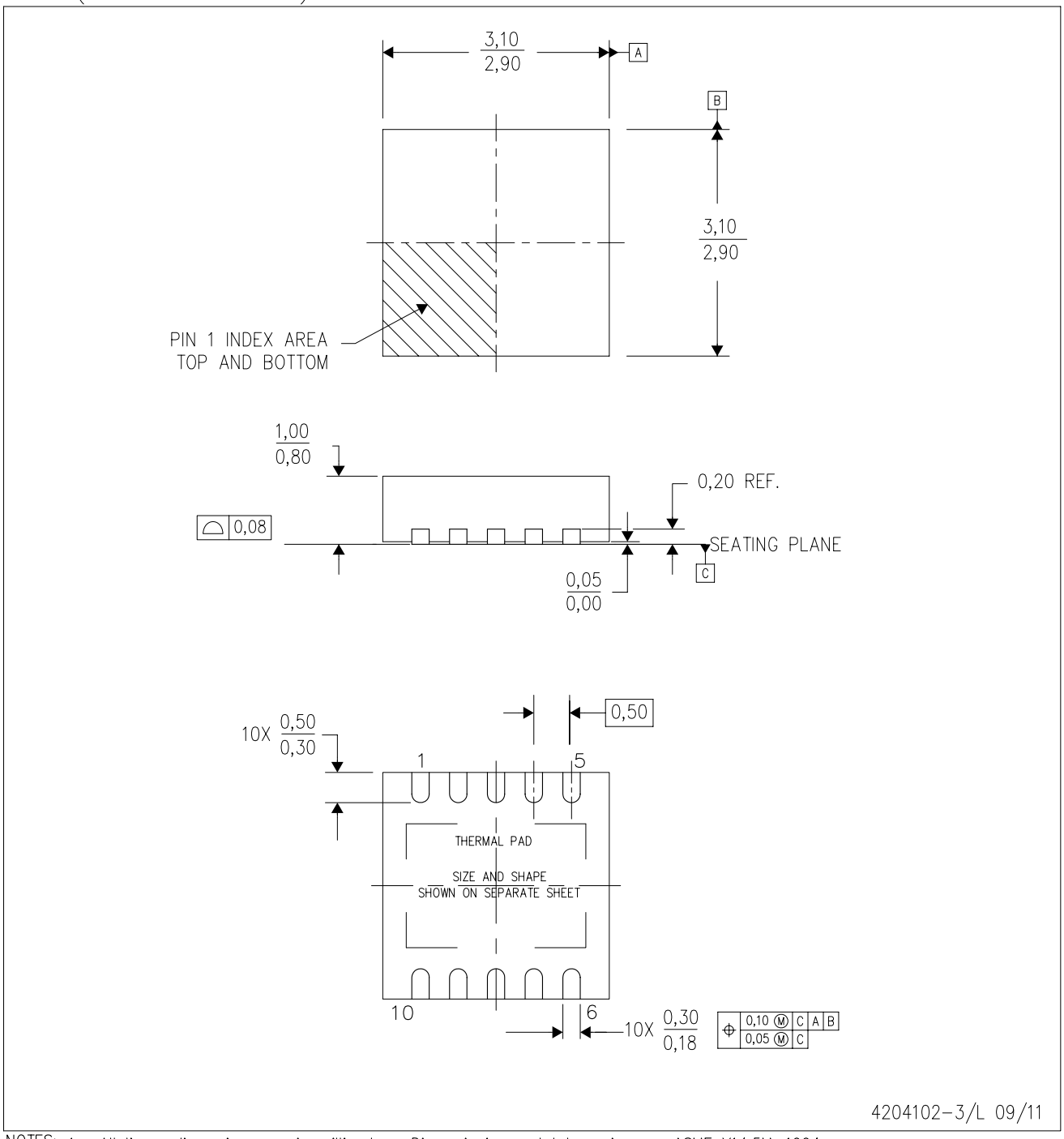
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS40192DRCR	VSON	DRC	10	3000	370.0	355.0	55.0
TPS40192DRCR	VSON	DRC	10	3000	367.0	367.0	35.0
TPS40192DRCT	VSON	DRC	10	250	195.0	200.0	45.0
TPS40192DRCT	VSON	DRC	10	250	210.0	185.0	35.0
TPS40193DRCR	VSON	DRC	10	3000	367.0	367.0	35.0
TPS40193DRCT	VSON	DRC	10	250	210.0	185.0	35.0

DRC (S–PVSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance, if present.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions, if present

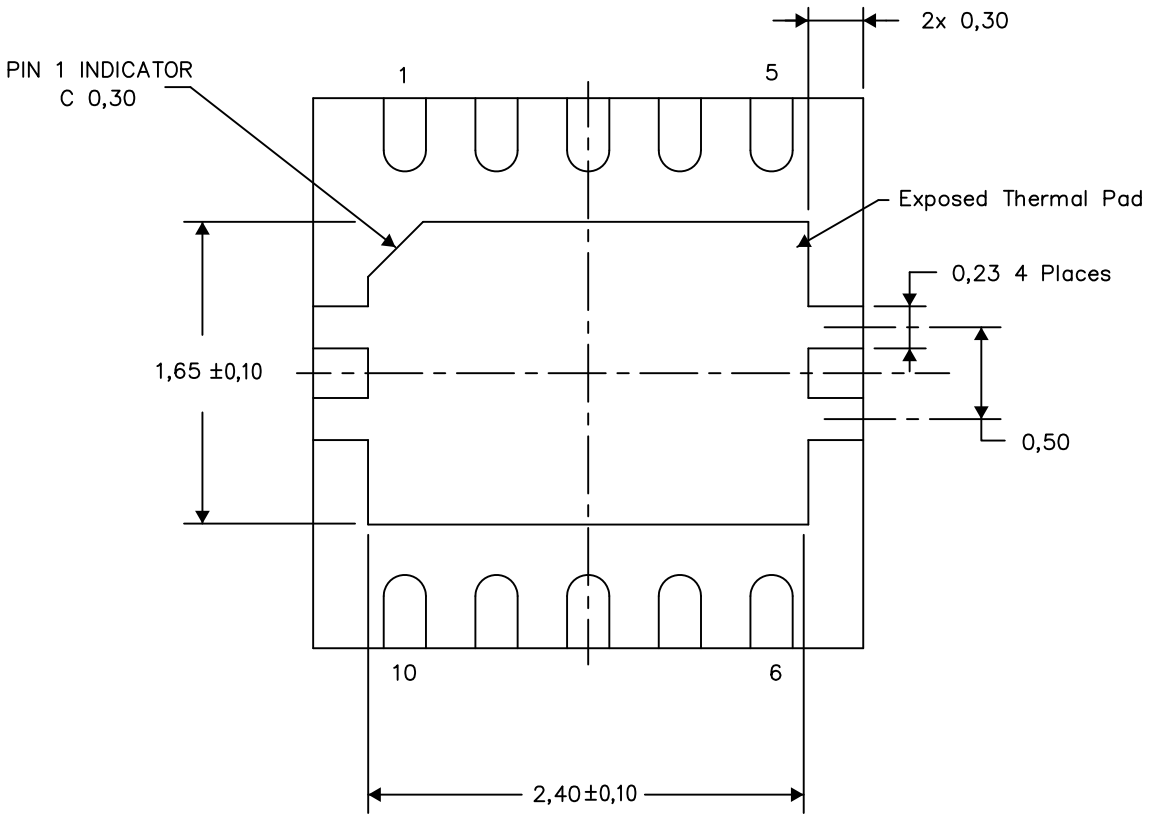
DRC (S–PVSON–N10) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



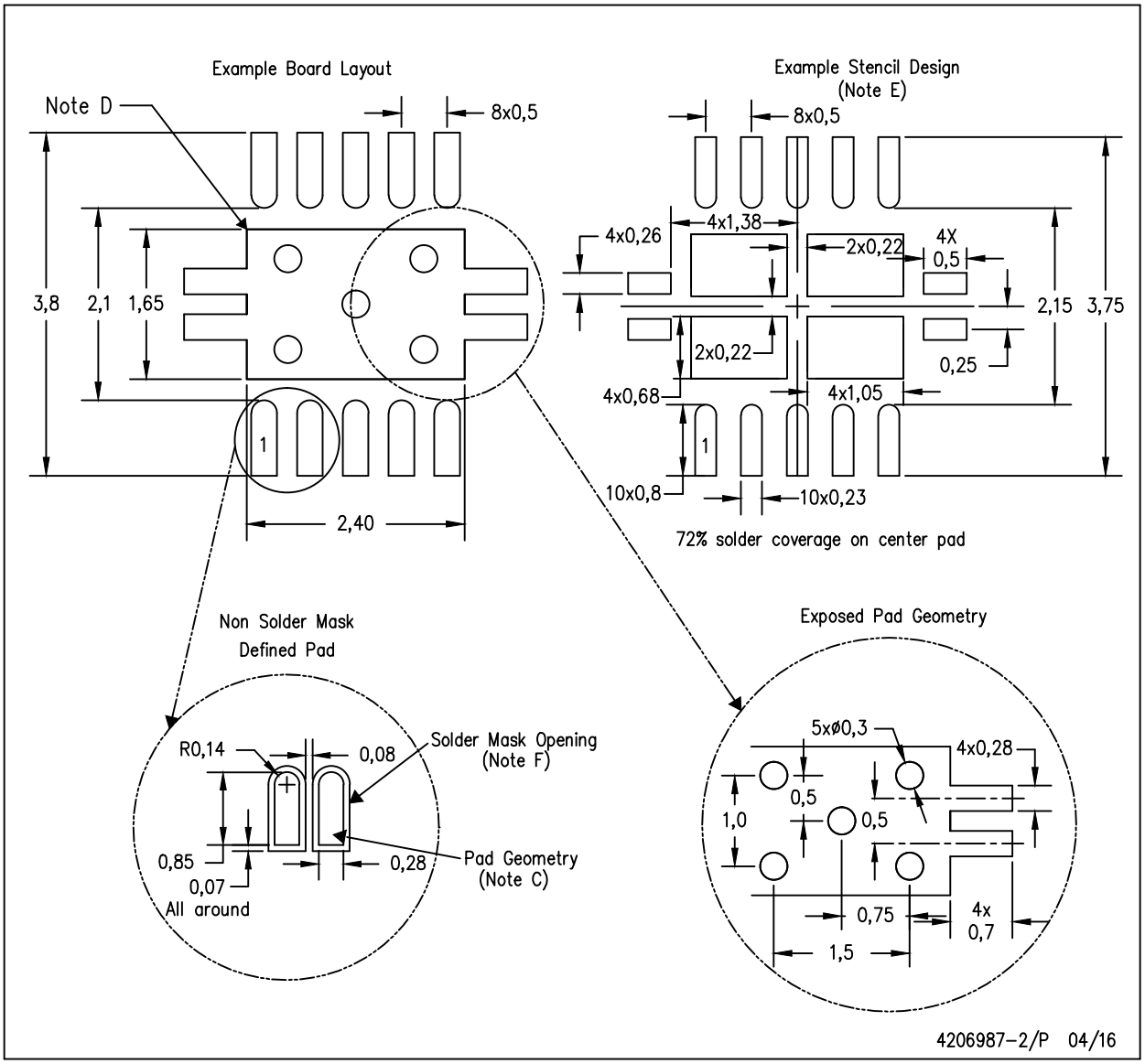
Bottom View

Exposed Thermal Pad Dimensions

4206565–3/Y 08/15

NOTE: A. All linear dimensions are in millimeters

DRC (S–PVSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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