

1.6-V TO 6.3-V INPUT, 6-A SYNCHRONOUS STEP DOWN SWIFT™ CONVERTER

 Check for Samples: [TPS50601-DIE](#)

FEATURES

- Split Power Rail: 1.6 V to 6.3 V on PVIN
- Power Rail: 3 V to 6.3 V on VIN
- Flexible Switching Frequency Options:
 - Adjustable Internal Oscillator
 - External Sync Capability
 - Sync Pin Can Be Configured as a 500-kHz Output for Master/Slave Applications
- Monotonic Start-Up into Pre-Biased Outputs
- Adjustable Slow Start and Power Sequencing
- Power Good Output Monitor for Undervoltage and Overvoltage
- Adjustable Input Undervoltage Lockout

APPLICATIONS

- Point of Load Regulation

DESCRIPTION

The TPS50601-DIE is a 6.3-V, 6-A synchronous step down converter which is optimized for small designs through high efficiency and integrating the high-side and low-side MOSFETs. Further space savings are achieved through current mode control, which reduces component count, and a high switching frequency, reducing the inductor's footprint.

The output voltage startup ramp is controlled by the SS/TR pin which allows operation as either a stand alone power supply or in tracking situations. Power sequencing is also possible by correctly configuring the enable and the open drain power good pins.

Cycle by cycle current limiting on the high-side FET protects the device in overload situations and is enhanced by a low-side sourcing current limit which prevents current runaway. There is also a low-side sinking current limit which turns off the low-side MOSFET to prevent excessive reverse current. Thermal shutdown disables the part when die temperature exceeds thermal shutdown temperature.

ORDERING INFORMATION⁽¹⁾

PRODUCT	PACKAGE DESIGNATOR	PACKAGE	ORDERABLE PART NUMBER	PACKAGE QUANTITY
TPS50601	TD	Bare die in waffle pack ⁽²⁾	TPS50601VTDC1	77
			TPS50601VTDC2	10

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
- (2) Processing is per the Texas Instruments space production baseline and is in compliance with the Texas Instruments Quality Control System in effect at the time of manufacture. Electrical screening consists of DC parametric and functional testing at room temperature only. Unless otherwise specified by Texas Instruments AC performance and performance over temperature is not warranted. Visual Inspection is performed in accordance with MIL-STD-883 Test Method 2010 Condition B at 75X minimum.



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

BARE DIE INFORMATION

DIE THICKNESS	BACKSIDE FINISH	BACKSIDE POTENTIAL	BOND PAD METALLIZATION COMPOSITION	BOND PAD THICKNESS
15 mils.	Silicon with backgrind	Floating	Al5TiN	557.5 nm

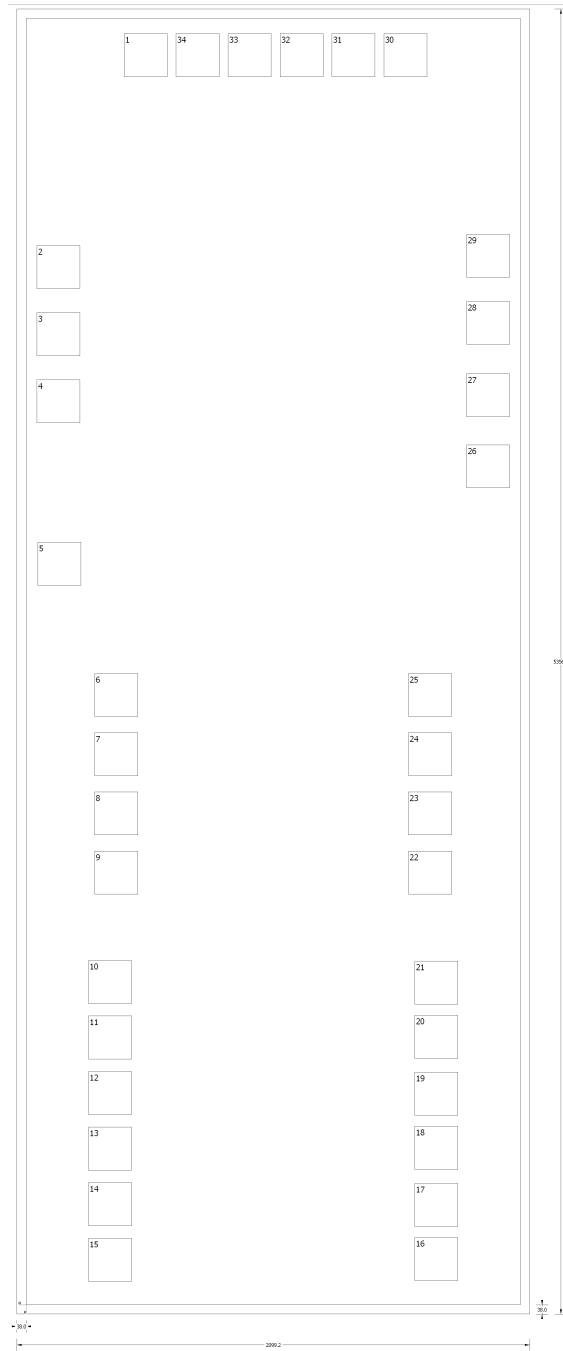


Table 1. Bond Pad Coordinates in Microns

DESCRIPTION	PAD NUMBER	X MIN	Y MIN	X MAX	Y MAX
GND	1	400.77	5039.325	578.07	5216.625
EN	2	44.19	4169.79	221.49	4347.09
RT	3	44.19	3894.21	221.49	4071.51
SYNC	4	44.19	3618.63	221.49	3795.93
VIN	5	47.565	2952.27	224.865	3129.57
PVIN	6	280.215	2414.115	457.515	2591.415
PVIN	7	280.215	2170.665	457.515	2347.965
PVIN	8	280.215	1928.115	457.515	2105.415
PVIN	9	280.215	1684.665	457.515	1861.965
PVIN	10	254.52	1236.285	431.82	1413.585
PVIN	11	254.52	1008.315	431.82	1185.615
PVIN	12	254.52	780.345	431.82	957.645
PVIN	13	254.52	552.375	431.82	729.675
PVIN	14	254.52	324.405	431.82	501.705
PVIN	15	254.52	96.435	431.82	273.735
PGND	16	1590.12	99.405	1767.42	276.705
PGND	17	1590.12	321.435	1767.42	498.735
PGND	18	1590.12	555.345	1767.42	732.645
PGND	19	1590.12	777.375	1767.42	954.675
PGND	20	1590.12	1011.285	1767.42	1188.585
PGND	21	1590.12	1233.315	1767.42	1410.615
PGND	22	1564.335	1684.665	1741.635	1861.965
PGND	23	1564.335	1928.115	1741.635	2105.415
PGND	24	1564.335	2170.665	1741.635	2347.965
PGND	25	1564.335	2414.115	1741.635	2591.415
PGND	26	1801.71	3352.14	1979.01	3529.44
PGND	27	1801.71	3644.145	1979.01	3821.445
PH	28	1801.71	3940.92	1979.01	4118.22
PH	29	1801.71	4216.5	1979.01	4393.8
PH	30	1463.67	5039.325	1640.97	5216.625
GND	31	1251.09	5039.325	1428.39	5216.625
GND	32	1038.51	5039.325	1215.81	5216.625
GND	33	825.93	5039.325	1003.23	5216.625
GND	34	613.35	5039.325	790.65	5216.625

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS50601VTDC1	ACTIVE			0	77	TBD	Call TI	N / A for Pkg Type			Samples
TPS50601VTDC2	ACTIVE			0	10	TBD	Call TI	N / A for Pkg Type			Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

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Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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