Single Synchronous Step-down Controller for Low Voltage Power Rails

Check for Samples: TPS53015

FEATURES

- **D-CAP2™ Mode Control**
  - **Fast Transient Response**
  - **No External Parts Required For Loop Compensation**
  - **Compatible with Ceramic Output Capacitors**
- **High Initial Reference Accuracy (±1%)**
- **Wide Input Voltage Range: 4.5 V to 28 V**
- **Output Voltage Range: 0.77 V to 7.0 V**
- **Low-Side $R_{DS(on)}$ Loss-Less Current Sensing**
- **1.4 ms Fixed Soft Start**
- **Non-Sinking Pre-Biased Soft Start**
- **500 kHz Switching Frequency**
- **Cycle-By-Cycle Over Current Limiting Control**
- **Auto-Skip Eco-Mode™ for High Efficiency at Light load**
- **Power Good Output**
- **OCL/OVP/UVP/UVLO/TSD Protections**
- **Adaptive Gate Drivers with Integrated Boost PMOS Switch**
- **Thermally Compensated OCP, 4000 ppm/°C**
- **10 pin VSSOP**

APPLICATIONS

- **Point-of-Load Regulation in Low Power Systems for Wide Range of Applications**
  - **Digital TV Power Supply**
  - **Networking Home Terminal**
  - **Digital Set Top Box (STB)**
  - **DVD Player / Recorder**
  - **Gaming Consoles and Other**

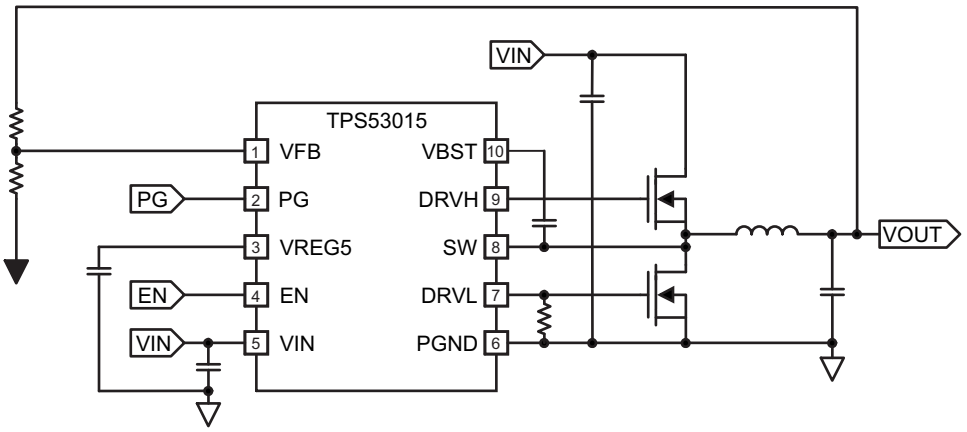
DESCRIPTION

The TPS53015 is a single, adaptive on-time D-CAP2™ mode synchronous buck controller. The TPS53015 enables system designers to complete the suite of various end equipment's power bus regulators with cost effective low external component count and low standby current solution. The main control loop for the TPS53015 uses the D-CAP2™ mode control which provides a very fast transient response with no external compensation components. The Adaptive on-time control supports seamless transition between PWM mode at higher load condition and Eco-mode™ operation at light load. Eco-mode™ allows the TPS53015 to maintain high efficiency during lighter load conditions. The TPS53015 is also able to adapt to both low equivalent series resistance (ESR) output capacitors such as POSCAP or SP-CAP and ultra-low ESR ceramic capacitors. The device provides convenient and efficient operation with input voltages from 4.5 V to 28 V and output voltage from 0.77 V to 7.0 V.

The TPS53015 is available in the 3.0mm x 3.0 mm 10-pin VSSOP (DGS) package, and is specified for an ambient temperature range of –40°C to 85°C.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

TYPICAL APPLICATION CIRCUITS



ORDERING INFORMATION (1)

T_A	PACKAGE(1)	ORDERING PART NUMBER	PINS	OUTPUT SUPPLY	ECO PLAN
–40°C to 85°C	VSSOP	TPS53015DGSR	10	Tape-and-Reel	Green (RoHS & no Sb/Br)
		TPS53015DGS		Tube	

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

Operating under free-air temperature range (unless otherwise noted) (1)

			VALUE	UNIT
Input voltage range		VIN, EN	–0.3 to 30	V
		VBST	–0.3 to 36	
		VBST - SW	–0.3 to 6	
		VFB	–0.3 to 6	
		SW	–0.3 to 30	
		SW (10 nsec transient)	–3.0 to 30	
Output voltage range		DRVH	–2 to 36	V
		DRVH - SW	–0.3 to 6	
		DRVL, VREG5, PG	–0.3 to 6	
		PGND	–0.3 to 0.3	
T_A	Operating ambient temperature range		–40 to 85	°C
T_{STG}	Storage temperature range		–55 to 150	°C
T_J	Junction temperature range		–40 to 150	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

THERMAL INFORMATION

THERMAL METRIC(1)		TPS53015 DGS (10 PINS)	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	172.2	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	44.0	
θ_{JB}	Junction-to-board thermal resistance	93.0	
ψ_{JT}	Junction-to-top characterization parameter	1.6	
ψ_{JB}	Junction-to-board characterization parameter	91.4	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
Supply input voltage range	VIN	4.5	28	V
Input voltage range	VBST	–0.1	33.5	V
	VBST - SW	–0.1	5.5	
	VFB	–0.1	5.5	
	EN	–0.1	28	
	SW	–1.0	28	
Output Voltage range	DRVH	–1.0	33.5	V
	DRVH - SW	–0.1	5.5	
	DRVL, VREG5, PG	–0.1	5.5	
	PGND	–0.1	0.1	
T_A Operating free-air temperature		–40	85	°C
T_J Operating junction temperature		–40	125	°C

ELECTRICAL CHARACTERISTICS

over recommended free-air temperature range, VIN = 12 V (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I_{IN}	VIN Supply current	VIN current, T_A = 25°C, EN = 5V, V_{VFB} = 0.8V, V_{SW} = 0 V		660		µA
I_{VINSDN}	VIN Shutdown current	VIN current, T_A = 25°C, No Load , V_{EN} = 0V, VREG5 = OFF		6.0		µA
VFB VOLTAGE and DISCHARGE RESISTANCE						
V_{VFBTHL}	VFB Threshold voltage	T_A = 25°C , V_{OUT} = 1.05 V	765.3	773.0	780.7	mV
TC_{VFB}	VFB Temperature coefficient	Relative to T_A = 25°C(1)	-140		140	ppm/°C
I_{VFB}	VFB Input current	VFB = 0.8V, T_A = 25°C	-150	-10	100	nA
VREG5 OUTPUT						
V_{VREG5}	VREG5 Output voltage	T_A=25°C, 6 V < V_{IN} < 28 V, I_{VREG5} = 5 mA		5.1		V
I_{VREG5}	Output current	VIN = 5.5V, V_{VREG5} = 4.0V, T_A = 25°C		120		mA
OUTPUT: N-CHANNEL MOSFET GATE DRIVERS						
R_{DRVH}	DRVH resistance	Source, I_{DRVH} = –50mA, T_A = 25°C		3.2	4.7	Ω
		Sink, I_{DRVH} = 50mA, T_A = 25°C		1.4	2.4	
R_{DRVL}	DRVL resistance	Source, I_{DRVL} = –50mA, T_A = 25°C		6.9	8.2	Ω
		Sink, I_{DRVL} = 50mA, T_A = 25°C		0.8	1.7	
T_D	Dead time	DRVH-low to DRVL-on(1)		15		ns
		DRVL-low to DRVH-on(1)		20		

(1) Ensured by design. Not production tested.

ELECTRICAL CHARACTERISTICS (continued)

over recommended free-air temperature range, VIN = 12 V (unless otherwise noted)

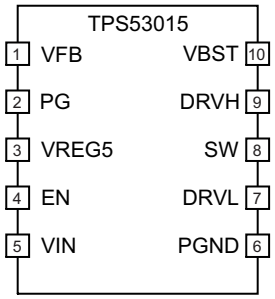
PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
INTERNAL BOOST DIODE						
V_{FBST}	Forward voltage	$V_{VREG5-VBST}$, I_F = 10mA, T_A = 25°C		0.1	0.2	V
SOFT START						
T_{ss}	Internal soft start time			1.4		ms
POWER GOOD						
V_{PGTH}	PGOOD threshold	PGOOD LOW		84		%
		PGOOD HIGH		116		%
I_{PG}	PGOOD sink current	V_{PG} = 0.5 V		5		mA
T_{PGDLY}	PGOOD delay time	Delay for PGOOD in		1.2		ms
		Delay for PGOOD out		2		µs
$T_{PGCOMPSS}$	PGODD comparator start up delay	PGOOD comparator wake up delay		2.3		ms
UVLO						
$V_{UVVREG5}$	VREG5 UVLO threshold	VREG5 Rising		4.0		V
		Hysteresis		0.3		
LOGIC THRESHOLD						
V_{ENH}	EN H-level threshold voltage		1.6			V
V_{ENL}	EN L-level threshold voltage				0.5	V
R_{EN}	EN pin resistance to GND	V_{EN} = 12 V	225	450	900	kΩ
CURRENT SENSE						
I_{TRIP}	TRIP Source current	V_{DRVL} = 0.1V, T_A = 25°C	14.3	15	15.8	µA
TC_{VTRIP}	V_{TRIP} Temperature coefficient	Relative to T_A = 25°C		4000		ppm/°C
V_{OCL}	Current limit threshold	R_{TRIP} = 75kΩ, T_A = 25°C	234	336	424	mV
		R_{TRIP} = 27kΩ, T_A = 25°C	121	174	220	
		R_{TRIP} = 6.8kΩ, T_A = 25°C	35	50	63	
ON-TIME TIMER CONTROL						
T_{ON}	On time	V_{OUT} = 1.05 V(2)		250		ns
$T_{OFF(MIN)}$	Minimum off time	V_{IN} = 4.5 V, V_{VFB} = 0.7 V, T_A = 25°C		230		ns
OUTPUT UNDERVOLTAGE AND OVERVOLTAGE PROTECTION						
V_{OVP}	Output OVP trip threshold	OVP detect voltage	115	120	125	%
T_{OVPDEL}	Output OVP propagation delay				10	µs
V_{UVP}	Output UVP trip threshold	UVP detect voltage	63	68	73	%
T_{UVPDEL}	Output UVP delay			1		ms
T_{UVPEN}	Output UVP enable delay		1.7	2.2	2.7	ms
THERMAL SHUTDOWN						
T_{SDN}	Thermal shutdown threshold	Shutdown temperature(2)		150		°C
		Hysteresis(2)		25		

(2) Ensured by design. Not production tested.

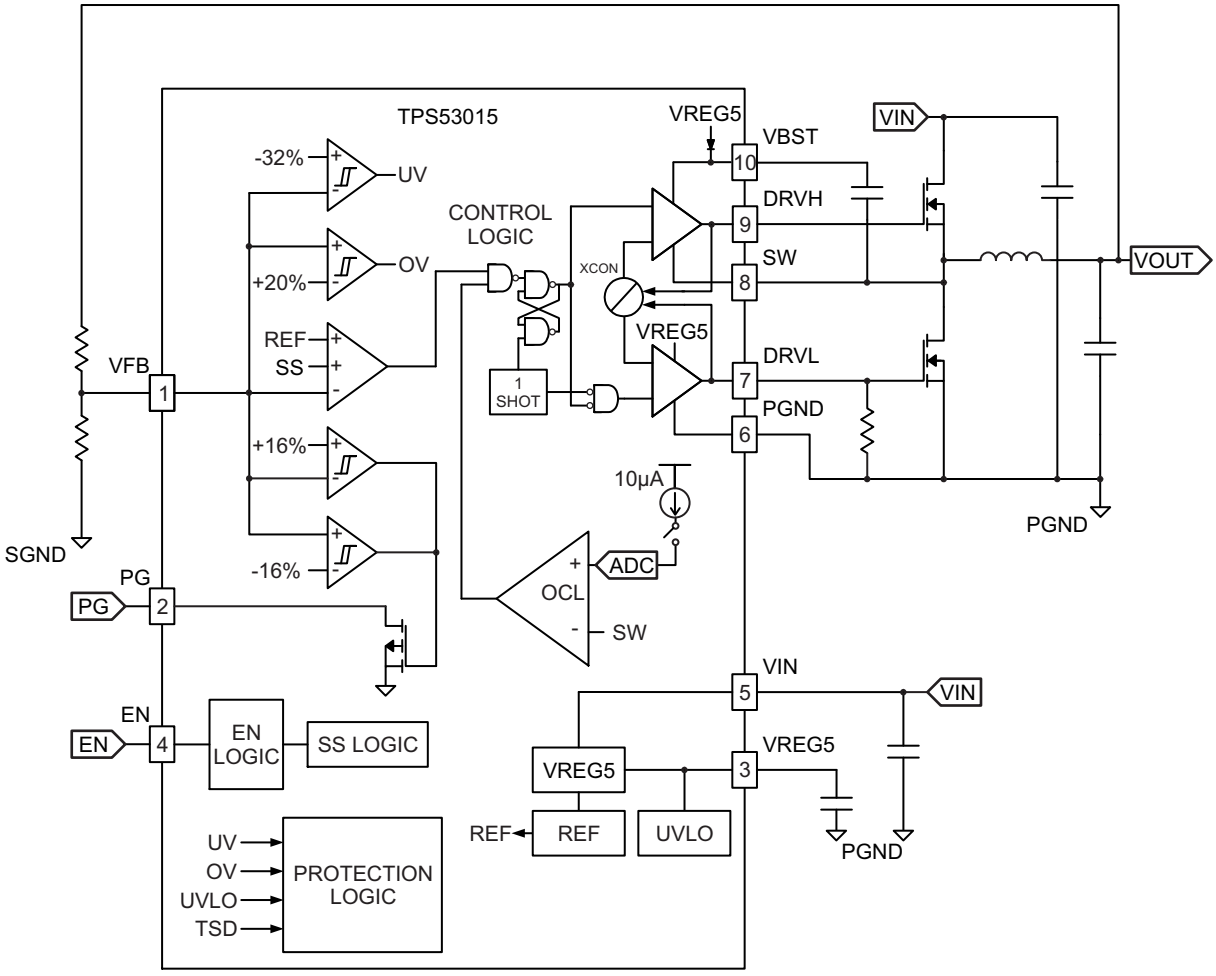
PIN FUNCTIONS

PIN		I/O	DESCRIPTION
NAME	VSSOP-10		
VFB	1	I	D-CAP2 feedback input. Connect to output voltage with resistor divider.
PG	2	O	Open drain power good output.
VREG5	3	O	Output of 5-V linear regulator and supply for MOSFET driver. Bypass to GND with a minimum 4.7-µF high quality ceramic capacitor. VREG5 is active when EN is asserted high.
EN	4	I	Enable. Pull High to enable converter.
VIN	5	I	Supply Input for 5-V linear regulator. Bypass to GND with a minimum 0.1-µF high quality ceramic capacitor.
PGND	6	I	System ground.
DRVL	7	O	Low-side N-Channel MOSFET gate driver output. PGND referenced driver switches between PGND(OFF) and VREG5(ON).
SW	8	I/O	Switch node connections for both the high-side driver and over current comparator.
DRVH	9	O	High-side N-channel MOSFET gate driver output. SW referenced driver switches between SW(OFF) and VBST(ON).
VBST	10	I	High-side MOSFET gate driver bootstrap voltage input. Connect a capacitor from VBST to SW. An internal diode is connected between VREG5 and VBST

10 PIN VSSOP
(TOP VIEW)



FUNCTIONAL BLOCK DIAGRAM



OVERVIEW

The TPS53015 is single synchronous step-down (buck) controller. It operates using D-CAP2™ mode control. The fast transient response of D-CAP2™ control reduces the required amount of output capacitance to meet a specific level of performance. Proprietary internal circuitry allows the use of low ESR output capacitors including ceramic and special polymer types.

DETAILED DESCRIPTION

PWM OPERATION

The main control loop of the TPS53015 is an adaptive on-time pulse width modulation (PWM) controller that supports a proprietary D-CAP2™ control mode. D-CAP2™ control combines constant on-time control with an internal compensation circuit for pseudo-fixed frequency and low external component count configuration with both low ESR and ceramic output capacitors. It is stable even with virtually no ripple at the output. At the beginning of each cycle, the high-side MOSFET is turned on. this MOSFET is turned off when the internal timer expires. This timer is set by the converter input voltage VIN, and the output voltage VO, to maintain a pseudo-fixed frequency over the input voltage range, hence it is called adaptive on-time control. The timer is reset and the high-side MOSFET is turned on again when the feedback voltage falls below the nominal output voltage. An internal ramp is added to the reference voltage to simulate output ripple, eliminating the need for ESR induced output ripple from D-CAP2™ mode control.

AUTO-SKIP Eco-Mode™ CONTROL

The TPS53015 is designed with Auto-Skip Eco-mode™ to increase light load efficiency. As the output current decreases from heavy load condition, the inductor current is also reduced and eventually comes to point where its rippled valley touches zero level, which is the boundary between continuous conduction and discontinuous conduction modes. The rectifying MOSFET is turned off when its zero inductor current is detected. As the load current further decreases the converter run into discontinuous conduction mode. The on-time is kept almost half as is was in the continuous conduction mode because it takes longer time to discharge the output capacitor with smaller load current to the level of the reference voltage. The transition point to the light load operation IOX(LL) current can be calculated in Equation 1 with 500kHz used as fsw.

$$I_{OUT(LL)} = \frac{1}{2 \times L \times f_{SW}} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \quad (1)$$

DRIVERS

TPS53015 contains two high-current resistive MOSFET gate drivers. The low-side driver is a PGND referenced, VREG5 powered driver designed to drive the gate of a high-current, low $R_{DS(on)}$ N-channel MOSFET whose source is connected to PGND. The high-side driver is a floating SW referenced, VBST powered driver designed to drive the gate of a high-current, low $R_{DS(on)}$ N-channel MOSFET. To maintain the VBST voltage during the high-side driver ON time, a capacitor is placed from SW to VBST. Each driver draws average current equal to Gate Charge (Q_g @ V_{gs} = 5V) times Switching frequency (fsw). To prevent cross-conduction, there is a narrow dead-time when both high-side and low-side drivers are OFF between each driver transition. During this time the inductor current is carried by one of the MOSFETs body diodes.

5-VOLT REGULATOR

The TPS53015 has an internal 5V Low-Dropout (LDO) Regulator to provide a regulated voltage for all both drivers and the ICs internal logic. A high-quality 4.7µF or greater ceramic capacitor from VREG5 to GND is required to stabilize the internal regulator.

SOFT START AND PRE-BIASED SOFT START

The TPS53015 has an internally set, 1.4 ms soft start time. When the EN pin becomes high and the VREG5 voltage is above the UVLO threshold, an internal DAC ramps up the reference voltage to the PWM comparator. Smooth control of the output voltage is maintained during start up.

The TPS53015 contains a unique circuit to prevent current from being pulled from the output during startup if the output is pre-biased. When the soft-start commands a voltage higher than the pre-bias level (internal soft start becomes greater than internal feedback voltage VFB), the controller slowly activates synchronous rectification by starting the first low side FET gate driver pulses with a narrow on-time. It then increments that on-time on a cycle-by-cycle basis until it coincides with the time dictated by (1-D), where D is the duty cycle of the converter. This scheme prevents the initial sinking of the pre-biased output, and ensures that the output voltage (VO) starts and ramps up smoothly into regulation from pre-biased startup to normal mode operation.

OVER CURRENT PROTECTION

TPS53015 has a cycle-by-cycle over current limit feature. The over current limits the inductor valley current by monitoring the voltage drop across the low-side MOSFET $R_{DS(on)}$ during the low-side driver on-time. If the inductor current is larger than the over current limit (OCL), the TPS53015 delays the start of the next switching cycle until the sensed inductor current falls below the OCL current. MOSFET $R_{DS(on)}$ current sensing is used to provide an accuracy and cost effective solution without external devices. To program the OCL, a resister should be connected between DRVL and PGND. The recommended values are given inTable 1.

Table 1. OCL Resistor Values

Resister Value (kΩ)	V_{trip} (V)
6.8	0.050
11	0.087
18	0.125
27	0.174
39	0.224
56	0.274
75	0.336

I_{OCL} is determined by Equation 2.

$$I_{OCL} = \left(\frac{(V_{IN} - V_{OUT})}{2 \times L \times f_{SW}} \times \frac{V_{OUT}}{V_{IN}} \right) + \frac{V_{TRIP}}{R_{DS(ON)}} \quad (2)$$

The trip voltage is set between 0.05V to 0.336V over all operational temperature, including the 4000ppm/°C temperature slope compensation for the temperature dependency of the $R_{DS(on)}$. If the load current exceeds the over-current limit, the voltage will begin to drop. If the over-current conditions continues the output voltage will fall below the under voltage protection threshold and the TPS53015 will shut down.

OVER/UNDER VOLTAGE PROTECTION

TPS53015 monitors a resistor divided feedback voltage to detect over and under voltage. If the feedback voltage is higher than 120% of the reference voltage, the OVP comparator output goes high and the circuit latches the high-side MOSFET driver OFF and the low-side MOSFET driver ON.

When the feedback voltage is lower than 68% of the reference voltage, the UVP comparator output goes high and an internal UVP delay counter begins counting. After 1ms, TPS53015 latches OFF both top and bottom MOSFET drivers. This function is enabled approximately 2.2 ms after power-on. The OVP and UVP latch off is reset when EN goes low.

UVLO PROTECTION

TPS53015 has under voltage lock out protection (UVLO) that monitors the voltage of VREG5 pin. When the VREG5 voltage is lower than UVLO threshold voltage, the device is shut off. All output drivers are OFF. The UVLO is non-latch protection.

THERMAL SHUTDOWN

TPS53015 monitors its temperature. If the temperature exceeds the threshold value (typically 150°C), the device shuts off. When the temperature falls below the threshold, the IC starts again. When VIN starts up and VREG5 output voltage is below its nominal value, the thermal shutdown threshold is kept lower than 150°C. As long as VIN rises, T_J must be kept less than 110°C.

POWER GOOD

The TPS53015 has a power-good output that this is measured on VFB. The power-good function is activated after soft-start has finished. If the output voltage is within ±16% of the target voltage, the internal comparator detects the power-good state and the power-good signal becomes high after 1.2ms delay. During start-up, this internal delay starts after 2.2 times the soft-start time to avoid a glitch of power-good signal. If the feedback voltage goes outside ±16% of target value, the power-good signal becomes low after 2µs delay.

TYPICAL CHARACTERISTICS

V_{IN} = 12 V, T_A = 25 °C (unless otherwise noted)

VIN SUPPLY CURRENT vs JUNCTION TEMPERATURE

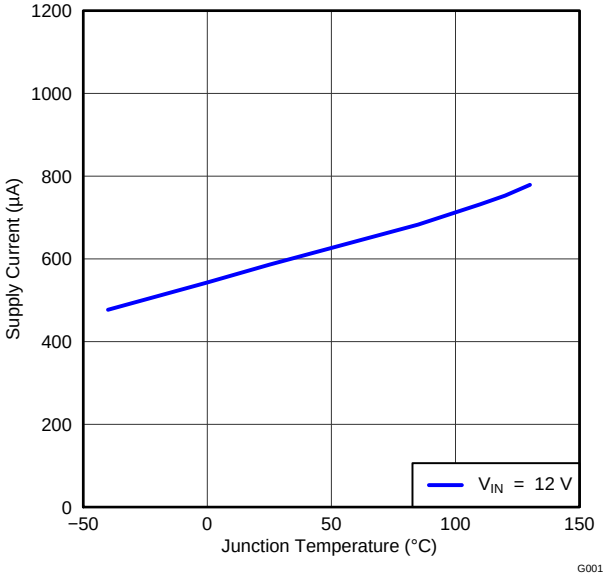


Figure 1.

VIN SHUTDOWN CURRENT vs JUNCTION TEMPERATURE

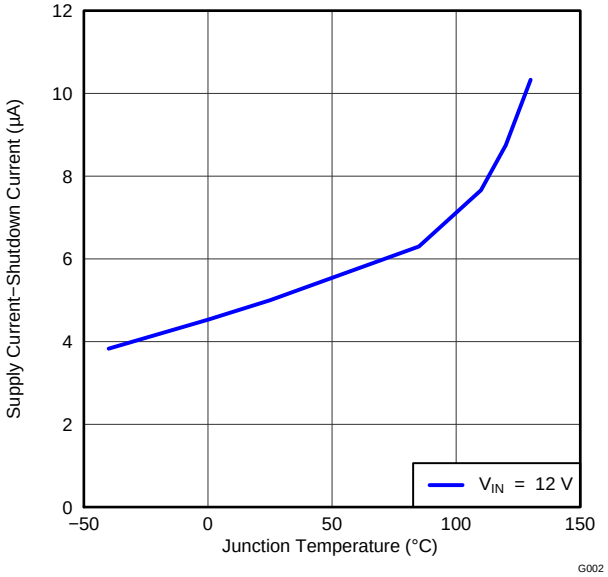


Figure 2.

EN INPUT CURRENT VS EN INPUT VOLTAGE

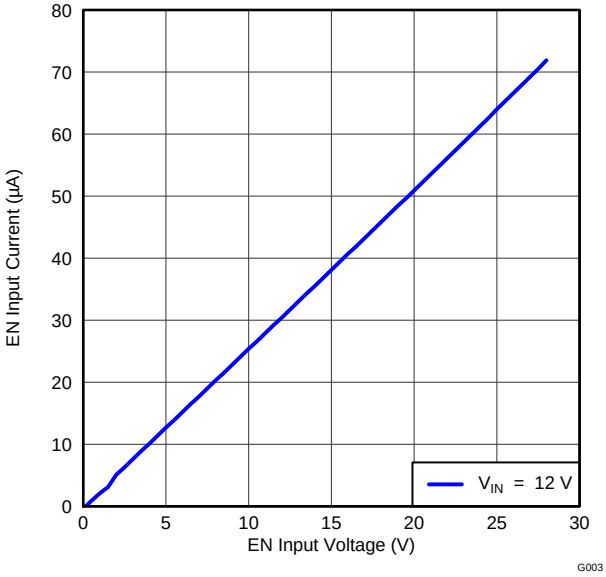


Figure 3.

SWITCHING FREQUENCY vs JUNCTION TEMPERATURE

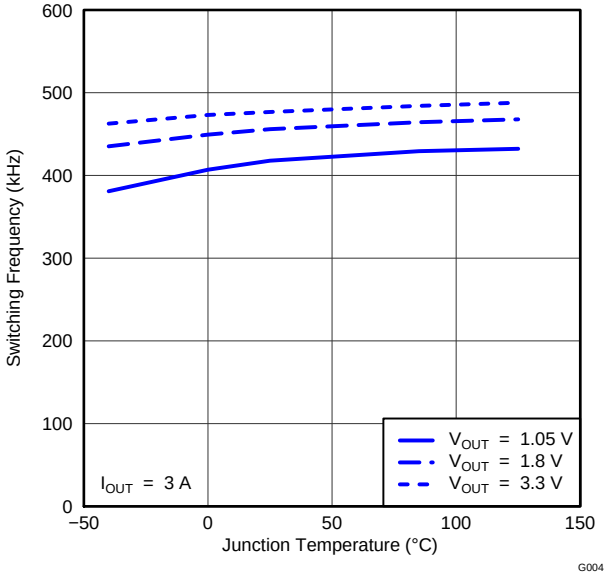


Figure 4.

TYPICAL CHARACTERISTICS (continued)

V_{IN} = 12 V, T_A = 25 °C (unless otherwise noted)

SWITCHING FREQUENCY vs INPUT VOLTAGE

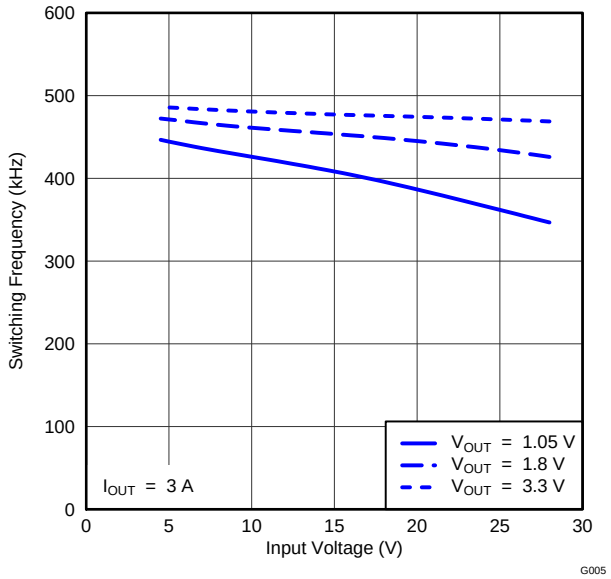


Figure 5.

VFB VOLTAGE vs INPUT VOLTAGE

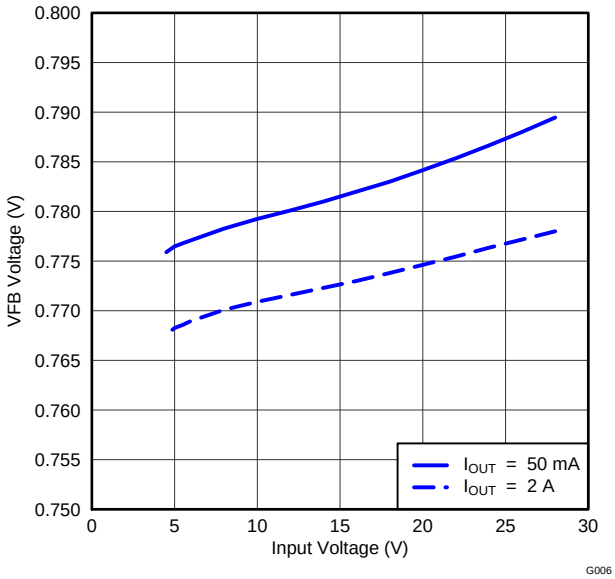


Figure 6.

VFB VOLTAGE vs AMBIENT TEMPERATURE

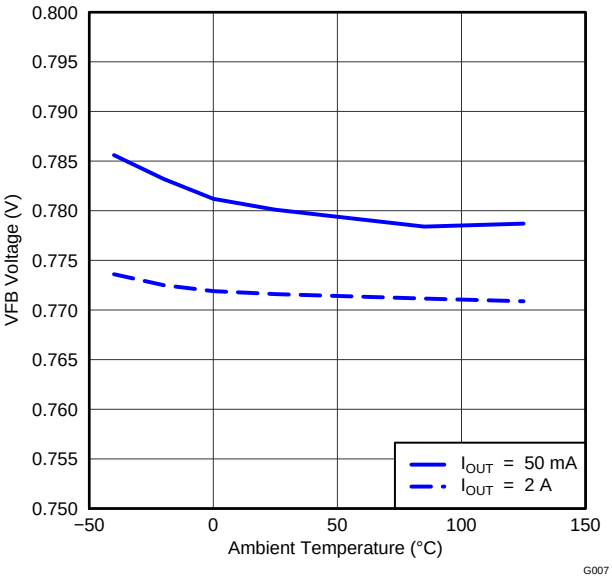


Figure 7.

LOAD REGULATION

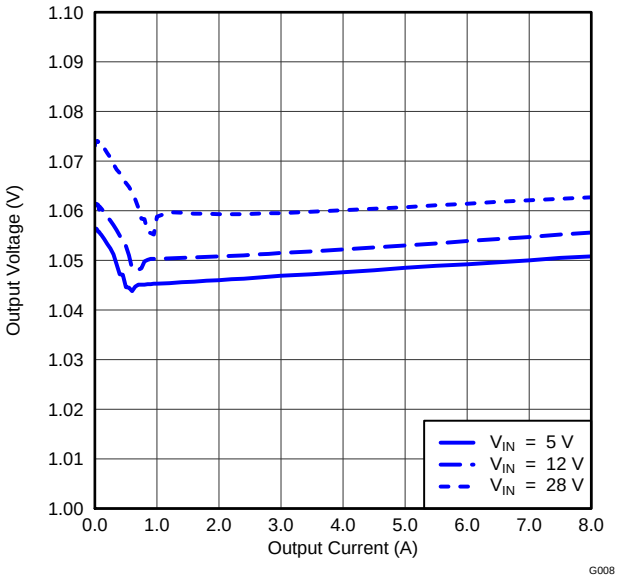


Figure 8.

TYPICAL CHARACTERISTICS (continued)

V_{IN} = 12 V, T_A= 25 °C (unless otherwise noted)

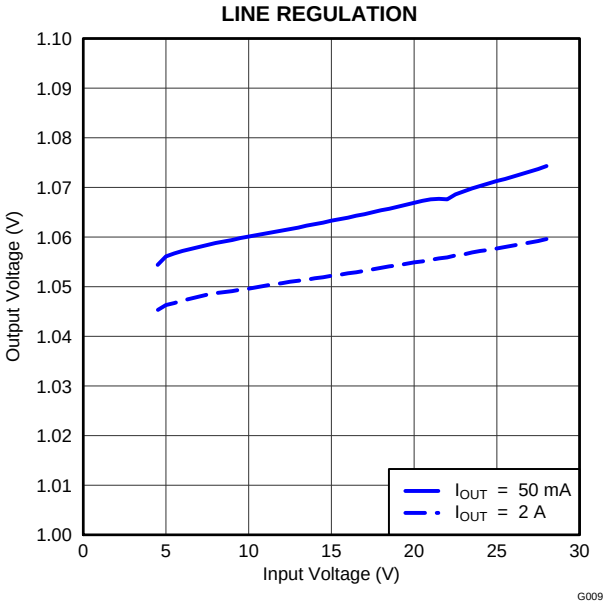


Figure 9.

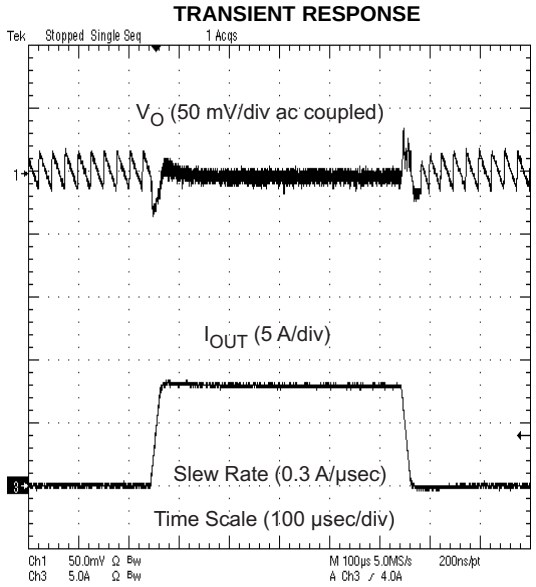


Figure 10.

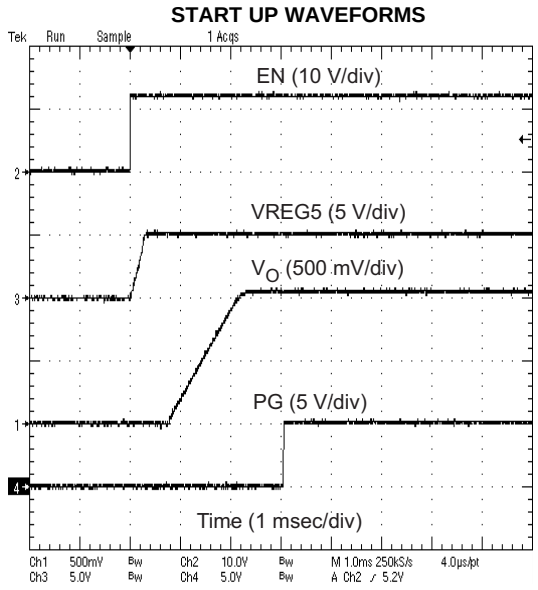


Figure 11.

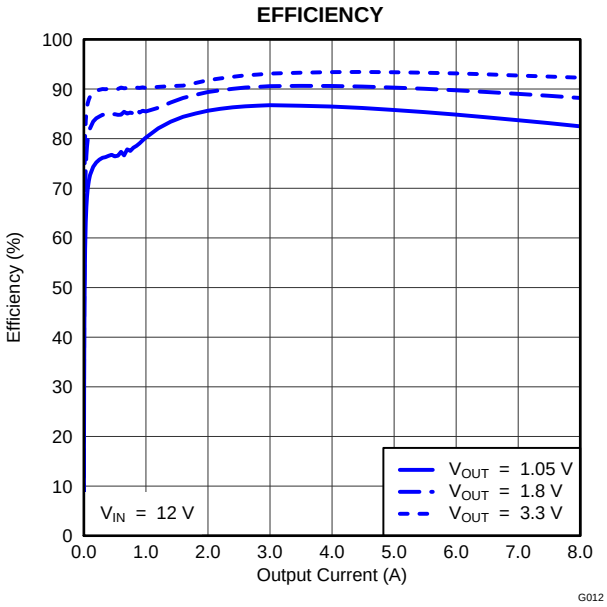


Figure 12.

TYPICAL CHARACTERISTICS (continued)

V_{IN} = 12 V, T_A = 25 °C (unless otherwise noted)

LIGHT LOAD EFFICIENCY

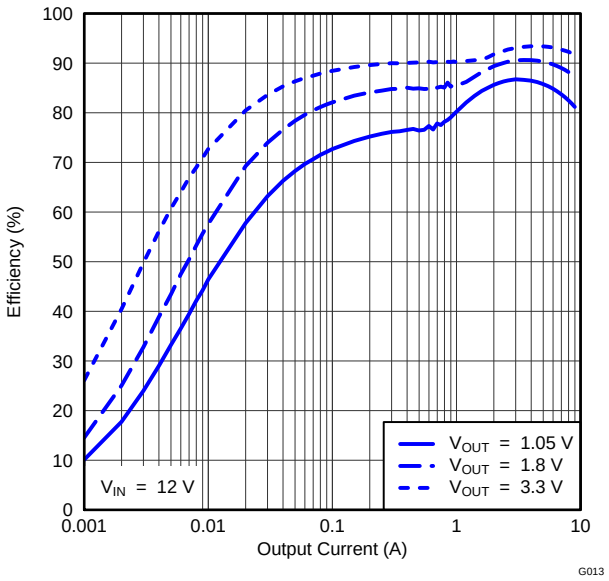


Figure 13.

OUTPUT VOLTAGE RIPPLE, I_{OUT} = 8 A

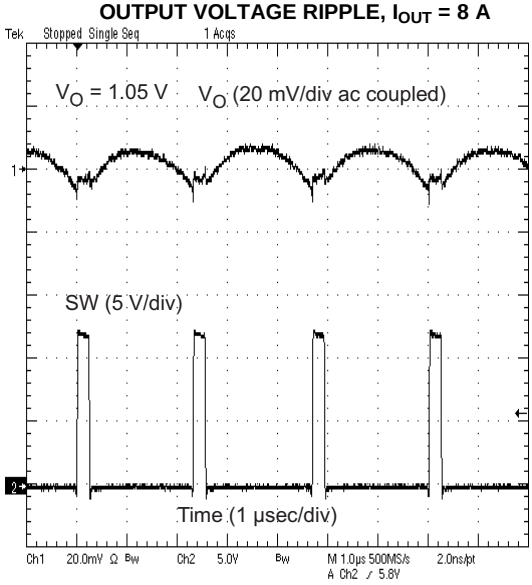


Figure 14.

OUTPUT VOLTAGE RIPPLE, I_{OUT} = 50 mA

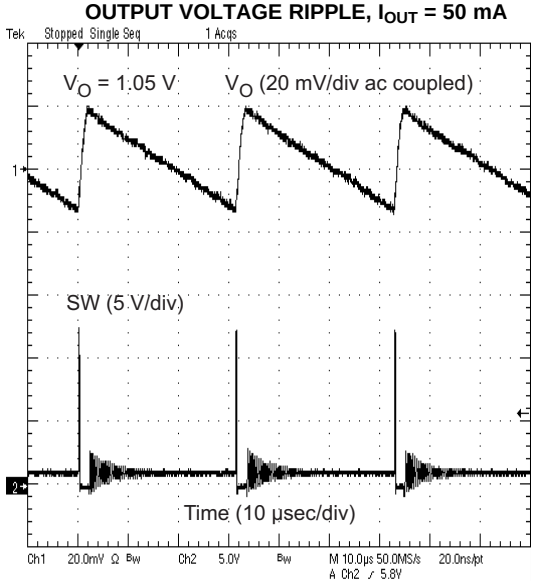


Figure 15.

INPUT VOLTAGE RIPPLE, I_{OUT} = 8 A

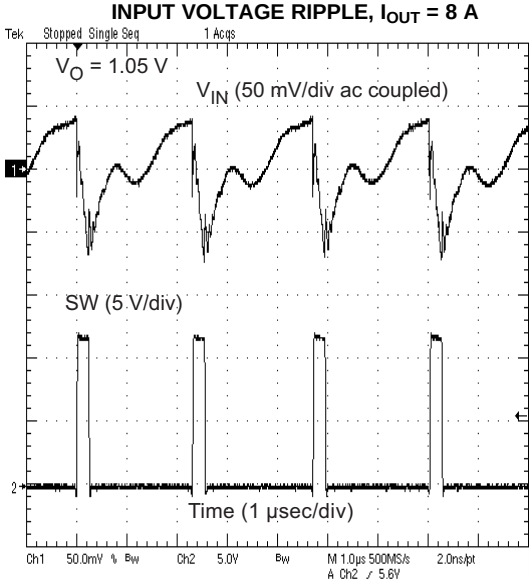


Figure 16.

TYPICAL CHARACTERISTICS (continued)

V_{IN} = 12 V, T_A= 25 °C (unless otherwise noted)

INPUT VOLTAGE RIPPLE, I_{OUT} = 50 mA

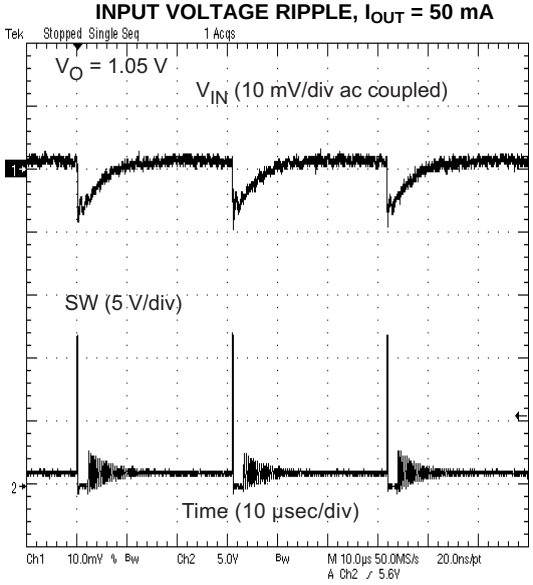


Figure 17.

APPLICATION INFORMATION

APPLICATION SCHEMATIC

A typical application schematic is shown in Figure 18.

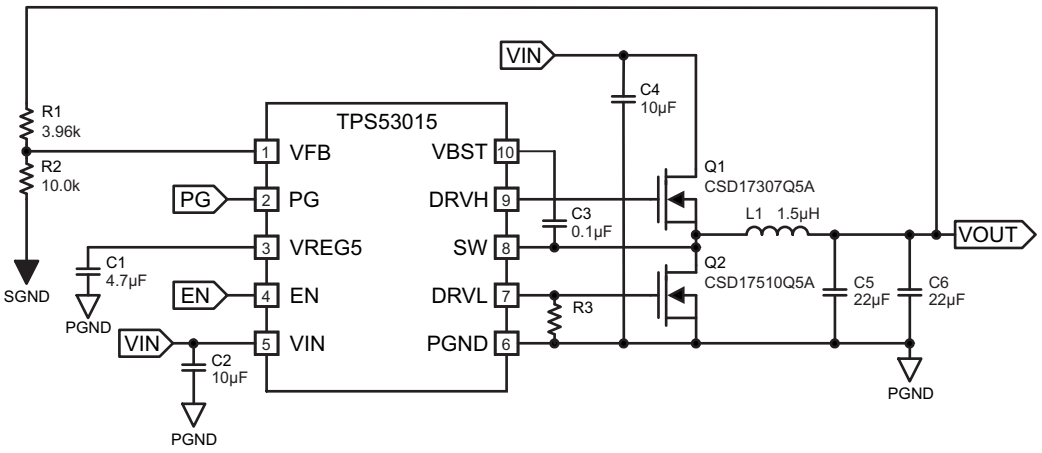


Figure 18. Application Schematic

COMPONENT SELECTION

INDUCTOR

The inductance value is selected to provide approximately 30% peak to peak ripple current at maximum load. Larger ripple current increases output ripple voltage, improve S/N ratio and contribute to stable operation. Equation 3 can be used to calculate te value for L_{OUT}.

$$L_{OUT} = \frac{V_{IN(MAX)} - V_{OUT}}{I_{L(RIPPLE)} \times f_{SW}} \times \frac{V_{OUT}}{V_{IN(MAX)}} \quad (3)$$

The inductors current ratings needs to support both the RMS (thermal) current and the peak (saturation) current. The RMS and peak inductor current can be estimated as follows:

$$I_{L(RIPPLE)} = \frac{V_{IN(MAX)} - V_{OUT}}{L_{OUT} \times f_{SW}} \times \frac{V_{OUT}}{V_{IN(MAX)}} \quad (4)$$

$$I_{L(PEAK)} = \frac{V_{TRIP}}{R_{DS(ON)}} + I_{L(RIPPLE)} \quad (5)$$

$$I_{L(RMS)} = \sqrt{I_{OUT}^2 + \frac{1}{12} \times I_{L(RIPPLE)}^2} \quad (6)$$

Note:

The calculation above shall serve as a general reference. To further improve transient response, the output inductance could be reduced further. This needs to be considered along with the selection of the output capacitor.

OUTPUT CAPACITOR

The capacitor value and ESR determines the amount of output voltage ripple and load transient response. Ceramic output capacitors with X5R dielectric or better are recommended .

$$C_{OUT} = \frac{I_{L(RIPPLE)}}{8 \times V_{OUT(RIPPLE)}} \times \frac{1}{f_{SW}} \quad (7)$$

$$C_{OUT} = \frac{\Delta I_{LOAD}^{2}}{2 \times V_{OUT} \times \Delta V_{OS}} \times L_{OUT} \quad (8)$$

$$C_{OUT} = \frac{\Delta I_{LOAD}^{2}}{2 \times K \times \Delta V_{US}} \times L_{OUT} \quad (9)$$

Where:

$$K = (V_{IN} - V_{OUT}) \times \frac{T_{ON}}{T_{ON} - T_{OFF(MIN)}} \quad (10)$$

- ΔV_{OS} = The allowable amount of overshoot voltage in load transition
- ΔV_{US} = The allowable amount of undershoot voltage in load transition
- $T_{OFF(MIN)}$ = Minimum off time

Select the capacitance value greater than the largest value calculated from Equation 7, Equation 8 and Equation 9. The minimum recommended output capacitance is 44 µF.

INPUT CAPACITOR

The TPS53015 requires an input decoupling capacitor and a bulk capacitor is needed depending on the application. A minimum 10-µF high-quality ceramic capacitor is recommended for the input capacitor. The capacitor voltage rating needs to be greater than the maximum input voltage.

BOOTSTRAP CAPACITOR

The TPS53015 requires a bootstrap capacitor from SW to VBST to provide the floating supply for the high-side drivers. A minimum 0.1-µF high-quality ceramic capacitor is recommended. The capacitor voltage rating should be greater than 10 V.

VREG5 CAPACITOR

The TPS53015 requires that the VREG5 regulator is bypassed. A minimum 4.7-µF high-quality ceramic capacitor must be connected between the VREG5 and PGND for proper operation. The capacitor voltage rating should be greater than 10 V.

CHOOSE OUTPUT VOLTAGE RESISTORS

The output voltage is set with a resistor divider from output voltage node to the VFB pin. It is recommended to use 1% tolerance or better resistors. Select R2 between 10 kΩ and 100 kΩ and use Equation 11 to calculate R1.

$$R1 = \left(\frac{V_{OUT}}{V_{VFB}} - 1 \right) \times R2 \quad (11)$$

LAYOUT SUGGESTIONS

- Keep the input switching current loop as small as possible.
- Place the input capacitor close to the top switching FET. The output current loop should also be kept as small as possible.
- Keep the SW node as physically small and short as possible as to minimize parasitic capacitance and inductance and to minimize radiated emissions. Kelvin connections should be brought from the output to the feedback pin (VFB) of the device.
- Keep analog and non-switching components away from switching components.
- Make a single point connection from the signal ground to power ground.
- Do not allow switching current to flow under the device.

REVISION HISTORY

Changes from Original (July 2012) to Revision A **Page**

- Added revision A to literature number 1
- Changed Package designator from DDA to DGS in Thermal Information table header 3

Changes from Revision A (July 2012) to Revision B **Page**

- Changed literature number from revision A to revision B 1
- Changed "Adjustable Soft Start" to "1.4 ms Fixed Soft Start" in Features list 1
- Added "Power Good Output" to Features list 1
- Changed from "SS" to "PG" in the Absolute Maximum Ratings table 2
- Changed from "SS" to "PG" in the Recommended Operating Conditions table 3
- Changed T_{SS} spec from "1.0 ms" to "1.4 ms" Typical 4
- Changed T_{PGDLY} spec from "1.5 ms" to "1.2 ms" 4
- Changed $T_{PGCOMPSS}$ spec from "2.2 ms" to "2.3 ms" 4
- Changed T_{UVPEN} spec from "1.4 ms, 1.7 ms, 2.0 ms" MIN, TYP, MAX to "1.7 ms, 2.2 ms, 2.7 ms" respectively. 4
- Changed "+10%" and "-10%" to "+16%" and "-16%" in the Functional Block Diagram 6
- Changed soft start time from "1.0 ms" to "1.4 ms" 7
- Changed timing from "1.7 ms" to "2.2 ms" in the OVER/UNDER VOLTAGE PROTECTION section 8
- Added section describing POWER GOOD operation 8

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TPS53015DGS	ACTIVE	VSSOP	DGS	10	80	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	53015	Samples
TPS53015DGSR	ACTIVE	VSSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	53015	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

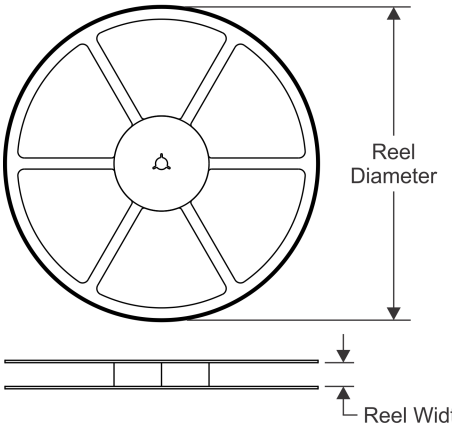
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

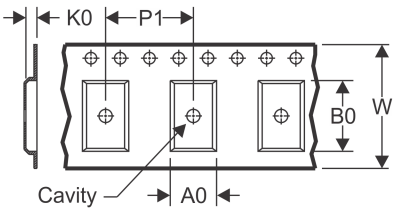
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

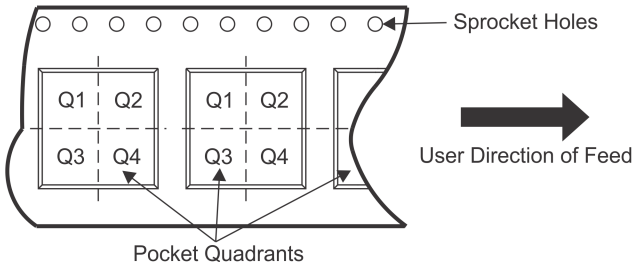


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

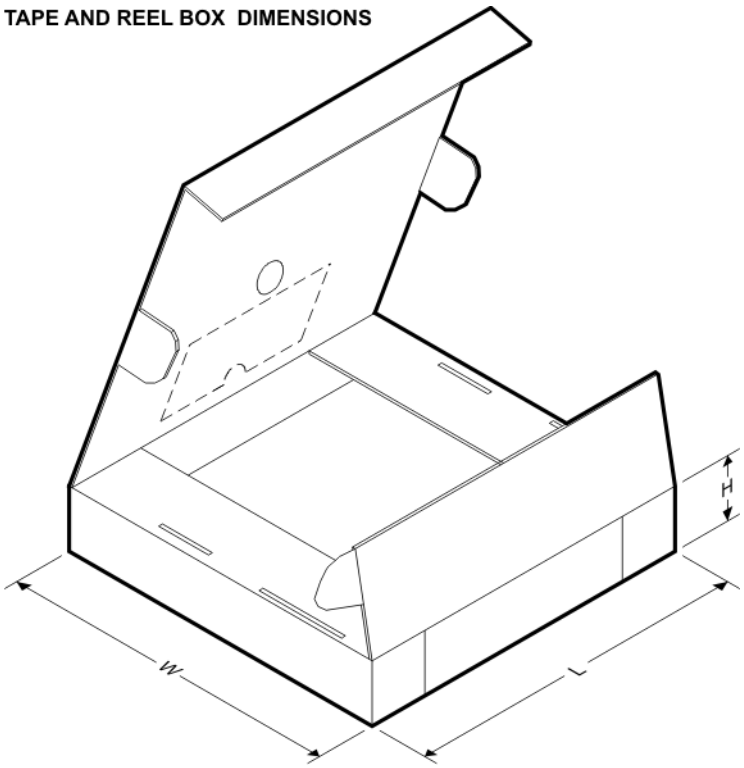
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS53015DGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

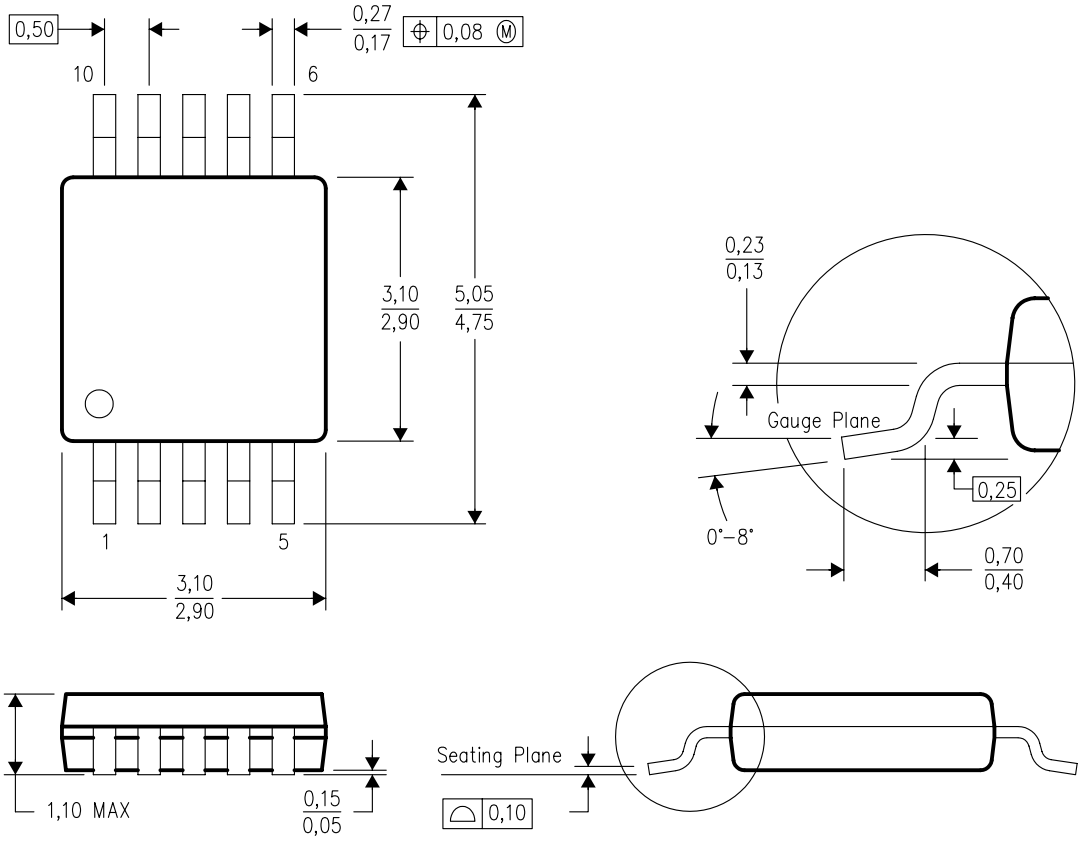
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS53015DGSR	VSSOP	DGS	10	2500	366.0	364.0	50.0

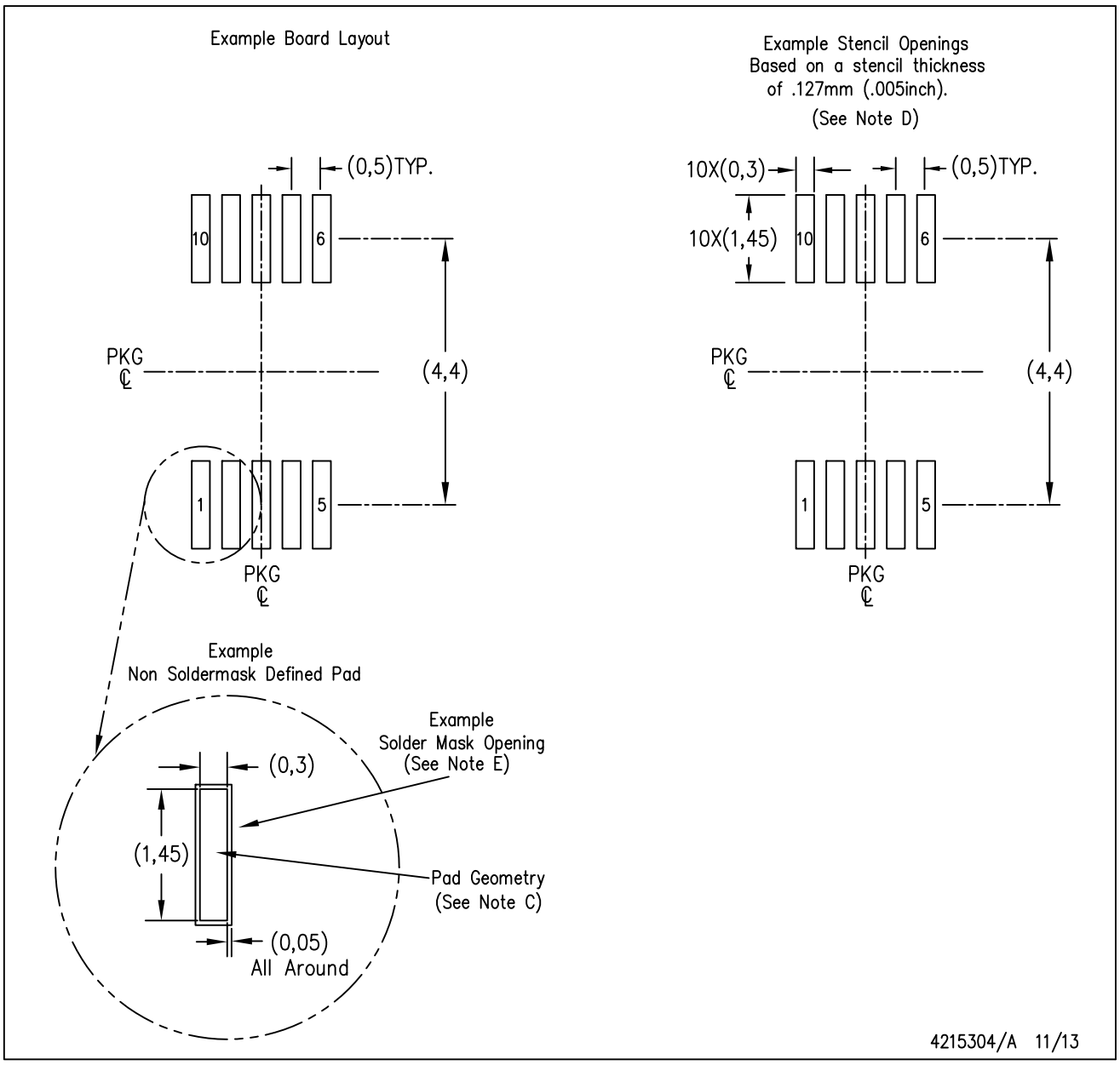
DGS (S–PDSO–G10) PLASTIC SMALL–OUTLINE PACKAGE



4073272/C 02/04

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–187 variation BA.

DGS (S–PDSO–G10) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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