TEXAS INSTRUMENTS

TPS5410

SLVS675D – AUGUST 2006 – REVISED DECEMBER 2014

TPS5410 1-A, Wide Input Range, Step-Down Converter

1 Features

- Wide Input Voltage Range: 5.5 V to 36 V
- Up to 1-A Continuous (1.2-A Peak) Output Current
- High Efficiency Up to 95% Enabled by 110-mΩ Integrated MOSFET Switch
- Wide Output Voltage Range: Adjustable Down to 1.22 V with 1.5% Initial Accuracy
- Internal Compensation Minimizes External Parts Count
- Fixed 500-kHz Switching Frequency for Small Filter Size
- Improved Line Regulation and Transient Response by Input Voltage Feed-Forward
- System Protected by Overcurrent Limiting, Overvoltage Protection and Thermal Shutdown
- –40°C to 125°C Operating Junction Temperature Range
- Available in Small 8-Pin SOIC Package

2 Applications

- Consumer: Set-Top Box, DVD, LCD Displays
- Industrial and Car Audio Power Supplies
- Battery Chargers, High-Power LED Supply
- 12-V/24-V Distributed Power Systems

3 Description

The TPS5410 is a high-output-current PWM converter that integrates a low-resistance, high-side, N-channel MOSFET. Included on the substrate with the listed features is a high performance voltage error amplifier that provides tight voltage regulation accuracy under transient conditions; an undervoltage-lockout circuit to prevent start-up until the input voltage reaches 5.5 V; an internally set slow-start circuit to limit inrush currents; and a voltage feed-forward circuit to improve the transient response. Using the ENA pin, shutdown supply current is reduced to 18 µA typically. Other features include an active high enable, overcurrent limiting, overvoltage protection and thermal shutdown. To reduce design complexity and external component count, the TPS5410 feedback loop is internally compensated.
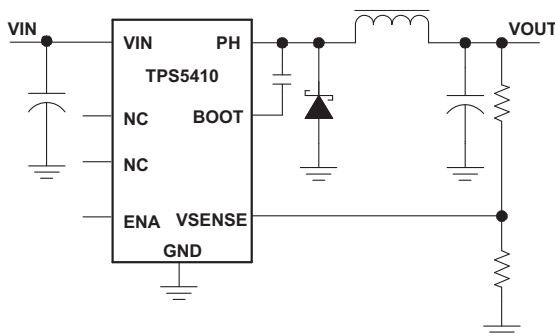
The TPS5410 device is available in an easy to use 8-pin SOIC package. TI provides evaluation modules and software tools to aid in quickly achieving high-performance power supply designs to meet aggressive equipment development cycles.
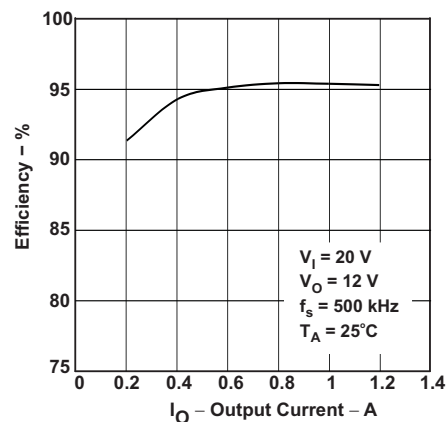
Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS5410D	SOIC (8)	3.91 mm x 4.90 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic

Efficiency vs Output Current

V_I = 20 V
V_O = 12 V
f_s = 500 kHz
T_A = 25°C

I_O – Output Current – A

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (September 2013) to Revision D   **Page**

- Added ESD Ratings table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section. 1

Changes from Revision B (January 2013) to Revision C   **Page**

- Deleted SWIFT from the data sheet Title, Features , and Description 1

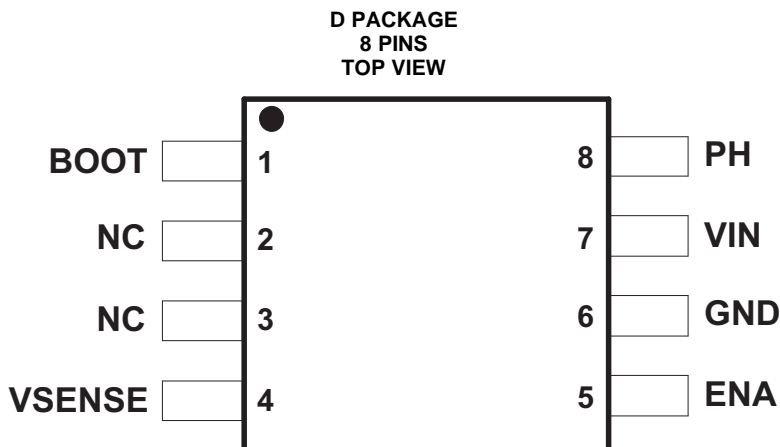**Changes from Revision A (November 2006) to Revision B**   **Page**

- Replaced the DISSIPATION RATINGS with the THERMAL INFORMATION table.. 4

Changes from Original (August 2006) to Revision A   **Page**

- Changed the Efficiency vs Output Current graph... 1
- Changed the Functional Block Diagram 8

Product Folder Links: *TPS5410*

5 Pin Configuration and Functions

D PACKAGE
8 PINS
TOP VIEW

	PIN		I/O	DESCRIPTION
NAME		**NO.**		
BOOT		1	O	Boost capacitor for the high-side FET gate driver. Connect 0.01 µF low ESR capacitor from BOOT pin to PH pin.
NC		2, 3	—	Not connected internally.
VSENSE		4	I	Feedback voltage for the regulator. Connect to output voltage divider.
ENA		5	I	On/off control. Below 0.5 V, the device stops switching. Float the pin to enable.
GND		6	—	Ground.
VIN		7	I	Input supply voltage. Bypass VIN pin to GND pin close to device package with a high quality, low ESR ceramic capacitor.
PH		8	O	Source of the high side power MOSFET. Connected to external inductor and diode.

Pin Functions

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) [1] [2]

			MIN	MAX	UNIT
V_I	Input voltage range	VIN	−0.3	40[3]	V
		PH (steady-state)	−0.6	40[3]	
		EN	−0.3	7	
		VSENSE	−0.3	3	
		BOOT-PH	−0.3	10	
		PH (transient < 10 ns)	−1.2		
I_O	Source current	PH		Internally Limited	
I_{lkg}	Leakage current	PH		10	µA
T_J	Operating virtual junction temperature		−40	150	°C
T_{stg}	Storage temperature		−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) Approaching the absolute maximum rating for the VIN pin may cause the voltage on the PH pin to exceed the absolute maximum rating.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{VIN}	Input voltage range	5.5		36	V
T_J	Operating junction temperature	−40		125	°C

6.4 Thermal Information

	THERMAL METRIC[1]	TPS5410	UNIT
		D	
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance (custom board) [2]	75	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance (standard board)	105.9	
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	45.0	
$R_{\theta JB}$	Junction-to-board thermal resistance	47.8	
ψ_{JT}	Junction-to-top characterization parameter	5.7	
ψ_{JB}	Junction-to-board characterization parameter	47.0	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) Test boards conditions:
    (a) 3 in x 3 in, 2 layers, thickness: 0.062 inch.
    (b) 2 oz. copper traces located on the top and bottom of the PCB.
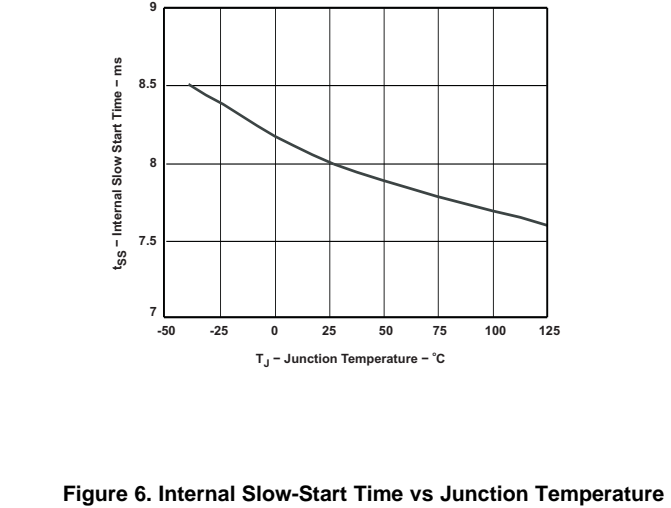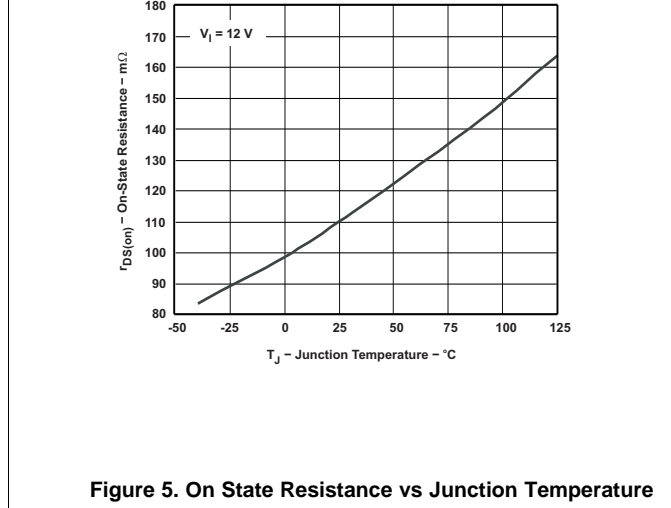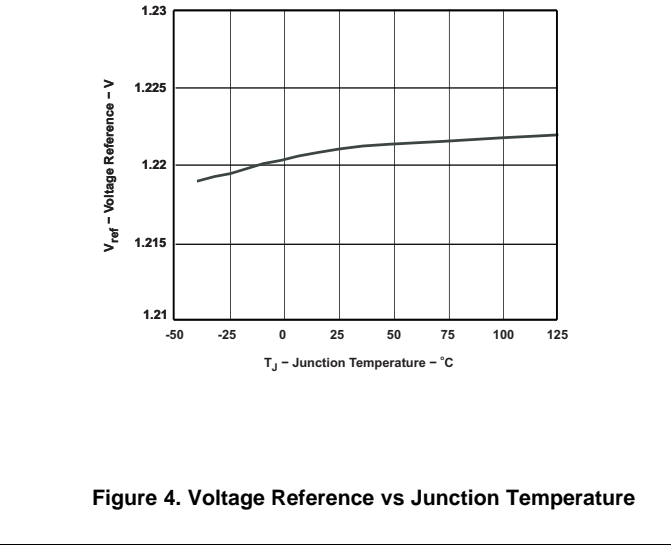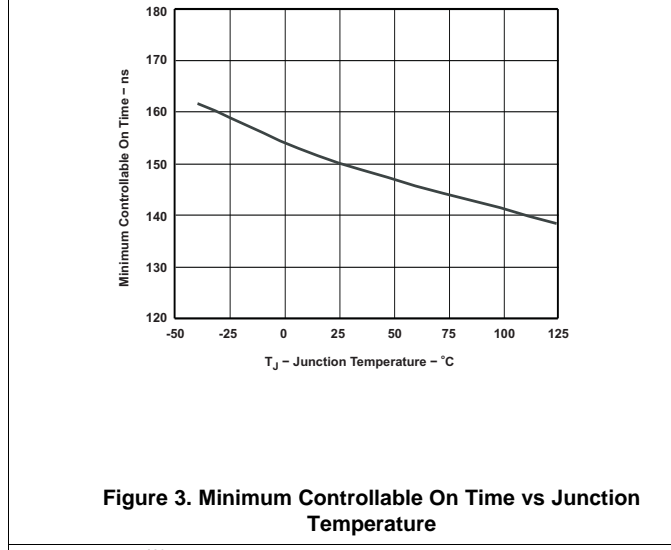
6.5 Electrical Characteristics

T_J = –40°C to 125°C, VIN = 5.5 V to 36 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE (VIN PIN)						
I_Q	Quiescent current	VSENSE = 2 V, Not switching, PH pin open		3	4.4	mA
		Shutdown, ENA = 0 V		18	50	µA
UNDERVOLTAGE LOCK OUT (UVLO)						
	Start threshold voltage, UVLO			5.3	5.5	V
	Hysteresis voltage, UVLO			330		mV
VOLTAGE REFERENCE						
	Voltage reference accuracy	T_J = 25°C	1.202	1.221	1.239	V
		I_O = 0 A – 1 A	1.196	1.221	1.245	
OSCILLATOR						
	Internally set free-running frequency		400	500	600	kHz
	Minimum controllable on time			150	200	ns
	Maximum duty cycle		87%	89%		
ENABLE (ENA PIN)						
	Start threshold voltage, ENA				1.3	V
	Stop threshold voltage, ENA		0.5			V
	Hysteresis voltage, ENA			450		mV
	Internal slow-start time (0 ~ 100%)		6.6	8	10	ms

Product Folder Links: *TPS5410*

Electrical Characteristics (continued)

T_J = −40°C to 125°C, VIN = 5.5 V to 36 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CURRENT LIMIT						
	Current limit		1.2	1.5	1.8	A
	Current limit hiccup time		13	16	20	ms
THERMAL SHUTDOWN						
	Thermal shutdown trip point		135	162		°C
	Thermal shutdown hysteresis			14		°C
OUTPUT MOSFET						
$r_{DS(on)}$	High-side power MOSFET switch	VIN = 5.5 V		150		mΩ
		VIN = 10 V - 36 V		110	230	

6.6 Typical Characteristics

Figure 1. Oscillator Frequency vs Junction Temperature

Figure 2. Operating Quiescent Current vs Junction Temperature

Figure 3. Minimum Controllable On Time vs Junction Temperature

Figure 4. Voltage Reference vs Junction Temperature

Figure 5. On State Resistance vs Junction Temperature

Figure 6. Internal Slow-Start Time vs Junction Temperature

Product Folder Links: *TPS5410*
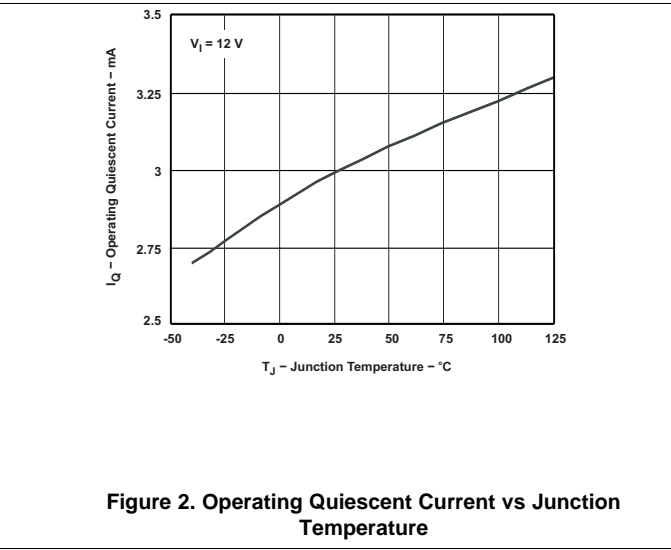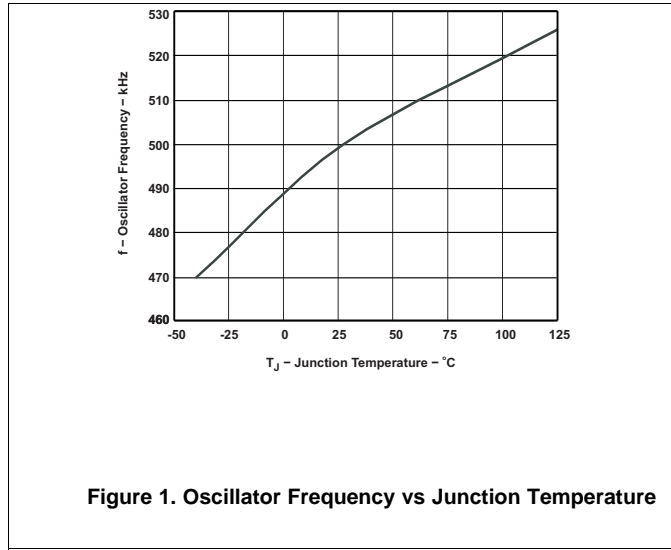
Typical Characteristics (continued)
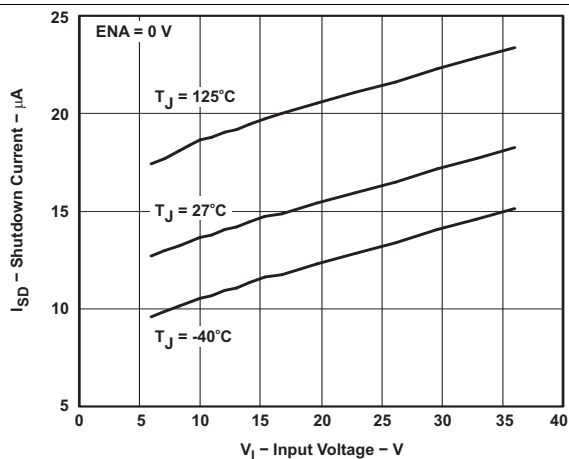
Figure 7. Shutdown Quiescent Current vs Input Voltage
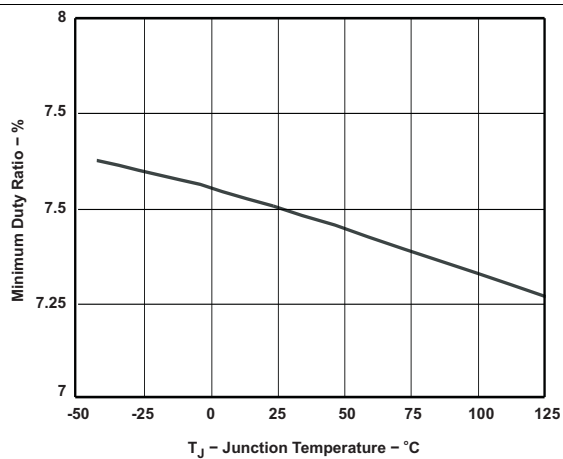
Figure 8. Minimum Controllable Duty Ratio vs Junction Temperature

Product Folder Links: *TPS5410*

7 Detailed Description

7.1 Overview

The TPS5410 is a 36-V, 1-A step-down (buck) regulator with an integrated, high-side, N-channel MOSFET. These devices implement constant-frequency voltage-mode control with voltage feed-forward for improved line regulation and line transient response. Internal compensation reduces design complexity and external component count.

The integrated 110-mΩ high-side MOSFET supports high-efficiency power-supply designs capable of delivering 1-A of continuous current to a load. The gate-drive bias voltage for the integrated high-side MOSFET is supplied by a bootstrap capacitor connected from the BOOT to PH pins. The TPS5410 reduces the external component count by integrating the bootstrap recharge diode.

The TPS5410 has a default input start-up voltage of 5.3 V typical. The ENA pin can be used to disable the TPS5410 reducing the supply current to 18 µA. An internal pullup current source enables operation when the ENA pin is floating. The TPS5410 includes an internal slow-start circuit that slows the output rise time during start up to reduce in rush current and output voltage overshoot.

The minimum output voltage is the internal 1.221-V feedback reference. Output overvoltage transients are minimized by an Overvoltage Protection (OVP) comparator. When the OVP comparator is activated, the high-side MOSFET is turned off and remains off until the output voltage is less than 112.5% of the desired output voltage.

Internal cycle-by-cycle overcurrent protection limits the peak current in the integrated high-side MOSFET. For continuous overcurrent fault conditions the TPS5410 will enter hiccup mode overcurrent limiting. Thermal protection protects the device from overheating.

7.2 Functional Block Diagram
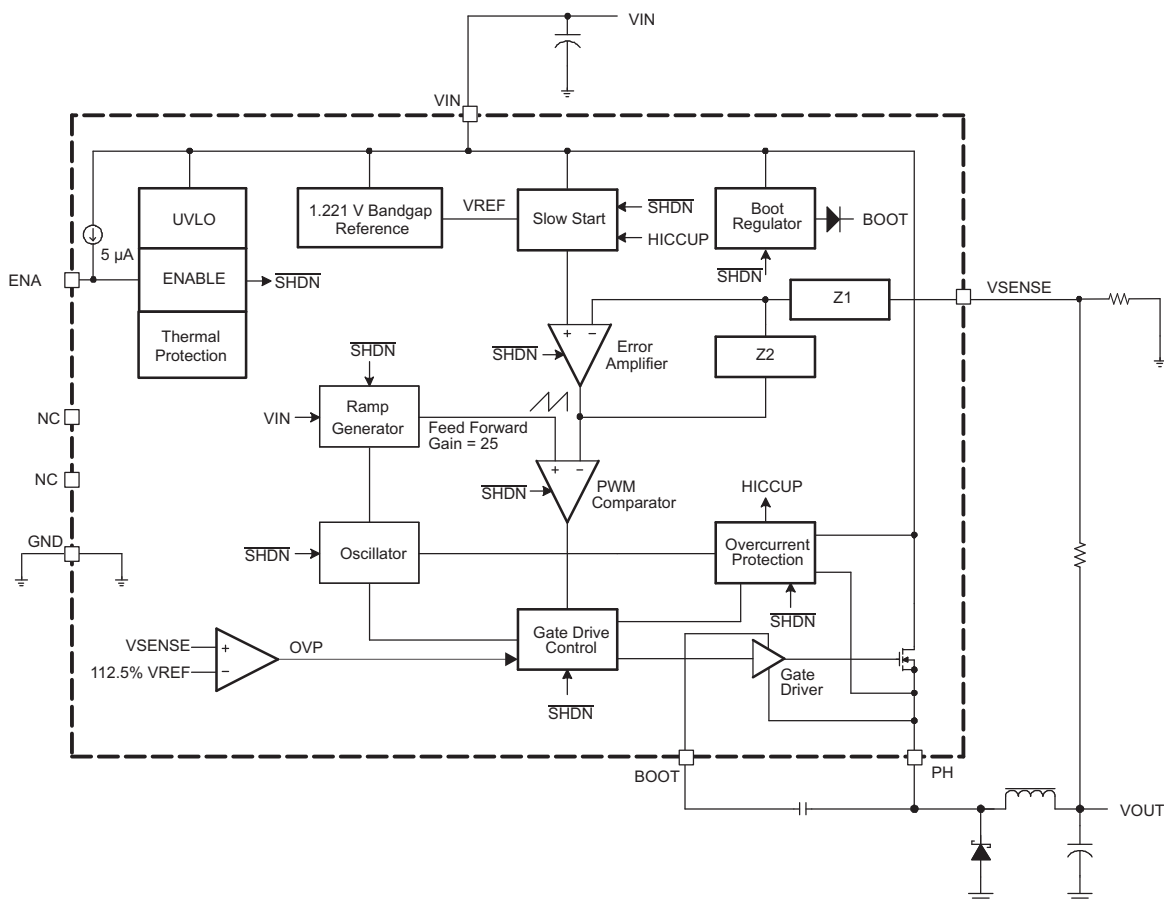
7.3 Feature Description

7.3.1 Oscillator Frequency

The internal free running oscillator sets the PWM switching frequency at 500 kHz. The 500-kHz switching frequency allows less output inductance for the same output ripple requirement resulting in a smaller output inductor.

7.3.2 Voltage Reference

The voltage reference system produces a precision reference signal by scaling the output of a temperature stable bandgap circuit. The bandgap and scaling circuits are trimmed during production testing to an output of 1.221 V at room temperature.

7.3.3 Enable (ENA) and Internal Slow-Start

The ENA pin provides electrical on/off control of the regulator. Once the ENA pin voltage exceeds the threshold voltage, the regulator starts operation and the internal slow-start begins to ramp. If the ENA pin voltage is pulled below the threshold voltage, the regulator stops switching and the internal slow-start resets. Connecting the pin to ground or to any voltage less than 0.5 V disables the regulator and activate the shutdown mode. The quiescent current of the TPS5410 in shutdown mode is typically 18 µA.

The ENA pin has an internal pullup current source, allowing the user to float the ENA pin. If an application requires controlling the ENA pin, use open drain or open collector output logic to interface with the pin. To limit the start-up inrush current, an internal slow-start circuit is used to ramp up the reference voltage from 0 V to its final value linearly. The internal slow-start time is 8 ms typically.

7.3.4 Undervoltage Lockout (UVLO)

The TPS5410 incorporates an undervoltage lockout circuit to keep the device disabled when VIN (the input voltage) is below the UVLO start voltage threshold. During power up, internal circuits are held inactive and the internal slow-start is grounded until VIN exceeds the UVLO start threshold voltage. Once the UVLO start threshold voltage is reached, the internal slow-start is released and device start-up begins. The device operates until VIN falls below the UVLO stop threshold voltage. The typical hysteresis in the UVLO comparator is 330 mV.

7.3.5 Boost Capacitor (BOOT)

Connect a 0.01-µF low-ESR ceramic capacitor between the BOOT pin and PH pin. This capacitor provides the gate drive voltage for the high-side MOSFET. X7R or X5R grade dielectrics are recommended due to their stable values over temperature.

7.3.6 Output Feedback (VSENSE)

The output voltage of the regulator is set by feeding back the center point voltage of an external resistor divider network to the VSENSE pin. In steady-state operation, the VSENSE pin voltage should be equal to the voltage reference 1.221 V.

7.3.7 Internal Compensation

The TPS5410 implements internal compensation to simplify the regulator design. Since the TPS5410 uses voltage mode control, a type 3 compensation network has been designed on chip to provide a high crossover frequency and a high phase margin for good stability. See the *Internal Compensation Network* in the Applications section for more details.

7.3.8 Voltage Feed-Forward

The internal voltage feed-forward provides a constant DC power stage gain despite any variations with the input voltage. This greatly simplifies the stability analysis and improves the transient response. Voltage feed-forward varies the peak ramp voltage inversely with the input voltage so that the modulator and power stage gain are constant at the feed-forward gain, for example:

$$\text{Feed Forward Gain} = \frac{\text{VIN}}{\text{Ramp}_{\text{pk-pk}}}$$

(1)

The typical feed-forward gain of TPS5410 is 25.

Feature Description (continued)

7.3.9 Pulse-Width-Modulation (PWM) Control

The regulator employs a fixed frequency pulse-width-modulator (PWM) control method. First, the feedback voltage (VSENSE pin voltage) is compared to the constant voltage reference by the high gain error amplifier and compensation network to produce a error voltage. Then, the error voltage is compared to the ramp voltage by the PWM comparator. In this way, the error voltage magnitude is converted to a pulse width which is the duty cycle. Finally, the PWM output is fed into the gate drive circuit to control the on-time of the high-side MOSFET.

7.3.10 Overcurrent Liming

Overcurrent limiting is implemented by sensing the drain-to-source voltage across the high-side MOSFET. The drain to source voltage is then compared to a voltage level representing the overcurrent threshold limit. If the drain-to-source voltage exceeds the overcurrent threshold limit, the overcurrent indicator is set true. The system will ignore the overcurrent indicator for the leading edge blanking time at the beginning of each cycle to avoid any turn-on noise glitches.

Once overcurrent indicator is set true, overcurrent limiting is triggered. The high-side MOSFET is turned off for the rest of the cycle after a propagation delay. The overcurrent limiting scheme is called cycle-by-cycle current limiting.

Sometimes under serious overload conditions such as short-circuit, the overcurrent runaway may still happen when using cycle-by-cycle current limiting. A second mode of current limiting is used, for example hiccup mode overcurrent limiting. During hiccup mode overcurrent limiting, the voltage reference is grounded and the high-side MOSFET is turned off for the hiccup time. Once the hiccup time duration is complete, the regulator restarts under control of the slow-start circuit.

7.3.11 Overvoltage Protection

The TPS5410 has an overvoltage protection (OVP) circuit to minimize voltage overshoot when recovering from output fault conditions. The OVP circuit includes an overvoltage comparator to compare the VSENSE pin voltage and a threshold of 112.5% x VREF. Once the VSENSE pin voltage is higher than the threshold, the high-side MOSFET will be forced off. When the VSENSE pin voltage drops lower than the threshold, the high-side MOSFET will be enabled again.

7.3.12 Thermal Shutdown

The TPS5410 protects itself from overheating with an internal thermal shutdown circuit. If the junction temperature exceeds the thermal shutdown trip point, the voltage reference is grounded and the high-side MOSFET is turned off. The part is restarted under control of the slow-start circuit automatically when the junction temperature drops 14°C below the thermal shutdown trip point.

7.4 Device Functional Modes

7.4.1 Minimum Input Voltage

Confid The TPS5410 is recommended to operate with input voltages above 5.5 V. The typical VIN UVLO threshold is 5.3 V and the device may operate at input voltages down to the UVLO voltage. At input voltages below the actual UVLO voltage the device will not switch. If ENA is floating or externally pulled up to greater up than 1.3 V, when $V_{(VIN)}$ passes the UVLO threshold the TPS5410 will become active. Switching is enabled and the slow-start sequence is initiated. The TPS5410 starts linearly ramping up the internal reference voltage from 0 V to its final value over the internal slow-start time period.

7.4.2 ENA Control

T The enable start threshold voltage is 1.3 V max. With ENA held below the 0.5 V minimum stop threshold voltage the TPS5410 is disabled and switching is inhibited even if VIN is above its UVLO threshold. The quiescent current is reduced in this state. If the ENA voltage is increased above the max start threshold while $V_{(VIN)}$ is above the UVLO threshold, the device becomes active. Switching is enabled and the slow-start sequence is initiated. The TPS5410 starts linearly ramping up the internal reference voltage from 0 V to its final value over the internal slow-start time period.

Product Folder Links: *TPS5410*

8 Applications and Implementation

NOTE
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS5410 is a 1-A, step down regulator with an integrated high-side MOSFET. This device is typically used to convert a higher DC voltage to a lower DC voltage with a maximum available output current of 1 A. Example applications are: High Density Point-of-Load Regulators for Set-top Box, DVD, LCD and Plasma Displays, High Power LED Supply, Car Audio, Battery Chargers, and other 12-V and 24-V Distributed Power Systems. Use the following design procedure to select component values for the TPS5410. This procedure illustrates the design of a high frequency switching regulator. Alternatively, use the WEBENCH software to generate a complete design. The WEBENCH software uses an iterative design procedure and accesses a comprehensive database of components when generating a design.

8.2 Typical Applications

8.2.1 Application Circuit

Figure 9 shows the schematic for a typical TPS5410 application. The TPS5410 can provide up to 1-A output current at a nominal output voltage of 12 V.
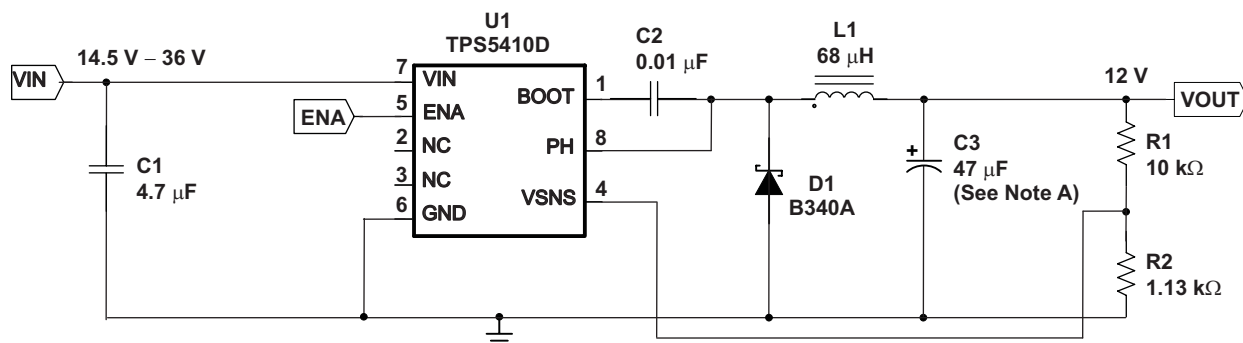
A.   C3 = Tantalum AVX TPSE476M020R0150

Figure 9. Application Circuit, 14.5-V — 36 V to 12-V

Typical Applications (continued)

8.2.1.1 Design Requirements

For this design example, use the following as the input parameters:

Table 1. Design Requirements

DESIGN PARAMETER[1]	EXAMPLE VALUE
Input voltage range	14.5 V to 36 V
Output voltage	12 V
Input ripple voltage	300 mV
Output ripple voltage	50 mV
Output current rating	1 A
Operating frequency	500 kHz

(1)   As an additional constraint, the design is set up to be small size and low component height.

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Switching Frequency

The switching frequency for the TPS5410 is internally set to 500 kHz. It is not possible to adjust the switching frequency.

8.2.1.2.2 Input Capacitors

The TPS5410 requires an input decoupling capacitor and, depending on the application, a bulk input capacitor. The minimum recommended value for the decoupling capacitor is 4.7 µF. A high quality ceramic type X5R or X7R is required. For some applications, a smaller value decoupling capacitor may be used, if the input voltage and current ripple ratings are not exceeded. The voltage rating must be greater than the maximum input voltage, including ripple. For this design, a 4.7 µF capacitor, C1 issued to allow for smaller 1812 case size to be used while maintaining a 50 V rating.

This input ripple voltage can be approximated by Equation 2 :

$$\Delta V_{IN} = \frac{I_{OUT(MAX)} \times 0.25}{C_{BULK} \times f_{SW}} + \left(I_{OUT(MAX)} \times ESR_{MAX} \right)$$

(2)

Where $I_{OUT(MAX)}$ is the maximum load current, f_{SW} is the switching frequency, C_I is the input capacitor value and ESR_{MAX} is the maximum series resistance of the input capacitor.

The maximum RMS ripple current also needs to be checked. For worst case conditions, this is approximated by Equation 3:

$$I_{CIN} = \frac{I_{OUT(MAX)}}{2}$$

(3)

In this example, the calculated input ripple voltage is 137 mV, and the RMS ripple current is 0.5 A. The maximum voltage across the input capacitors would be VIN max plus delta VIN/2. The chosen input decoupling capacitors are rated for 50 V, and the ripple current capacity for each is 3 A at 500 kHz, providing ample margin. The actual measured input ripple voltage may be larger than the calculated value due to the output impedance of the input voltage source, decrease in actual capacitance due to bias voltage and parasitics associated with the layout.

> **CAUTION**
>
> The maximum ratings for voltage and current are not to be exceeded under any circumstance.

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Additionally, some bulk capacitance may be needed, especially if the TPS5410 circuit is not located within approximately 2 inches from the input voltage source. The value for this capacitor is not critical but it should be rated to handle the maximum input voltage including ripple voltage and should filter the output so that input ripple voltage is acceptable.

8.2.1.2.3 Output Filter Components

Two components need to be selected for the output filter, L1 and C3. Since the TPS5410 is an internally compensated device, a limited range of filter component types and values can be supported.

8.2.1.2.3.1 Inductor Selection

To calculate the minimum value of the output inductor, use Equation 4:

$$L_{MIN} = \frac{V_{OUT} \times \left(V_{IN(MAX)} - V_{OUT}\right)}{V_{IN(max)} \times K_{IND} \times I_{OUT} \times F_{SW} \times 0.8} \tag{4}$$

K_{IND} is a coefficient that represents the amount of inductor ripple current relative to the maximum output current. Three things need to be considered when determining the amount of ripple current in the inductor: the peak to peak ripple current affects the output ripple voltage amplitude, the ripple current affects the peak switch current, and the amount of ripple current determines at what point the circuit becomes discontinuous. For designs using the TPS5410, K_{IND} of 0.2 to 0.3 yields good results. Low output ripple voltages is obtained when paired with the proper output capacitor, the peak switch current is below the current limit set point, and low load currents can be sourced before discontinuous operation.

For this design example, use $K_{IND} = 0.3$, and the minimum inductor value is 66 μH. The next highest standard value used in this design is 68 μH.

For the output filter inductor, it is important that the RMS current and saturation current ratings not be exceeded. The RMS inductor current can be found from Equation 5:

$$I_{L(RMS)} = \sqrt{I_{OUT(MAX)}^2 + \frac{1}{12} \times \left(\frac{V_{OUT} \times \left(V_{IN(MAX)} - V_{OUT}\right)}{V_{IN(MAX)} \times L_{OUT} \times F_{SW} \times 0.8}\right)^2} \tag{5}$$

and the peak inductor current can be determined using Equation 6:

$$I_{L(PK)} = I_{OUT(MAX)} + \frac{V_{OUT} \times \left(V_{IN(MAX)} - V_{OUT}\right)}{1.6 \times V_{IN(MAX)} \times L_{OUT} \times F_{SW}} \tag{6}$$

For this design, the RMS inductor current is 1.004 A, and the peak inductor current is 1.147 A. The chosen inductor is a Coilcraft MSS1260-683 type. The nominal inductance is 68μH. It has a saturation current rating of 2.3 A and a RMS current rating of 2.3 A, which meets the requirements. Inductor values for use with the TPS5410 are in the range of 10 μH to 100 μH.

8.2.1.2.3.2 Capacitor Selection

The important design factors for the output capacitor are dc voltage rating, ripple current rating, and equivalent series resistance (ESR). The dc voltage and ripple current ratings cannot be exceeded. The ESR is important because along with the inductor ripple current it determines the amount of output ripple voltage. The actual value of the output capacitor is not critical, but some practical limits do exist. Consider the relationship between the desired closed loop crossover frequency of the design and LC corner frequency of the output filter. Due to the design of the internal compensation, it is recommended to keep the closed loop crossover frequency in the range 3 kHz to 30 kHz as this frequency range has adequate phase boost to allow for stable operation. For this design example, the intended closed loop crossover frequency is between 2590 Hz and 24 kHz, and below the ESR zero of the output capacitor. Under these conditions, the closed loop crossover frequency is related to the LC corner frequency as:

$$f_{CO} = \frac{f_{LC}^2}{85 \, V_{OUT}} \tag{7}$$

Product Folder Links: TPS5410

and the desired output capacitor value for the output filter to:

$$C_{OUT} = \frac{1}{3357 \times L_{OUT} \times f_{CO} \times V_{OUT}}$$

(8)

For a desired crossover of 10 kHz and a 68-µH inductor, the calculated value for the output capacitor is 36.5 µF. The capacitor type should be chosen so that the ESR zero is above the loop crossover. The maximum ESR is:

$$ESR_{MAX} = \frac{1}{2\pi \times C_{OUT} \times f_{CO}}$$

(9)

The maximum ESR of the output capacitor also determines the amount of output ripple as specified in the initial design parameters. The output ripple voltage is the inductor ripple current times the ESR of the output filter. Check that the maximum specified ESR as listed in the capacitor data sheet results in an acceptable output ripple voltage:

$$V_{PP}(MAX) = \frac{ESR_{MAX} \times V_{OUT} \times \left(V_{IN(MAX)} - V_{OUT}\right)}{N_C \times V_{IN(MAX)} \times L_{OUT} \times F_{SW} \times 0.8}$$

(10)

Where:

ΔV_{PP} is the desired peak-to-peak output ripple.

N_C is the number of parallel output capacitors.

F_{SW} is the switching frequency.

The minimum ESR of the output capacitor should also be considered. For a good phase margin, if the ESR is zero when the ESR is at its minimum, it should not be above the internal compensation poles at 24 kHz and 54 kHz.

The selected output capacitor must also be rated for a voltage greater than the desired output voltage plus one half the ripple voltage. Any derating amount must also be included. The maximum RMS ripple current in the output capacitor is given by Equation 11:

$$I_{COUT(RMS)} = \frac{1}{\sqrt{12}} \times \left[\frac{V_{OUT} \times \left(V_{IN(MAX)} - V_{OUT}\right)}{V_{IN(MAX)} \times L_{OUT} - F_{SW} \times 0.8 \times N_C} \right]$$

(11)

Where:

N_C is the number of output capacitors in parallel.

F_{SW} is the switching frequency.

For this design example, a single 47-µF output capacitor is chosen for C3. This value is close to the calculated value of 36.5 µF and yields an actual closed loop cross over frequency of 10.05 kHz. The calculated RMS ripple current is 84.9 mA and the maximum ESR required is 339 mΩ. A capacitor that meets these requirements is a AVX TPSE476M020R0150, rated at 20 V with a maximum ESR of 150 mΩ and a ripple current rating of 1.369 A. This capacitor results in a peak-to-peak output ripple of 44 mV using equation 10. An additional small 0.1-µF ceramic bypass capacitor may also used, but is not included in this design.

Other capacitor types can be used with the TPS5410, depending on the needs of the application.

8.2.1.2.4 Output Voltage Setpoint

The output voltage of the TPS5410 is set by a resistor divider (R1 and R2) from the output to the VSENSE pin. Calculate the R2 resistor value for the output voltage of 12 V using Equation 12:

$$R2 = \frac{R1 \times 1.221}{V_{OUT} - 1.221}$$

(12)

For any TPS5410 design, start with an R1 value of 10 kΩ. R2 is then 1.13 kΩ.

8.2.1.2.5 Boot Capacitor

The boot capacitor should be 0.01 µF.

Product Folder Links: *TPS5410*

8.2.1.2.6 Catch Diode

The TPS5410 is designed to operate using an external catch diode between PH and GND. The selected diode must meet the absolute maximum ratings for the application: Reverse voltage must be higher than the maximum voltage at the PH pin, which is VINMAX + 0.5 V. Peak current must be greater than IOUTMAX plus on half the peak-to-peak inductor current. Forward voltage drop should be small for higher efficiencies. It is important to note that the catch diode conduction time is typically longer than the high-side FET on time; therefore, the diode parameters improve the overall efficiency. Additionally, check that the device chosen is capable of dissipating the power losses. For this design, a Diodes, Inc. B340A is chosen, with a reverse voltage of 40 V, forward current of 3 A, and a forward voltage drop of 0.5 V.

8.2.1.2.7 Advanced Information

8.2.1.2.7.1 Output Voltage Limitations

Due to the internal design of the TPS5410, there are both upper and lower output voltage limits for any given input voltage. The upper limit of the output voltage set point is constrained by the maximum duty cycle of 87% and is given by:

$$V_{OUTMAX} = 0.87 \times \left(\left(V_{INMIN} - I_{OMAX} \times 0.230 \right) + V_D \right) - \left(I_{OMAX} \times R_L \right) - V_D \tag{13}$$

Where:

V_{INMIN} = minimum input voltage

I_{OMAX} = maximum load current

V_D = catch diode forward voltage.

R_L = output inductor series resistance.

This equation assumes maximum on resistance for the internal high side FET.

The lower limit is constrained by the minimum controllable on time which may be as high as 200 ns. The approximate minimum output voltage for a given input voltage and minimum load current is given by:

$$V_{OUTMIN} = 0.12 \times \left(\left(V_{INMAX} - I_{OMIN} \times 0.110 \right) + V_D \right) - \left(I_{OMIN} \times R_L \right) - V_D \tag{14}$$

Where:

V_{INMAX} = maximum input voltage

I_{OMIN} = minimum load current

V_D = catch diode forward voltage.

R_L = output inductor series resistance.

This equation assumes nominal on resistance for the high side FET and accounts for worst case variation of operating frequency set point. Any design operating near the operational limits of the device should be checked to assure proper functionality.

8.2.1.2.7.2 Internal Compensation Network

The design equations given in the example circuit can be used to generate circuits using the TPS5410. These designs are based on certain assumptions, and always select output capacitors within a limited range of ESR values. If a different capacitor type is desired, it may be possible to fit one to the internal compensation of the TPS5410. Equation 15 gives the nominal frequency response of the internal voltage-mode type III compensation network:

$$H(s) = \frac{\left(1 + \frac{s}{2\pi \times Fz1}\right) \times \left(1 + \frac{s}{2\pi \times Fz2}\right)}{\left(\frac{s}{2\pi \times Fp0}\right) \times \left(1 + \frac{s}{2\pi \times Fp1}\right) \times \left(1 + \frac{s}{2\pi \times Fp2}\right) \times \left(1 + \frac{s}{2\pi \times Fp3}\right)} \tag{15}$$

Where

Fp0 = 2165 Hz, Fz1 = 2170 Hz, Fz2 = 2590 Hz

Fp1 = 24 kHz, Fp2 = 54 kHz, Fp3 = 440 kHz

Fp3 represents the non-ideal parasitics effect.

Using this information along with the desired output voltage, feed-forward gain and output filter characteristics, the closed loop transfer function can be derived.

8.2.1.2.7.3 Thermal Calculations

The following formulas show how to estimate the device power dissipation under continuous conduction mode operations. They should not be used if the device is working at light loads in the discontinuous conduction mode.

Conduction Loss: $Pcon = I_{OUT}^2 \times Rds(on) \times V_{OUT} / V_{IN}$

Switching Loss: $Psw = V_{IN} \times I_{OUT} \times 0.01$

Quiescent Current Loss: $Pq = V_{IN} \times 0.01$

Total Loss: $Ptot = Pcon + Psw + Pq$

Given T_A => Estimated Junction Temperature: $T_J = T_A + Rth \times Ptot$

Given $T_{JMAX} = 125°C$ => Estimated Maximum Ambient Temperature: $T_{AMAX} = T_{JMAX} - Rth \times Ptot$

8.2.1.3 Application Curves

The performance graphs in Figure 10 to Figure 17 are applicable to the circuit in Figure 9. $T_A = 25$ °C. unless otherwise specified.

Figure 10. Efficiency vs. Output Current

Figure 11. Output Voltage Regulation % vs. Output Current
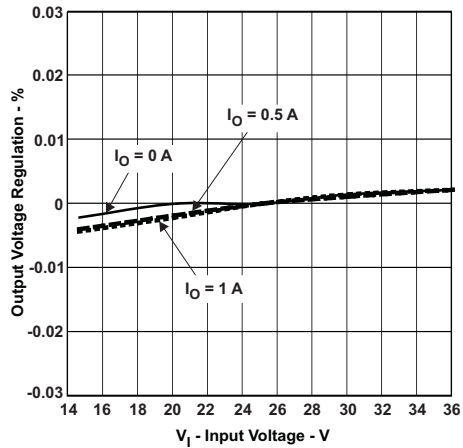

Figure 12. Output Voltage Regulation % vs. Input Voltage

Figure 13. Input Voltage Ripple and PH Node, $I_O = 1$ A

Product Folder Links: *TPS5410*
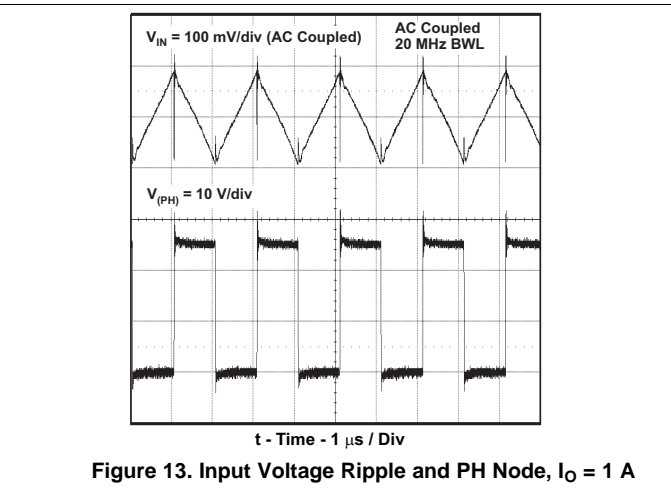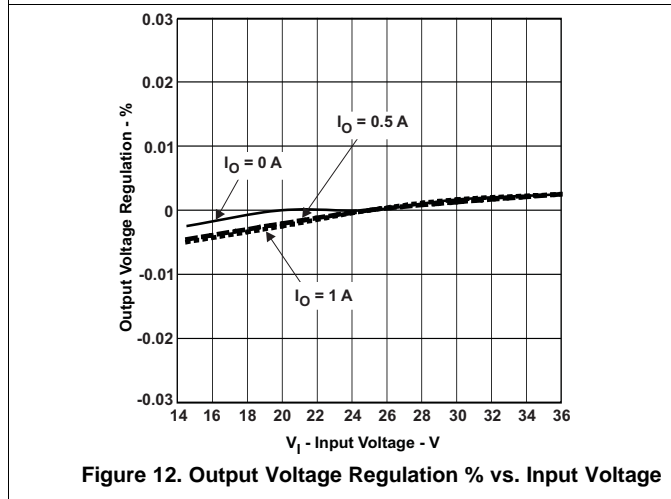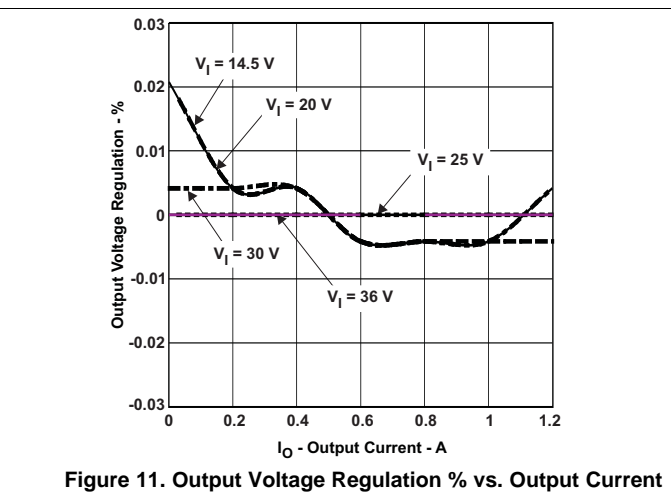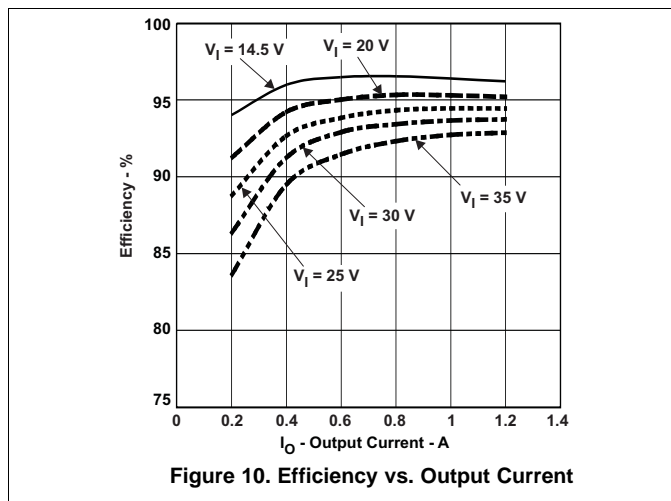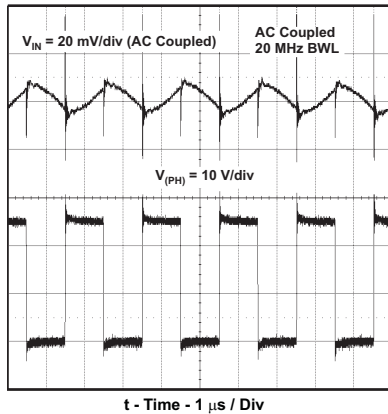
Figure 14. Output Voltage Ripple and PH Node, I_O = 1 A
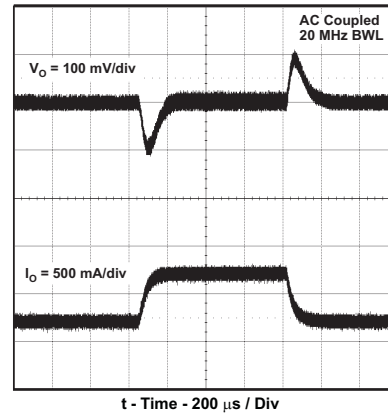
Figure 15. Transient Response, I_O Step 0.25 to 0.75 A
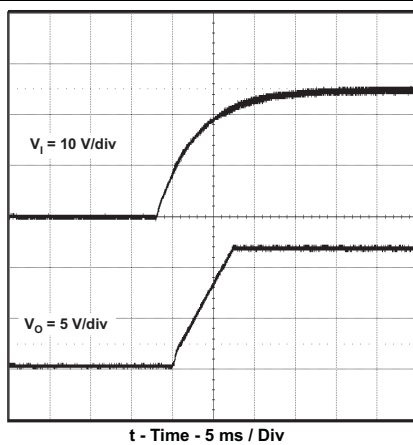
Figure 16. Startup Waveform, V_I and V_O
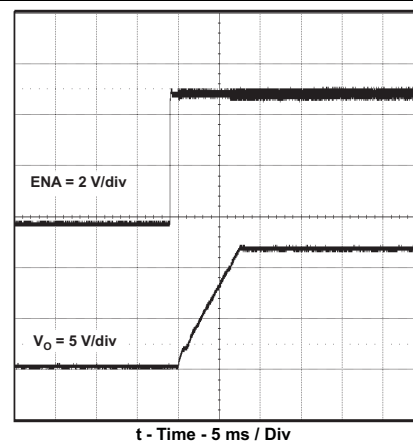
Figure 17. Startup Waveform, ENA and V_O

8.2.2 Using All Ceramic Capacitors

Figure 18 shows an application circuit using all ceramic capacitors for the input and output filters. The design procedure is similar to those given for the design example, except for the selection of the output filter capacitor values and the design of the additional compensation components required to stabilize the circuit.
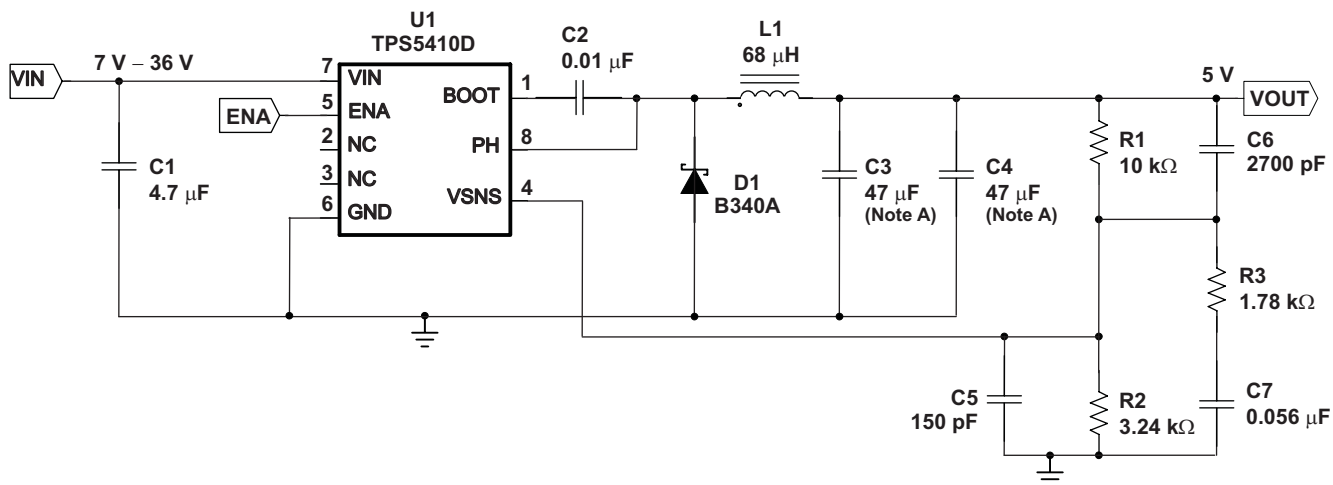
A. C3, C4 = Ceramic TDKC4532X5R1A476MT

Figure 18. 7-V — 36-V Input to 5-V Output Application Circuit with Ceramic Capacitors

8.2.2.1 Design Requirements

For this design example, use Table 1 as the input parameters.

8.2.2.2 Detailed Design Procedure

8.2.2.2.1 Output Filter Capacitor Selection

When using ceramic output filer capacitors, the recommended LC resonant frequency should be no more than 7 kHz. Since the output inductor is already selected at 68 µH, this limits the minimum output capacitor value to:

$$C_O \, (MIN) \geq \frac{1}{(2\pi \ \times \ 7000)^2 \ \times \ L_O}$$

(16)

The minimum capacitor value is calculated to be 7.6 µF. For this circuit a larger value of capacitor will yield better transient response. Two output capacitors are used for C3 and C4 with a value of 47 uF each. It is important to note that the actual capacitance of ceramic capacitors decreases with applied voltage. In this case the effective value used for the calculations is approximately 70 % of the rated value or 70 µF.

8.2.2.2.2 External Compensation Network

When using ceramic output capacitors, additional circuitry is required to stabilize the closed loop system. For this circuit the external components are R3, C5, C6 and C7. To determine the value of these components, first calculate the LC resonant frequency of the output filter:

$$F_{LC} = \frac{1}{2\pi \ \sqrt{L_O \ \times C_O \, (EFF)}}$$

(17)

For this example the effective resonant frequency is calculated as 2306 Hz

The network composed of R1, R2, R3, C5, C6 and C7 has two poles and two zeros that are used to tailor the overall response of the feedback network to accommodate the use of the ceramic output capacitors. The pole and zero locations are given by the following equations:

$$Fp1 = 500000 \ \times \frac{V_O}{F_{LC}}$$

(18)

Product Folder Links: *TPS5410*

$$Fz1 \ = \ 0.7 \ x \ F_{LC} \tag{19}$$

$$Fz2 \ = \ 2.5 \ x \ F_{LC} \tag{20}$$

The final pole is located at a frequency too high to be of concern. The values for R1 and R2 are fixed by the 5-V output voltage as calculated using Equation 12. Now the values of R3, C5, C6 and C7 are determined using Equation 21, Equation 22, and Equation 23:

$$C7 \ = \ \frac{1}{2\pi \ x \ Fp1 \ x \ (R1 \parallel R2)} \tag{21}$$

$$R3 \ = \ \frac{1}{2\pi \ x \ Fz1 \ x \ C7} \tag{22}$$

$$C6 \ = \ \frac{1}{2\pi \ x \ Fz2 \ x \ R1} \tag{23}$$

For this design, using the closest standard values, C7 is 0.056 µF, R3 is 1.76 kΩ and C6 is 2700 pF. C5 is added to improve load regulation performance. It is effectively in parallel with C6 in the location of the second pole frequency, so it should be small in relationship to C6. C5 should be less the 1/10 the value of C6. For this example, 150 pF works well.

For additional information on external compensation of the TPS5410 or other wide voltage range devices, see *Using TPS5410/20/30/31 With Aluminum/Ceramic Output Capacitors*, SLVA237.

8.2.2.3 Application Curves

The performance graphs in Figure 19 to Figure 24 are applicable to the circuit in Figure 18. T_A = 25 °C. unless otherwise specified.

Figure 19. Efficiency vs. Output Current

Figure 20. Output Voltage Regulation % vs. Output Current

Product Folder Links: *TPS5410*
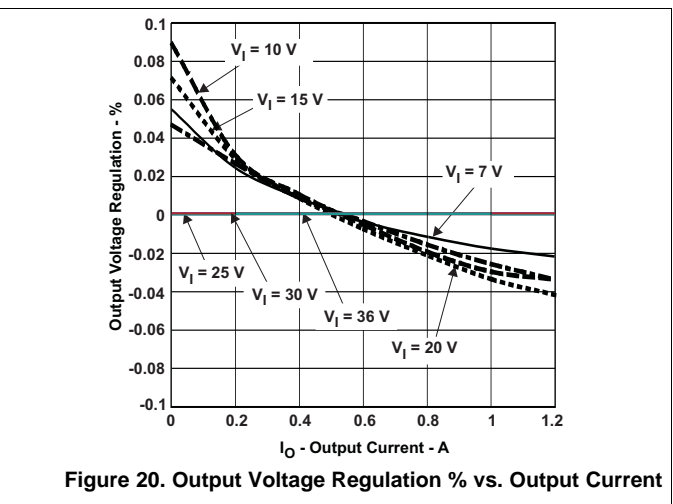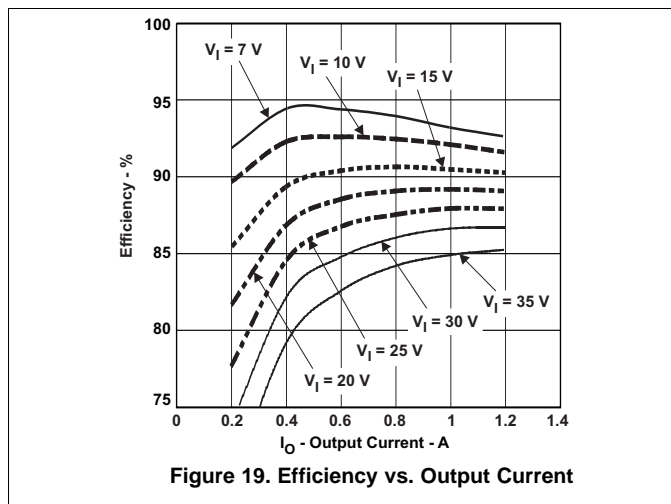
Figure 21. Output Voltage Regulation % vs. Input Voltage
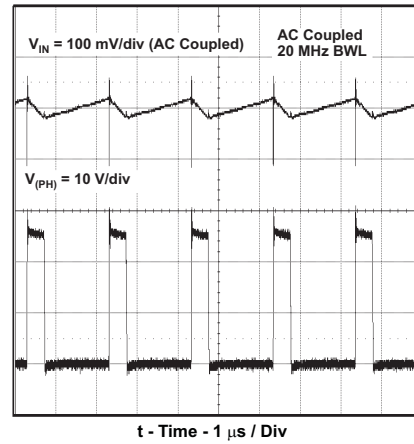
Figure 22. Input Voltage Ripple and PH Node, I_O = 1 A
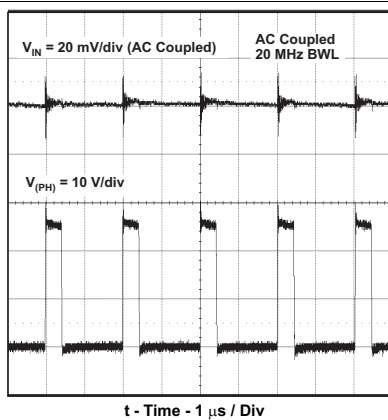
Figure 23. Output Voltage Ripple and PH Node, I_O = 1 A
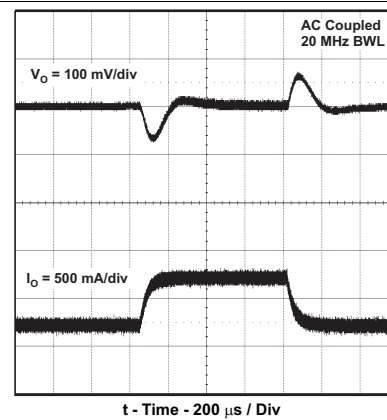
Figure 24. Transient Response, I_O Step 0.25 to 0.75 A

Product Folder Links: *TPS5410*

9   Power Supply Recommendations

The TPS5410 is designed to operate from an input voltage supply range between 5.5 V and 36 V. This input supply should remain within the input voltage supply range. If the input supply is located more than a few inches from the TPS5410 converter bulk capacitance may be required in addition to the ceramic bypass capacitors. An electrolytic capacitor with a value of 100 µF is a typical choice.

10   Layout

10.1   Layout Guidelines

Connect a low ESR ceramic bypass capacitor to the VIN pin. Care should be taken to minimize the loop area formed by the bypass capacitor connections, the VIN pin, and the TPS5410 ground pin. The best way to do this is to extend the top side ground area from under the device adjacent to the VIN trace, and place the bypass capacitor as close as possible to the VIN pin. The minimum recommended bypass capacitance is 4.7µF ceramic with a X5R or X7R dielectric.

There should be a ground area on the top layer directly underneath the IC to connect the GND pin of the device and the anode of the catch diode. The GND pin should be tied to the PCB ground by connecting it to the ground area under the device as shown in Figure 25.

The PH pin should be routed to the output inductor, catch diode and boot capacitor. Since the PH connection is the switching node, the inductor should be located close to the PH pin, and the area of the PCB conductor minimized to prevent excessive capacitive coupling. The catch diode should also be placed close to the device to minimize the output current loop area. Connect the boot capacitor between the phase node and the BOOT pin as shown. Keep the boot capacitor close to the IC and minimize the conductor trace lengths. The component placements and connections shown work well, but other connection routings may also be effective.

Connect the output filter capacitor(s) as shown between the VOUT trace and GND. It is important to keep the loop formed by the PH pin, Lout, Cout and GND as small as is practical.

Connect the VOUT trace to the VSENSE pin using the resistor divider network to set the output voltage. Do not route this trace too close to the PH trace. Due to the size of the IC package and the device pinout, the trace may need to be routed under the output capacitor. The routing may be done on an alternate layer if a trace under the output capacitor is not desired.

If the grounding scheme shown is used via a connection to a different layer to route to the ENA pin.

10.2 Layout Example

Figure 25. Design Layout

All dimensions in inches
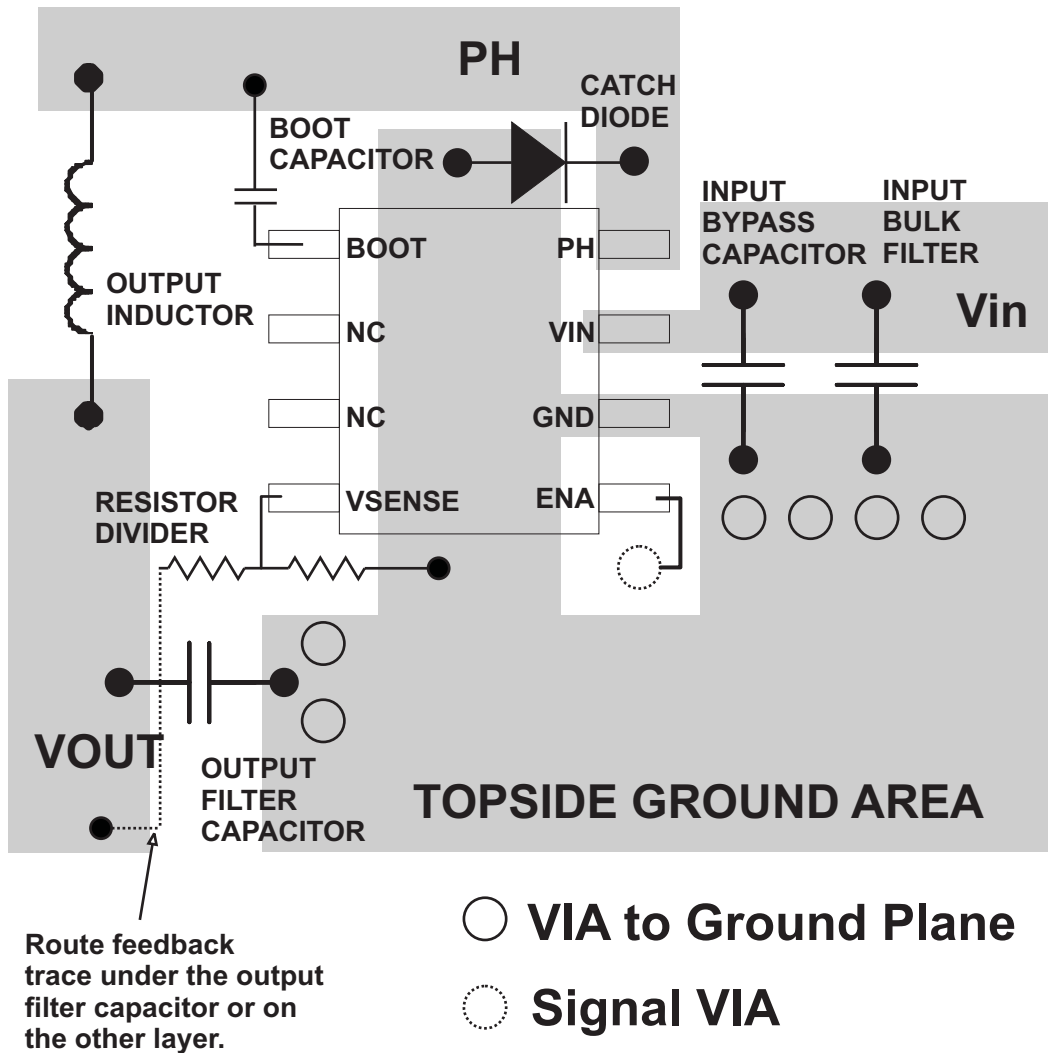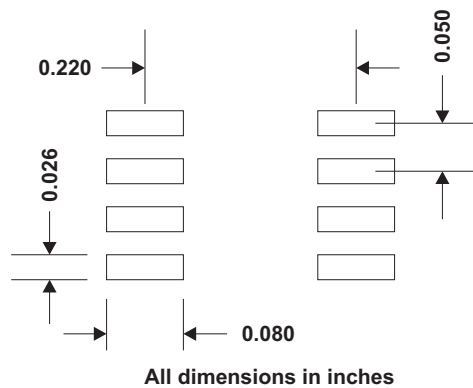
Figure 26. TPS5410 Land Pattern

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

Using TPS5410/20/30/31/50 With Aluminum/Ceramic Output Capacitors, application report, SLVA237

11.2 Trademarks

All trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
HPA00568DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS5410	Samples
TPS5410D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS5410	Samples
TPS5410DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS5410	Samples
TPS5410DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS5410	Samples
TPS5410DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS5410	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS5410 :

• Automotive: TPS5410-Q1

• Enhanced Product: TPS5410-EP

NOTE: Qualified Version Definitions:

　　　• Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

　　　• Enhanced Product - Supports Defense, Aerospace and Medical Applications

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS5410DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

![Texas Instruments logo] **TEXAS INSTRUMENTS**

PACKAGE MATERIALS INFORMATION

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS5410DR	SOIC	D	8	2500	367.0	367.0	35.0

D (R−PDSO−G8)   PLASTIC SMALL OUTLINE

0.197 (5,00)
0.189 (4,80)
△C

8   5

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80) △D

Pin 1
Index Area

1   4

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ 0.010 (0,25) Ⓜ

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.005 (0,13)

0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)

0°−8°

0.050 (1,27)
0.016 (0,40)

4040047−3/M   06/11

NOTES: A.   All linear dimensions are in inches (millimeters).
            B.   This drawing is subject to change without notice.
           △C   Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
               not exceed 0.006 (0,15) each side.
           △D   Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
            E.   Reference JEDEC MS−012 variation AA.

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D (R-PDSO-G8)   PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)

6x1,27

5,40

Stencil Openings
(Note D)

8x0,55

8x1,50

6x1,27

5,40

Example
Non Soldermask Defined Pad

Example
Pad Geometry
(See Note C)

0,60

1,55

0,07

All Around

Example
Solder Mask Opening
(See Note E)

4211283-2/E 08/12

NOTES: A.   All linear dimensions are in millimeters.
            B.   This drawing is subject to change without notice.
            C.   Publication IPC−7351 is recommended for alternate designs.
            D.   Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
                contact their board assembly site for stencil design recommendations. Refer to IPC−7525 for other stencil recommendations.
            E.   Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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