TPS6105x 1.2-A High-Power White LED Driver 2-MHz Synchronous Boost Converter With I²C Compatible Interface

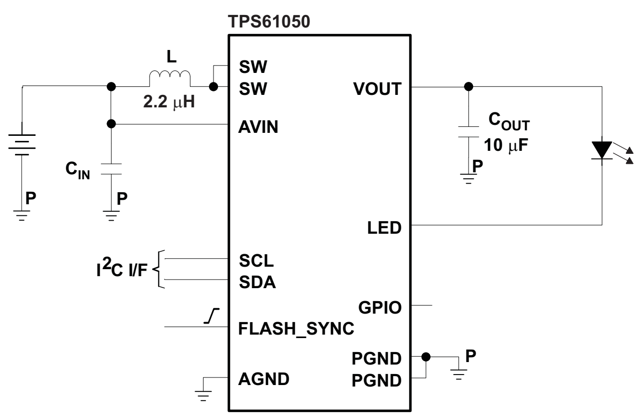
1 Features

- Four Operational Modes
  - Torch and Flash up to I_{LED} = 1200 mA
  - Voltage-Regulated Boost Converter: 4.5 V, 5 V, and 5.25 V
  - Shutdown: 0.3 µA (Typical)
- Total Solution Circuit Area < 25 mm^2
- Up to 96% Efficiency
- I^2C-Compatible Interface up to 400 kbps
- Integrated LED Turnon Safety Timer
- Zero Latency TX-Masking Input (TPS61050)
- Hardware Voltage Mode Selection Input (TPS61052)
- Integrated ADC for LED V_F Monitoring
- Integrated Low Light Dimming Mode
- LED Disconnect During Shutdown
- Open and Shorted LED Protection
- Overtemperature Protection
- Available in a 12-Pin NanoFree™ (CSP) and 10-Pin QFN Packaging

2 Applications

- Camera White LED Torch/Flash for Cell Phones, Smart-Phones and PDAs
- Audio Amplifier Power Supply

Typical Application Schematic



3 Description

The TPS6105x device is based on a high-frequency synchronous-boost topology with constant current sink to drive single white LEDs. The device uses an inductive fixed-frequency PWM control scheme using small external components, minimizing input ripple current.

The 2-MHz switching frequency allows the use of small and low profile 2.2-µH inductors. To optimize overall efficiency, the device operates with only a 250-mV LED feedback voltage.

The TPS6105x device not only operates as a regulated current source, but also as a standard voltage-boost regulator. This additional operating mode can be useful to supply other high-power devices in the system, such as a hands-free audio power amplifier, or any other component requiring a supply voltage higher than the battery voltage (refer to TPS61052).

For highest flexibility, the LED current or the desired output voltage can be programmed through an I^2C compatible interface. To simplify flash synchronization with the camera module, the device offers a trigger pin (FLASH_SYNC) for fast LED turnon time.

When the TPS6105x is not in use, it can be put into shutdown mode through the I^2C-compatible interface, reducing the input current to 0.3 µA (typical). During shutdown, the LED pin is high impedance to avoid leakage current through the LED.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS61050 TPS61052	VSON (10)	3.00 mm × 3.00 mm
	DSBGA (12)	1.96 mm × 1.46 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

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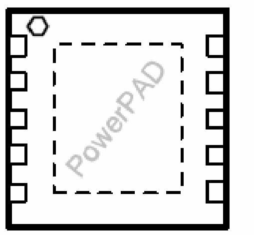
4 Revision History

Changes from Original (March 2007) to Revision A — **Page**

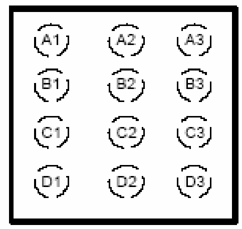
- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Updated names of the pinout drawings to reflect the new standards ... 3
- Deleted *Dissipation Ratings* table ... 4

5 Pin Configuration and Functions

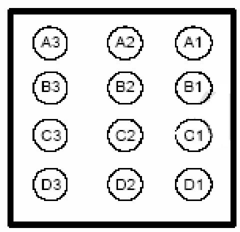
DRC Package
10-Pin VSON
Top View



YZG Package
12-Pin DSBGA
Top View



YZG Package
12-Pin DSBGA
Bottom View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	VSON	DSBGA		
AVIN	5	D3	I	This is the input voltage pin of the device. Connect directly to the input bypass capacitor.
VOUT	9	A2	O	Boost converter output.
LED	6	D2	I	LED return input. This feedback pin regulates the LED current through the internal sense resistor by regulating the voltage across it. The regulation operates with typically 250 mV dropout voltage. Connect to the cathode of the LED.
FLASH_SYNC	10	A1	I	Flash strobe pulse synchronization input.
				FLASH_SYNC = LOW (GND): The device is operating and regulating the LED current to the torch current level (TC).
				FLASH_SYNC = HIGH (VIN): The device is operating and regulating the LED current to the flash current level (FC).
SCL	2	B3	I	Serial interface clock line. This pin must not be left floating and must be terminated.
SDA	1	A3	I/O	Serial interface address/data line. This pin must not be left floating and must be terminated.
GPIO	3	C3	I/O	General purpose input/output (refer to REGISTER2). This pin can either be configured as a logic input or as an open-drain output (TPS61050).
ENVM	3	C3	I	Enable pin for voltage mode boost converter (TPS61052).
SW	8	B1, B2	I/O	Inductor connection. Drain of the internal power MOSFET. Connect to the switched side of the inductor. SW is high impedance during shutdown.
PGND	7	C1, C2	—	Power ground. Connect to AGND underneath IC.
AGND	4	D1	—	Analog ground.
PowerPAD™	—	—	—	Internally connected to PGND.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
	Voltage on AVIN, VOUT, SW, LED (2)	–0.3	7	V
	Voltage on SCL, SDA, FLASH_SYNC, GPIO, ENVM (2)	–0.3	7	V
	Input current on GPIO		25	mA
T_A	Operating ambient temperature (3)	–40	85	°C
$T_{J\ (MAX)}$	Maximum operating junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature ($T_{A(max)}$) is dependent on the maximum operating junction temperature ($T_{J(max)}$), the maximum power dissipation of the device in the application ($P_{D(max)}$), and the junction-to-ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A(max)} = T_{J(max)} - (\theta_{JA} \times P_{D(max)})$.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±1000	
		Machine model (MM)	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage range	2.5	3.6	6	V
V_{OUT}	Output voltage range in Current regulator mode	V_{IN}		5.5	V
	Output voltage range in Voltage regulator mode	4.5		5.25	
L	Inductance effective value range	1.3	2.2	2.9	V
C_{IN}	Input capacitance range		10		µH
C_{OUT}	Output capacitance effective value range	3	10	50	µF
T_J	Operating junction temperature	–40		125	

6.4 Thermal Information

THERMAL METRIC (1)		TPS6105x DRC (VSON) 10 PINS	TPS6105x YZG (DSBGA) 12 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	48.5	82	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	67.4	0.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	23	35	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.8	2.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	23.1	19.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	5.3	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

Unless otherwise noted the specification applies for V_{IN} = 3.6 V over an operating junction temp. of –40°C ≤ T_J ≤ 125°C. Typical values are for T_A = 25°C.

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
V_{IN}	Input voltage		2.5		6	V
	Minimum input voltage for start-up	MODE_CTRL[1:0] = 11, OV[1:0] = 01, R_L = 10 Ω			2.5	V
I_Q	Operating quiescent current into AVIN	MODE_CTRL[1:0] = 01, I_{LED} = 0 mA		8.5		mA
I_{SD}	Shutdown current into AVIN	MODE_CTRL[1:0] = 00, OV[1:0] ≠ 11 –40°C ≤ T_J ≤ 85°C		0.3	3	µA
		MODE_CTRL[1:0] = 00, OV[1:0] = 11 –40°C ≤ T_J ≤ 85°C		140		µA
V_{UVLO}	Undervoltage lockout threshold	V_{IN} falling		2.3	2.4	V
OUTPUT						
V_{OUT}	Output voltage	Current regulator mode	V_{IN}		5.5	V
		Voltage regulator mode	4.5		5.25	
OVP	OVP Output overvoltage protection	V_{OUT} rising	5.7	6	6.25	V
	Output overvoltage protection hysterisis			0.15		V
D	Minimum duty cycle			7.5%		
	LED current accuracy(1)	0.25 V ≤ V_{LED} ≤ 2 V, 50 mA ≤ I_{LED} ≤ 250 mA, T_J = 50°C	–15%		15%	
		0.25 V ≤ V_{LED} ≤ 2 V, 200 mA ≤ I_{LED} ≤ 1200 mA, T_J = 50°C	–12%		12%	
	LED current temperature coefficient			0.08		%/°C
	DC output voltage accuracy	2.5 V ≤ V_{IN} ≤ 0.9 V_{OUT}, PWM operation	–3%		3%	
V_{LED}	LED sense voltage	I_{LED} = 1200 mA		250		mV
	LED input leakage current	V_{LED} = V_{OUT} = 5 V, –40°C ≤ T_J ≤ 85°C		0.1	1	µA
POWER SWITCH						
$r_{DS(on)}$	Switch MOSFET on-resistance	V_{OUT} = V_{GS} = 3.6 V		80		mΩ
	Rectifier MOSFET on-resistance			80		
$I_{lkg(SW)}$	Switch MOSFET leakage	V_{DS} = 6 V, –40°C ≤ T_J ≤ 85°C		0.1	1	µA
	Rectifier MOSFET leakage			0.1	1	
I_{lim}	Switch current limit	2.5 V ≤ V_{IN} ≤ 6 V, ILIM bits = 00	850	1000	1150	mA
		2.5 V ≤ V_{IN} ≤ 6 V, ILIM bits = 01, 10 (1)	1275	1500	1725	
		2.5 V ≤ V_{IN} ≤ 6 V, ILIM bits = 11 (1)	1700	2000	2300	
	Thermal shutdown(1)		140	160		°C
	Thermal shutdown hysteresis(1)			20		°C
OSCILLATOR						
f_{SW}	Oscillator frequency		1.8	2	2.2	MHz
ADC						
	Resolution		3			Bits
	Total error(1)	V_{LED} = 0.25 V, assured monotonic by design		±0.25	±1	LSB
SDA, SCL, GPIO, ENVM, FLASH_SYNC						
$V_{(IH)}$	High-level input voltage		1.2			V
$V_{(IL)}$	Low-level input voltage				0.4	V
$V_{(OL)}$	Low-level output voltage (SDA)	I_{OL} = 8 mA			0.3	V
	Low-level output voltage (GPIO)	DIR = 1, I_{OL} = 8 mA			0.3	
$I_{(LKG)}$	Logic input leakage current	Input connected to V_{IN} or GND, –40°C ≤ T_J ≤ 85°C		0.01	0.1	µA
	GPIO pulldown resistance	DIR = 0, GPIO ≤ 0.4 V (TPS61050)		400		kΩ
	ENVM pulldown resitance	ENVM ≤ 0.4 V (TPS61052)		400		kΩ
	FLASH_SYNC pulldown resistance	FLASH_SYNC ≤ 0.4 V		400		kΩ

(1) Assured by design. Not tested in production.

Electrical Characteristics (continued)

Unless otherwise noted the specification applies for V_{IN} = 3.6 V over an operating junction temp. of –40°C ≤ T_J ≤ 125°C. Typical values are for T_A = 25°C.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
TIMING					
Start-up time	From shutdown into torch mode I_{LED} = 75 mA		1.2		ms
	From shutdown into voltage mode through ENVM I_{OUT} = 0 mA		650		µs
LED current settling time(2) triggered by rising edge on FLASH_SYNC	MODE_CTRL[1:0] = 10, I_{LED} = from 0 mA to 900 mA		400		µs
LED current settling time(2) triggered by TX mask	MODE_CTRL[1:0] = 10, I_{LED} = 900 mA to 150 mA		20		µs

(2) Settling time to ±15% of the target value

6.6 I²C Interface Timing Characteristics(1)

			MIN	TYP	MAX	UNIT
f_{SCL}	SCL clock frequency	Standard mode			100	kHz
		Fast mode			400	kHz
t_{BUF}	Bus free time between a STOP and START condition	Standard mode	4.7			µs
		Fast mode	1.3			µs
t_{HD}; t_{STA}	Hold time (repeated) START condition	Standard mode	4			µs
		Fast mode	600			ns
t_{LOW}	LOW period of the SCL clock	Standard mode	4.7			µs
		Fast mode	1.3			µs
t_{HIGH}	HIGH period of the SCL clock	Standard mode	4			µs
		Fast mode	600			ns
t_{SU}; t_{STA}	Setup time for a repeated START condition	Standard mode	4.7			µs
		Fast mode	600			ns
t_{SU}; t_{DAT}	Data setup time	Standard mode	250			ns
		Fast mode	100			ns
t_{HD}; t_{DAT}	Data hold time	Standard mode	0		3.45	µs
		Fast mode	0		0.9	µs
t_{RCL}	Rise time of SCL signal	Standard mode	20 + 0.1C_B		1000	ns
		Fast mode	20 + 0.1C_B		300	ns
t_{RCL1}	Rise time of SCL signal after a repeated START condition and after an acknowledge bit	Standard mode	20 + 0.1C_B		1000	ns
		Fast mode	20 + 0.1C_B		1000	ns
t_{FCL}	Fall time of SCL signal	Standard mode	20 + 0.1C_B		300	ns
		Fast mode	20 + 0.1C_B		300	ns
t_{RDA}	Rise time of SDA signal	Standard mode	20 + 0.1C_B		1000	ns
		Fast mode	20 + 0.1C_B		300	ns
t_{FDA}	Fall time of SDA signal	Standard mode	20 + 0.1C_B		300	ns
		Fast mode	20 + 0.1C_B		300	ns
t_{SU}; t_{STO}	Setup time for STOP condition	Standard mode	4			µs
		Fast mode	600			ns
C_B	Capacitive load for SDA and SCL				400	pF

(1) Assured by design. Not tested in production.

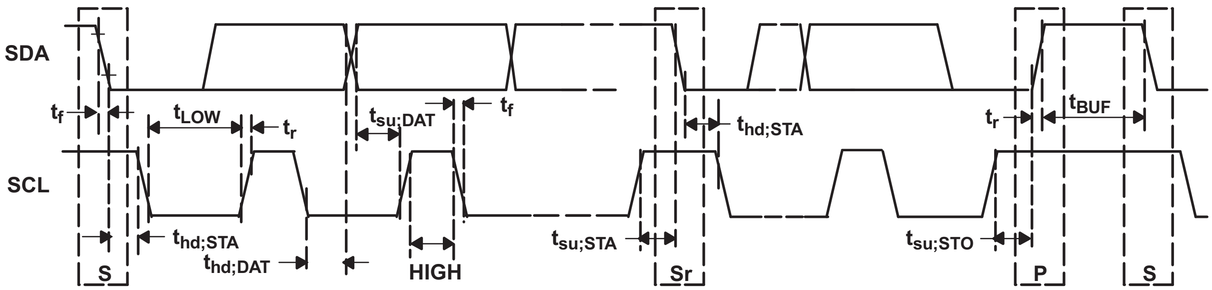


Figure 1. Serial Interface Timing For F/S-Mode

6.7 Typical Characteristics

Table 1. Table of Graphs

GRAPH TITLE		FIGURE
LED Power Efficiency	vs Input Voltage	Figure 2, Figure 3
DC Input Current	vs Input Voltage	Figure 4
LED Current	vs LED Pin Headroom Voltage	Figure 5
LED Current	vs LED Current Digital Code	Figure 6, Figure 7, Figure 8
Voltage Mode Efficiency	vs Output Current	Figure 9
DC Output Voltage	vs Load Current	Figure 10
DC Output Voltage	vs Input Voltage	Figure 11
Quiescent Current	vs Input Voltage	Figure 12
Shutdown Current	vs Input Voltage	Figure 13
Junction Temperature	vs GPIO Voltage	Figure 14

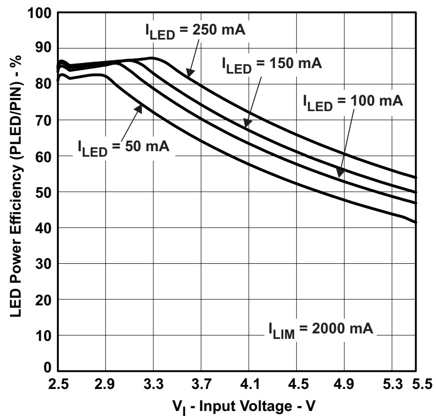


Figure 2. LED Power Efficiency vs Input Voltage

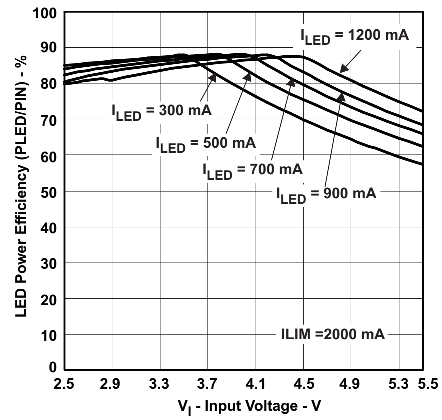


Figure 3. LED Power Efficiency vs Input Voltage

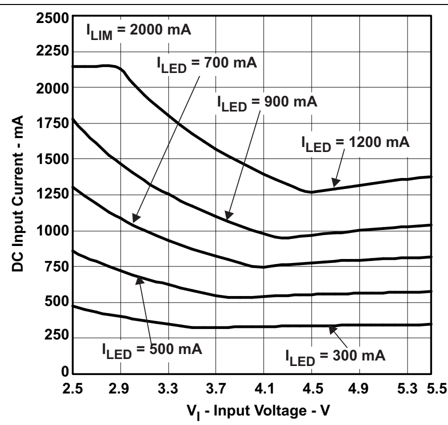


Figure 4. DC Input Current vs Input Voltage

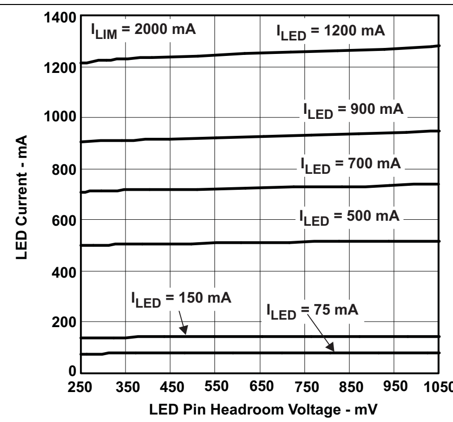


Figure 5. LED Current vs LED Pin Headroom Voltage

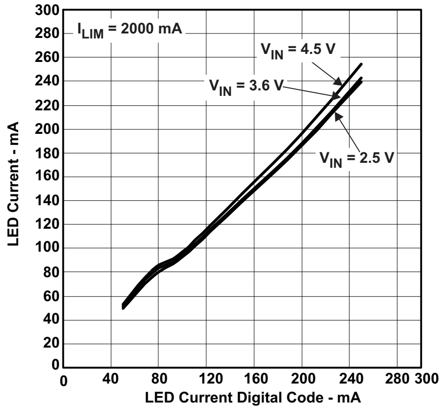


Figure 6. LED Current vs LED Current Digital Code

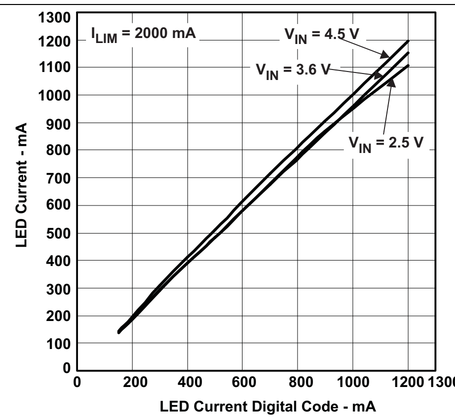


Figure 7. LED Current vs LED Current Digital Code

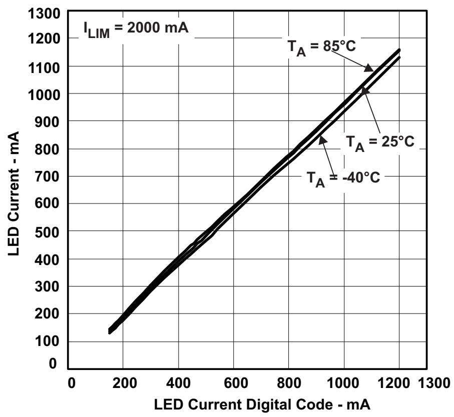


Figure 8. LED Current vs LED Current Digital Code

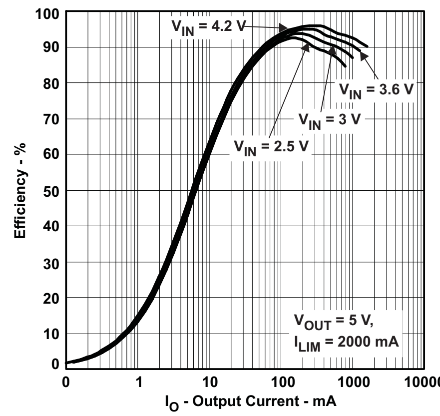


Figure 9. Voltage Mode Efficiency vs Load Current

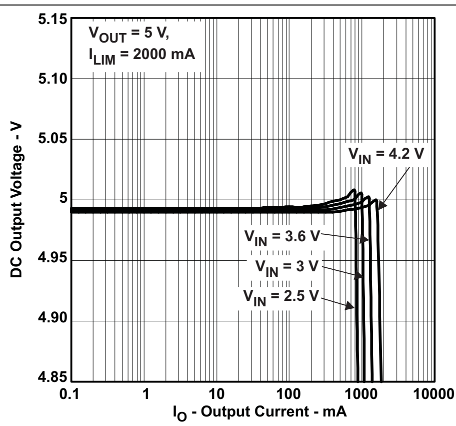


Figure 10. DC Output Voltage vs Output Current

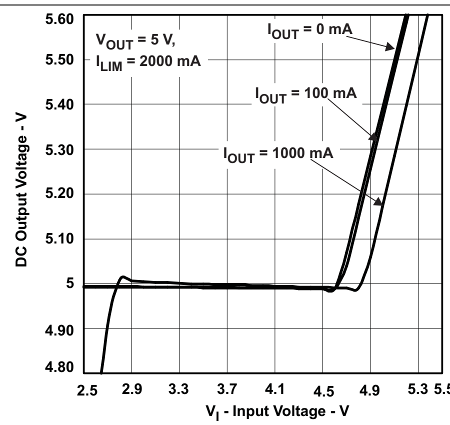


Figure 11. DC Output Voltage vs Input Voltage

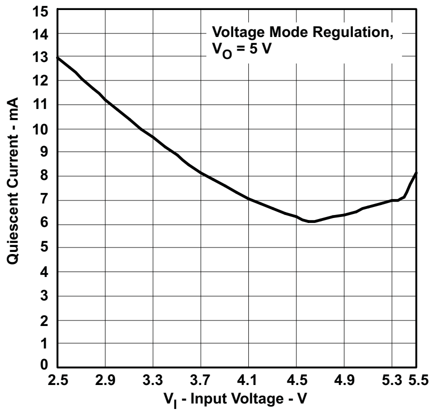


Figure 12. Quiescent Current vs Input Voltage

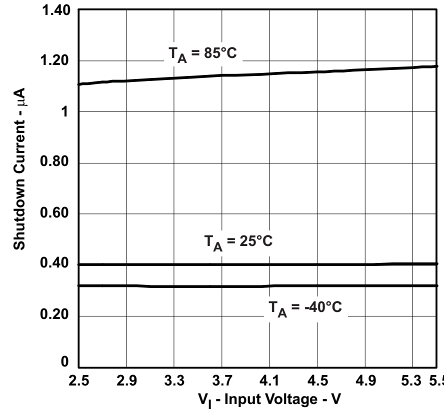


Figure 13. Shutdown Current vs Input Voltage

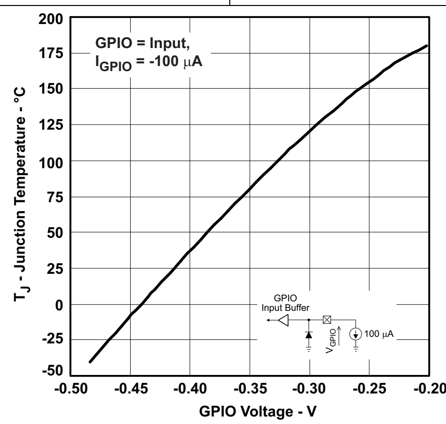


Figure 14. Junction Temperature vs GPIO Voltage

7 Detailed Description

7.1 Overview

The TPS6105x family employs a 2-MHz constant-frequency, current-mode PWM converter to generate the output voltage required to drive high-power LEDs. The device integrates a power stage based on an NMOS switch and a synchronous NMOS rectifier. The device also implements a linear low-side current regulator to control the LED current when the battery voltage is higher than the diode forward voltage.

In boost mode, the duty cycle of the converter is set by the error amplifier and the saw-tooth ramp applied to the comparator. Because the control architecture is based on a current-mode control, a compensation ramp is added to allow stable operation at duty cycles larger than 50%. The converter is a fully-integrated synchronous-boost converter, always operating in continuous-conduction mode. This allows low-noise operation, and avoids ringing on the switch pin, which would be seen on a converter when entering discontinuous-conduction mode.

The TPS6105x device not only operates as a regulated current source but also as a standard voltage-boost regulator. In the TPS61052 device, the voltage-mode operation can be activated either by a software command or by means of a hardware signal (ENVM). This additional operating mode can be useful to properly synchronize the converter when supplying other high-power devices in the system, such as a hands-free audio power amplifier, or any other component requiring a supply voltage higher than the battery voltage.

The TPS6105x integrates an I^2C-compatible interface, allowing transfers up to 400 kbps. This communication interface can be used to

- set the operating mode (shutdown, constant output current mode vs. constant output voltage mode).
- control the brightness of the external LED (torch and flash modes).
- adjust the output voltage (4.5 V / 5 V / 5.25 V) or to program the safety timer.

For more details, refer to the I^2C *Register Description* section.

The torch and flash functions can be controlled by the I^2C interface. To simplify flash synchronization with the camera module, the device offers a FLASH_SYNC strobe input pin to switch (with zero latency) the LED current from flash to torch light. The maximum duration of the flash pulse can be limited by means of an internal user-programmable safety timer (STIM).

7.2 Functional Block Diagram

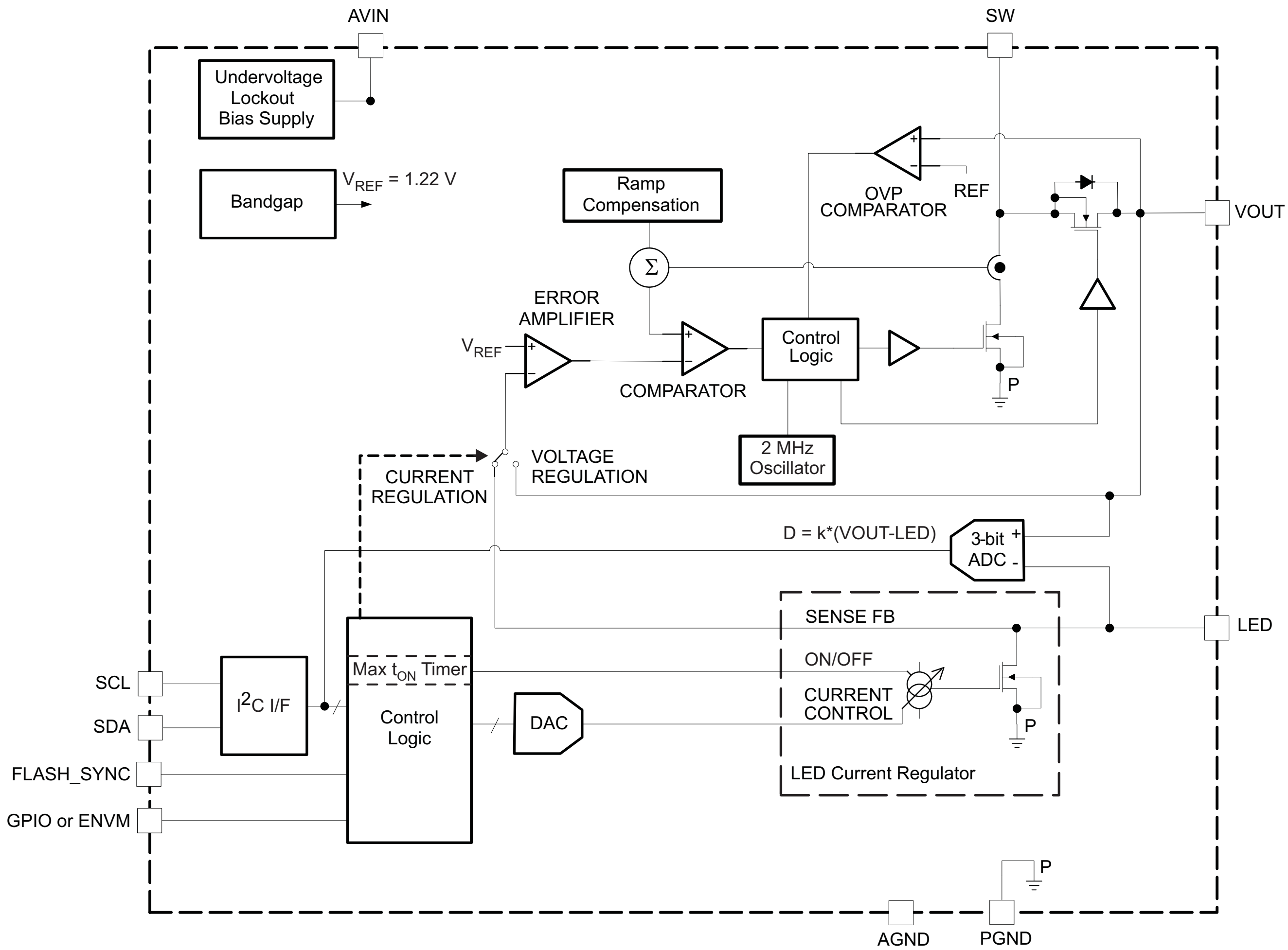


Figure 15. Functional Block Diagram

Functional Block Diagram (continued)

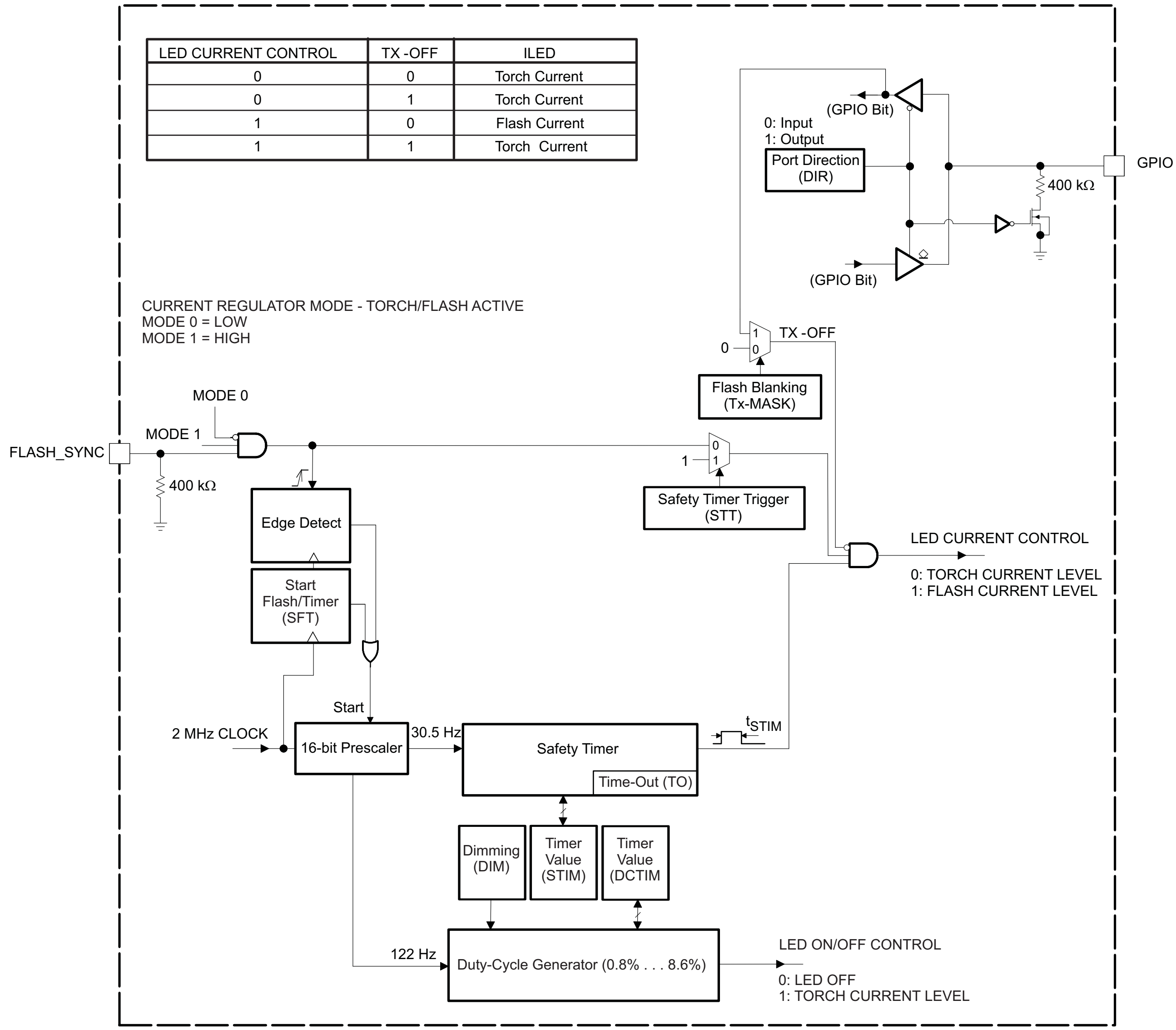


Figure 16. Timer Block Diagram (TPS61050)

Functional Block Diagram (continued)

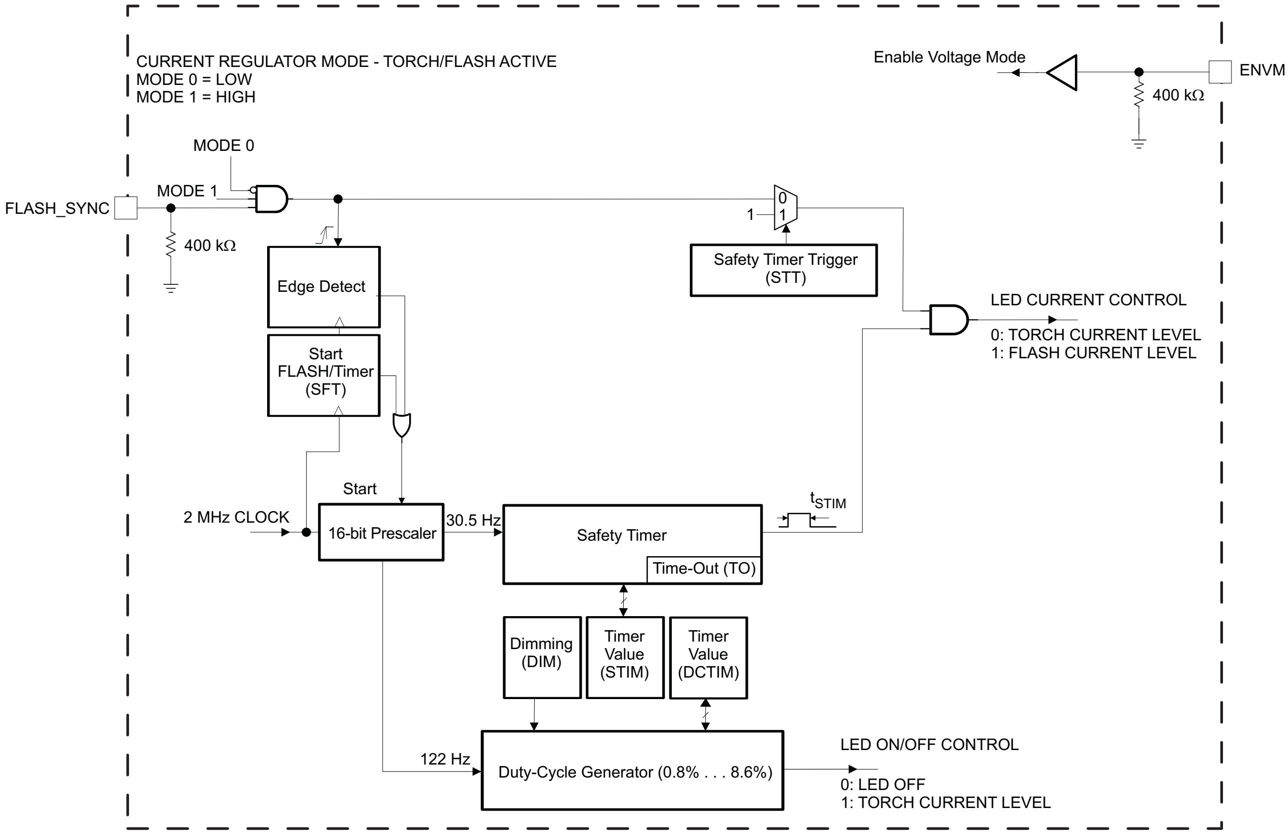


Figure 17. Timer Block Diagram (TPS61052)

7.3 Feature Description

7.3.1 Efficiency

The sense voltage has a direct effect on the converter's efficiency. Because the voltage across the low-side current regulator does not contribute to the output power (LED brightness), the lower the sense voltage, the higher the efficiency will be.

When running in boost mode ($V_{F(LED)} > V_{IN}$), the voltage present at the LED pin of the low-side current regulator is typically 250 mV, which contributes to high power-conversion efficiency.

When running in the linear down-converter mode ($V_{F(LED)} < V_{IN}$), the low-side current regulator drops the voltage difference between the input voltage and the LED forward voltage. Depending on the input voltage and the LED forward voltage characteristic, the converter displays efficiency of approximately 80% to 90%.

7.3.2 Soft-Start

Because the output capacitor always remains biased to the input voltage, the TPS6105x can immediately start switching once it has been enabled through the I^2C-compatible interface (refer to MODE_CTRL[1:0] bits). The device starts-up by smoothly ramping up its internal reference voltage, thus limiting the inrush current.

7.3.3 Shutdown

The MODE_CTRL[1:0] bits are low, the device is forced into shutdown. Depending on the setting of OV[1:0] the device can enter different shutdown modes. In shutdown mode, the regulator stops switching and the LED pin is high impedance thus eliminating any DC conduction path.

Feature Description (continued)

If OV[1:0] ≠ 11, the internal switch and rectifier MOSFET are turned off. VOUT is one body-diode drop below the input voltage and the device consumes only a shutdown current of 0.3 μA (typical). The output capacitor remains biased to the input voltage.

If OV[1:0] = 11, the internal switch MOSFET is turned off and the rectifier MOSFET is turned on. In this shutdown mode there is almost no dropout voltage between the converter's input and output. The shutdown current is 150 μA (typical).

7.3.4 LED Failure Modes

If the LED fails as a short circuit, the low-side current regulator limits the maximum output current and the LED FAILURE (LF) flag will be set.

If the LED fails as an open circuit, the control loop initially attempts to regulate off of its low-side current regulator feedback signal. This drives VOUT higher. Because the open-circuited LED will never accept its programmed current, VOUT must be voltage-limited by means of a secondary control loop. In this failure mode, the TPS6105x limits VOUT to 6 V (typical) and sets the LED FAILURE (LF) flag.

7.3.5 Undervoltage Lockout

The undervoltage lockout circuit prevents the device from misoperation at low input voltages. It prevents the converter from turning on the switch or rectifier MOSFET under undefined conditions.

7.3.6 Thermal Shutdown

As soon as the junction temperature, T_J, exceeds 160°C typical, the device goes into thermal shutdown. In this mode, the *boost* power stage and the low-side current regulator are turned off, the MODE_CTRL[1:0] bits are reset, the OVERTEMP bit is set and can only be reset by a readout.

7.4 Device Functional Modes

7.4.1 Operating Modes: Torch and Flash

The device operation is more easily understood by referring to the timer block diagram. Depending on the settings of MODE_CTRL[1:0] bits the device can enter 4 different operating modes:

- MODE_CTRL[1:0] = 00: The device is in shutdown mode.
- MODE_CTRL[1:0] = 01: The device is regulating the LED current to the torch current level (TC bits) regardless of the FLASH_SYNC input and START_FLASH/TIMER (SFT) bit. The safety timer is disabled in this operating mode.
- MODE_CTRL[1:0] = 11: The device is regulating a constant output voltage according to OV[1:0] bits settings. The low-side LED current regulator is disabled and the LED is disconnected from the output. In this operating mode, the safety timer is disabled and the general purpose timer (DCTIM) can be used to generate a software time-out (TO) flag. DCTIM start is triggered on the rising edge of START_FLASH/TIMER (SFT).
- MODE_CTRL[1:0] = 10: The flash pulse can be either trigger by a hardware signal (FLASH_SYNC) or by a software bit (SFT).

Flash strobe is level sensitive (STT = 0): LED strobe pulse follows FLASH_SYNC

- FLASH_SYNC and (SFT) = 0: LED operation is set to the torch current level and the safety timer is disabled.
- FLASH_SYNC or (SFT) = 1: The LED is driven at the flash current level and the safety timer is running.

The maximum duration of the flash pulse is defined in the STIM register.

Device Functional Modes (continued)

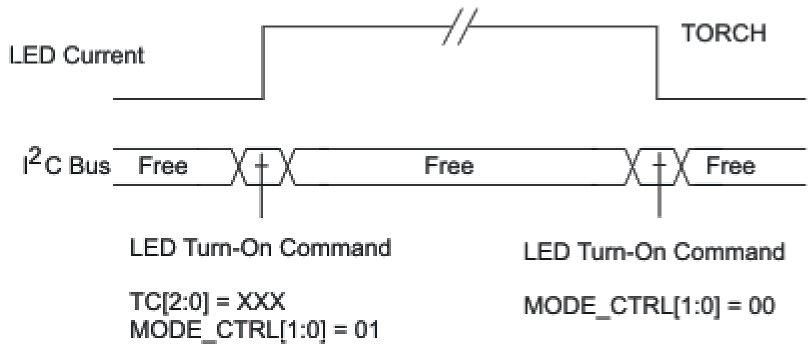


Figure 18. Torch Mode Operation

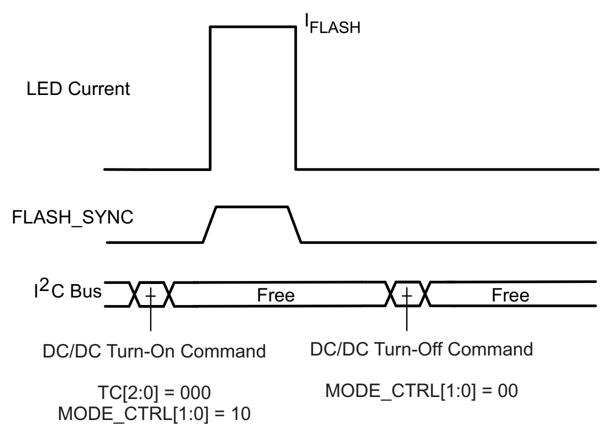


Figure 19. Synchronized Flash Strobe

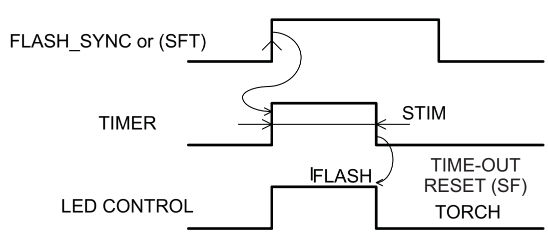


Figure 20. Level Sensitive Safety Timer (Time-Out)

Device Functional Modes (continued)

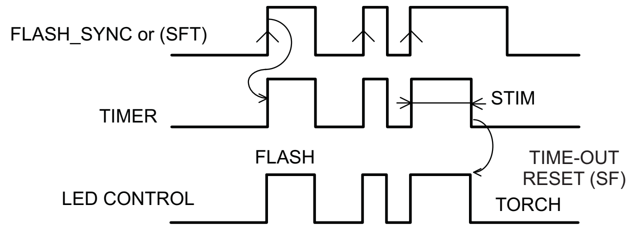


Figure 21. Level Sensitive Safety Timer (Normal Operation + Time-Out)

The safety timer is started by:

- a rising edge of FLASH_SYNC signal.
- a rising edge of START_FLASH/TIMER (SFT) bit.

The safety timer is stopped by:

- a low level of FLASH_SYNC signal or START_FLASH/TIMER (SFT) bit.
- a time-out signal (TO).

The START-FLASH/TIMER (SFT) bit is reset by the time-out (TO) signal.

The Flash strobe is edge sensitive (STT = 1): The LED strobe pulse is triggered by a rising edge

When FLASH_SYNC and START_FLASH/TIMER (SFT) are both low, the LED operation is set to the torch current level without time-out.

The duration of the flash pulse is defined in the STIM register. The flash strobe is started by:

- a rising edge of FLASH_SYNC signal.
- a rising edge of START_FLASH/TIMER (SFT) bit.

Once running, the timer ignores any triggering signal, and only stops after a time-out (TO). The START-FLASH/TIMER (SFT) bit is reset by the time-out (TO) signal.

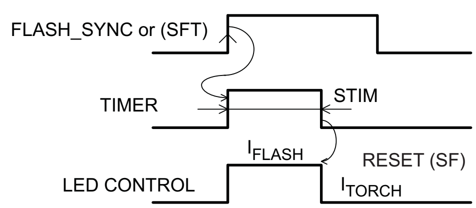


Figure 22. Edge Sensitive Timer (Single Trigger Event)

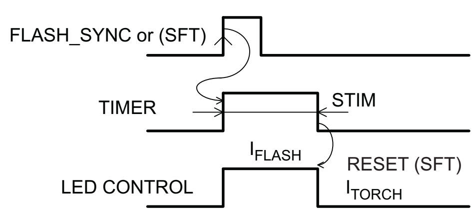


Figure 23. Edge Sensitive Timer (Single Trigger Event)

Device Functional Modes (continued)

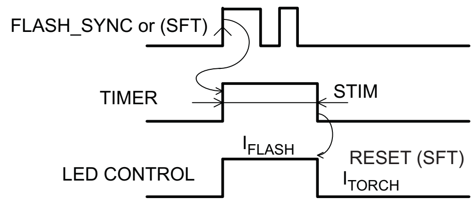


Figure 24. Edge Sensitive Timer (Multiple Trigger Events)

7.4.2 Mode of Operation: Flash Blanking (TPS61050)

The TPS61050 device also integrates a general purpose I/O pin (GPIO) that can be configured either as a standard logic input/output or as a flash masking input (Tx-MASK). This blanking function turns the LED from flash to torch light, thereby reducing almost instantaneously the peak current loading from the battery. The Tx-MASK function has no influence on the safety timer duration.

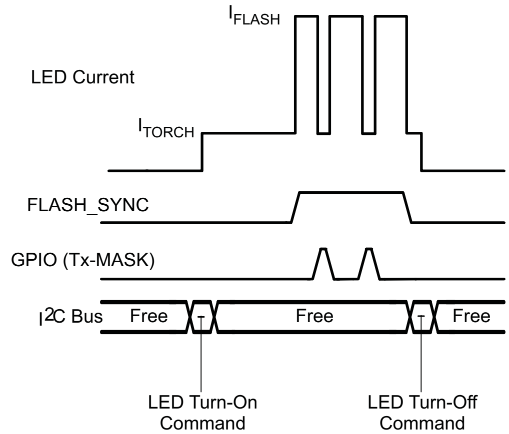


Figure 25. Synchronized Flash With Blanking Periods

7.4.3 Hardware Voltage Mode Selection (TPS61052)

The TPS61052 device integrates a logic input (ENVM) that can be used to force the converter to run in voltage mode regulation. This additional operating mode can be useful to supply other high power consumption devices in the system (for example, hands-free audio power amplifier) or any other component requiring a supply voltage higher than the battery voltage.

Table 2 gives an overview of the different mode of operation of TPS61052.

Table 2. TPS61052 Operating Modes

INTERNAL REGISTER SETTINGS MODE_CTRL[1:0]	ENVM	OPERATING MODES
00	0	Power stage is in shutdown. The output is either connected directly to the battery (OV[1:0]=11, rectifier is bypassed) or through the rectifer's body diode (OV[1:0]=01). In both case the power stage LC filter is connected in series between the battery and the output.
01	0	LED is turned-on for DC light operation. The converter is operating in the current regulation mode (CM). The output voltage is controlled by the forward voltage characteristic of the LED.
10	0	LED is turned-on for flash operation. The converter is operating in the current regulation mode (CM). The output voltage is controlled by the forward voltage characteristic of the LED.
11	0	LED is turned-off and the converter is operating in the voltage regulation mode (VM). The output voltage is set through the register OV[1:0].
00	1	LED is turned-off and the converter is operating in the voltage regulation mode (VM). The output voltage is set through the register OV[1:0].

Device Functional Modes (continued)

Table 2. TPS61052 Operating Modes (continued)

INTERNAL REGISTER SETTINGS MODE_CTRL[1:0]	ENVM	OPERATING MODES
01	1	The converter is operating in the voltage regulation mode (VM) and it's output voltage is set through the register OV[1:0]. The LED is turned-on for torch operation according to the register TC[2:0]. The LED current is regulated by the means of the low-side current sink.
10	1	The converter is operating in the voltage regulation mode (VM) and it's output voltage is set through the register OV[1:0]. The LED is turned-on for flash operation according to the register FC[2:0]. The LED current is regulated by the means of the low-side current sink.
11	1	LED is turned-off and the converter is operating in the voltage regulation mode (VM). The output voltage is set through the register OV[1:0].

7.4.4 Low Light Dimming Mode

The TPS6105x device features white LED drive capability at very low light intensity. To generate a reduced LED average current, the device employs a 122-Hz fixed frequency PWM modulation scheme. Operation is understood best by referring to the timer block diagram.

The torch current is modulated with a duty cycle defined by the DCTIM[2:0] bits. The low light dimming mode can only be activated in the torch only mode, MODE_CTRL[1:0] = 01.

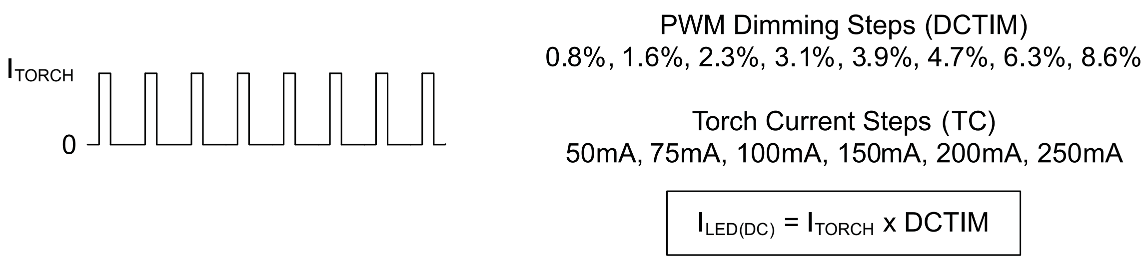


Figure 26. PWM Dimming Principle

White LED blinking can be achieved by turning on/off periodically the LED dimmer through the (DIM) bit, see Figure 27.

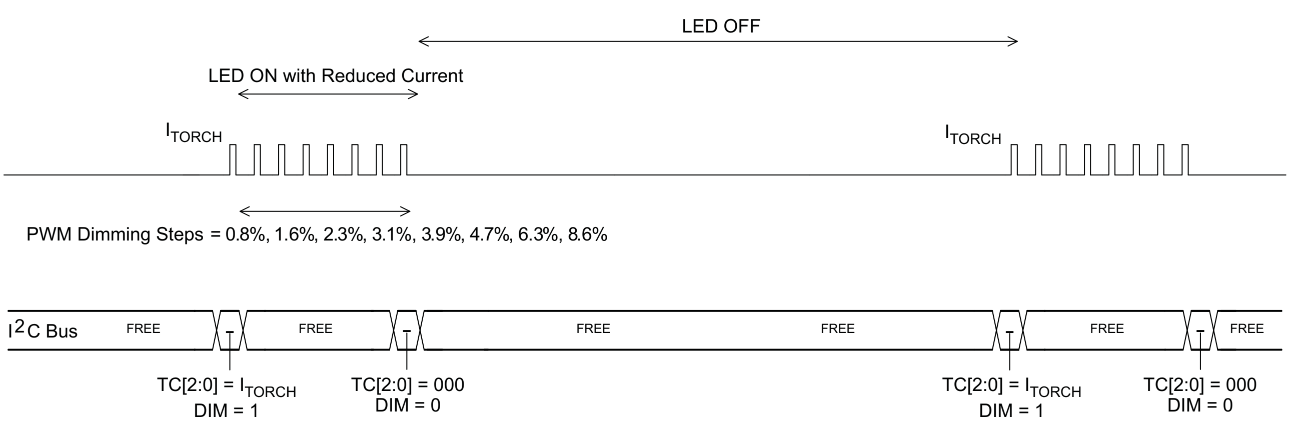


Figure 27. White LED Blinking Control

7.5 Programming

7.5.1 3-Bit ADC

The TPS6105x device integrates a 3 bit A/D converter to measure the differential voltage across the output and the low-side current regulator. To get a proper settling of the LED forward voltage, the data acquisition is done approximately 10 ms after the start of the flash sequence.

When running in the linear down-mode ($V_{F(LED)} < V_{IN}$), the low-side current regulator drops the voltage difference between the input voltage and the LED forward voltage. This may result in thermal limitations (especially for CSP-12 packaging) when running high LED current under high battery conditions ($V_{IN} \geq 4.5$ V) with low forward voltage LEDs and/or high ambient temperature.

The LED forward voltage measurement can be started either by a START FLASH event (FLASH_SYNC or SFT bit) or by setting ADC[2:0] bits (whilst MODE_CTRL[1:0]=01 or 10).

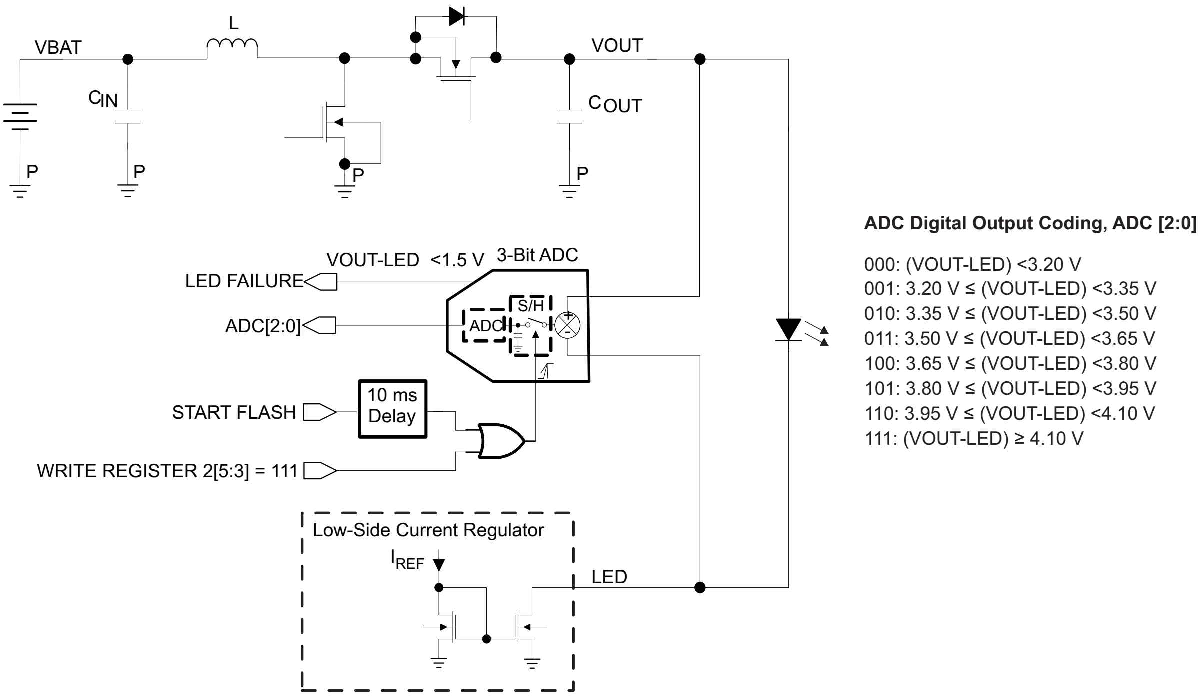


Figure 28. LED VF Measurement Principle

7.5.2 Serial Interface Description

I^2C is a 2-wire serial interface developed by Philips Semiconductor (see I^2C-Bus Specification, Version 2.1, January 2000). The bus consists of a data line (SDA) and a clock line (SCL) with pullup structures. When the bus is *idle*, both SDA and SCL lines are pulled high. All the I^2C compatible devices connect to the I^2C bus through open-drain I/O pins, SDA and SCL. A *master* device, usually a microcontroller or a digital signal processor, controls the bus. The master is responsible for generating the SCL signal and device addresses. The master also generates specific conditions that indicate the START and STOP of data transfer. A *slave* device receives and/or transmits data on the bus under control of the master device.

The TPS6105x device works as a *slave* and supports the following data transfer *modes*, as defined in the I^2C-Bus Specification: standard mode (100 kbps) and fast mode (400 kbps). The interface adds flexibility to the power supply solution, enabling most functions to be programmed to new values depending on the instantaneous application requirements. Register contents remain intact as long as the supply voltage remains greater than approximately 2 V.

The data transfer protocol for standard and fast modes is exactly the same, therefore they are referred to as F/S-mode in this document. The TPS6105x device supports 7-bit addressing; 10-bit addressing and general call address are not supported. The device 7-bit address is defined as 011 0011.

Programming (continued)

7.5.3 F/S-Mode Protocol

The master initiates data transfer by generating a start condition. The start condition is when a high-to-low transition occurs on the SDA line while SCL is high, as shown in Figure 29 All I²C-compatible devices should recognize a start condition.

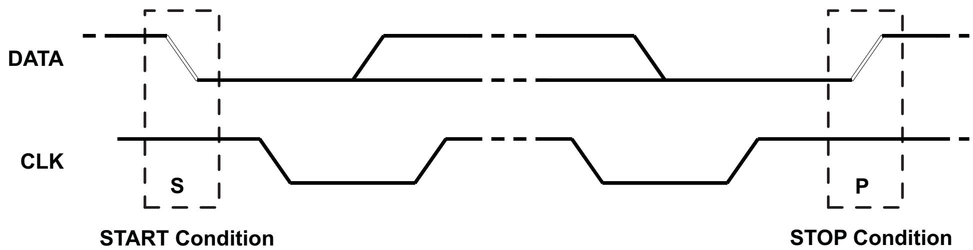


Figure 29. Start and Stop Conditions

The master then generates the SCL pulses, and transmits the 7-bit address and the read/write direction bit R/W on the SDA line. During all transmissions, the master ensures that data is valid. A valid data condition requires the SDA line to be stable during the entire high period of the clock pulse (see Figure 30). All devices recognize the address sent by the master and compare it to their internal fixed addresses. Only the slave device with a matching address generates an acknowledge (see Figure 31) by pulling the SDA line low during the entire high period of the ninth SCL cycle. Upon detecting this acknowledge, the master knows that communication link with a slave has been established.

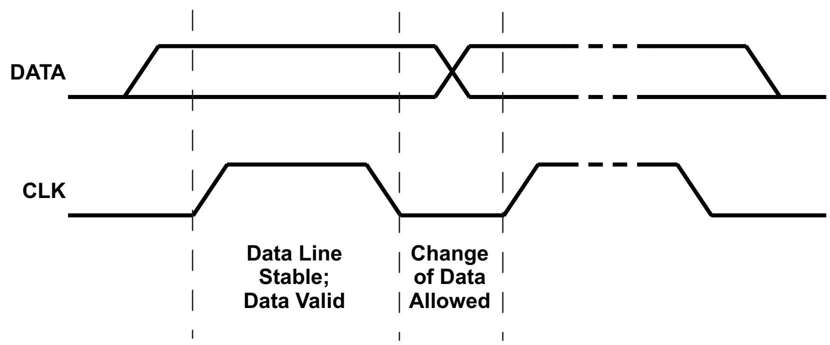


Figure 30. Bit Transfer on the Serial Interface

The master generates further SCL cycles to either transmit data to the slave (R/W bit 1) or receive data from the slave (R/W bit 0). In either case, the receiver must acknowledge the data sent by the transmitter. So an acknowledge signal can either be generated by the master or by the slave, depending on which one is the receiver. 9-bit valid data sequences consisting of 8-bit data and 1-bit acknowledge can continue as long as necessary.

To signal the end of the data transfer, the master generates a stop condition by pulling the SDA line from low to high while the SCL line is high (see Figure 29). This releases the bus and stops the communication link with the addressed slave. All I²C compatible devices must recognize the stop condition. Upon the receipt of a stop condition, all devices know that the bus is released, and they wait for a start condition followed by a matching address.

Attempting to read data from register addresses not listed in this section will result in 00h being read out.

Programming (continued)

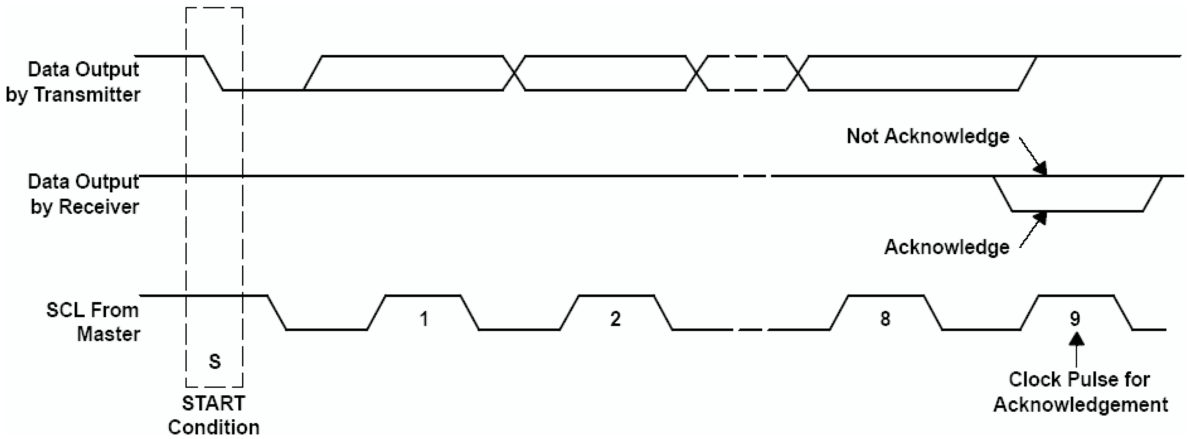


Figure 31. Acknowledge on the I²C Bus

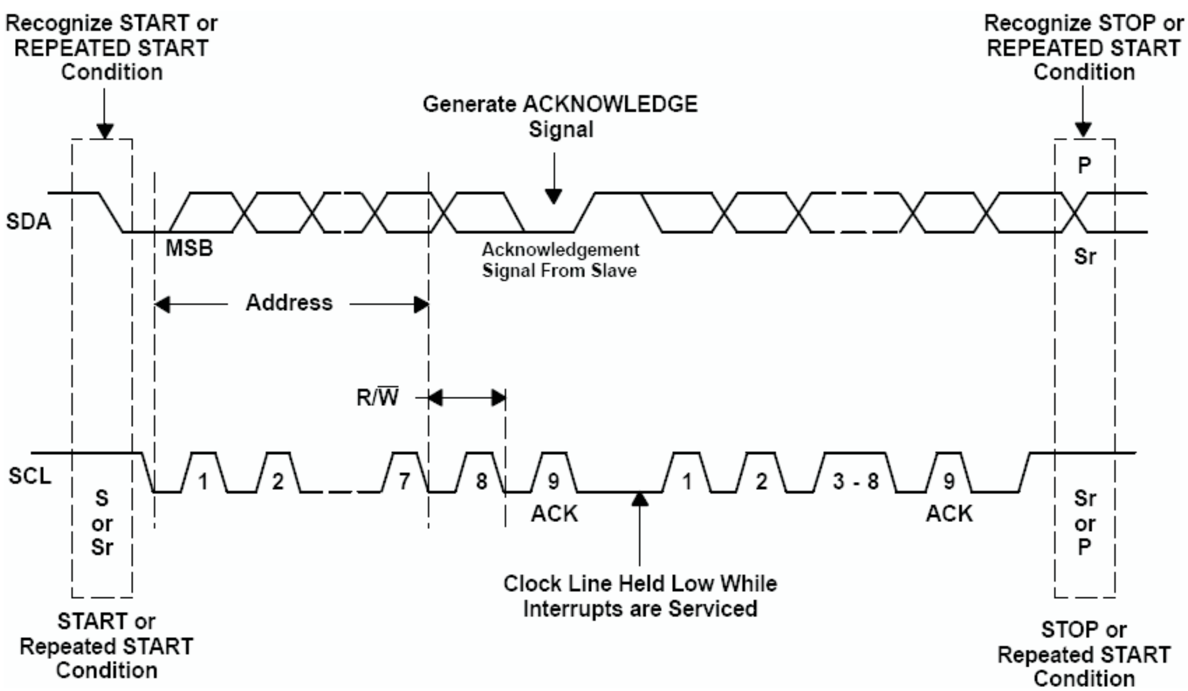


Figure 32. Bus Protocol

7.5.4 TPS6105X I²C Update Sequence

The TPS6105x requires a start condition, a valid I²C address, a register address byte, and a data byte for a single update. After the receipt of each byte, TPS6105x device acknowledges by pulling the SDA line low during the high period of a single clock pulse. A valid I²C address selects the TPS6105x. TPS6105x performs an update on the rising edge of the SCL clock that follows the ACK bit transmission.

Programming (continued)

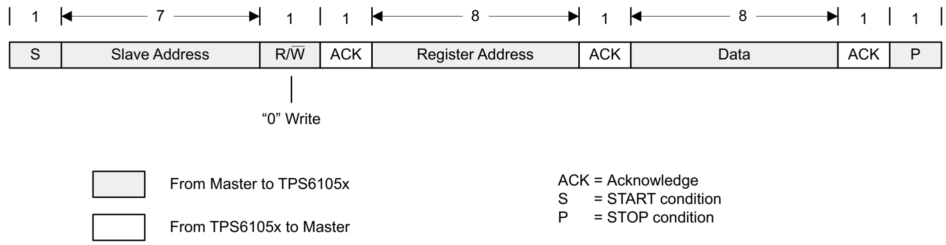


Figure 33. Write Data Transfer Format In F/S-Mode

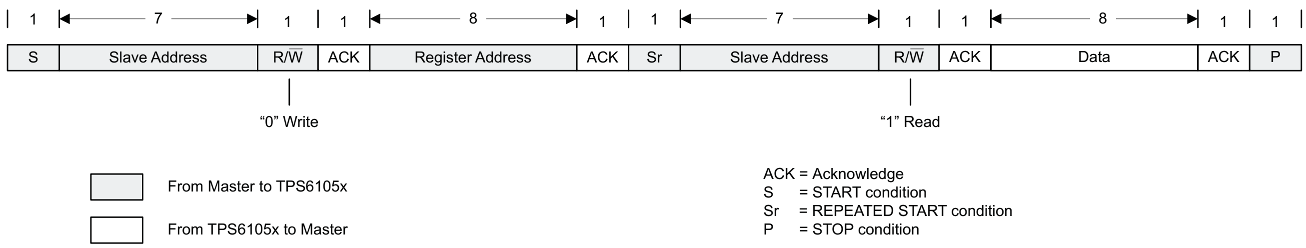


Figure 34. Read Data Transfer Format In F/S-Mode

SLAVE ADDRESS BYTE

MSB							LSB
X	0	1	1	0	0	1	1

The slave address byte is the first byte received following the START condition from the master device.

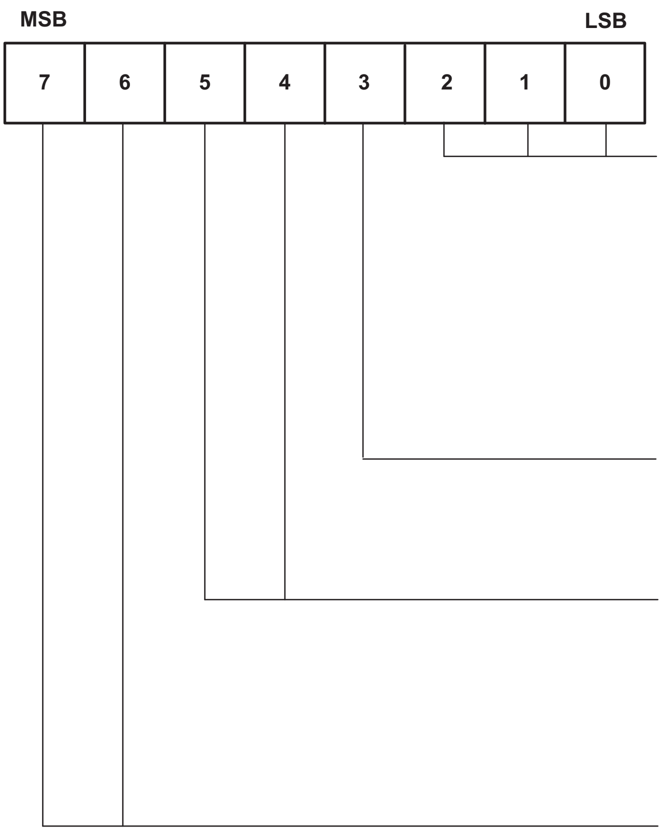
REGISTER ADDRESS BYTE

MSB							LSB
0	0	0	0	0	0	D1	D0

Following the successful acknowledgement of the slave address, the bus master will send a byte to the TPS6105x, which will contain the address of the register to be accessed. The TPS6105x contains four 8-bit registers accessible through a bidirectional I²C-bus interface. All internal registers have read and write access.

7.6 Register Maps

7.6.1 Register Description



Memory location: 00
Reset state: 0001 0010

TORCH CURRENT, TC[2:0]

000: 0 mA
(dc/dc switching, LED Off, VOUT set according to OV[1:0]
001: 50 mA
010: 75 mA (default)
011: 100 mA
100: 150 mA
101: 200 mA
110: 250 mA / 400 mA (1)
111: 250 mA / 500 mA (1)

LED DIMMING, DIM

This bit is only valid for MODE_CTRL[1:0] = 01
0: LED current is unchanged (default)
1: LED current is PWM dimmed (see DCTIM bits)

OUTPUT VOLTAGE, OV[1:0]

This bit is only valid for MODE_CTRL[1:0] = 11
00: 4.5 V constant output voltage (2)
01: 5.0 V constant output voltage (2) (default)
10: 5.25 V constant output voltage (2)
11: 5.0 V constant output voltage (3)

MODE CONTROL,MODE_CTRL[1:0]

00: Device in shutdown mode (default)
01: Device operates in torch only mode
10: Device operates in torch and flash modes
11: Device operates as constant voltage source

Writing to REGISTERS[7:6] automatically updates REGISTER[7:6].

(1) 400 mA/500 mA current level can only be activated when DIR = 0, Tx-MASK = 1 and GPIO input is set high. This operating mode only applies to TPS61050.

(2) MODE_CTRL[1:0] = 00, VOUT is one body diode below the input voltage, I_Q = 0.3 μA (typical).

(3) MODE_CTRL[1:0] = 00, rectifier MOSFET is turned on shorting VOUT and SW, I_Q = 150 μA (typical).

Figure 35. Register0 (Read/Write) (TPS6105X)

Register Maps (continued)

MSB LSB

7	6	5	4	3	2	1	0

Memory location: 01
Reset state: 0000 0100

FLASH CURRENT, FC[2:0] (bits 2–0)

000: 150 mA
001: 200 mA
010: 300 mA
011: 400 mA
100: 500 mA (default)
101: 700 mA
110: 900 mA
111: 1200 mA

START FLASH/TIMER,SFT (bit 3)

This bit is reset by the time-out of the safety timer
0: No change in LED current (default)
1: LED current ramps to the flash current level

SAFETY TIMER TRIGGER, STT (bit 4)

This bit is only valid for MODE_CTRL[1:0] = 10
0: LED safety timer is level sensitive (default)
1: LED safety timer is rising edge sensitive

TIME-OUT FLAG, TO (READ ONLY) (bit 5)

Time-out flag is reset at re-start of the safety timer.
0: No time-out event (default)
1: Time-out occurred

MODE CONTROL, MODE_CTRL[1:0] (bits 7–6)

00: Device in shutdown mode (default)
01: Device operates in torch only mode
10: Device operates in torch and flash modes
11: Device operates as constant voltage source

Writing to REGISTER1[7:6] automatically updates REGISTER0[7:6]

Figure 36. Register1 (Read/Write) (TPS6105X)

Register Maps (continued)

MSB LSB

7	6	5	4	3	2	1	0

Memory location: 02
Reset state: 000X X000

GPIO DIRECTION, DIR

0: GPIO configured as input (default)
1: GPIO configured as open-drain output

GPIO PORT BIT, GPIO

This bit contains the GPIO port value

FLASH BLANKING, Tx-MASK

This bit is only valid for DIR = 0
In write mode, this bit enables/disables the flash blanking function.
0: Flash blanking is disabled (default)
1: LED current is reduced to torch current level when GPIO = 1

In read mode, this flag indicates whether or not the flashlight masking input has been activated.
Tx-MASK flag is reset after readout of the flag.
0: No flash blanking event occured
1: Flash blanking triggered

ADC OUTPUT(1), ADC[2:0] (READ ONLY)

Refer to 3-Bit ADC section for more details.

CURRENT LIMIT(2) (3), ILIM[1:0] (WRITE ONLY)

ILIM[1:0] can only be written once whilst the device is in shutdown.
00: 1000 mA (typ) (default)
01: 1500 mA (typ)
10: 1500 mA (typ)
11: 2000 mA (typ)

LED FAILURE (3), LF (READ ONLY)

LED failure flag is reset after readout of the flag.
0: Proper LED operation
1: LED failed (open or shorted)

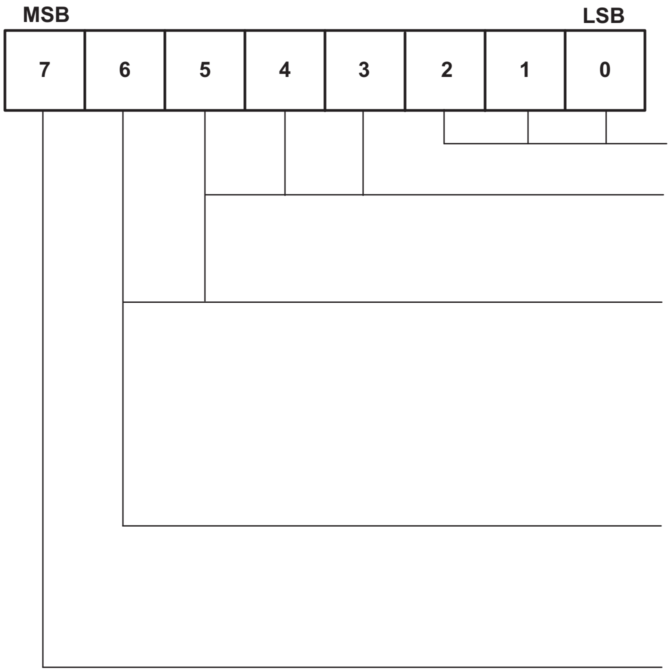
OVERTEMP (READ ONLY)

Time-out flag is reset after readout of the flag.
0: Normal operation (default)
1: Thermal shutdown tripped

(1) Setting bits 3, 4 and 5 (whilst MODE_CTRL[1:0]=01 or 10) starts an LED forward voltage measurement.
(2) A write operation on bit 5 and 6 points to the ILIM[1:0] bits.
(3) A read operation on bit 5 and 6 points to the LF and ADC[2] bits.

Figure 37. Register2 (Read/Write) (TPS61050)

Register Maps (continued)



Memory location: 02
Reset state: 011X X000

RESERVED, DO NOT CARE

ADC OUTPUT[1], ADC[2:0] (READ ONLY)

Refer to 3-Bit ADC section for more details.

CURRENT LIMIT[2] [3], ILIM[1:0] (WRITE ONLY)

ILIM[1:0] can only be writen once whilst the device is in shutdown.
00: 1000 mA (typ)
01: 1500 mA (typ)
10: 1500 mA (typ)
11: 2000 mA (typ) (default)

LED FAILURE[3], LF (READ ONLY)

LED failure flag is reset after readout of the flag.
0: Proper LED operation
1: LED failed (open or shorted)

OVERTEMP (READ ONLY)

Time-out flag is reset after readout of the flag.
0: Normal operation (default)
1: Thermal shutdown tripped

(1) Setting bits 3, 4 and 5 (whilst MODE_CTRL[1:0]=01 or 10) starts an LED forward voltage measurement.
(2) A write operation on bit 5 and 6 points to the ILIM[1:0] bits.
(3) A read operation on bit 5 and 6 points to the LF and ADC[2] bits.

Figure 38. Register2 (Read/Write) (TPS61052)

Register Maps (continued)

MSB ... LSB

7	6	5	4	3	2	1	0

Memory location: 03
Reset state: 1101 0001

SAFETY TIMER, STIM[4:0]

5-bit unsigned binary coding. STIM can only be Written once before the device has entered the flashlight mode.
Timer = STIM x32.8 ms, default is 557.6 ms

GENERAL PURPOSE TIMER, DCTIM[2:0]

If MODE_CTRL = 01 and DIM = 1, DCTIM sets the average LED current

000: 0.8% x ITORCH
001: 1.6% x ITORCH
010: 2.3% x ITORCH
011: 3.1% x ITORCH
100: 3.9% x ITORCH
101: 4.7% x ITORCH
110: 6.3% x ITORCH (default)
111: 8.6% x ITORCH

If MODE_CTRL = 11, DCTIM sets the duration of the timer till TO bit is set

3-bit unsigned binary coding
Timer = DCTIM x 1.02 s

Figure 39. Register3 (Read/Write) (TPS6105X)

8 Application and Implementation

NOTE

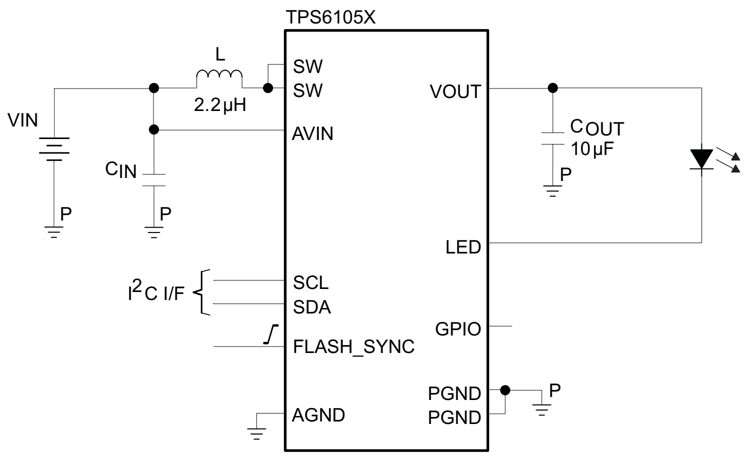
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS6105x device is based on a high-frequency synchronous-boost topology with constant current sink to drive single white LEDs. The TPS6105x device not only operates as a regulated current source but also as a standard voltage-boost regulator. This additional operating mode can be useful to supply other high-power devices in the system, such as a hands-free audio power amplifier, or any other component requiring a supply voltage higher than the battery voltage.

8.2 Typical Applications

8.2.1 Typical Application Schematic



List Of Components:
- L = Wuerth Elektronik WE-PD S Series
- C_{IN} = C_{OUT} = TDK C1605X5R0J106MT

Figure 40. Typical Application Schematic

8.2.1.1 Design Requirements

This example illustrates how to use the TPS6105x to drive high power white LED. Table 3 shows the design parameters and example values.

Table 3. Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUES
Input voltage range	3.3 V to 4.2 V
Output voltage	5 V
Flash current	500 mA

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Inductor Selecton

A boost converter requires two main passive components for storing energy during the conversion. A boost inductor and a storage capacitor at the output are required. The TPS6105x device integrates a current limit protection circuitry. The peak current of the NMOS switch is sensed to limit the maximum current flowing through the switch and the inductor. The typical peak current limit (1000 mA / 1500 mA / 2000 mA) is user selectable through the I^2C interface.

To optimize solution size the TPS6105x device has been designed to operate with inductance values from a minimum of 1.3 µH to a maximum of 2.9 µH. In typical high-current white LED applications, TI recommends an inductance of 2.2 µH.

To select the boost inductor, TI recommends keeping the possible peak inductor current below the current limit threshold of the power switch in the chosen configuration. The highest peak current through the inductor and the power switch depends on the output load, the input and output voltages. Estimation of the maximum average inductor current and the maximum inductor peak current can be done using Equation 1 and Equation 2:

$$I_L \approx I_{OUT} = \frac{V_{OUT}}{\eta \times V_{IN}} \tag{1}$$

$$I_L(PEAK) = \frac{V_{IN} \times D}{2 \times f \times L} + \frac{I_{OUT}}{(1-D) \times \eta} \text{ with } D = \frac{V_{OUT} - V_{IN}}{V_{OUT}} \tag{2}$$

with:

- f = switching frequency (2 MHz)
- L = inductance value (2.2 µH)
- η = estimated efficiency (85%)

For example, for an output current of 500 mA at 5 V, the TPS6105x device must be set for a 1000 mA current limit operation together with an inductor supporting this peak current.

The losses in the inductor caused by magnetic hysteresis losses and copper losses are a major parameter for total circuit efficiency.

Table 4. List of Inductors

MANUFACTURER	SERIES	DIMENSIONS	ILIM SETTINGS
TDK	VLF3010AT	2.6 mm × 2.8 mm × 1 mm maximum height	1000 mA (typical)
TAIYO YUDEN	NR3010	3 mm × 3 mm × 1 mm maximum height	
TDK	VLF3014AT	2.6 mm × 2.8 mm × 1.4 mm maximum height	1500 mA (typical)
COILCRAFT	LPS3015	3 mm × 3 mm × 1.5 mm maximum height	
MURATA	LQH3NP	3 mm × 3 mm × 1.5 mm maximum height	
TOKO	FDSE0312	3 mm × 3 mm × 1.2 mm maximum height	2000 mA (typical)

8.2.1.2.2 Capacitor Selection

8.2.1.2.2.1 Input Capacitor

For good input voltage filtering low ESR ceramic capacitors are recommended. A 10-µF input capacitor is recommended to improve transient behavior of the regulator and EMI behavior of the total power supply circuit. The input capacitor should be placed as close as possible to the input pin of the converter.

8.2.1.2.2.2 Output Capacitor

The primary parameter necessary to define the output capacitor is the maximum allowed output voltage ripple of the converter. This ripple is determined by two parameters of the capacitor, the capacitance and the ESR. It is possible to calculate the minimum capacitance needed for the defined ripple, supposing that the ESR is zero, by using Equation 3:

$$C_{min} \approx \frac{I_{OUT} \times (V_{OUT} - V_{IN})}{f \times \Delta V \times V_{OUT}} \tag{3}$$

Parameter f is the switching frequency and ΔV is the maximum allowed ripple.

With a chosen ripple voltage of 10mV, a minimum capacitance of 10 μF is needed. The total ripple is larger due to the ESR of the output capacitor. This additional component of the ripple can be calculated using Equation 4:

$$\Delta V_{ESR} = I_{OUT} \times R_{ESR} \quad (4)$$

The total ripple is the sum of the ripple caused by the capacitance and the ripple caused by the ESR of the capacitor. Additional ripple is caused by load transients. This means that the output capacitor must completely supply the load during the charging phase of the inductor. A reasonable value of the output capacitance depends on the speed of the load transients and the load current during the load change.

For the high current white LED application, a minimum of 3-μF effective output capacitance is usually required when operating with 2.2-μH (typical) inductors. For solution size reasons, this is usually one or more X5R/X7R ceramic capacitors. For stable operation of the internally compensated control loop, a maximum of 50 μF effective output capacitance is tolerable.

Depending on the material, size and margin to the rated voltage of the used output capacitor, degradation on the effective capacitance can be observed. This loss of capacitance is related to the DC bias voltage applied. It is therefore always recommended to check that the selected capacitors are showing enough effective capacitance under real operating conditions.

8.2.1.2.3 Checking Loop Stability

The first step of circuit and stability evaluation is to look from a steady-state perspective at the following signals:

- Switching node, SW
- Inductor current, I_L
- Output ripple voltage, $V_{OUT(AC)}$

These are the basic signals that must be measured when evaluating a switching converter. When the switching waveform shows large duty cycle jitter or the output voltage or inductor current shows oscillations the regulation loop may be unstable. This is often a result of board layout and/or L-C combination.

The next step in regulation loop evaluation is to perform a load transient test. Output voltage settling time after the load transient event is a good estimate of the control loop bandwidth. The amount of overshoot and subsequent oscillations (ringing) indicates the stability of the control loop. Without any ringing, the loop has usually more than 45° of phase margin.

Because the damping factor of the circuitry is directly related to several resistive parameters (for example, MOSFET $r_{DS(on)}$) that are temperature dependant, the loop stability analysis must be done over the input voltage range, output current range, and temperature range.

8.2.1.3 Application Curves

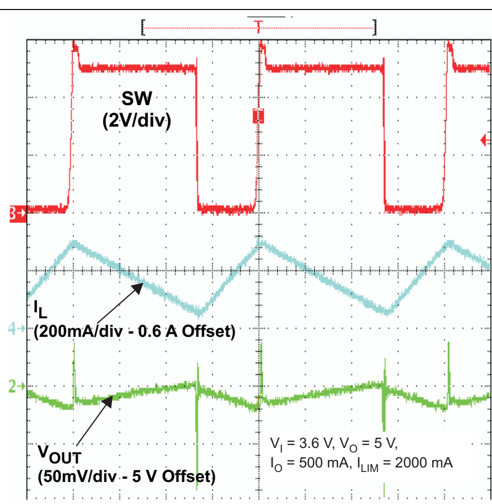


Figure 41. PWM Operation

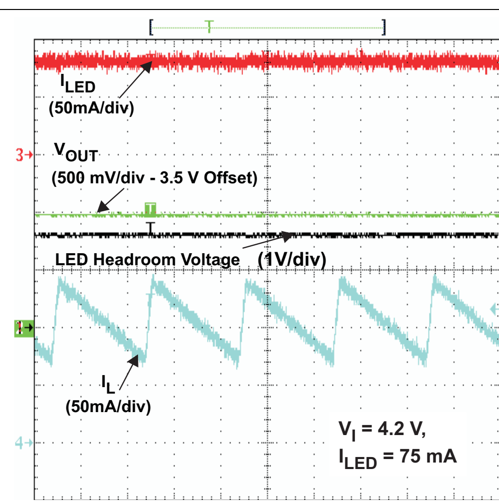


Figure 42. Down-Mode Operation

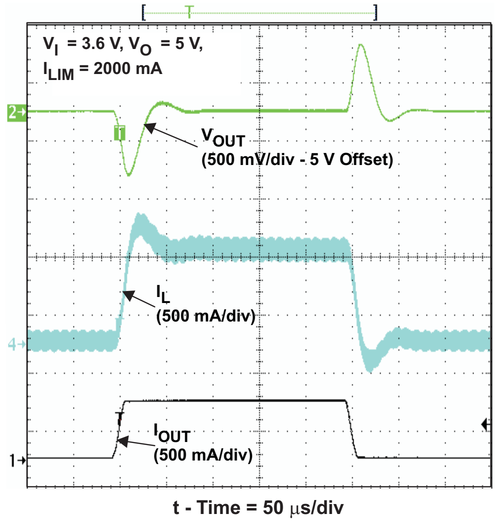


Figure 43. Voltage Mode Load Transient Response

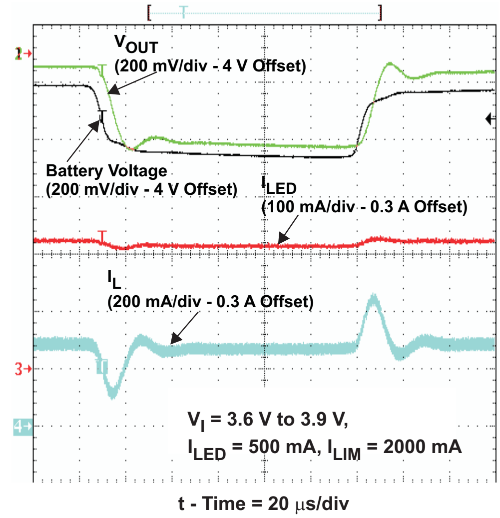


Figure 44. Down-Mode Line Transient Response

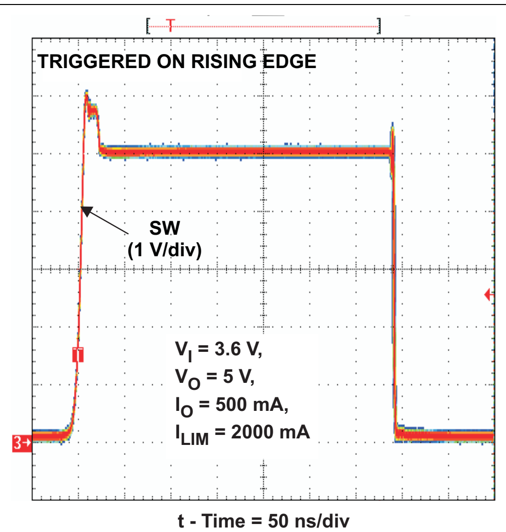


Figure 45. Duty Cycle Jitter

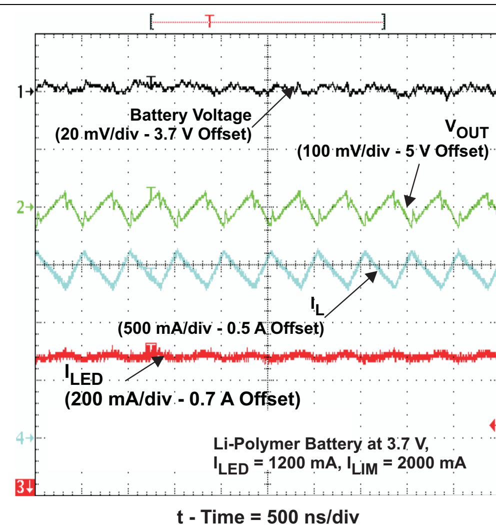


Figure 46. Input Ripple Voltage

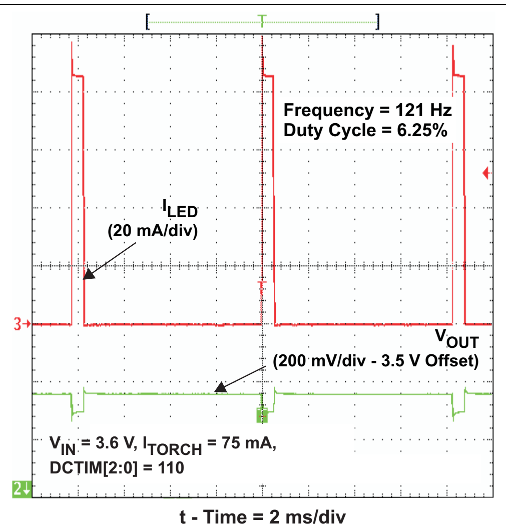


Figure 47. Low-Light Dimming Mode Operation

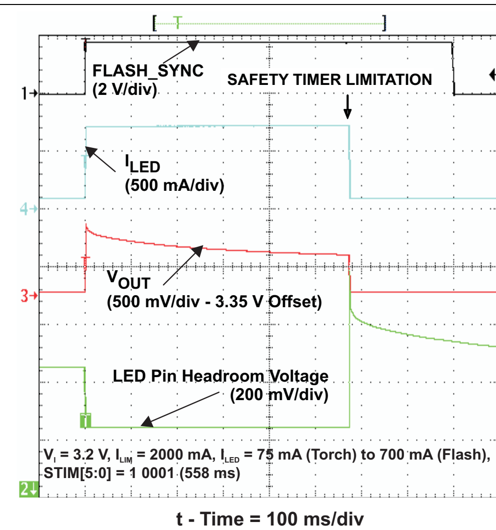


Figure 48. Torch/Flash Sequence

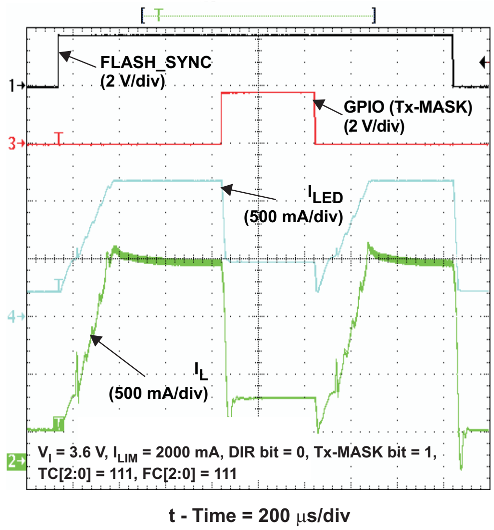


Figure 49. TX-Masking Operation

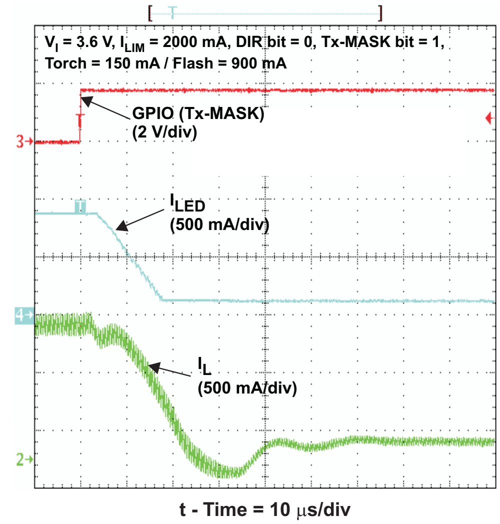


Figure 50. TX-Masking Operation

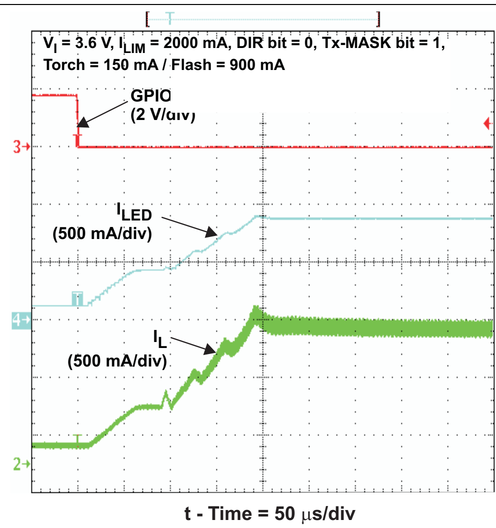


Figure 51. TX-Masking Operation

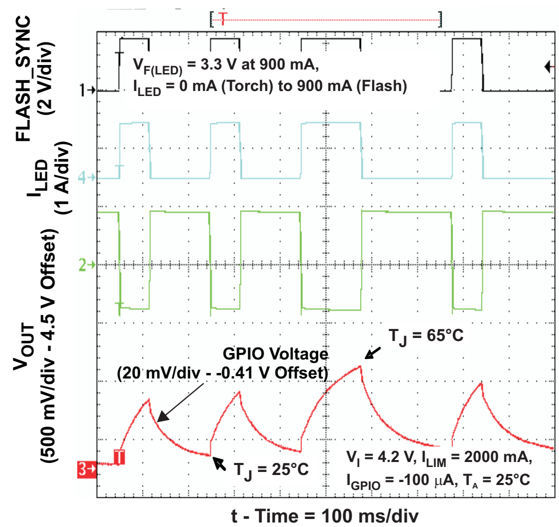


Figure 52. Junction Temperature Monitoring

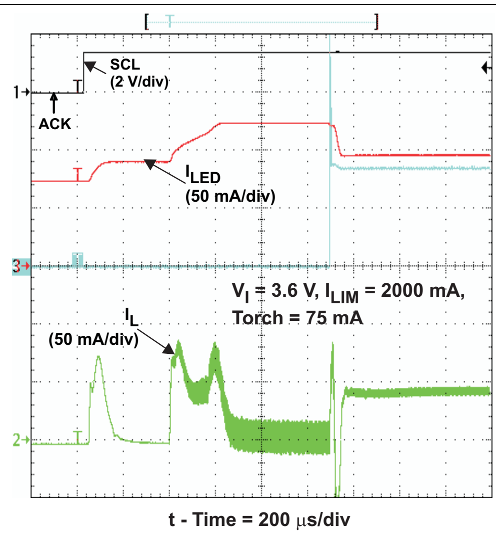


Figure 53. Start-Up in Torch Operation

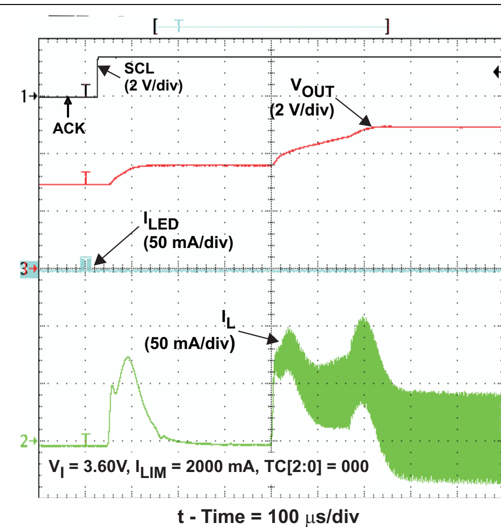


Figure 54. Start-Up in Torch Operation

8.2.2 High-Power White LED Solution Featuring Privacy Indicator

Figure 55 shows the typical application where TPS61050 is used to drive high-power white LED with a privacy indicator feature.

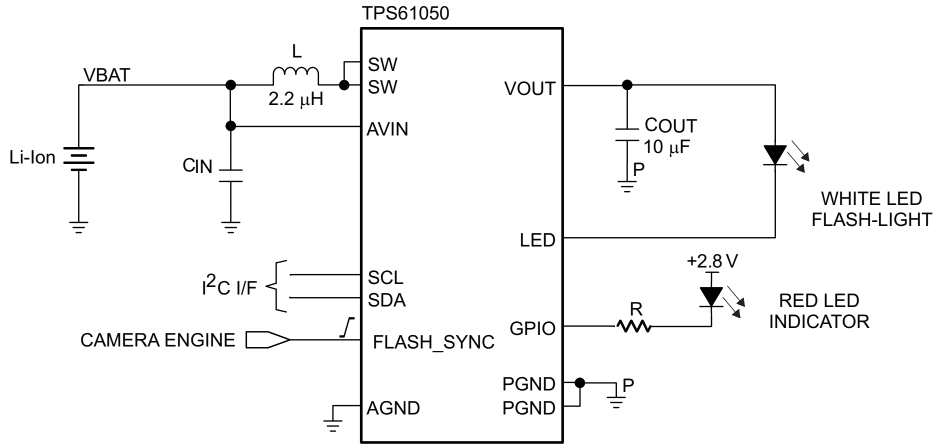


Figure 55. High-Power White LED Solution Featuring Privacy Indicator

8.2.3 High-Power White LED Solution Featuring No-Latency Turn-Down Through PA TX Signal

Figure 56 shows the typical application where TPS61050 is used to drive high-power white LED, and the RF PA TX signal is used to realize the no-latency turn down function.

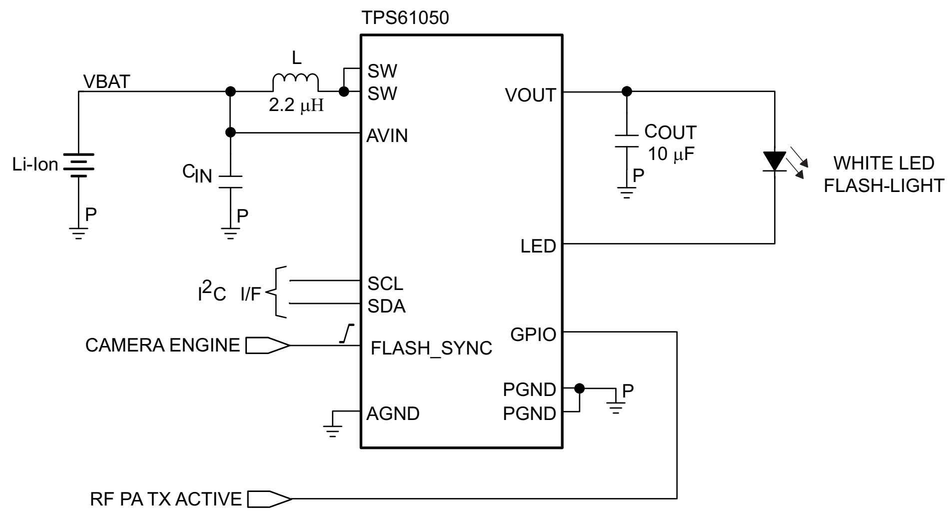


Figure 56. High-Power White LED Solution Featuring No-Latency Turn-Down Through PA TX Signal

8.2.4 High-Power White LED Flash Driver And AF/Zoom Motor Drive Supply

Figure 57 shows the typical application where TPS61052 is used as high-power white LED flash driver and meantime to provide the power supply to the AF/Zoom motor driver.

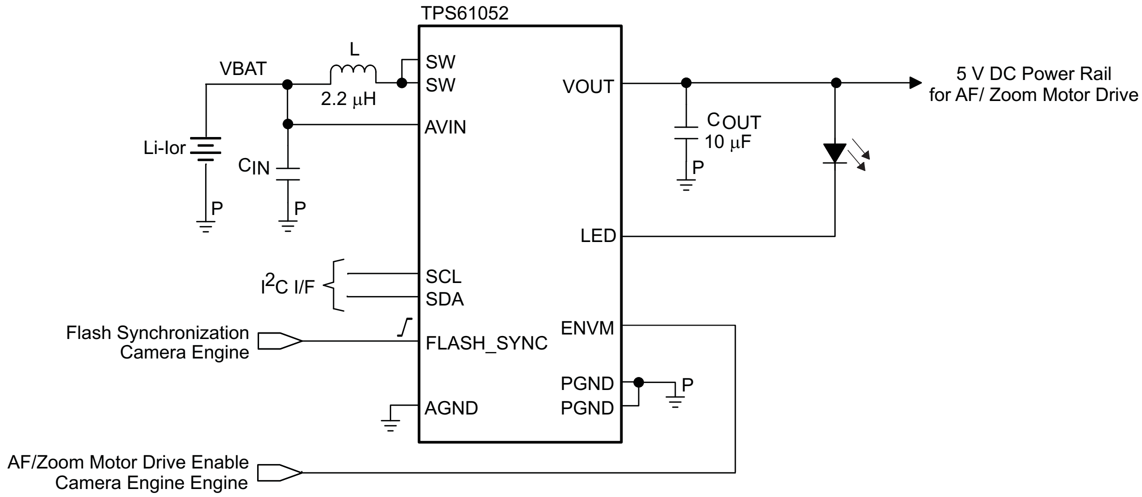


Figure 57. High-Power White LED Flash Driver And AF/Zoom Motor Drive Supply

8.2.5 White LED Flash Driver and Audio Amplifier Power Supply Exclusive Operation

Figure 58 shows the typical application where TPS61052 is used as white LED flash driver and it can also be used to provide the power supply to the audio amplifier exclusively by using a logic gate 1G97.

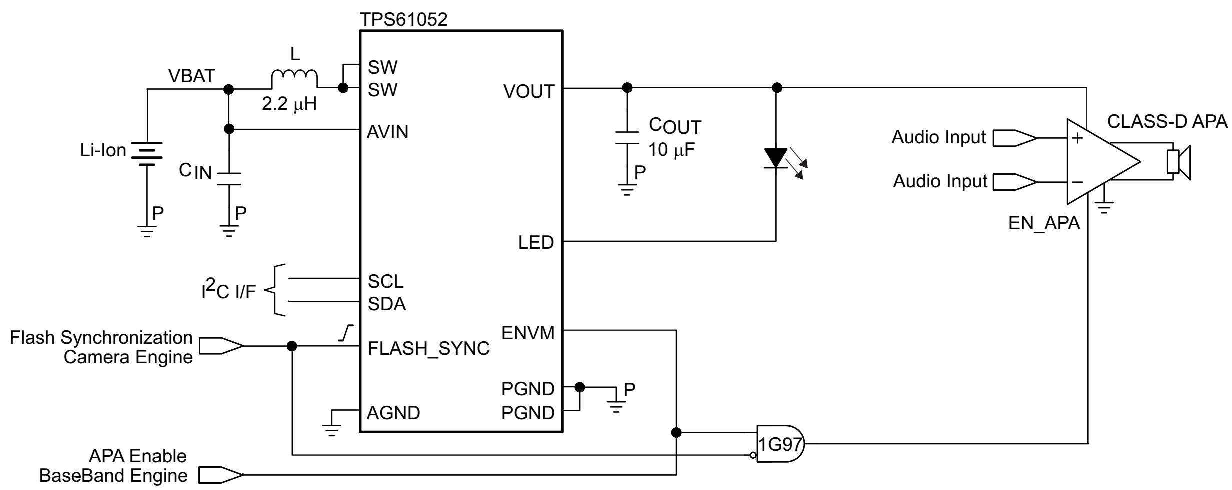


Figure 58. White LED Flash Driver and Audio Amplifier Power Supply Exclusive Operation

8.2.6 White LED Flash Driver and Audio Amplifier Power Supply Operating Simultaneously

Figure 59 shows the typical application where TPS61052 is used as white LED flash driver and meantime to provide the power supply to the audio amplifier simultaneously.

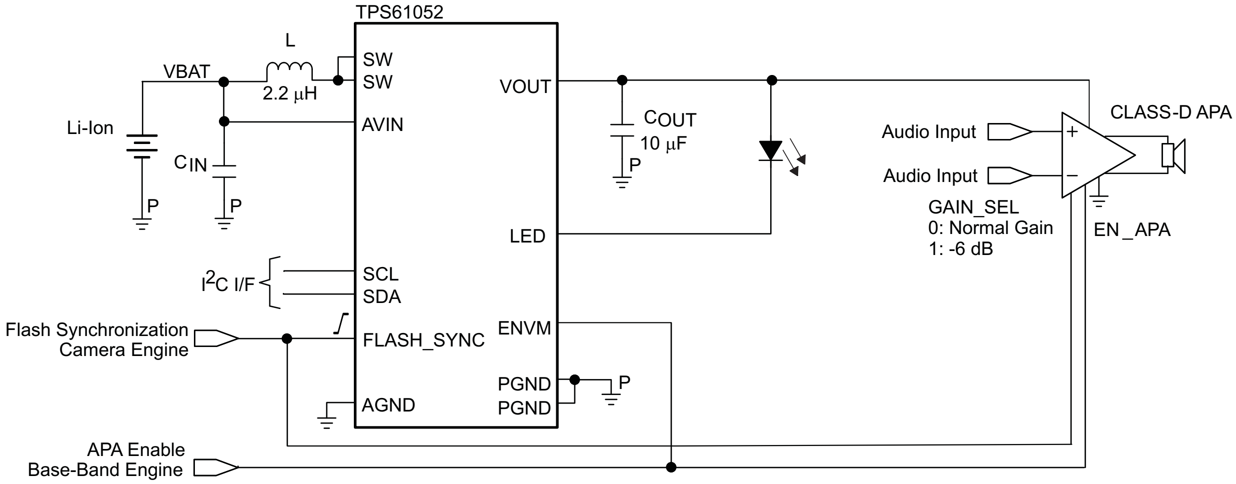


Figure 59. White LED Flash Driver and Audio Amplifier Power Supply Operating Simultaneously

8.2.7 White LED Flash Driver and Auxiliary Lighting Zone Power Supply

Figure 60 shows the typical application where TPS61052 is used as white LED flash driver and meantime to provide the supply to the auxiliary lighting zone (TCA6507 in this example).

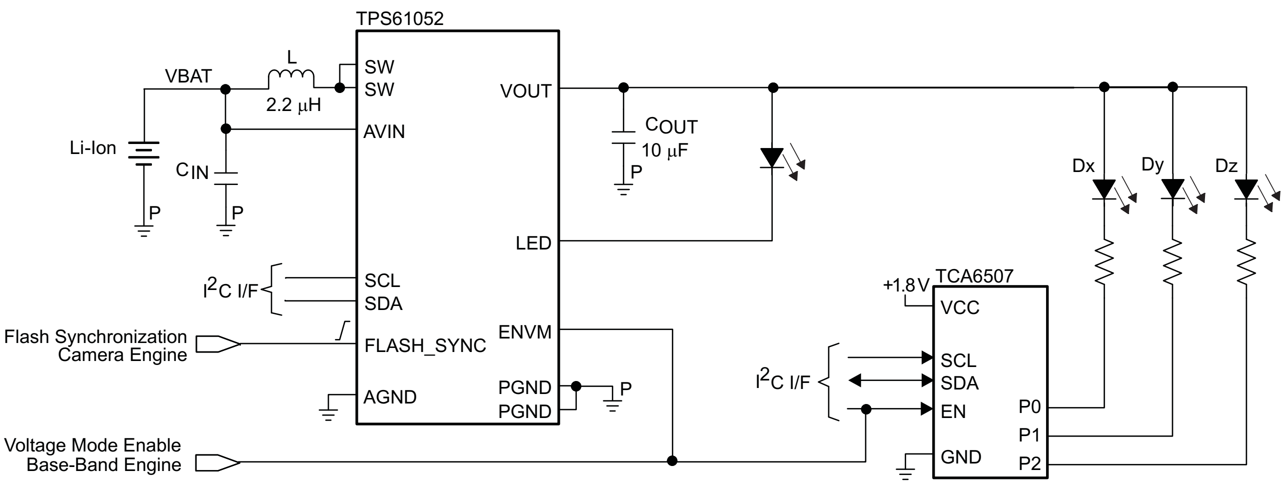


Figure 60. White LED Flash Driver and Auxiliary Lighting Zone Power Supply

8.2.8 2 × 300 mA Dual LED Camera Flash

Figure 61 shows the typical application where TPS61050 is used to drive dual LED camera flash (2 × 300 mA).

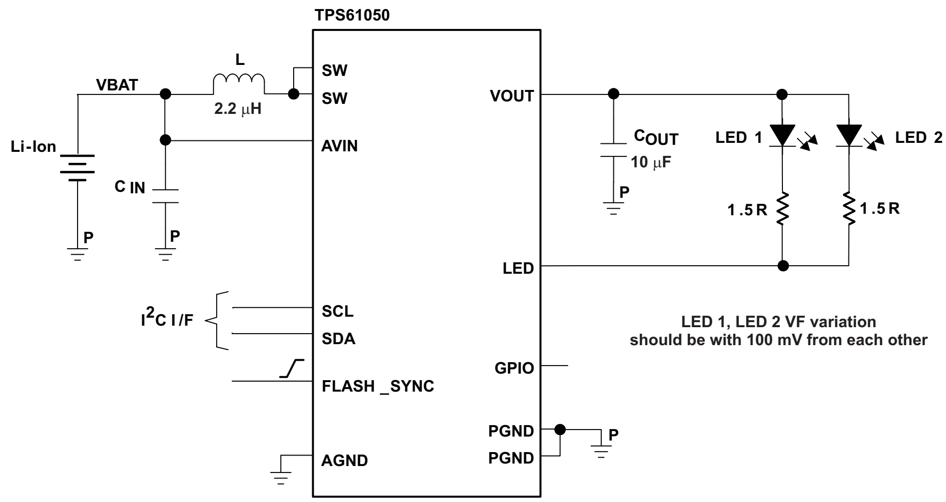


Figure 61. 2 × 300 mA Dual LED Camera Flash

9 Power Supply Recommendations

The device is designed to operate from an input voltage supply range from 2.5 V to 6 V. This input supply must be well regulated. If the input supply is located more than a few inches from the converter, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. A typical choice is an electrolytic or tantalum capacitor with a value of 47 µF.

10 Layout

10.1 Layout Guidelines

As for all switching power supplies, the layout is an important step in the design, especially at high peak currents and high switching frequencies. If the layout is not carefully done, the regulator could show stability problems as well as EMI problems. Therefore, use wide and short traces for the main current path and for the power ground tracks.

The input capacitor, output capacitor, and the inductor should be placed as close as possible to the IC. Use a common ground node for power ground and a different one for control ground to minimize the effects of ground noise. Connect these ground nodes at any place close to one of the ground pins of the IC.

To lay out the control ground, TI recommends using short traces as well, separated from the power ground traces. This avoids ground shift problems, which can occur due to superimposition of power ground current and control ground current.

10.2 Layout Example

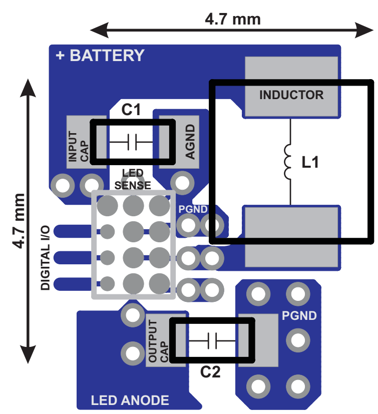


Figure 62. Typical PC-Board Layout

10.3 Thermal Considerations

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependant issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

Use the following three basic approaches for enhancing thermal performance:

- Improving the power dissipation capability of the PCB design
- Improving the thermal coupling of the component to the PCB
- Introducing airflow in the system

Junction-to-ambient thermal resistance is highly application and board-layout dependent. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues in board design. The maximum junction temperature (T_J) of the TPS6105x is 150°C.

Thermal Considerations (continued)

The maximum power dissipation gets especially critical when the device operates in the linear down mode at high LED current. For single pulse power thermal analysis (for example, flash strobe), the allowable power dissipation for the device is given by Figure 63.

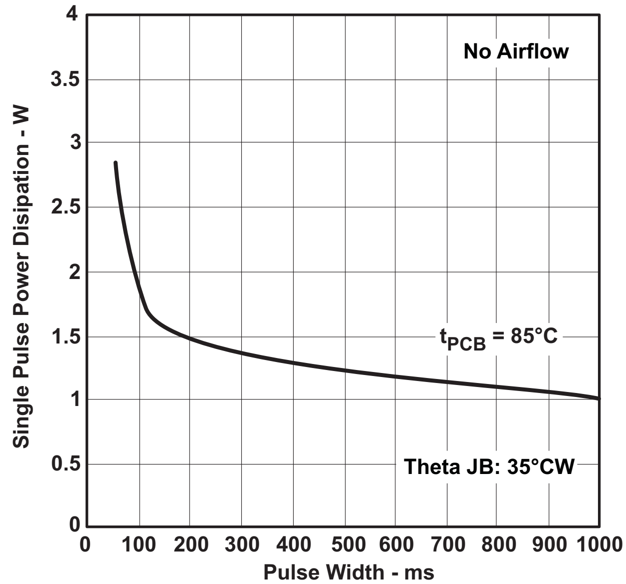


Figure 63. Single Pulse Power Capability (CSP Package)

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.2 Related Links

The following table lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 5. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS61050	Click here	Click here	Click here	Click here	Click here
TPS61052	Click here	Click here	Click here	Click here	Click here

11.3 Trademarks

NanoFree, PowerPAD are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.
This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

12.1 Package Summary

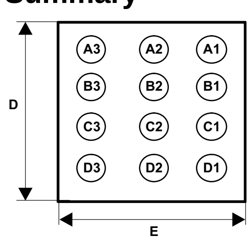

Figure 64. Chip Scale Package (Bottom View)

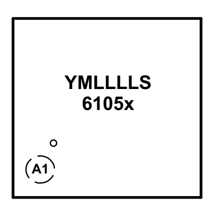

Figure 65. Chip Scale Package (Top View)

Code:

- Y — 2 digit date code
- LLLL - lot trace code
- S - assembly site code

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS61050DRCR	ACTIVE	VSON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BRV	Samples
TPS61050DRCT	ACTIVE	VSON	DRC	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BRV	Samples
TPS61050YZGR	ACTIVE	DSBGA	YZG	12	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	TPS61050	Samples
TPS61050YZGT	ACTIVE	DSBGA	YZG	12	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	TPS61050	Samples
TPS61052DRCR	ACTIVE	VSON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BRW	Samples
TPS61052DRCT	ACTIVE	VSON	DRC	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BRW	Samples
TPS61052YZGR	ACTIVE	DSBGA	YZG	12	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	TPS61052	Samples
TPS61052YZGT	ACTIVE	DSBGA	YZG	12	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	TPS61052	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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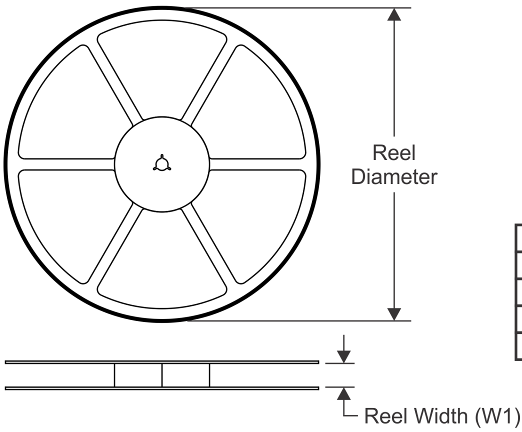
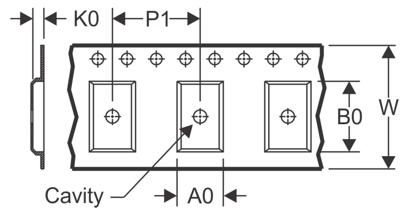
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

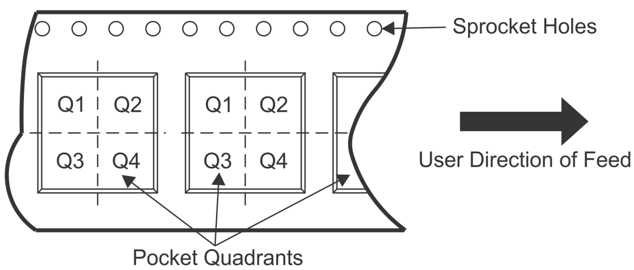


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

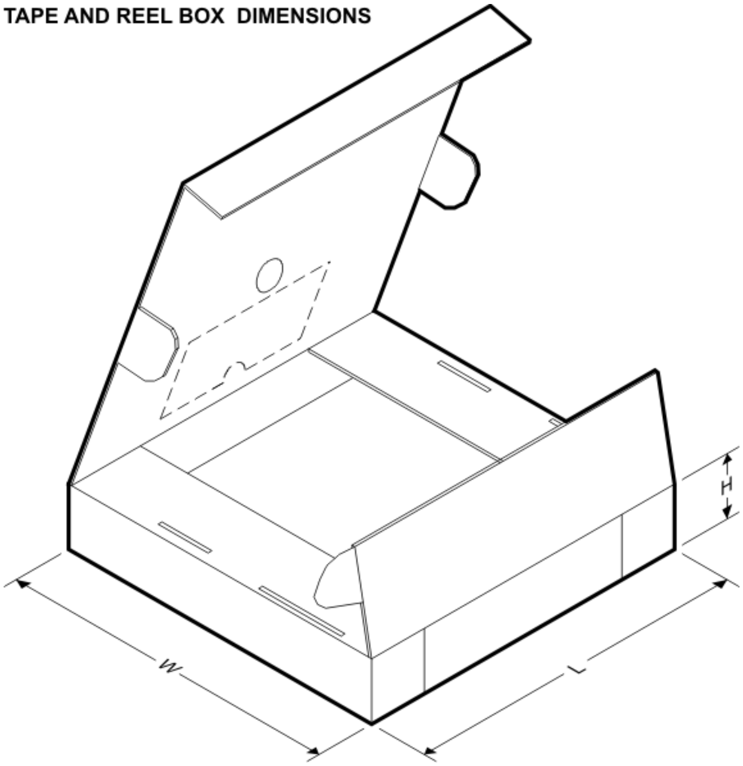
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS61050DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS61050DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS61050DRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS61050DRCT	VSON	DRC	10	250	180.0	12.5	3.3	3.3	1.1	8.0	12.0	Q2
TPS61050YZGR	DSBGA	YZG	12	3000	180.0	8.4	1.75	2.25	0.81	4.0	8.0	Q1
TPS61050YZGT	DSBGA	YZG	12	250	180.0	8.4	1.75	2.25	0.81	4.0	8.0	Q1
TPS61052DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS61052DRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS61052YZGR	DSBGA	YZG	12	3000	180.0	8.4	1.75	2.25	0.81	4.0	8.0	Q1
TPS61052YZGT	DSBGA	YZG	12	250	180.0	8.4	1.75	2.25	0.81	4.0	8.0	Q1

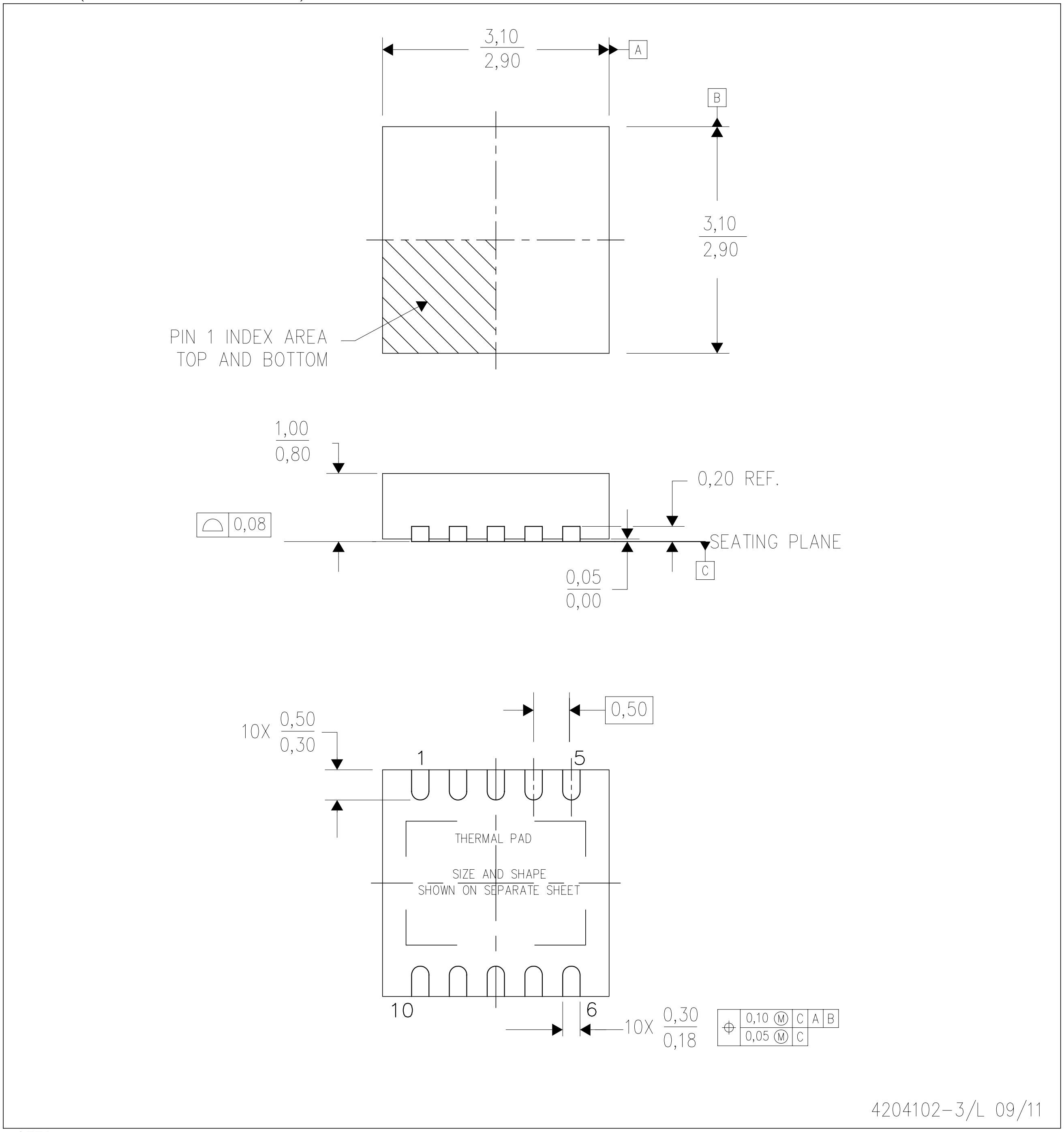
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS61050DRCR	VSON	DRC	10	3000	338.0	355.0	50.0
TPS61050DRCR	VSON	DRC	10	3000	367.0	367.0	35.0
TPS61050DRCT	VSON	DRC	10	250	210.0	185.0	35.0
TPS61050DRCT	VSON	DRC	10	250	338.0	355.0	50.0
TPS61050YZGR	DSBGA	YZG	12	3000	182.0	182.0	20.0
TPS61050YZGT	DSBGA	YZG	12	250	182.0	182.0	20.0
TPS61052DRCR	VSON	DRC	10	3000	367.0	367.0	35.0
TPS61052DRCT	VSON	DRC	10	250	210.0	185.0	35.0
TPS61052YZGR	DSBGA	YZG	12	3000	182.0	182.0	20.0
TPS61052YZGT	DSBGA	YZG	12	250	182.0	182.0	20.0

DRC (S–PVSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance, if present.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions, if present

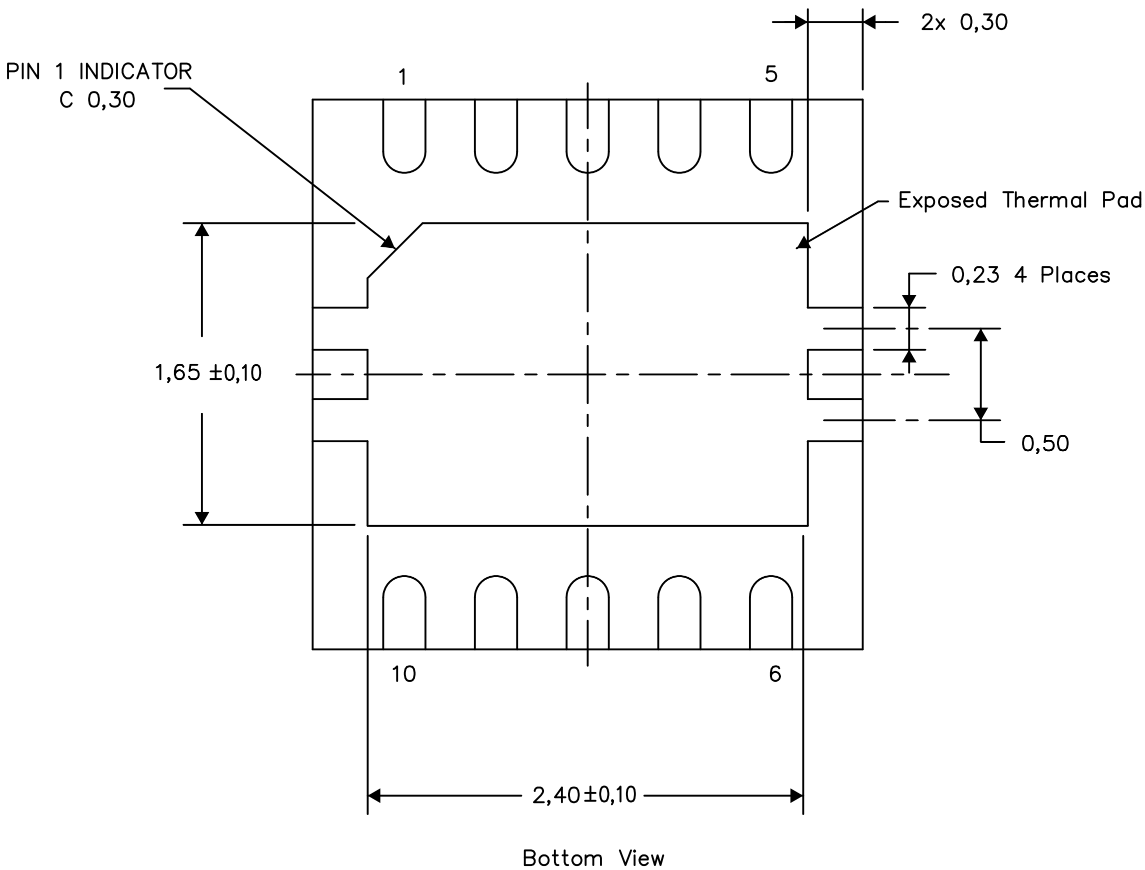
DRC (S-PVSON-N10) PLASTIC SMALL OUTLINE NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

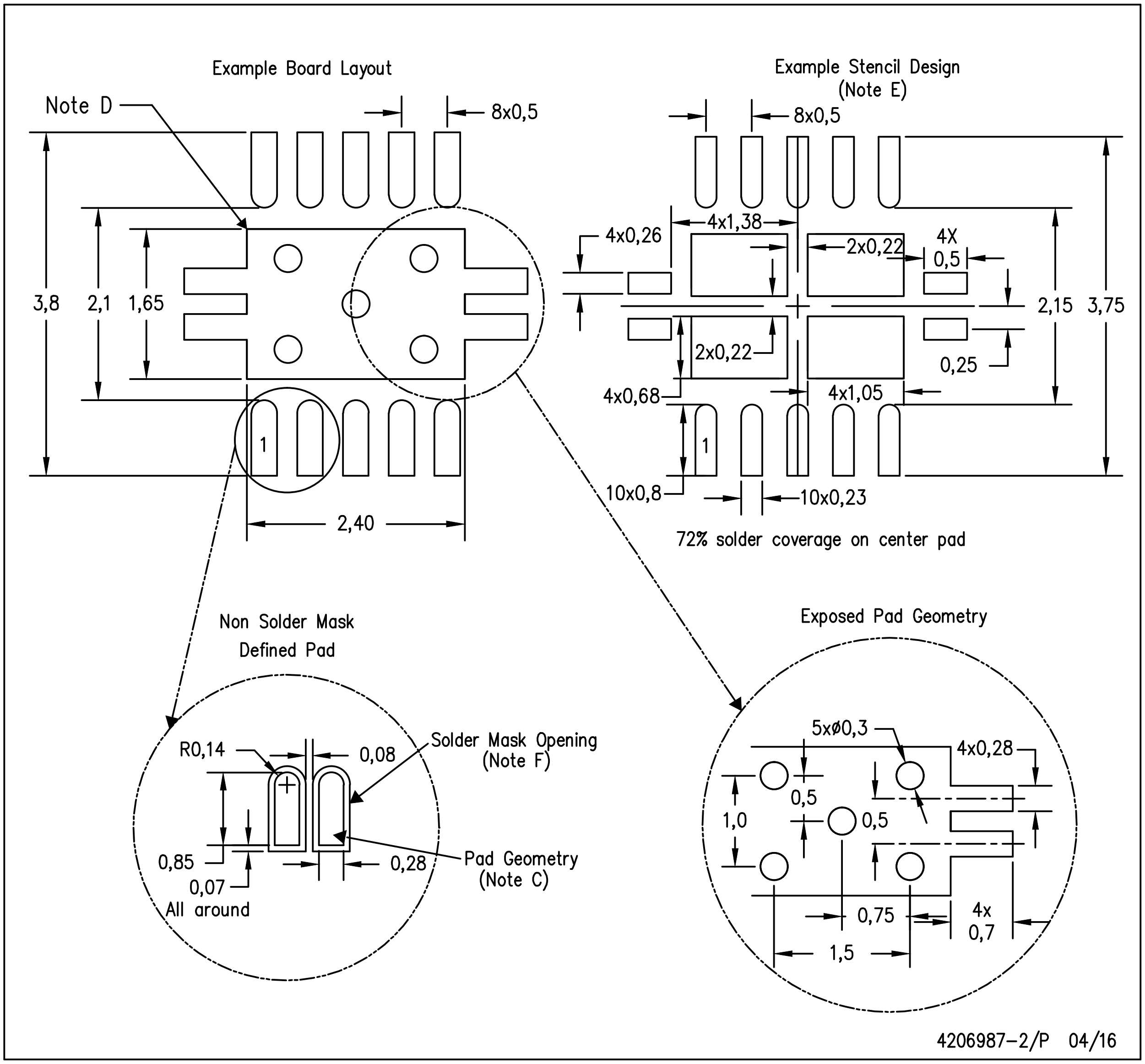


Exposed Thermal Pad Dimensions

4206565-3/Y 08/15

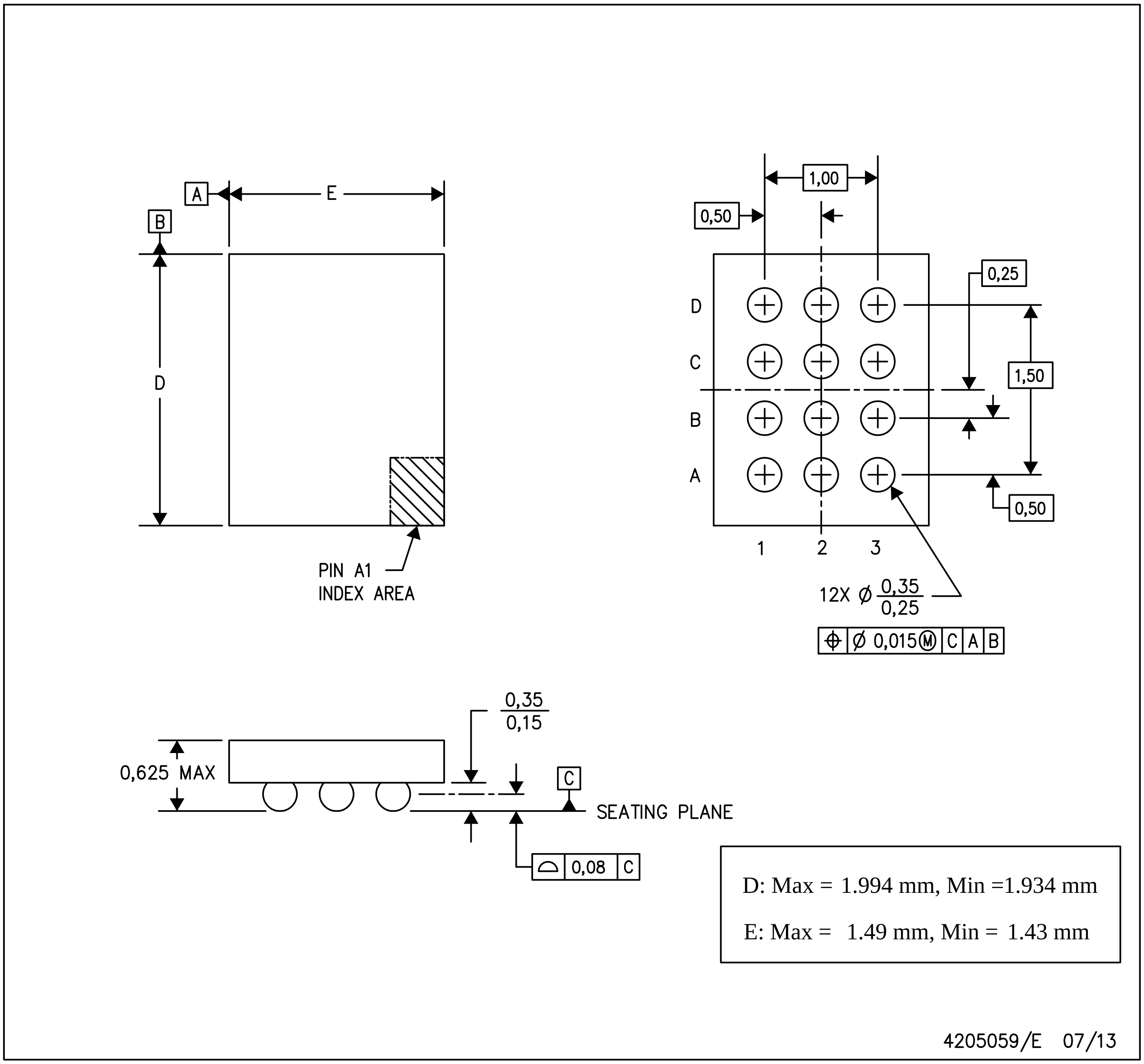
NOTE: A. All linear dimensions are in millimeters

DRC (S-PVSON-N10) PLASTIC SMALL OUTLINE NO-LEAD



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

YZG (R–XBGA–N12) DIE–SIZE BALL GRID ARRAY



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.

NanoFree is a trademark of Texas Instruments.

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