TPS61158 30-V WLED Driver with Integrated Power Diode

1 Features

- 2.7-V to 5.5-V Input Voltage Range
- 28-V Open LED Protection (up to 8 LEDs)
- Integrated 0.6-A, 30-V Internal Switch FET and Power Diode
- 750-kHz Switching Frequency
- Flexible Digital and PWM Brightness Control
  - 1-Wire Control Interface (EasyScale™)
  - PWM Dimming Control Interface
- Up to 100:1 PWM Dimming Ratio
- Integrated Loop Compensation
- Built-in Soft Start
- Built-in WLED Open protection
- Thermal Shutdown

2 Applications

- Feature Phones
- Smart Phones
- Portable Media Players
- Ultra Mobile Devices
- GPS Receivers
- Backlight for Small and Media Form Factor LCD Displays

3 Description

With a 30V-rated integrated switch FET and power diode, the TPS61158 is a boost converter that drives LEDs in series. The boost converter runs at 750-kHz fixed switching frequency to reduce output ripple, improve conversion efficiency, and allows for the use of small external components.

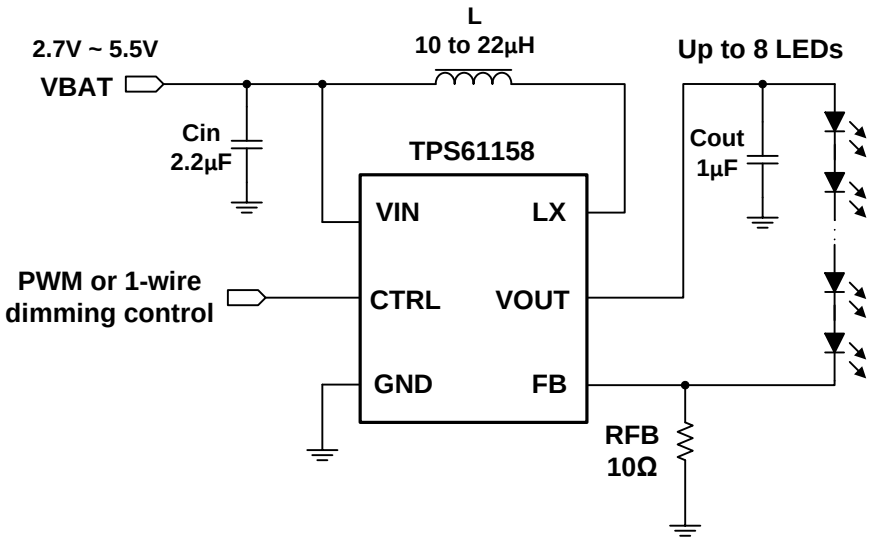
The default white LED current is set with the external sensor resistor RFB, and the feedback voltage is regulated to 200 mV, as shown in *Typical Application*. During the operation, the LED current can be controlled using the 1-wire digital interface (EasyScale™ protocol) through the CTRL pin. Alternatively, a pulse width modulation (PWM) signal can be applied to the CTRL pin through which the duty cycle determines the feedback reference voltage. In either digital or PWM mode, the TPS61158 does not burst the LED current; therefore, it does not generate audible noises on the output capacitor. For maximum protection, the device features integrated open LED protection that disables the TPS61158 to prevent the output voltage from exceeding the device absolute maximum voltage ratings during open LED conditions.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS61158	WSON (6)	2.00 mm x 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application



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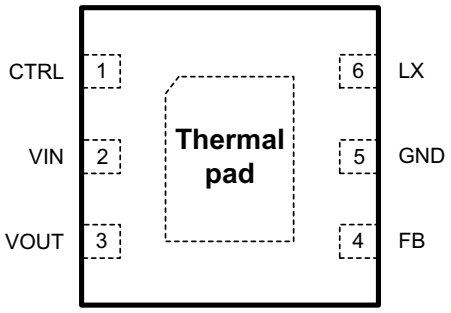
4 Revision History

Changes from Original (May 2013) to Revision A **Page**

- Added *Pin Configuration and Functions* section, *ESD Rating* table, *Feature Description*, *Device Functional Modes*, *Application and Implementation*, *Power Supply Recommendations*, *Layout*, *Device and Documentation Support* , and *Mechanical, Packaging, and Orderable Information* sections ... 1

5 Pin Configuration and Functions

DRV Package
6-Pin WSON
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	CTRL	I	Control pin of the boost converter. It is a multi-functional pin which can be used for enable control, PWM and digital dimming.
2	VIN	I	The input supply pin for the device. Connect VIN to a supply voltage between 2.7 V and 5.5 V.
3	VOUT	O	Output of the boost converter.
4	FB	I	Feedback pin for current. Connect the sense resistor from FB to GND.
5	GND	O	Ground
6	LX	I	This is the switching node of the device. Connect the inductor between the VIN and LX pin.
7	Thermal Pad		The thermal pad should be soldered to the analog ground plane. If possible, use thermal via to connect to ground plane for ideal power dissipation.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage range(2)	VIN	–0.3	6	V
	VOUT, LX	–0.3	30	V
	FB, CTRL	–0.3	7	V
Continuous power dissipation				
Operating junction temperature		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	2.7		5.5	V
V_{OUT}	Output voltage	V_{IN}		29	V
I_{OUT}	Output load current			30	mA
L	Inductor	10		22	µH
C_I	Input capacitor	1		10	µF
C_O	Output capacitor	0.47		2.2	µF
F_{PWM}	Input PWM signal frequency	20		100	kHz
T_A	Operating ambient temperature	–40		85	°C
T_J	Operating junction temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		TPS61158 DRV (WSON) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	70.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	94.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	39.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	40.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	10.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

V_{IN} = 3.6 V, CTRL = High, IFB current = 20 mA, IFB voltage = 200 mV, T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
V_{IN}	Input voltage range		2.7		5.5	V
V_{IN_UVLO}	V_{IN} undervoltage lockout threshold	V_{IN} ramp down		2.2	2.35	V
		V_{IN} ramp up		2.5	2.65	
V_{IN_HYS}	V_{IN} undervoltage lockout hysteresis			275		mV
I_Q	Operating quiescent current into VIN	Device enable, no switching and no load (V_{FB} = 0.4 V)		0.3	0.5	mA
		Device enable, switching 750 kHz and no load (V_{FB} = 0 V)		0.5	1.65	
I_{SD}	Shutdown current	CTRL = GND		0.1	1	µA
CONTROL LOGIC AND TIMING						
V_H	CTRL logic high voltage		1.2			V
V_L	CTRL logic Low voltage				0.4	V
R_{PD}	CTRL pin internal pull-down resistor	V_{CTRL} = 1.8 V		300		kΩ
t_{SD}	CTRL pulse width to shutdown	CTRL from high to low	3.5			ms
VOLTAGE AND CURRENT REGULATION						
V_{REF}	Voltage feedback regulation voltage	Duty = 100%	194	200	206	mV
I_{FB}	FB pin bias current	V_{FB} = 200 mV			2	µA
t_{REF}	V_{REF} filter time constant			230		µs
POWER SWITCH AND DIODE						
$R_{DS(ON)}$	N-channel MOSFET on-resistance	V_{IN} = 3.6 V, T_A = 25°C, I_{OUT} = 100 mA		0.6	1	Ω
V_F	Power diode forward voltage	I_{DIODE} = 0.2 A		0.75	1	V
I_{LEAK_LX}	LX pin leakage current	V_{LX} = 28 V		0.1	2	µA
OSCILLATOR						
f_{SW}	Oscillator frequency		600	750	900	kHz
D_{max}	Maximum duty cycle of boost switching	V_{FB} = 0 V, measured on the drive signal of the switch MOSFET	88%	94%		
PROTECTION AND SOFT START						
I_{LIM}	NMOS current limit	V_{IN} = 3.6 V, D = D_{MAX} T_A = 0°C to 85°C	0.5	0.6	0.7	A
I_{LIM_Start}	Start up current limit			360		mA
t_{ILIM_Start}	Time step for start up current limit			8		ms
V_{OVP}	Open LED protection threshold	Tested at VOUT pin	27.5	28.2	29	V
V_{ACKNL}	Acknowledge output voltage low	Open drain, R_{pullup} = 15 kΩ to V_{IN}			0.4	V
THERMAL SHUTDOWN						
$T_{shutdown}$	Thermal shutdown threshold			160		°C
T_{hys}	Thermal shutdown hysteresis			15		°C

6.6 EasyScale Timing Requirements

		MIN	NOM	MAX	UNIT
t_{es_detect}	EasyScale detection time(1), CTRL low	450			µs
t_{es_delay}	EasyScale detection delay	100			µs
t_{es_win}	EasyScale detection window time, measured from CTRL high	3.5			ms
t_{start}	Start time of program stream	3.5			µs
t_{EOS}	End time of program stream	3.5		600	µs
t_{H_LB}	High time of low bit, Logic 0	3.5		300	µs
t_{L_LB}	Low time of low bit, Logic 0	2 × t_{H_LB}		600	µs
t_{H_HB}	High time of high bit, Logic 1	2 × t_{L_HB}		600	µs
t_{L_HB}	Low time of high bit, Logic 1	3.5		300	µs
t_{valACK}	Acknowledge valid time (see(2))			3.5	µs
t_{ACKN}	Duration of acknowledge condition (see(2))			900	µs

(1) To select EasyScale mode, the CTRL pin has to be low for more than t_{es_detect} during t_{es_win}
(2) Acknowledge condition active 0, this condition will only be applied in case the RFA bit is set. Open drain output, line needs to be pulled high by the host with resistor load.

6.7 Typical Characteristics

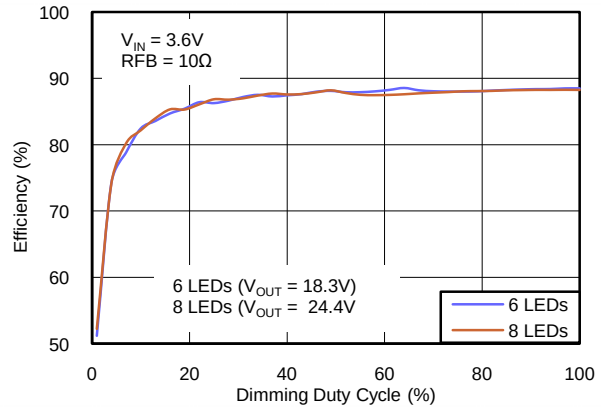


Figure 1. Efficiency vs Dimming Duty Cycle

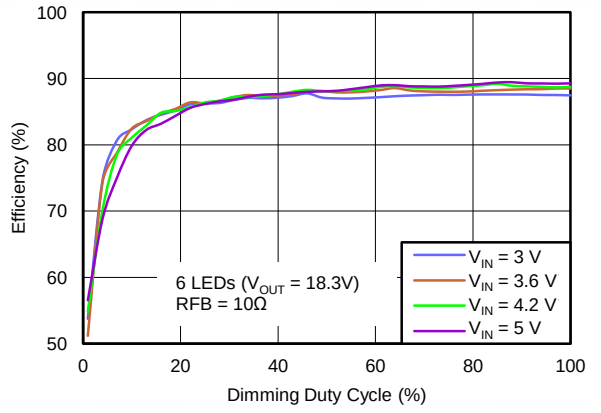


Figure 2. Efficiency vs Dimming Duty Cycle

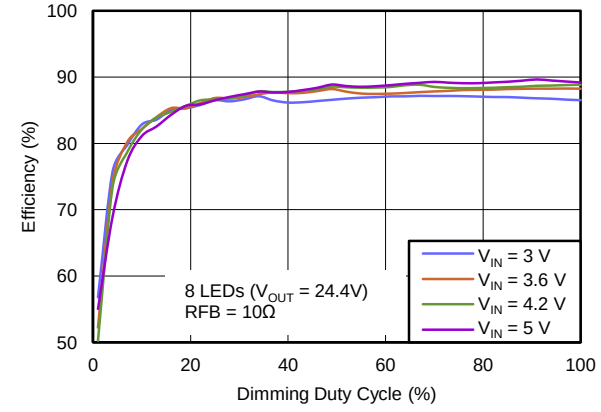


Figure 3. Efficiency vs Dimming Duty Cycle

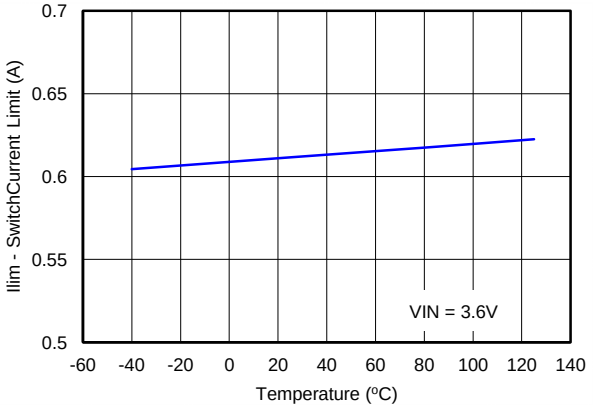


Figure 4. Switch Current Limit vs Duty Cycle

Typical Characteristics (continued)

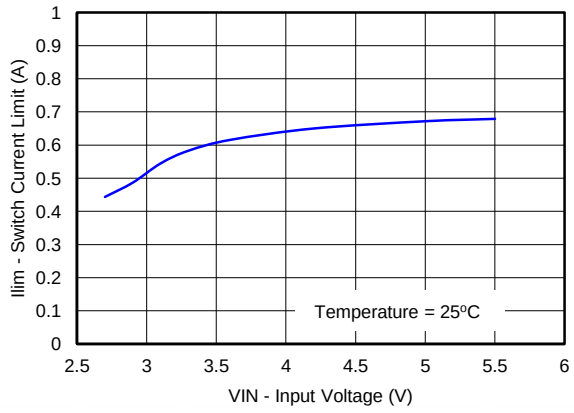


Figure 5. Switch Current Limit vs Temperature

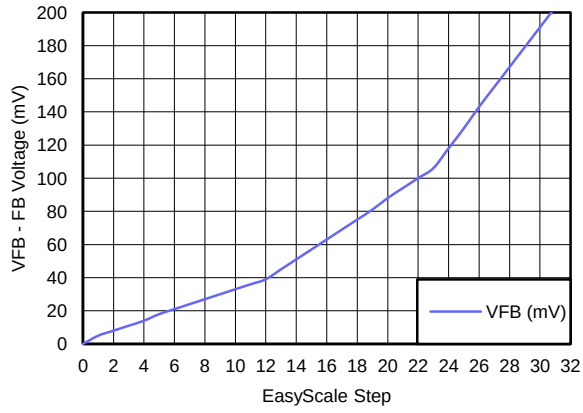


Figure 6. FB Voltage vs EasyScale Step

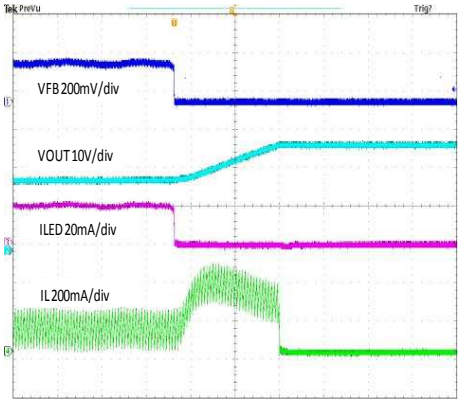


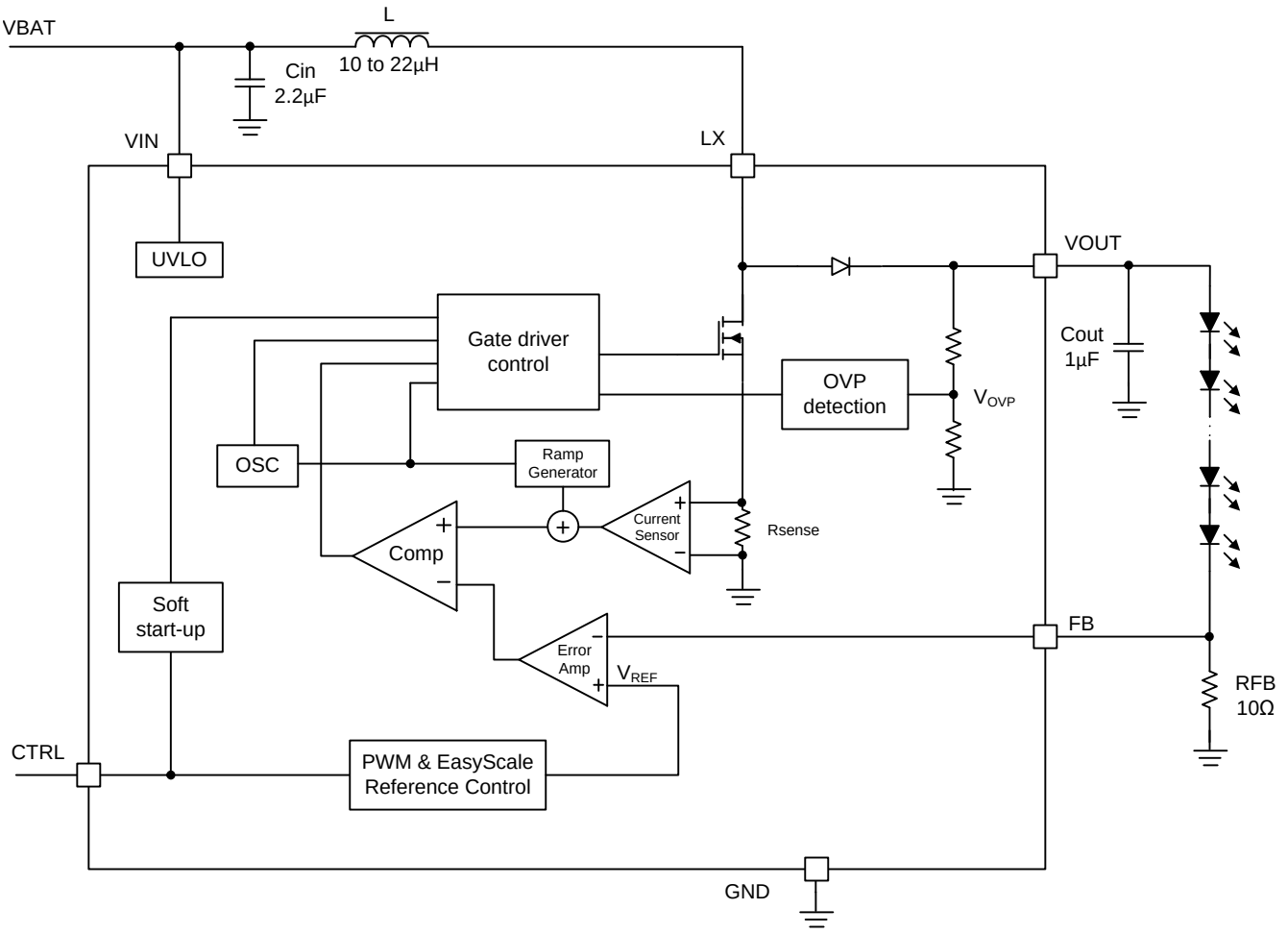
Figure 7. Open LED Protection

7 Detailed Description

7.1 Overview

The TPS61158 is a high efficiency boost converter with integrated power diode in a small package size. The device is ideal for driving white LED in series. The serial LED connection provides even illumination by sourcing the same output current through all LEDs, eliminating the need for expensive factory calibration. The device integrates a 30-V, 0.6-A low-side switch MOSFET and a 30-V power diode, and operates in pulse width modulation (PWM) with 750-kHz fixed switching frequency. For operation see the block diagram. The duty cycle of the converter is set by the error amplifier output and the current signal applied to the PWM control comparator. The control architecture is based on traditional current-mode control; therefore, slope compensation is added to the current signal to allow stable operation for duty cycles larger than 50%. The feedback loop regulates the FB pin to a low reference voltage (200 mV typical), reducing the power dissipation in the current sense resistor.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Soft Start-Up

Soft-start circuitry is integrated into the device to avoid a high inrush current during start-up. After the device is enabled, the voltage at FB pin ramps up to the reference voltage in 32 steps with each step taking 341 µs. This ensures that the output voltage rises slowly to reduce the input current. Additionally, during the start up process, the current limit of the switch is set to half of the normal current limit specification. During this period, the input current is kept below 360 mA (typical). See the start-up waveform of a typical example.

Feature Description (continued)

7.3.2 Shutdown

The TPS61158 enters shutdown mode when the CTRL voltage is logic low for more than 3.5 ms. During shutdown, the input supply current for the device is less than 1 µA (maximum). Although the internal FET does not switch in shutdown mode, there is still a DC current path between the input and the LEDs through the inductor and the power diode. The minimum forward voltage of the LED array must exceed the maximum input voltage to ensure that the LEDs remain off in shutdown. In the typical application with two or more LEDs, the forward voltage is large enough to reverse bias the diode and keep leakage current low.

7.3.3 Current Program

The FB voltage is regulated by a low 0.2-V reference voltage. The LED current is programmed externally using a current-sense resistor RFB in series with the LED string. The value of the RFB is calculated using Equation 1:

$$R_{FB} = \frac{V_{FB}}{I_{LED}}$$

where

- R_{FB} = current sense resistor at FB pin
- V_{FB} = 200 mV (regulated voltage of FB pin)
- I_{LED} = full-scale output current of LEDs
- The output current tolerance depends on the FB voltage accuracy and the current sensor resistor accuracy. (1)

7.3.4 Undervoltage Lockout

An undervoltage lockout prevents operation of the device at input voltages below typical 2.2 V. When the input voltage is below the undervoltage threshold, the device is shut down, and the internal switch FET is turned off. If the input voltage rises by undervoltage lockout hysteresis, the device restarts.

7.3.5 Open LED Protection

Open LED protection circuitry prevents device damage as the result of white LED disconnection. The TPS61158 monitors the voltages at the VOUT pin and FB pin. The circuitry turns off the switch FET and shuts down the device completely if both of the following two conditions are met: 1) the VOUT voltage reaches OVP threshold (28.2 V typical); and 2) FB voltage is lower than half of its regulation voltage. This means the LED string is open or the FB pin is short to ground. As a result, the output voltage falls to the level of the input supply. The device remains in shutdown mode until it is enabled by pulling down the CTRL pin logic low for at least 3.5 ms and then pulling it high.

7.3.6 Thermal Shutdown

An internal thermal shutdown turns off the device when the typical junction temperature of 160°C is exceeded. The device is released from shutdown automatically when the junction temperature decreases by 15°C.

7.4 Device Functional Modes

7.4.1 LED Brightness Dimming Mode Selection

The CTRL pin is used for the control input for both dimming modes, PWM dimming and 1 wire dimming. The dimming mode for the TPS61158 is selected each time the device is enabled. The default dimming mode is PWM dimming. To enter the 1 wire mode, the following digital pattern on the CTRL pin must be recognized by the device every time the device starts from the shutdown mode.

1. Pull CTRL pin high to enable the TPS61158 and to start the 1-wire detection window.
2. After the EasyScale detection delay (t_{es_delay}, 100 µs) expires, drive CTRL low for more than the EasyScale detection time (t_{es_detect}, 450 µs).
3. The CTRL pin has to be low for more than EasyScale detection time before the EasyScale detection window (t_{es_win}, 3.5 ms) expires. EasyScale detection window starts from the first CTRL pin low-to-high transition.

Device Functional Modes (continued)

The device immediately enters the 1 wire mode once the above 3 conditions are met. The EasyScale communication can start before the detection window expires. Once the dimming mode is programmed, it can not be changed without another start up. This means the device needs to be shutdown by pulling the CTRL low for 3.5 ms and restarts. See Figure 8 for a graphical explanation.

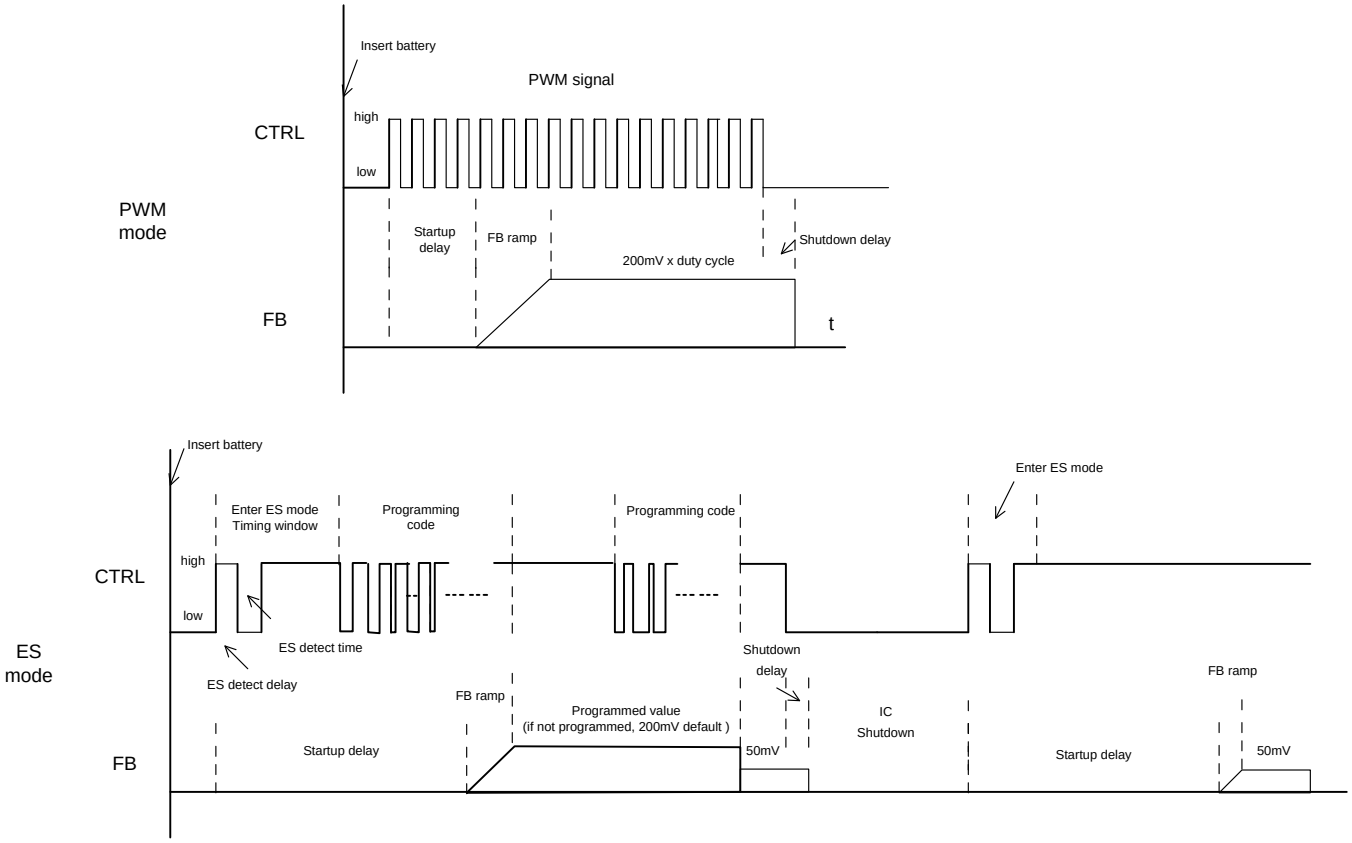


Figure 8. Dimming Mode Detection and Soft Start

7.4.1.1 PWM Brightness Dimming

When the CTRL pin is constantly high, the FB voltage is regulated to 200 mV typically. However, the CTRL pin allows a PWM signal to reduce this regulation voltage; therefore, it achieves LED brightness dimming. The relationship between the duty cycle and FB voltage is given by Equation 2.

$$V_{FB} = \text{Duty} \times 200\ \text{mV} \quad (2)$$

where

- Duty = duty cycle of the PWM signal
- 200 mV = internal reference voltage

As shown in Figure 9, the device chops up the internal 200-mV reference voltage at the duty cycle of the PWM signal. The pulse signal is then filtered by an internal low pass filter. The output of the filter is connected to the error amplifier as the reference voltage for the FB pin regulation. Therefore, although a PWM signal is used for brightness dimming, only the WLED DC current is modulated, which is often referred as analog dimming. This eliminates the audible noise which often occurs when the LED current is pulsed in replica of the frequency and duty cycle of PWM control. Unlike other scheme which filters the PWM signal for analog dimming, the TPS61158 regulation voltage is independent of the PWM logic voltage level which often has large variations.

For optimum performance, use the PWM dimming frequency in the range of 20 kHz to 100 kHz. Since the CTRL pin is logic only pin, adding an external RC filter applied to the pin does not work.

Device Functional Modes (continued)

The minimum dimming duty cycle the device can support is 1% within the PWM dimming frequency range 20 kHz to 100 kHz.

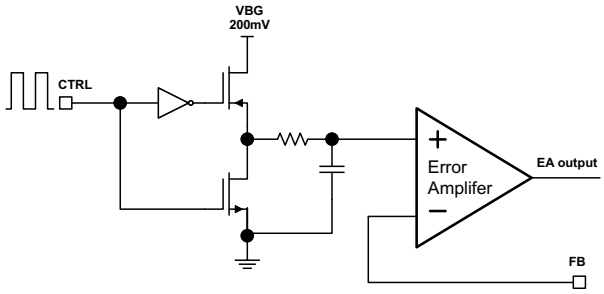


Figure 9. Block Diagram of Programmable FB Voltage Using PWM Signal

7.4.1.1.1 Digital 1-Wire Brightness Dimming

The CTRL pin features a simple digital interface to allow digital brightness control. The digital dimming can save the processor power and battery life as it does not require a PWM signal all the time, and the processor can enter idle mode if available.

The TPS61158 adopts the EasyScale™ protocol for the digital dimming, which can program the FB voltage to any of the 32 steps with single command. The step increment increases with the voltage to produce pseudo logarithmic curve for the brightness step. See the Table 1 for the FB pin voltage steps. The default step is full scale when the device is first enabled (V_{FB} = 200 mV). The programmed reference voltage is stored in an internal register. A power reset clears the register value and reset it to default.

7.4.1.1.2 Easyscale: 1-Wire Digital Dimming

EasyScale is a simple but flexible one-pin interface to configure the FB voltage. The interface is based on a master-slave structure, where the master is typically a microcontroller or application processor. Figure 10 and Table 2 give an overview of the protocol. The protocol consists of a device specific address byte and a data byte. The device specific address byte is fixed to 58 hex. The data byte consists of five bits for information, two address bits ("00"), and the RFA bit. The RFA bit set to high indicates the Request for Acknowledge condition. The Acknowledge condition is only applied if the protocol was received correctly. The advantage of EasyScale compared with other one pin interfaces is that its bit detection is in a large extent independent from the bit transmission rate. It can automatically detect bit rates between 1.1 kBit/sec and up to 100 kBit/sec.

Table 1. Selectable FB Voltage

	FB VOLTAGE (mV)	D4	D3	D2	D1	D0
0	0	0	0	0	0	0
1	5	0	0	0	0	1
2	8	0	0	0	1	0
3	11	0	0	0	1	1
4	14	0	0	1	0	0
5	17	0	0	1	0	1
6	20	0	0	1	1	0
7	23	0	0	1	1	1
8	26	0	1	0	0	0
9	29	0	1	0	0	1
10	32	0	1	0	1	0
11	35	0	1	0	1	1
12	38	0	1	1	0	0
13	44	0	1	1	0	1
14	50	0	1	1	1	0
15	56	0	1	1	1	1
16	62	1	0	0	0	0
17	68	1	0	0	0	1
18	74	1	0	0	1	0
19	80	1	0	0	1	1
20	86	1	0	1	0	0
21	92	1	0	1	0	1
22	98	1	0	1	1	0
23	104	1	0	1	1	1
24	116	1	1	0	0	0
25	128	1	1	0	0	1
26	140	1	1	0	1	0
27	152	1	1	0	1	1
28	164	1	1	1	0	0
29	176	1	1	1	0	1
30	188	1	1	1	1	0
31	200	1	1	1	1	1

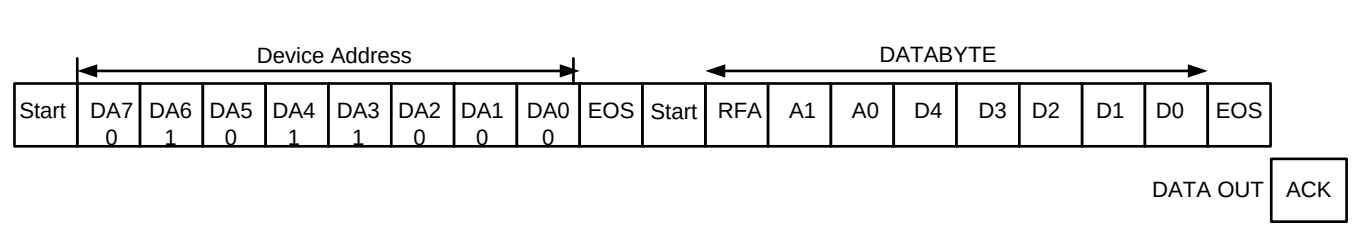


Figure 10. EasyScale Protocol Overview

Table 2. EasyScale Bit Description

BYTE	BIT NUMBER	NAME	TRANSMISSION DIRECTION	DESCRIPTION
Device Address Byte 72 hex	7	DA7	IN	0 (MSB device address)
	6	DA6		1
	5	DA5		0
	4	DA4		1
	3	DA3		1
	2	DA2		0
	1	DA1		0
	0	DA0		0 (LSB device address)
Data byte	7 (MSB)	RFA	IN	Request for acknowledge. If high, acknowledge is applied by device.
	6	A1		0 (Address bit A1)
	5	A0		0 (Address bit A0)
	4	D4		Data bit D4
	3	D3		Data bit D3
	2	D2		Data bit D2
	1	D1		Data bit D1
	0 (LSB)	D0		Data bit D0
		ACK	OUT	Acknowledge condition active 0, this condition will only be applied to case RFA bit is set. Open drain output, line needs to be pulled high by the host with a pullup resistor. This feature can only be used if the master has an open drain output stage. In case of a push pull output stage Acknowledge condition may not be requested!

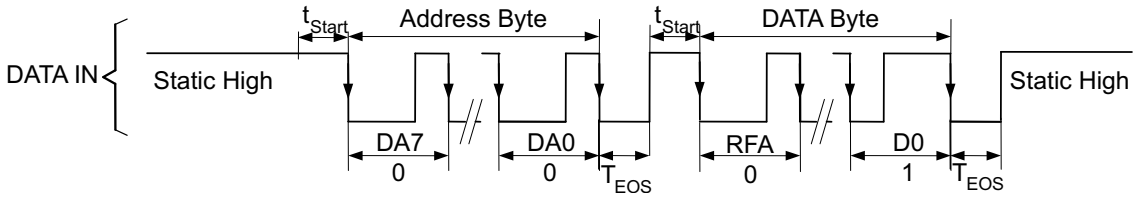


Figure 11. EasyScale Timing, Without Acknowledge (RFA = 0)

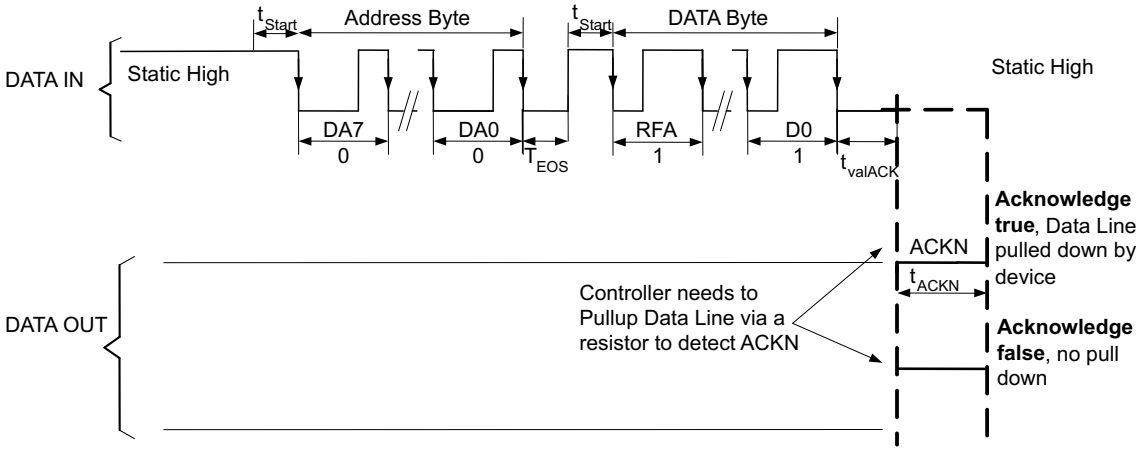


Figure 12. EasyScale Timing, With Acknowledge (RFA = 1)

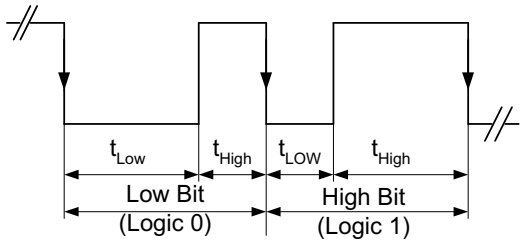


Figure 13. EasyScale— Bit Coding

All bits are transmitted MSB first and LSB last. Figure 11 shows the protocol without acknowledge request (Bit RFA = 0), Figure 12 with acknowledge (Bit RFA = 1) request. Prior to both bytes, device address byte and data byte, a start condition must be applied. For this, the CTRL pin must be pulled high for at least t_{start} (3.5µs) before the bit transmission starts with the falling edge. If the CTRL pin is already at high level, no start condition is needed prior to the device address byte. The transmission of each byte is closed with an End of Stream condition for at least t_{EOS} (3.5µs).

The bit detection is based on a Logic Detection scheme, where the criterion is the relation between t_{LOW} and t_{HIGH} (refer to Figure 13). It can be simplified to:

- Low Bit (Logic 0): $t_{LOW} \geq 2 \times t_{HIGH}$
- High Bit (Logic 1): $t_{HIGH} \geq 2 \times t_{LOW}$

The bit detection starts with a falling edge on the CTRL pin and ends with the next falling edge. Depending on the relation between t_{HIGH} and t_{LOW}, the logic 0 or 1 is detected.

The acknowledge condition is only applied if:

- Acknowledge is requested by setting RFA bit to 1.
- The transmitted device address matches with the device address of the device.
- Device address byte and data byte are received correctly.

If above conditions are met, after t_{valACK} (3.5 µs) delay from the moment when the last falling edge of the protocol is detected, an internal ACKN-MOSFET is turned on to pull the CTRL pin low for the time t_{ACKN} (900 µs maximum), then the Acknowledge condition is valid. During the t_{valACK} delay, the master controller keeps the line low; after the delay, it should release the line by outputting high impedance and then detect the acknowledge condition. If it reads back a logic 0, it means the device has received the command correctly. The CTRL pin can be used again by the master when the acknowledge condition ends after t_{ACKN} time.

Note that the acknowledge condition can only be requested in case the master device has an open drain output. For a push-pull output stage, the use a series resistor in the CTRL line to limit the current to 500 µA is recommended to for such cases as:

- an accidentally requested acknowledge, or
- to protect the internal ACKN-MOSFET.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS61158 provides a high-performance LED lighting solution for mobile handsets and other low power LCD backlit displays. The device can drive from 2 to 8 series LEDs in a compact and high efficient solution. An internal rectifying diode eliminates the need for an external Schottky. The LED current is controlled via a logic level PWM input with an internal low pass filter. This low pass filtered (analog) dimming, reduces the output capacitor requirement and provides noise free current control.

8.2 Typical Application

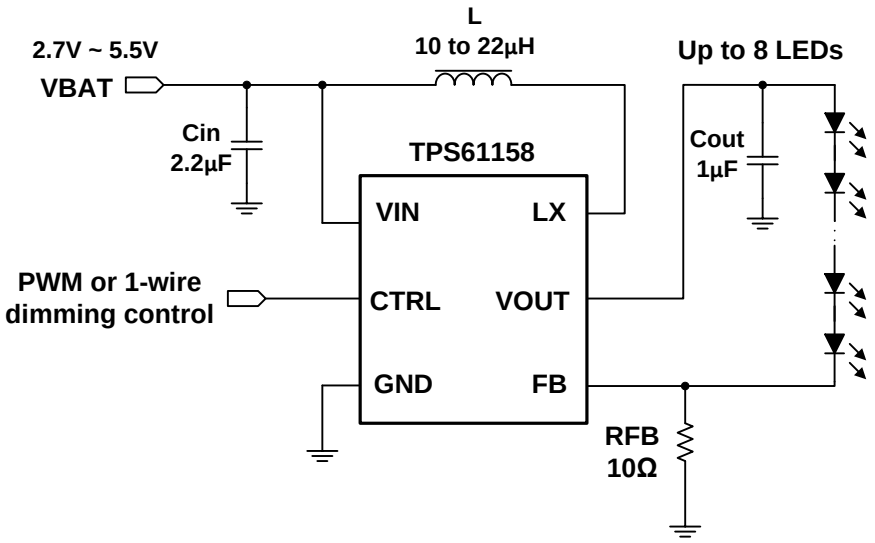


Figure 14. Typical Application for TPS61158

8.2.1 Design Requirements

For TPS61158 typical applications, use the parameters listed in Table 3 as the input parameters.

Table 3. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Minimum input voltage	2.7 V
Number of series LED	up to 8
Switching frequency	750 MHz

8.2.2 Detailed Design Procedure

8.2.2.1 Inductor Selection

The selection of the inductor affects steady state operation as well as transient behavior, loop stability and the power conversion efficiency. These factors make it the most important component in power regulator design. There are three important inductor specifications, inductor value, DC resistance, and saturation current. Considering inductor value alone is not enough. The inductor value determines the inductor ripple current. Choose an inductor that can handle the necessary peak current without saturating, according to half of the peak-to-peak ripple current given by Equation 4, plus the inductor DC current given by:

$$I_{in\_DC} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta} \quad (3)$$

Inductor values can have ±20% or even ±30% tolerance with no current bias. When the inductor current approaches saturation level, its inductance can decrease 20% to 35% from the 0A value depending on how the inductor vendor defines saturation. When selecting an inductor, please make sure its rated current, especially the saturation current, is larger than its peak current during the operation. Using an inductor with a smaller inductance value causes larger current ripple. This reduces the boost converter's maximum output current, causes large input voltage ripple and reduces efficiency. Large inductance value provides much more output current and higher conversion efficiency. For these reasons, a 10-µH to 22-µH inductor value range is recommended. A 22-µH inductor optimizes the efficiency for most application while maintaining low inductor peak-to-peak ripple. Table 4 lists the recommended inductors for TPS61158. TPS61158 has built-in slope compensation to avoid sub-harmonic oscillation associated with current mode control. If the inductor value is lower than 10 µH, the slope compensation may not be adequate, and the loop can be unstable. Therefore, customers need to verify the inductor in their application if it is different from the recommended values.

Table 4. Recommended Inductors

PART NUMBER	L (µH)	DCR MAX (mΩ)	SATURATION CURRENT (A)	Size (L x W x H mm)	VENDOR
LPS3015-103ML	10	440	0.73	3.0 x 3.0 x 1.5	Coilcraft
LPS3015-223ML	22	825	0.5	3.0 x 3.0 x 1.5	Coilcraft
1229AS-H-100M	10	288	0.75	3.5 x 3.7 x 1.2	TOKO
1229AS-H-220M	22	672	0.5	3.5 x 3.7 x 1.2	TOKO
VLS3012ET-100M	10	336	0.64	3.0 x 3.0 x 1.2	TDK
VLS3012ET-220M	22	756	0.44	3.0 x 3.0 x 1.2	TDK

8.2.2.2 Maximum Output Current

The overcurrent limit in a boost converter limits the maximum input current and thus maximum input power for a given input voltage. Maximum output power is less than maximum input power due to power conversion losses. Therefore, the current limit setting, input voltage, output voltage and efficiency can all change maximum current output. The current limit clamps the peak inductor current; therefore, the ripple has to be subtracted to derive maximum DC current. The ripple current is a function of switching frequency, inductor value and duty cycle. The following equations take into account of all the above factors for maximum output current calculation.

$$I_P = \frac{1}{L \times F_S \times \left(\frac{1}{V_{OUT} + V_F - V_{IN}} + \frac{1}{V_{IN}}\right)} \quad (4)$$

where

- I_P = inductor peak to peak ripple
- L = inductor value
- F_S = switching frequency
- V_{OUT} = output voltage of the boost converter. It is equal to the sum of V_{FB} and the voltage drop across LEDs.
- V_F = forward voltage of internal power diode. 0.75 V, typical

$$I_{OUT\_max} = \frac{V_{IN} \times (I_{LIM} - I_P / 2) \times \eta}{V_{OUT}}$$

where

- I_{OUT_max} = maximum output current of the boost converter
- I_{LIM} = overcurrent limit
- η = boost efficiency (85%, typical) (5)

To calculate the maximum output current in the worst case, use the minimum input voltage, maximum output voltage and maximum forward voltage of internal power diode (1 V). In order to leave enough design margin, the minimum current limit value 0.5 A, the minimum switching frequency 600 kHz, the inductor value with –30% tolerance, and a low power conversion efficiency, such as 80% or lower are recommended for the calculation. For instance, when minimum V_{IN} is 3 V, 8 LEDs output equivalent to V_{OUT} is 26 V, and the inductor is 22 µH, then the maximum output current is 33 mA in the worst case.

8.2.2.3 Input and Output Capacitor Selection

The output capacitor is mainly selected to meet the requirements for the output ripple and loop stability. This ripple voltage is related to the capacitor's capacitance and its equivalent series resistance (ESR). Assuming a capacitor with zero ESR, the minimum capacitance needed for a given ripple can be calculated by

$$C_{OUT} = \frac{(V_{OUT} - V_{IN}) \times I_{OUT}}{V_{OUT} \times F_S \times V_{ripple}}$$

where

- V_{ripple} = peak-to-peak output ripple. (6)

The additional output ripple component caused by ESR is calculated using Equation 7:

$$V_{ripple\_ESR} = I_{OUT} \times R_{ESR} \quad (7)$$

Due to its low ESR, V_{ripple_ESR} can be neglected for ceramic capacitors, but must be considered if tantalum or electrolytic capacitors are used.

Care must be taken when evaluating a ceramic capacitor's derating under DC bias, aging and AC signal. The DC bias can significantly reduce capacitance. Ceramic capacitors can lose as much as 50% of its capacitance at its rated voltage. Therefore, leave the margin on the voltage rating to ensure adequate capacitance at the required output voltage.

The capacitor in the range of 1 µF to 10 µF is recommended for input side. The output requires a capacitor in the range of 0.47 µF to 2.2 µF. The output capacitor affects the loop stability of the boost regulator. If the output capacitor is below the range, the boost regulator can potentially become unstable.

The popular vendors for high value ceramic capacitors are:

TDK (http://www.component.tdk.com/components.php)

Murata (http://www.murata.com/cap/index.html)

8.2.3 Application Curves

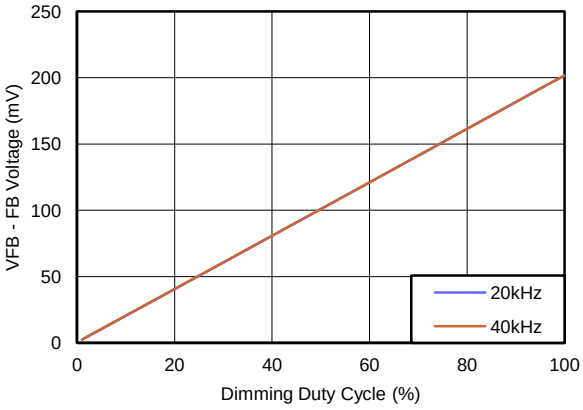


Figure 15. FB Voltage vs Dimming Duty Cycle

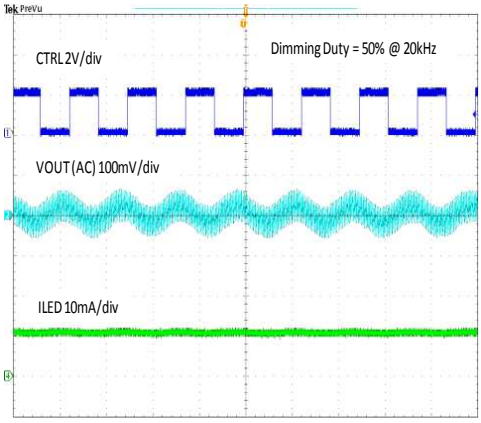


Figure 16. Output Ripple at PWM Dimming

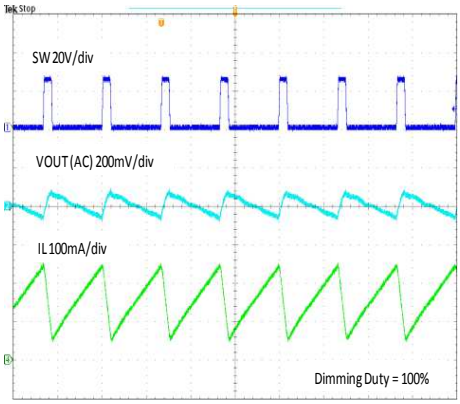


Figure 17. Switching Waveform - Dimming Duty = 100%

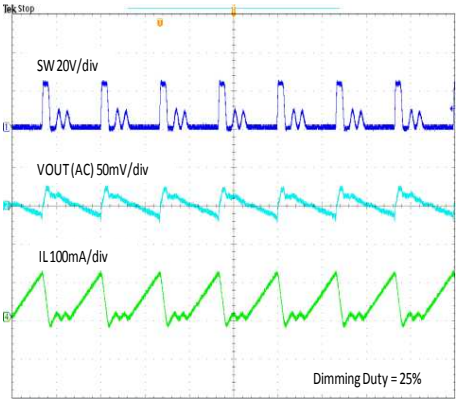


Figure 18. Switching Waveform - Dimming Duty = 25%

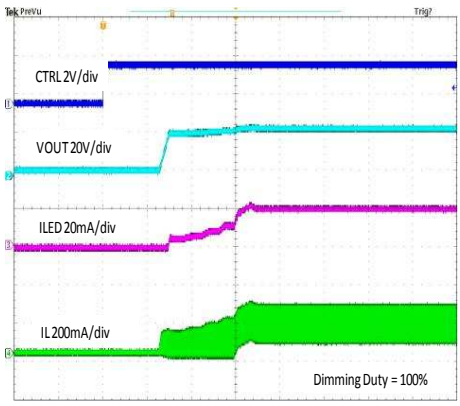


Figure 19. Start-Up Dimming Duty = 100%

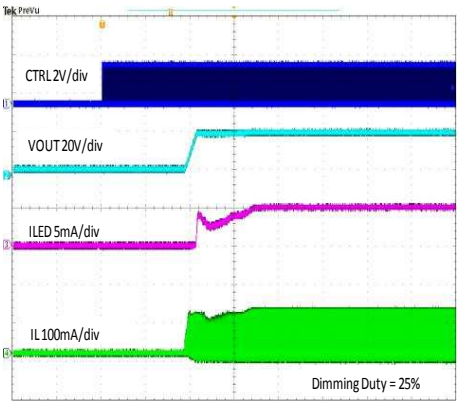


Figure 20. Start-Up Dimming Duty = 25%

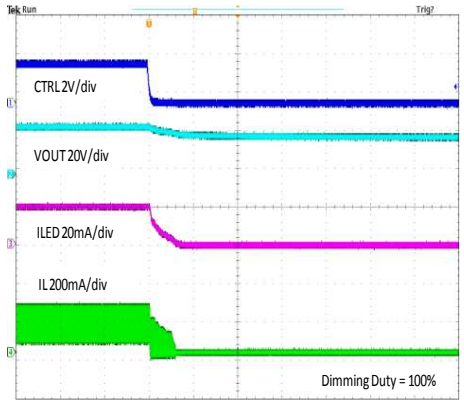


Figure 21. Shutdown Dimming Duty = 100%

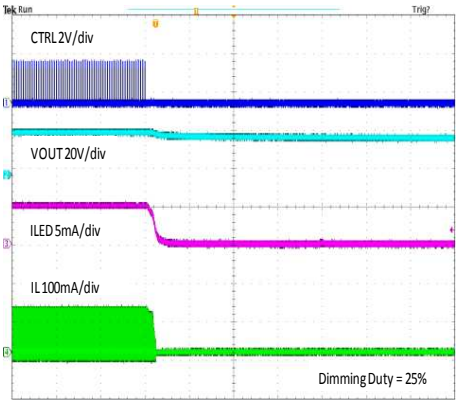


Figure 22. Shutdown Dimming Duty = 25%

8.2.4 Additional Application Circuits

8.2.4.1 TPS61158 To Drive Up To 8 LEDs

Figure 23 shows a typical application for the TPS61158. This can drive from 2 to 8 series WLEDs.

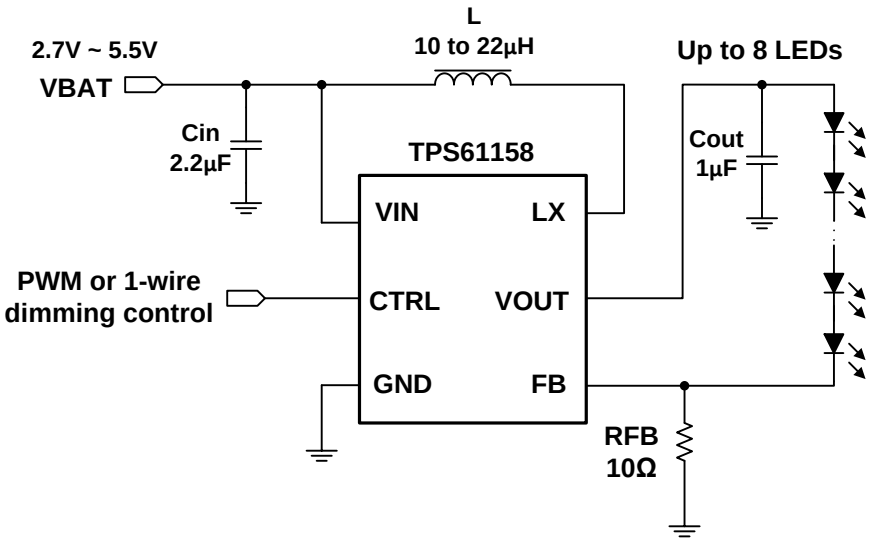


Figure 23. TPS61158 to Drive up to 8 LEDs

8.2.4.2 TPS61158 to Drive up to 8 LEDs with RC Filter at VIN Pin

Figure 24 is typical application circuit with RC filter at IN.

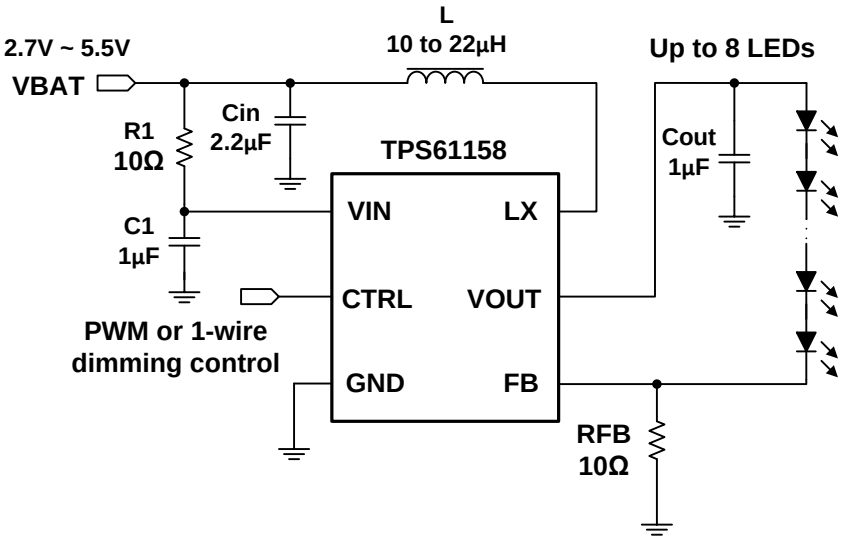


Figure 24. TPS61158 to Drive up to 8 LEDs With RC Filter at VIN Pin

9 Power Supply Recommendations

The TPS61158 requires a single supply input voltage. This voltage can range between 2.7 V to 5.5 V and must be able to supply enough current for a given application.

10 Layout

10.1 Layout Guidelines

As for all switching power supplies, especially those high frequency and high current ones, layout is an important design step. If layout is not carefully done, the regulator could suffer from instability as well as noise problems. Therefore, use wide and short traces for high current paths. The input capacitor C_{IN} needs to be close to the VIN pin and GND pin in order to reduce the input ripple seen by the device. If possible, choose higher capacitance value for it. If the ripple seen at VIN pin is so large that it affects the boost loop stability or internal circuits operation, R1 and C1 is recommended to compose a filter to decouple the noise (refer to Figure 24). The SW pin carries high current with fast rising and falling edges. Therefore, the connection between the SW pin to the inductor should be kept as short and wide as possible. The output capacitor C_{OUT} should be put close to VOUT pin. It is also beneficial to have the ground of C_{OUT} close to the GND pin since there is large ground return current flowing between them. FB resistor should be put close to FB pin. When laying out signal grounds, it is recommended to use short traces separated from power ground traces, and connect them together at a single point close to the GND pin.

10.2 Layout Example

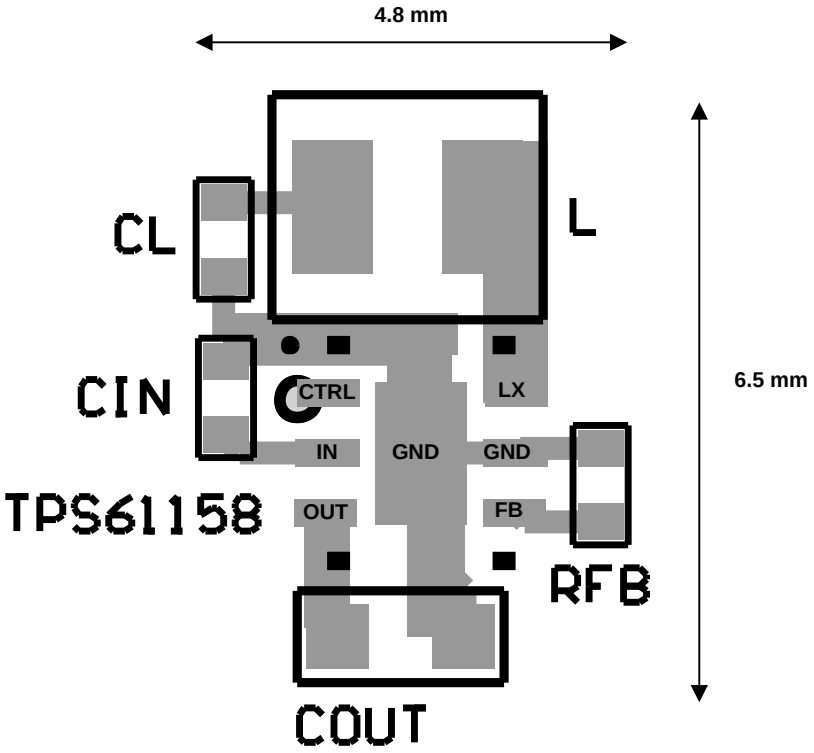


Figure 25. TPS61158 Example Layout

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.2 Community Resources

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

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All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS61158DRVR	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	SIW	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

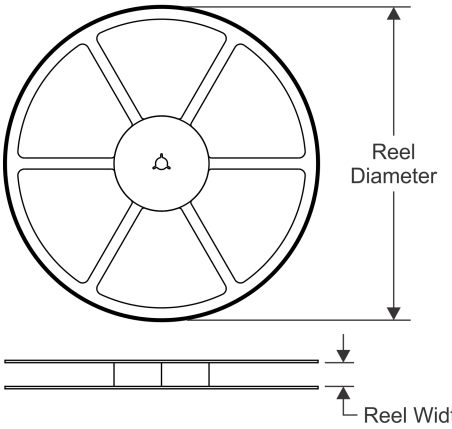
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

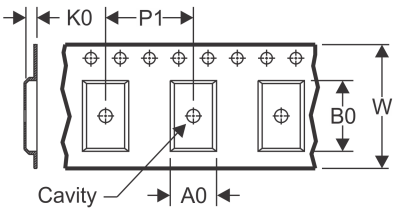
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

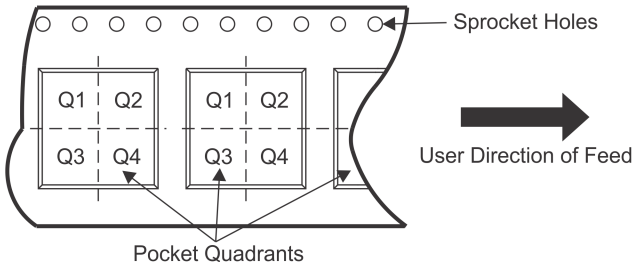


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

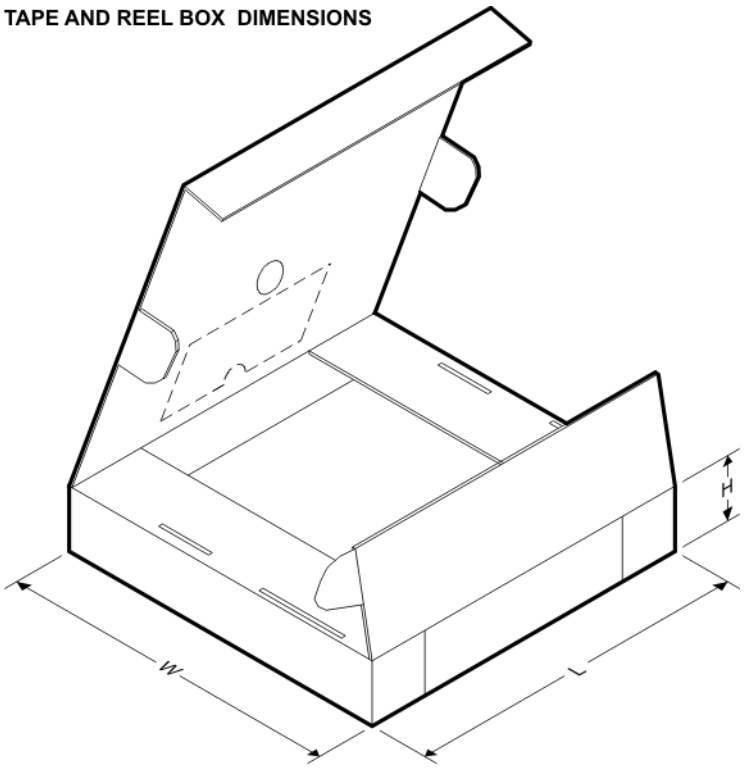
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS61158DRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

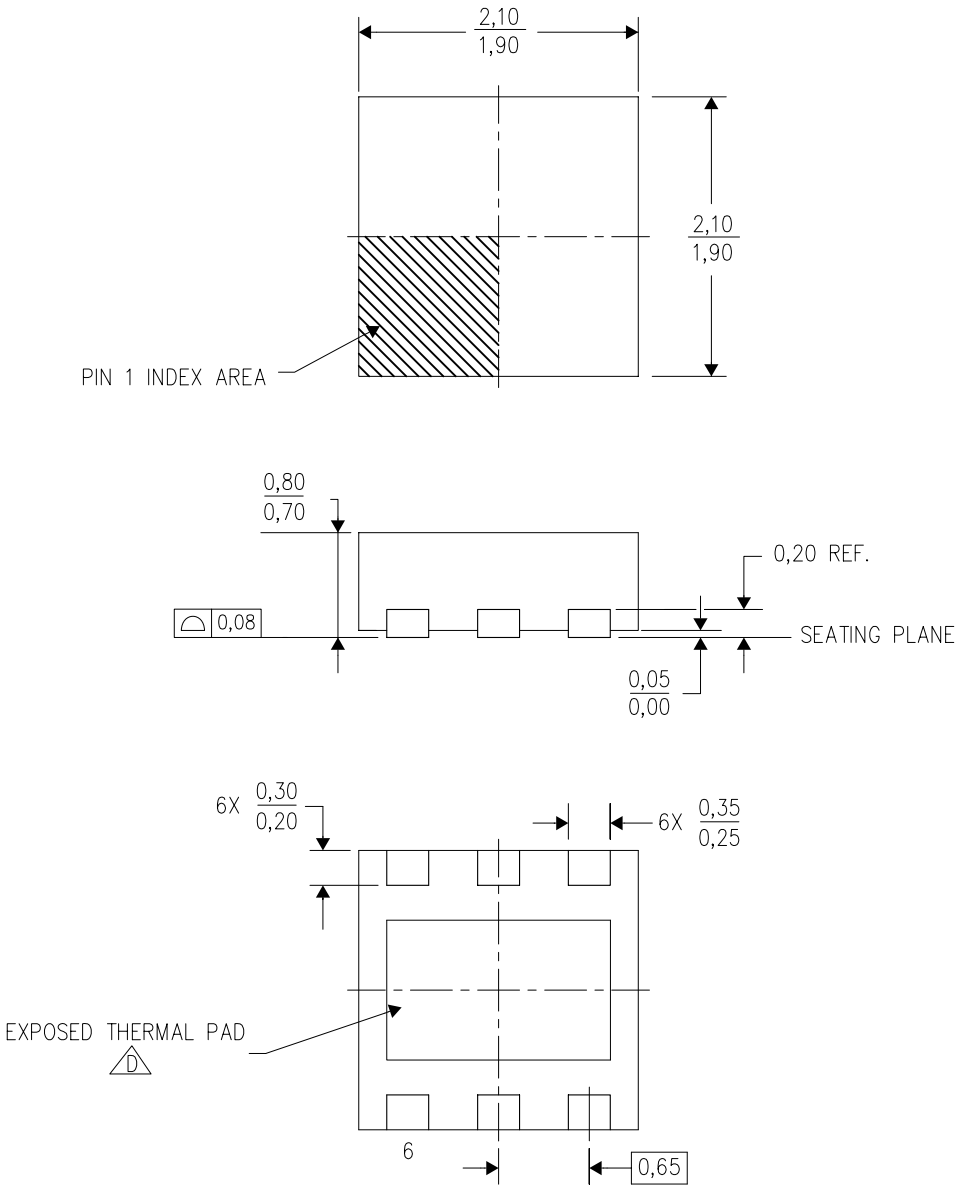
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS61158DRVR	WSON	DRV	6	3000	210.0	185.0	35.0

DRV (S–PWSON–N6) PLASTIC SMALL OUTLINE NO–LEAD



4206925/E 10/10

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

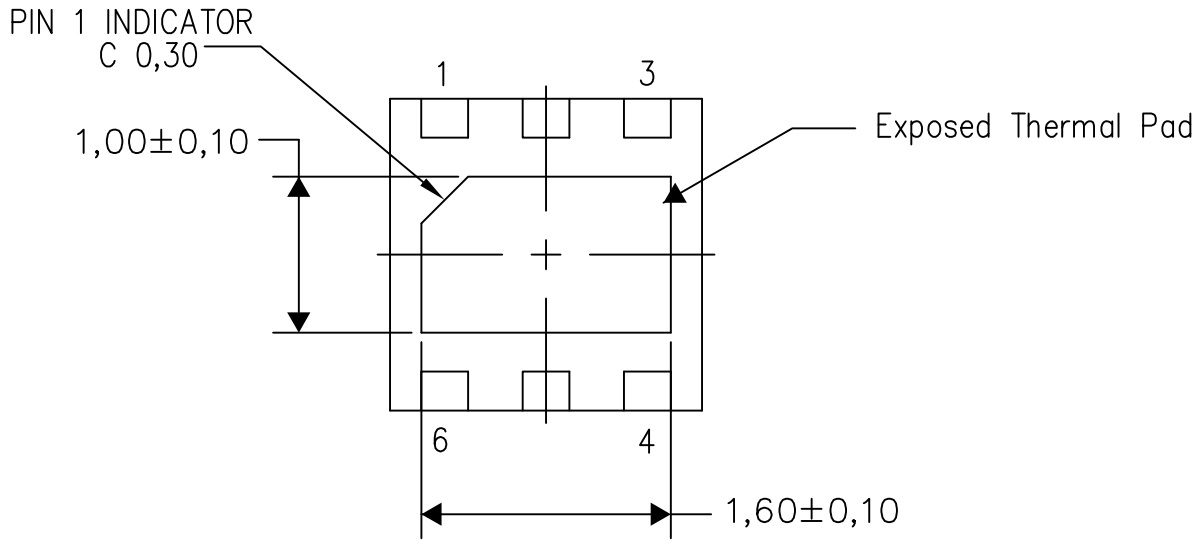
DRV (S–PWSON–N6) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



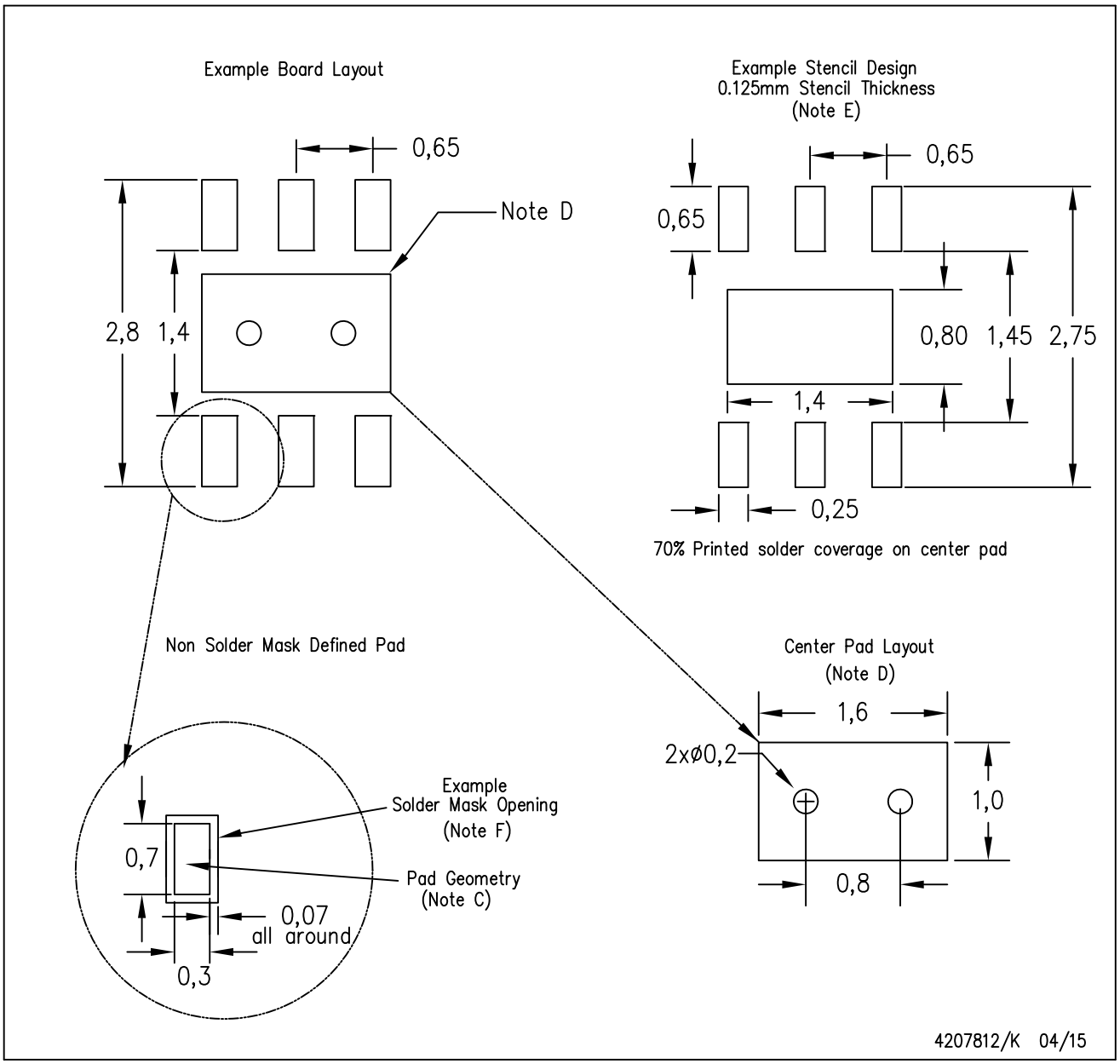
Bottom View

Exposed Thermal Pad Dimensions

4206926/Q 04/15

NOTE: All linear dimensions are in millimeters

DRV (S–PWSON–N6) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

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