TPS6505x 6-Channel Power-Management IC With Two Step-Down Converters and Four Low-Input Voltage LDOs

TPS65052 is Obsolete

1 Features

- Up To 95% Efficiency
- Output Current for DC-DC Converters:
  - TPS65050, TPS65054: 2 × 0.6 A
  - TPS65051, TPS65052 and TPS65056: DCDC1 = 1 A; DCDC2 = 0.6 A
- Output Voltages for DC-DC Converters
  - Externally Adjustable and Fixed Versions Available
  - Digital Voltage Selection for the DCDC2
- V_I Range for DC-DC Converters From 2.5 V to 6 V
- 2.25-MHz Fixed-Frequency Operation
- Power Save Mode at Light Load Current
- 180° Out-of-Phase Operation
- Output Voltage Accuracy in PWM Mode ±1%
- Total Typical 32-μA Quiescent Current for Both DC-DC Converters
- 100% Duty Cycle for Lowest Dropout
- Two General-Purpose 400-mA, High PSRR LDOs
- Two General-Purpose 200-mA, High PSRR LDOs
- V_I range for LDOs From 1.5 V to 6.5 V
- Digital Voltage Selection for the LDOs

2 Applications

- Cell Phones, Smart Phones
- WLAN
- PDAs, Pocket PCs
- OMAP™ and Low-Power TMS320™ DSP Supply
- Samsung S3C24xx Application Processor Supply
- Portable Media Players

3 Description

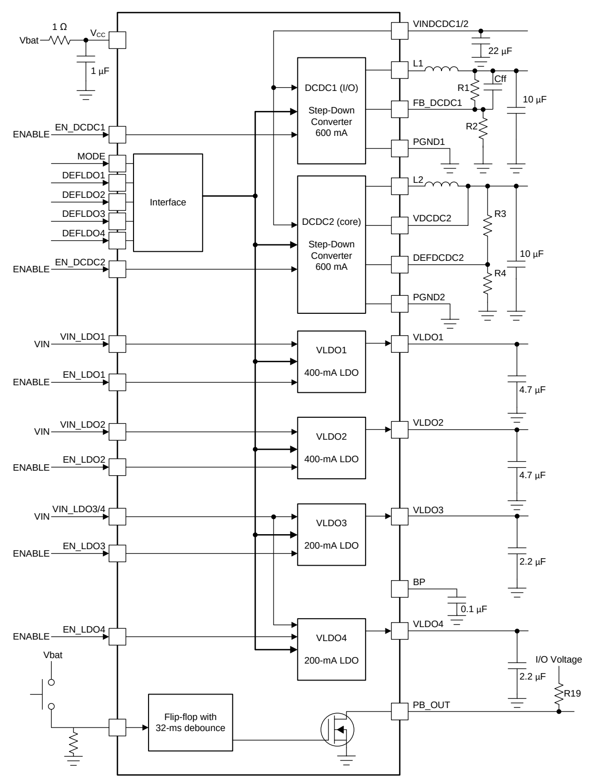
The TPS6505x family of devices are integrated power-management ICs for applications powered by one Li-Ion or Li-Polymer cell, which require multiple power rails. The TPS6505x devices provide two highly efficient, 2.25-MHz step-down converters targeted at providing the core voltage and I/O voltage in a processor-based system. Both step-down converters enter a low-power mode at light load for maximum efficiency across the widest possible range of load currents. For low noise applications, the devices can be forced into fixed-frequency PWM mode by pulling the MODE pin high. The TPS6505x devices also integrate two 400-mA LDO and two 200-mA LDO voltage regulators. Each LDO operates with an input voltage range from 1.5 V to 6.5 V, allowing them to be supplied from one of the step-down converters or directly from the main battery.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS6505x	VQFN (32)	4.00 mm × 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Block Diagram



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (June 2015) to Revision C	Page
• Deleted package marking and package information from the *Device Options* table. See the *Device and Documentation Support* section for packaging information	3
• Replaced references to PowerPAD with thermal pad	5
• Updated the functional block diagrams	12
• Specified the maximum dropout voltage for each LDO in the *Low Dropout Voltage Regulators* section	21
• Changed the resistor labels of R3, R4, and R5 to R13, R14, and R15 in the $\overline{RESET}$ section and updated the $\overline{RESET}$ *Circuit* figure	29
• Updated the *Typical Characteristics* and *Application Curves* sections	30
• Added the *Receiving Notification of Documentation Updates* section	35
• Changed the *Electrostatic Discharge Caution* statement	35

Changes from Revision A (August 2007) to Revision B	Page
• Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1
• Changed graph in Figure 14: should be PF_IN and PB_OUT not PB_IN and /RESPWRON	21

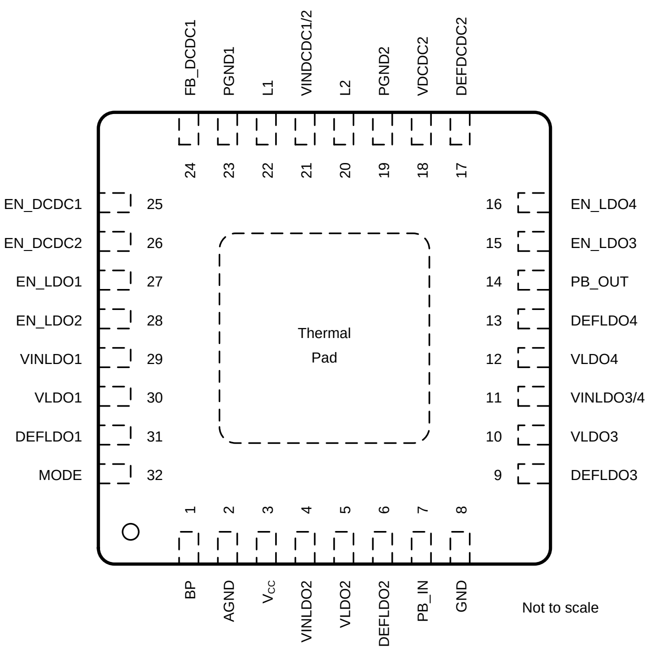
Changes from Original (January 2007) to Revision A	Page
• Added quantities of 3000 parts to ordering information note	3
• Added Output voltage range to absolute maximum ratings table	5
• Changed LDO1/2 Output voltage range maximum value to 3.6 V	6
• Changed Output voltage 2.8-V R5 resistor value to 360 kΩ in typical resistor values table	28

5 Device Options

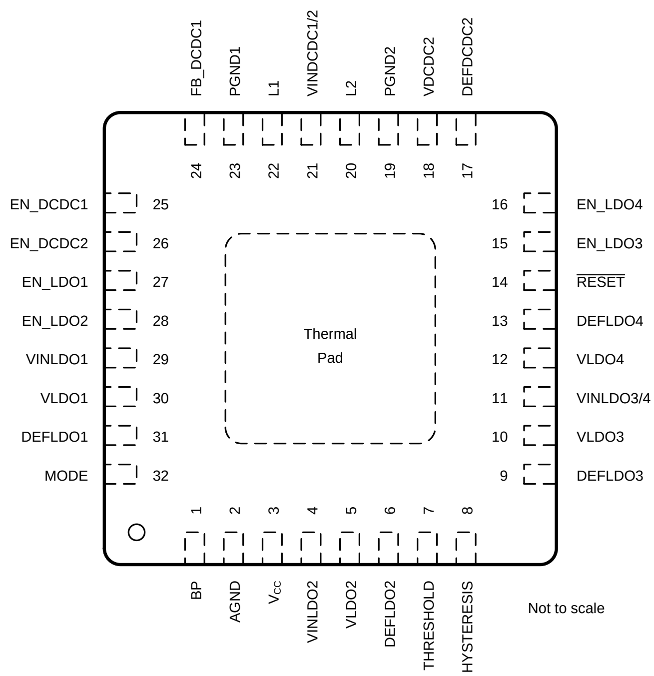
PART NUMBER	OPTION	OUTPUT CURRENT for DC-DC CONVERTERS
TPS65050	LDO voltages according to Table 1 DC-DC converters externally adjustable	2 × 600 mA
TPS65051	LDO voltages externally adjustable DC-DC converters externally adjustable	DCDC1 = 1 A DCDC2 = 600 mA
TPS65052	LDO voltages according to Table 1 DCDC1 = 3.3 V; DCDC2 = 1 V / 1.3 V	DCDC1 = 1 A DCDC2 = 600 mA
TPS65054	LDO voltages externally adjustable DCDC1 = externally adjustable DCDC2 = 1.3 V / 1.05 V	2 × 600 mA
TPS65056	LDO voltages externally adjustable DCDC1 = 3.3 V DCDC2 = 1 V / 1.3 V	DCDC1 = 1A DCDC2 = 600 mA

6 Pin Configuration and Functions

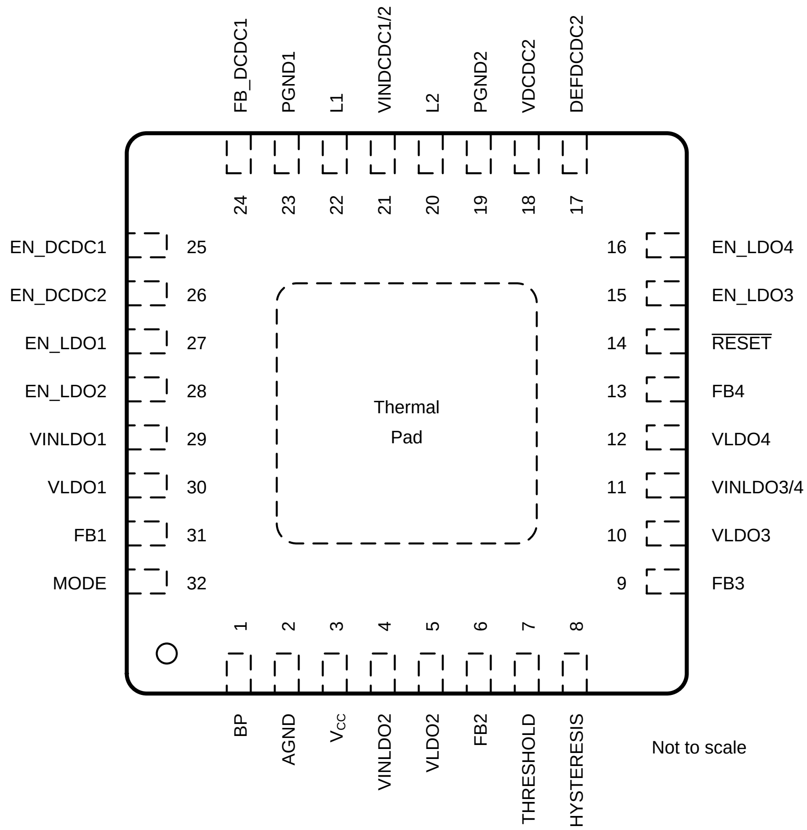
TPS65050 RSM Package
32-Pin VQFN With Exposed Thermal Pad
Top View



TPS65052 RSM Package
32-Pin VQFN With Exposed Thermal Pad
Top View



TPS65051, TPS65054, TPS65056 RSM Package
32-Pin VQFN With Exposed Thermal Pad
Top View



Pin Functions

PIN				I/O	DESCRIPTION
NAME	TPS65050	TPS65051 TPS65054 TPS65056	TPS65052		
AGND	2	2	2	I	Analog GND, connect to PGND and thermal pad
BP	1	1	1	I	Input for bypass capacitor for internal reference.
DEFDCDC2	17	17	17	I	TPS65050 and TPS65051 devices: Feedback pin for converter 2. Connect DEFDCDC2 to the center of the external resistor divider. TPS65052 and TPS65056 devices: Select pin of converter 2 output voltage. High = 1.3 V, Low = 1 V TPS65054 device: Select pin of converter 2 output voltage. High = 1.05 V, Low = 1.3 V
DEFLDO1	31	—	31	I	Digital input, used to set the default output voltage of LDO1 to LDO4; LSB
DEFLDO2	6	—	6	I	Digital input, used to set the default output voltage of LDO1 to LDO4.
DEFLDO3	9	—	9	I	Digital input, used to set the default output voltage of LDO1 to LDO4.
DEFLDO4	13	—	13	I	Digital input, used to set the default output voltage of LDO1 to LDO4; MSB
EN_DCDC1	25	25	25	I	Enable Input for converter 1, active high
EN_DCDC2	26	26	26	I	Enable Input for converter 2, active high
EN_LDO1	27	27	27	I	Enable input for LDO1. Logic high enables the LDO, logic low disables the LDO.
EN_LDO2	28	28	28	I	Enable input for LDO2. Logic high enables the LDO, logic low disables the LDO.
EN_LDO3	15	15	15	I	Enable input for LDO3. Logic high enables the LDO, logic low disables the LDO.
EN_LDO4	16	16	16	I	Enable input for LDO4. Logic high enables the LDO, logic low disables the LDO.
FB1	—	31	—	I	Feedback input for the external voltage divider.
FB2	—	6	—	I	Feedback input for the external voltage divider.
FB3	—	9	—	I	Feedback input for the external voltage divider.

Pin Functions (continued)

PIN				I/O	DESCRIPTION
NAME	TPS65050	TPS65051 TPS65054 TPS65056	TPS65052		
FB4	—	13	—	I	Feedback input for the external voltage divider.
FB_DCDC1	24	24	24	I	Input to adjust output voltage of converter 1 between 0.6 V and V_I. Connect external resistor divider between VOUT1, this pin, and GND.
GND	8	—	—	—	Connect to GND
HYSTERESIS	--	8	8	I	Input for hysteresis on reset threshold
L1	22	22	22	O	Switch pin of converter 1. Connected to Inductor .
L2	20	20	20	O	Switch Pin of converter 2. Connected to Inductor.
MODE	32	32	32	I	Select between Power Safe Mode and forced PWM Mode for DCDC1 and DCDC2. In Power Safe Mode, PFM is used at light loads, PWM for greater loads. If PIN is set to high level, forced PWM Mode is selected. If Pin has low level, then the device operates in Power Safe Mode.
PB_IN	7	—	—	I	Input for the pushbutton ON-OFF function
PB_OUT	14	—	—	O	Open-drain output. Active low after the supply voltage (V_{CC}) exceeded the undervoltage lockout threshold. The pin can be toggled pulling PB_IN high.
PGND1	23	23	23	I	GND for converter 1
PGND2	19	19	19	I	GND for converter 2
$\overline{\text{RESET}}$	—	14	14	O	Open-drain active low reset output, 100-ms reset delay time.
THRESHOLD	—	7	7	I	Reset input
V_{CC}	3	3	3	I	Power supply for digital and analog circuitry of DCDC1, DCDC2 and LDOs. This pin must be connected to the same voltage supply as VINDCDC1/2.
VDCDC2	18	18	18	I	Feedback voltage sense input, connect directly to the output of converter 2.
VINDCDC1/2	21	21	21	I	Input voltage for VDCDC1 and VDCDC2 step-down converter. This must be connected to the same voltage supply as V_{CC}.
VINLDO1	29	29	29	I	Input voltage for LDO1
VINLDO2	4	4	4	I	Input voltage for LDO2
VINLDO3/4	11	11	11	I	Input voltage for LDO3 and LDO4
VLDO1	30	30	30	O	Output voltage of LDO1
VLDO2	5	5	5	O	Output voltage of LDO2
VLDO3	10	10	10	O	Output voltage of LDO3
VLDO4	12	12	12	O	Output voltage of LDO4
Thermal pad	—	—	—	—	Connect to GND

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_I	Input voltage range on all pins except AGND, PGND, and EN_LDO1 pins with respect to AGND	–0.3	7	V
	Input voltage range on EN_LDO1 pins with respect to AGND	–0.3	V_{CC} + 0.5	V
I_I	Current at VINDCDC1/2, L1, PGND1, L2, PGND2		1800	mA
	Current at all other pins		1000	mA
V_O	Output voltage range for LDO1, LDO2, LDO3, and LDO4	–0.3	4	V
	Continuous total power dissipation	See *Dissipation Ratings*		
T_A	Operating free-air temperature	–40	85	°C
T_J	Maximum junction temperature		125	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101[2]	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_I	Input voltage range for step-down converters, VINDCDC1/2	2.5		6	V
V_O	Output voltage range for step-down converter, VDCDC1	0.6		VINDCDC1/2	V
	Output voltage range for step-down converter, VDCDC2	0.6		VINDCDC1/2	V
V_I	Input voltage range for LDOs, VINLDO1, VINLDO2, VINLDO3/4	1.5		6.5	V
V_O	Output voltage range for LDO1, LDO2, LDO3 and LDO4	1		3.6	V
I_O	Output current at L1 (DCDC1) for TPS65051, TPS65052			1000	mA
	Output current at L1 (DCDC1) for TPS65050, TPS65054			600	mA
	Output current at L1 (DCDC2)			600	mA
	Output current at VLDO1, VLDO2			400	mA
	Output current at VLDO3, VLDO4			200	mA
	Inductor at L1, L2[1]	1.5	2.2		µH
C_O	Output capacitor at VDCDC1, VDCDC2[1]	10	22		µF
	Output capacitor at VLDO1, VLDO2, VLDO3, VLDO4[1]	2.2			µF
C_I	Input capacitor at VCC[1]	1			µF
	Input capacitor at VINLDO1/2/3/4[1]	2.2			µF
T_A	Operating ambient temperature range	–40		85	°C
T_J	Operating junction temperature range	–40		125	°C
R_{filter}	Resistor from battery voltage to V_{CC} used for filtering[2]		1	10	Ω

(1) See the *Application and Implementation* section of this data sheet for more details.
(2) Up to 2 mA can flow into V_{CC} when both converters are running in PWM, this resistor causes the UVLO threshold to be shifted accordingly.

7.4 Thermal Information

THERMAL METRIC[1]		TPS6505x RSM (VQFN) 32 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	37.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	30.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	7.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

V_{CC} = VINDCDC1/2 = 3.6 V, EN = V_{CC}, MODE = GND, L = 2.2 µH, C_O = 10 µF. T_A = -40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
V_I	Input voltage range at VINDCDC1/2		2.5		6	V
I_Q	Operating quiescent current Total current into V_{CC}, VINDCDC1/2, VINLDO1, VINLDO2, VINLDO3/4	One converter, I_O = 0 mA. PFM mode enabled (Mode = GND) device not switching, EN_DCDC1 = V_I OR EN_DCDC2 = V_I; EN_LDO1= EN_LDO2 = EN_LDO3/4 = GND		20	30	µA
		Two converters, I_O = 0 mA PFM mode enabled (Mode = 0) device not switching, EN_DCDC1 = V_I AND EN_DCDC2 = V_I; EN_LDO1 = EN_LDO2 = EN_LDO3/4 = GND		32	40	µA
		One converter, I_O = 0 mA. PFM mode enabled (Mode = GND) device not switching, EN_DCDC1 = V_I OR EN_DCDC2 = V_I; EN_LDO1 = EN_LDO2 = EN_LDO3 = EN_LDO4 = V_I		180	250	µA
I_Q	Operating quiescent current into V_{CC}	One converter, I_O = 0 mA. Switching with no load (Mode = V_I), PWM operation EN_DCDC1 = V_I OR EN_DCDC2 = V_I; EN_LDO1 = EN_LDO2 = EN_LDO3/4 = GND		0.85		mA
		Two converters, I_O = 0 mA Switching with no load (Mode = V_I), PWM operation EN_DCDC1 = V_I AND EN_DCDC2 = V_I; EN_LDO1 = EN_LDO2 = EN_LDO3/4 = GND		1.25		mA
$I_{(SD)}$	Shutdown current	EN_DCDC1 = EN_DCDC2 = GND EN_LDO1 = EN_LDO2 = EN_LDO3 = EN_LDO4 = GND		9	12	µA
$V_{(UVLO)}$	Undervoltage lockout threshold for DCDC converters and LDOs	Voltage at V_{CC}		1.8	2	V
EN_DCDC1, EN_DCDC2, DEFDCDC2, DEFLDO1, DEFLDO2, DEFLDO3, DEFLDO4, EN_LDO1, EN_LDO2, EN_LDO3, EN_LDO4						
V_{IH}	High-level input voltage	MODE/DATA, EN_DCDC1, EN_DCDC2, DEFDCDC2, DEFLDO1, DEFLDO2, DEFLDO3, DEFLDO4, EN_LDO1, EN_LDO2, EN_LDO3, EN_LDO4	1.2		V_{CC}	V
V_{IL}	Low-level input voltage	MODE/DATA, EN_DCDC1, EN_DCDC2, DEFLDO1, DEFLDO2, DEFLDO3, DEFLDO4, EN_LDO1, EN_LDO2, EN_LDO3, EN_LDO4, DEFDCDC2	0		0.4	V
I_{IB}	Input bias current	MODE/DATA = GND or V_I MODE/DATA, EN_DCDC1, EN_DCDC2, DEFDCDC2, DEFLDO1, DEFLDO2, DEFLDO3, DEFLDO4, EN_LDO1, EN_LDO2, EN_LDO3, EN_LDO4		0.01	1	µA
		TPS65051 and TPS65052 only V_FB_LDOx = 1 V FB_LDO1, FB_LDO2, FB_LDO3, FB_LDO4			100	nA
POWER SWITCH						
$r_{DS(on)}$	P-channel MOSFET on resistance	DCDC1, VINDCDC1/2 = 3.6 V		280	630	mΩ
		DCDC1, VINDCDC1/2 = 2.5 V		400		mΩ
		DCDC2, VINDCDC1/2 = 3.6 V		280	630	mΩ
		DCDC2, VINDCDC1/2 = 2.5 V		400		mΩ
I_{lkg}	P-channel leakage current	VDCDCx = $V_{(DS)}$ = 6 V			1	µA
$r_{DS(on)}$	N-channel MOSFET on resistance	DCDC1, VINDCDC1/2 = 3.6 V		220	450	mΩ
		DCDC1, VINDCDC1/2 = 2.5 V		320		mΩ
		DCDC2, VINDCDC1/2 = 3.6 V		220	450	mΩ
		DCDC2, VINDCDC1/2 = 2.5 V		320		mΩ
I_{lkg}	N-channel leakage current	VDCDCx = $V_{(DS)}$ = 6 V		7	10	µA
$I_{(LIMF)}$	Forward current limit PMOS (High-Side) and NMOS (Low side)	DCDC1: TPS65050, TPS65054; 2.5 V ≤ VINDCDC1/2 ≤ 6 V	0.85	1	1.15	A
		DCDC1: TPS65051, TPS65052, TPS65056; 2.5 V ≤ VINDCDC1/2 ≤ 6 V	1.19	1.4	1.65	A
		DCDC2: TPS65050 - TPS65056; 2.5 V ≤ VINDCDC1/2 ≤ 6 V	0.85	1	1.15	A

Electrical Characteristics (continued)

V_{CC} = VINDCDC1/2 = 3.6 V, EN = V_{CC}, MODE = GND, L = 2.2 µH, C_O = 10 µF. T_A = -40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted).

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Thermal shutdown		Increasing junction temperature		150		°C
	Thermal shutdown hysteresis		Decreasing junction temperature		20		°C
OSCILLATOR							
f_{SW}	Oscillator frequency			2.025	2.25	2.475	MHz
OUTPUT							
V_O	Output voltage range for DCDC1, DCDC2		externally adjustable versions	0.6		VINDCDC 1/2	V
	Output voltage for DCDC1		TPS65052 and TPS65056		3.3		V
	Output voltage for DCDC2		TPS65052, TPS65054 and TPS65056		set by DEFDCDC2, see Table 3		
V_{ref}	Reference voltage		externally adjustable versions		600		mV
V_O	DC output voltage accuracy	DCDC1, DCDC2[1]	VINDCDC1/2 = 2.5 V to 6 V 0 mA < I_O = < I_O(max) Mode = GND, PFM operation	–2%	0	2%	
			VINDCDC1/2 = 2.5 V to 6 V 0 mA < I_O = < I_O(max) Mode = V_I, PWM operation	–1%	0	1%	
ΔV_O	Power save mode ripple voltage[2]		I_O = 1 mA, Mode = GND, V_O = 1.3 V, Bandwith = 20 MHz		25		mV_{PP}
t_{Start}	Start-up time		time from active EN to Start switching		170		µs
t_{Ramp}	VOUT Ramp up Time		time to ramp from 5% to 95% of V_O		750		µs
t_{RESET_DELAY}	$\overline{RESET}$ delay time		Input voltage at threshold pin rising	80	100	120	ms
t_{PB_DB}	PB-ONOFF debounce time			26	32	38	ms
V_{OL}	$\overline{RESET}$, PB_OUT output low voltage		I_{OL} = 1 mA, Vhysteresis < 1 V, Vthreshold < 1 V			0.2	V
I_{OL}	$\overline{RESET}$, PB_OUT sink current				1		mA
I_{leak}	$\overline{RESET}$, PB_OUT output leakage current		After PB_IN has been pulled high once; Vthreshold > 1 V and Vhysteresis > 1 V, V_{OH} = 6 V		10		nA
V_{th}	Vthreshold, Vhysteresis threshold			0.98	1	1.02	V
VLDO1, VLDO2, VLDO3 and VLDO4 Low Dropout Regulators							
V_I	Input voltage range for LDO1, LDO2, LDO3, LDO4			1.5		6.5	V
V_O	LDO1 output voltage range		TPS65050, TPS65052 only	1.2		3.3	V
	LDO2 output voltage range		TPS65050, TPS65052 only	1.8		3.3	
	LDO3 output voltage range		TPS65050, TPS65052 only	1.1		3.3	
	LDO4 output voltage range		TPS65050, TPS65052 only	1.2		2.85	
$V_{(FB)}$	Feedback voltage for FB_LDO1, FB_LDO2, FB_LDO3, and FB_LDO4		TPS65051, TPS65054 and TPS65056 only		1		V
I_O	Maximum output current for LDO1, LDO2			400			mA
	Maximum output current for LDO3, LDO4			200			mA
$I_{(SC)}$	LDO1 short-circuit current limit		VLDO1 = GND			750	mA
	LDO2 short-circuit current limit		VLDO2 = GND			850	mA
	LDO3 and LDO4 short-circuit current limit		VLDO3 = GND, VLDO4 = GND			420	mA
	Dropout voltage at LDO1		I_O = 400 mA, VINLDO = 3.4 V			400	mV
	Dropout voltage at LDO2		I_O = 400 mA, VINLDO = 1.8 V			280	mV
	Dropout voltage at LDO3, LDO4		I_O = 200 mA, VINLDO = 1.8 V			280	mV

(1) Output voltage specification does not include tolerance of external voltage programming resistors.
(2) In Power Save Mode, operation is typically entered at I_{PSM} = V_I / 32 Ω.

Electrical Characteristics (continued)

V_{CC} = VINDCDC1/2 = 3.6 V, EN = V_{CC}, MODE = GND, L = 2.2 µH, C_O = 10 µF. T_A = -40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{lkg}	Leakage current from VinLDOx to VLDOx	LDO enabled, VINLDO = 6.5 V, V_O = 1 V, at T_A = 140°C		3		µA
V_O	Output voltage accuracy for LDO1, LDO2, LDO3, LDO4	I_O = 10 mA	–2%		1%	
	Line regulation for LDO1, LDO2, LDO3, LDO4	VINLDO1,2 = VLDO1,2 + 0.5 V (min. 2.5 V) to 6.5V, VINLDO3,4 = VLDO3,4 + 0.5 V (minimum 2.5 V) to 6.5 V, I_O = 10 mA	–1%		1%	
	Load regulation for LDO1, LDO2, LDO3, LDO4	I_O = 0 mA to 400 mA for LDO1, LDO2 I_O = 0 mA to 200 mA for LDO3, LDO4	–1%		1%	
	Regulation time for LDO1, LDO2, LDO3, LDO4	Load change from 10% to 90%		10		µs
PSRR	Power supply rejection ratio	f = 10 kHz; I_O = 50 mA; V_I = V_O + 1 V		70		dB
$R_{(DIS)}$	Internal discharge resistor at VLDO1, VLDO2, VLDO3, VLDO4	active when LDO is disabled		350		R
	Thermal shutdown	Increasing junction temperature		140		°C
	Thermal shutdown hysteresis	Decreasing junction temperature		20		°C

7.6 Dissipation Ratings

PACKAGE	$R_{\theta JA}$ (1)	POWER RATING T_A ≤ 25°C	DERATING FACTOR ABOVE T_A = 25°C	POWER RATING T_A = 70°C	POWER RATING T_A = 85°C
RSM	58 K/W	1.7 W	17 mW/K	0.95 W	0.68 W

(1) The thermal resistance junction to case of the RSM package is 4 K/W measured on a high K board

7.7 Typical Characteristics

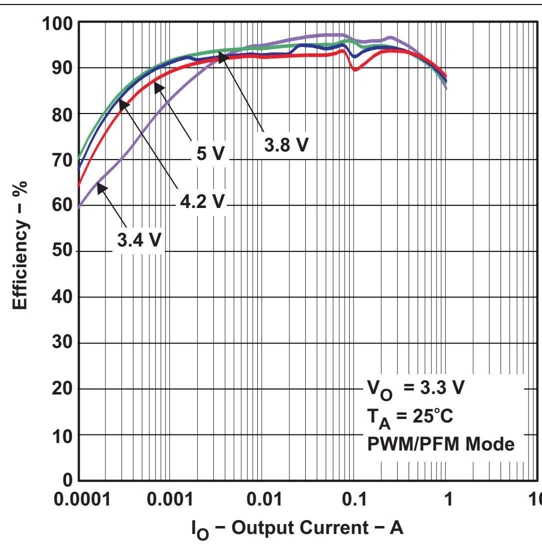


Figure 1. Efficiency vs Output Current

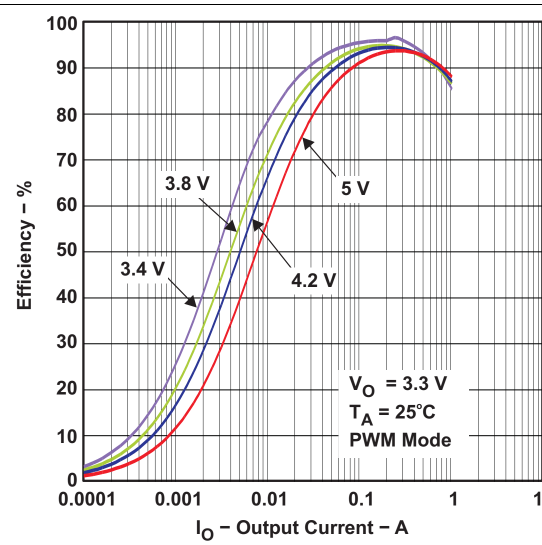


Figure 2. Efficiency vs Output Current

Typical Characteristics (continued)

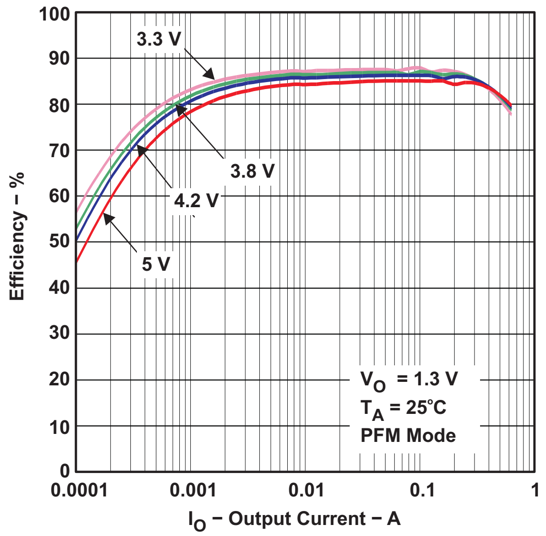


Figure 3. Efficiency vs Output Current

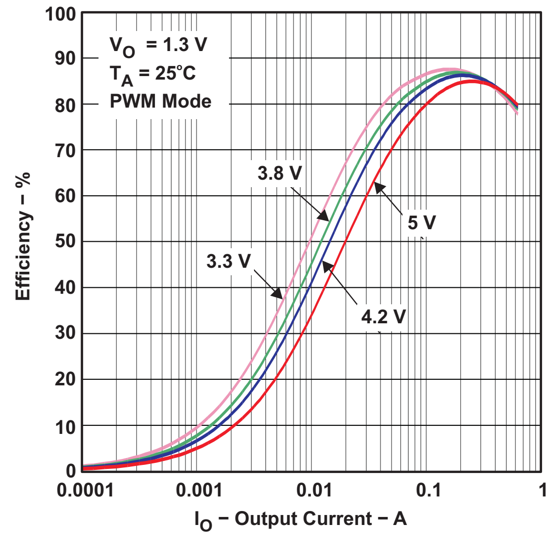


Figure 4. Efficiency vs Output Current

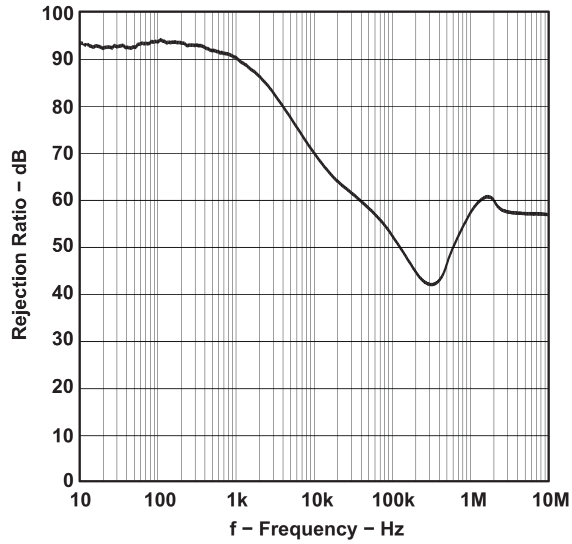


Figure 5. Power Supply Rejection Ratio vs Frequency

8 Detailed Description

8.1 Overview

The TPS6505x devices have 2 DC-DC buck converters and 4 LDOs. Each DC-DC and LDO have their own enable pins, allowing external sequence control of the PMU rails. The TPS6505x devices, (except the TPS65050 device), have a RESET feature that is generated from a THRESHOLD comparator. This RESET signal can be used to reset or warn of power shutdown to the embedded mircocontroller or processor. The TPS65050 device has a push-button feature for reset and sequence control. This feature can be used to shut down and start the converter with a single push on a button by connecting the PB_OUT output to the enable input of the converters. The TPS6505x devices make power system integration easy for a variety of embedded processors or FPGAs.

8.2 Functional Block Diagrams

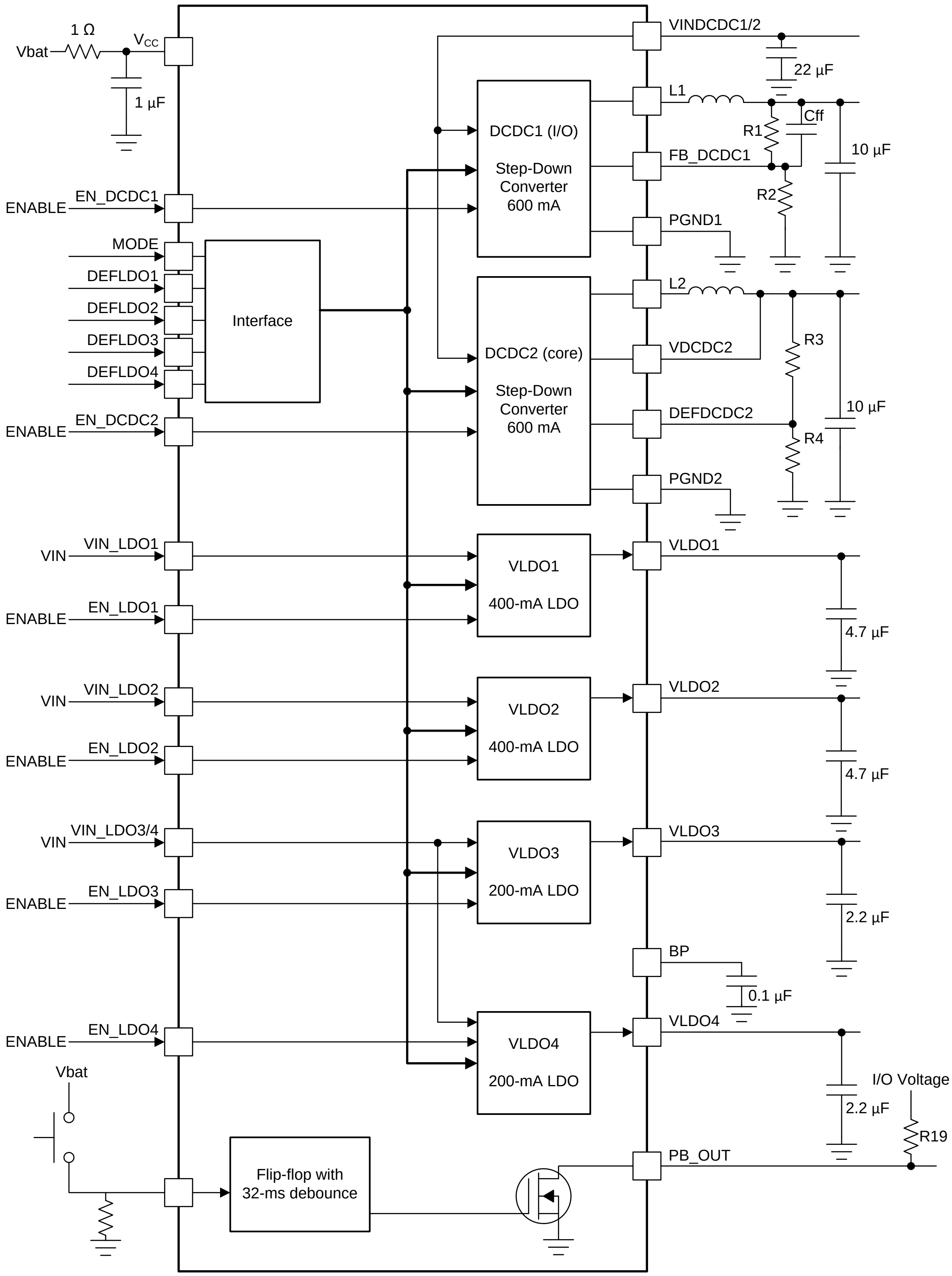


Figure 6. TPS65050 Block Diagram

Functional Block Diagrams (continued)

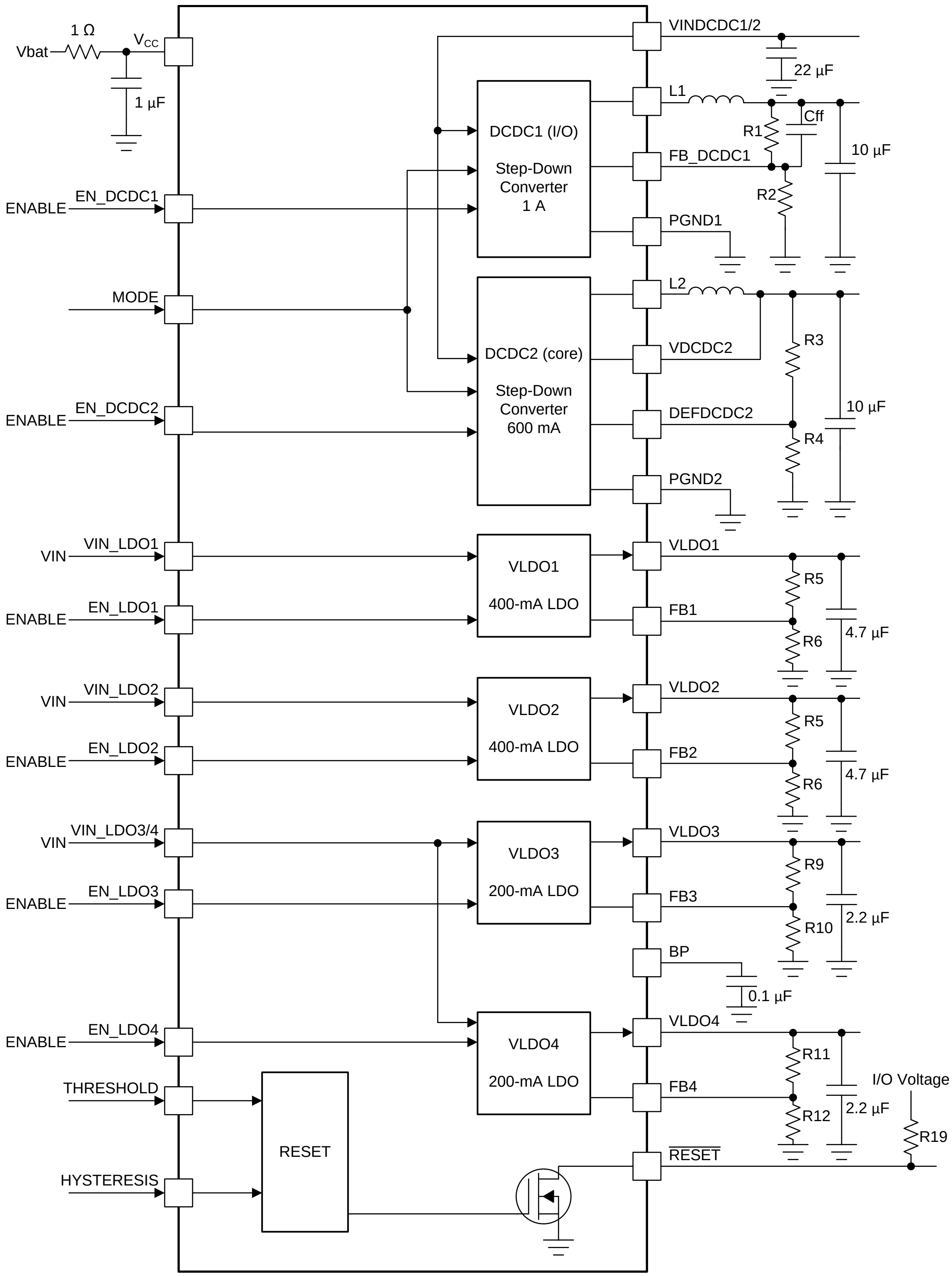


Figure 7. TPS65051 Block Diagram

Functional Block Diagrams (continued)

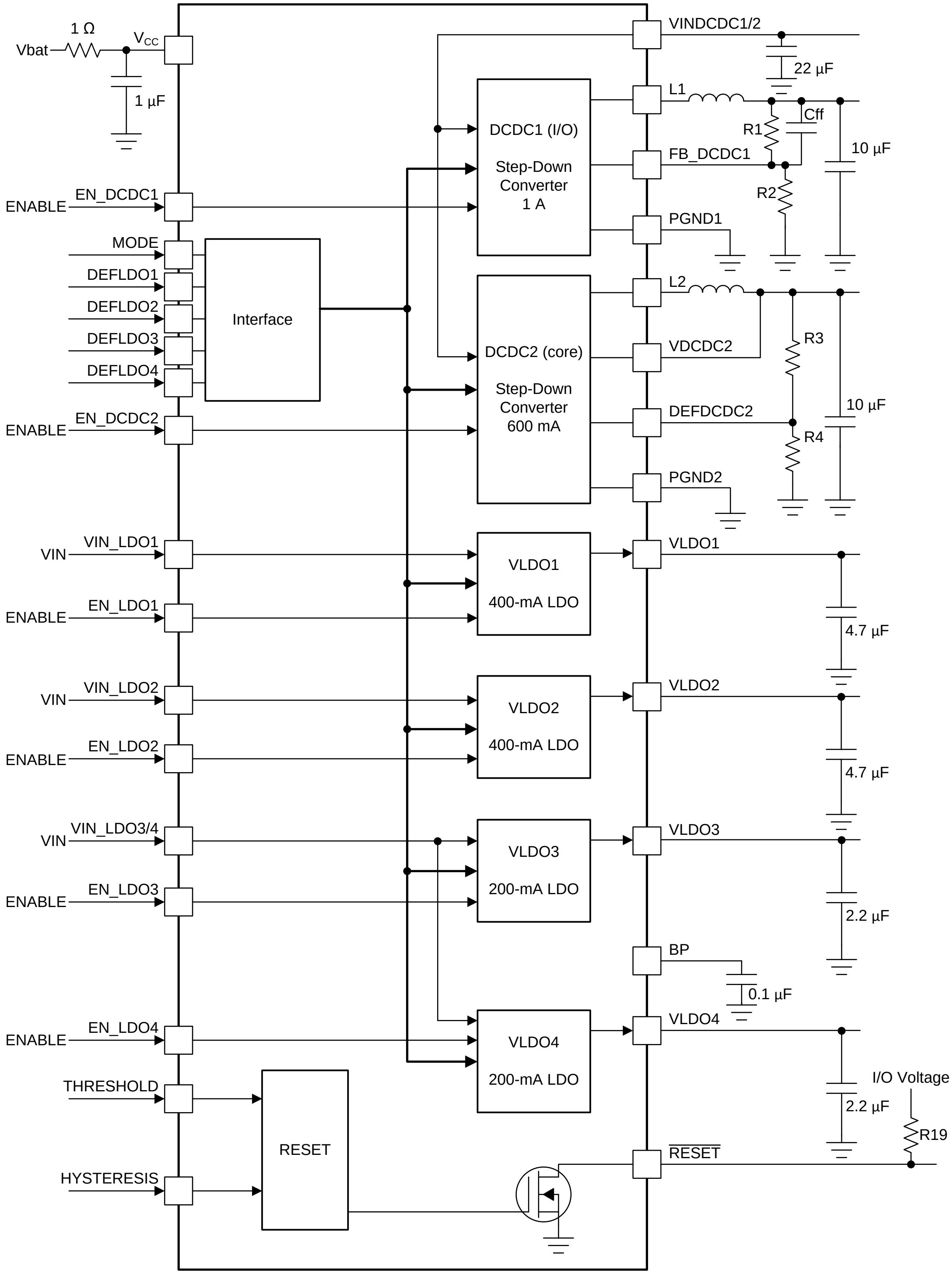


Figure 8. TPS65052 Block Diagram

Functional Block Diagrams (continued)

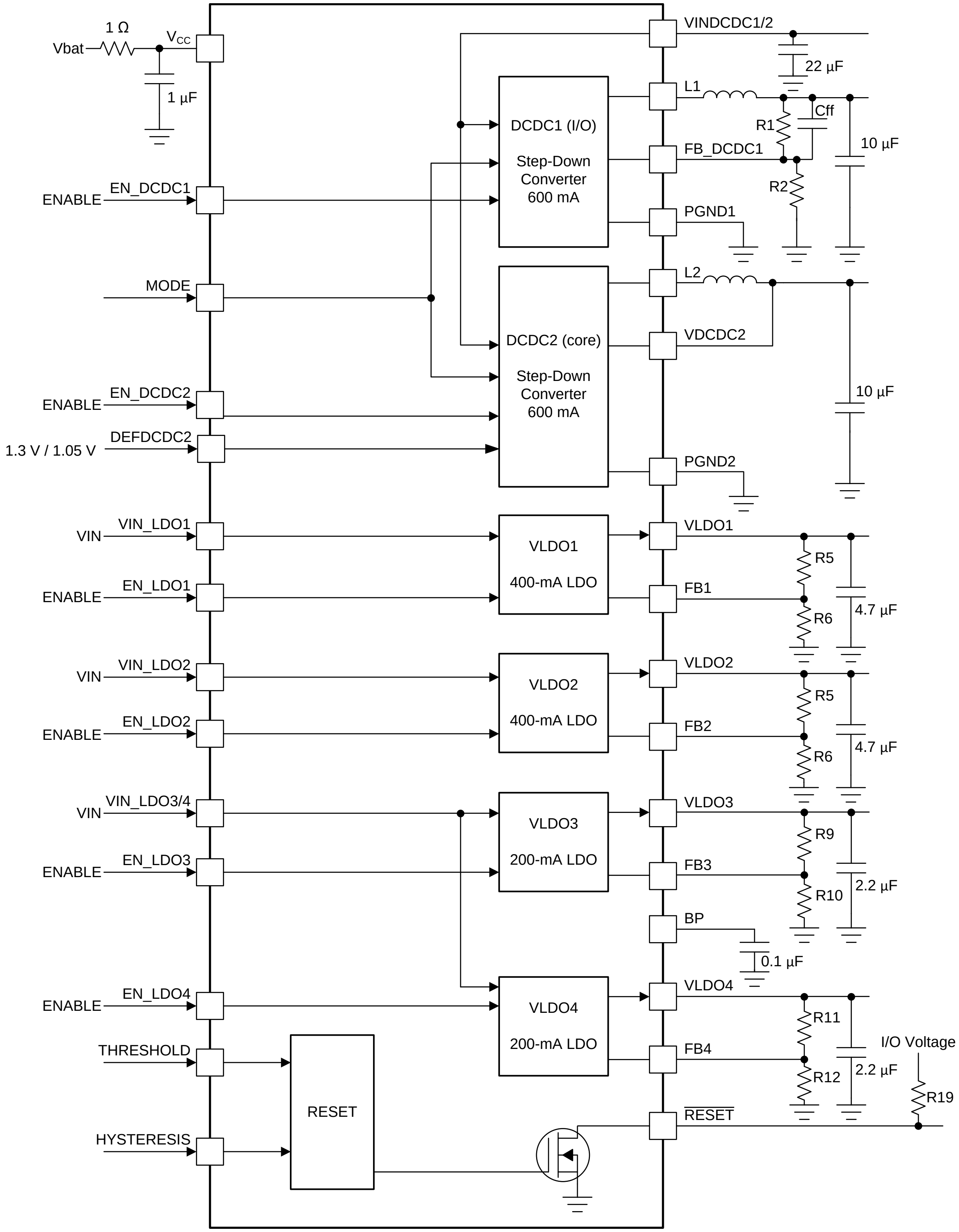


Figure 9. TPS65054 Block Diagram

Functional Block Diagrams (continued)

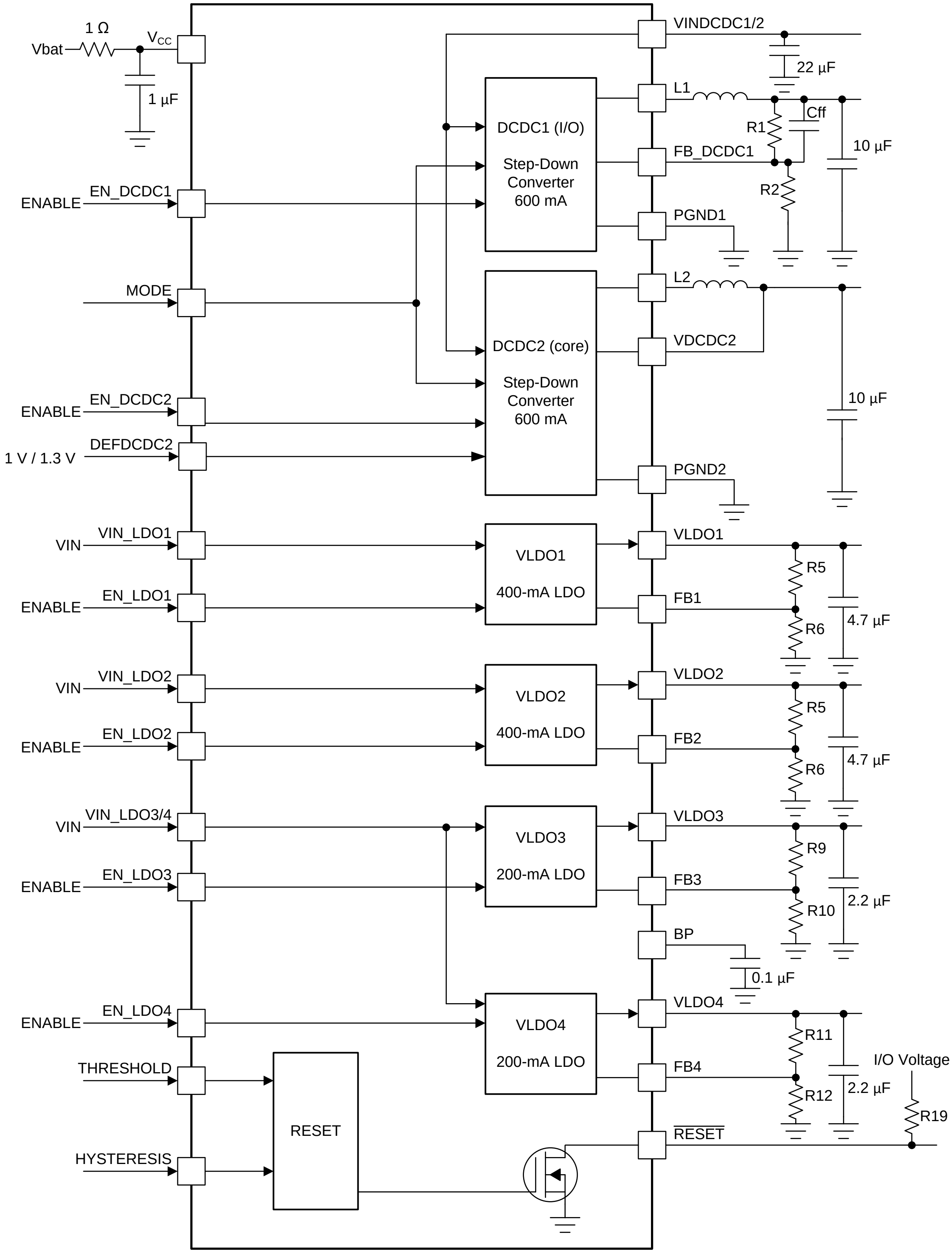


Figure 10. TPS65056 Block Diagram

8.3 Feature Description

8.3.1 Operation of DCDC Converters

The TPS6505x devices include each two synchronous step-down converters. The converters operate with 2.25-MHz (typical) fixed frequency pulse width modulation (PWM) at moderate to heavy load currents. At light load currents, the converters automatically enter Power Save Mode and operate with PFM (Pulse Frequency Modulation).

During PWM operation the converters use a unique fast response voltage mode controller scheme with input voltage feed-forward to achieve good line and load regulation allowing the use of small ceramic input and output capacitors. At the beginning of each clock cycle initiated by the clock signal, the P-channel MOSFET switch is turned on, and the inductor current ramps up until the current comparator trips, and the control logic turns off the switch. The current limit comparator turns off the switch if the current limit of the P-channel switch is exceeded. After the adaptive dead time, which prevents shoot through current, the N-channel MOSFET rectifier is turned on, and the inductor current ramps down. The next cycle is initiated by the clock signal turning off the N-channel rectifier, and turning on the on the P-channel switch.

The two DC-DC converters operate synchronized to each other, with converter 1 as the master. A 180° phase shift between converter 1 and converter 2 decreases the input RMS current. Therefore, smaller input capacitors can be used.

8.3.1.1 DCDC1 Converter

The converter 1 output voltage is set by an external resistor divider connected to FB_DCDC1 pin for the TPS65050 device, the TPS65051 device, and the TPS65054 device. For the TPS65052 device, the output voltage is fixed to 3.3 V and this pin needs to be directly connected to the output. See *Application and Implementation* for more details. The maximum output current on DCDC1 is 600 mA for the TPS65050 and TPS65054 devices. For the TPS65051 device, the TPS65052 device, and the TPS65056 device, the maximum output current is 1 A.

8.3.1.2 DCDC2 Converter

The VDCDC2 pin must be directly connected to the DCDC2 converter output voltage. The DCDC2 converter output voltage is selected through the DEFDCDC2 pin.

For the TPS65050 and TPS65051 devices, the output voltage is set with an external resistor divider. Connect the DEFDCDC2 pin to the external resistor divider.

For the TPS65052, TPS65054, and TPS65056 devices, the The DEFDCDC2 pin can either be connected to GND, or to V_{CC}. The converter 2 output voltage defaults to:

DEVICE	DEFDCDC2 = LOW	DEFDCDC2 = HIGH
TPS65052 , TPS65056	1 V	1.3 V
TPS65054	1.3 V	1.05 V

8.3.2 Power-Save Mode

The Power-Save Mode is enabled with the Mode pin set to 0. If the load current decreases, the converters enters Power-Save Mode operation automatically. During Power-Save Mode, the converters operate with reduced switching frequency in PFM mode, and with a minimum quiescent current to maintain high-efficiency. The converter positions the output voltage 1% above the nominal output voltage. This voltage positioning feature minimizes voltage drops caused by a sudden load step.

To optimize the converter efficiency at light load, the average current is monitored. If in PWM mode, the inductor current remains below a certain threshold, then Power-Save Mode is entered. The typical threshold is calculated according to Equation 1.

$$I_{(PFM\_enter)} = \frac{VINDCDC}{32\ \Omega}$$

A. Average output current threshold to enter PFM mode. (1)

$$I_{(PSMDCDC\_leave)} = \frac{VINDCDC}{24\ \Omega}$$

B. Average output current threshold to leave PFM mode. (2)

During the Power-Save Mode, the output voltage is monitored with a comparator. As the output voltage falls below the skip comparator threshold (skip comp), the P-channel switch turns on, and the converter effectively delivers a constant current. If the load is below the delivered current, the output voltage rises until the skip comp threshold is crossed again, then all switching activity ceases, reducing the quiescent current to a minimum until the output voltage has dropped below the threshold. If the load current is greater than the delivered current, the output voltage falls until it crosses the skip comparator low (Skip Comp Low) threshold set to 1% below nominal V_O, then Power-Save Mode is exited, and the converter returns to PWM mode

These control methods reduce the quiescent current to 12 μA per converter, and the switching frequency to a minimum, achieving the highest converter efficiency. The PFM mode operates with low output voltage ripple. The ripple depends on the comparator delay, and the size of the output capacitor; increasing capacitor values decreases the output ripple voltage.

The Power-Save Mode can be disabled by driving the MODE pin high. In forced PWM mode, both converters operate with fixed frequency PWM mode regardless of the load.

8.3.3 Dynamic Voltage Positioning

This feature reduces the voltage undershoots and overshoots at load steps from light to heavy load and vice versa. It is activated in Power-Save Mode operation when the converter runs in PFM Mode. It provides more headroom for both, the voltage drop at a load step and the voltage increase at a load throw-off. This improves load transient behavior.

At light loads, in which the converter operate in PFM Mode, the output voltage is regulated typically 1% greater than the nominal value. In the event of a load transient from light load to heavy load, the output voltage drops until it reaches the skip comparator low threshold set to –1% below the nominal value and enters PWM mode. During a release from heavy load to light load, the voltage overshoot is also minimized due to active regulation turning on the N-channel switch.

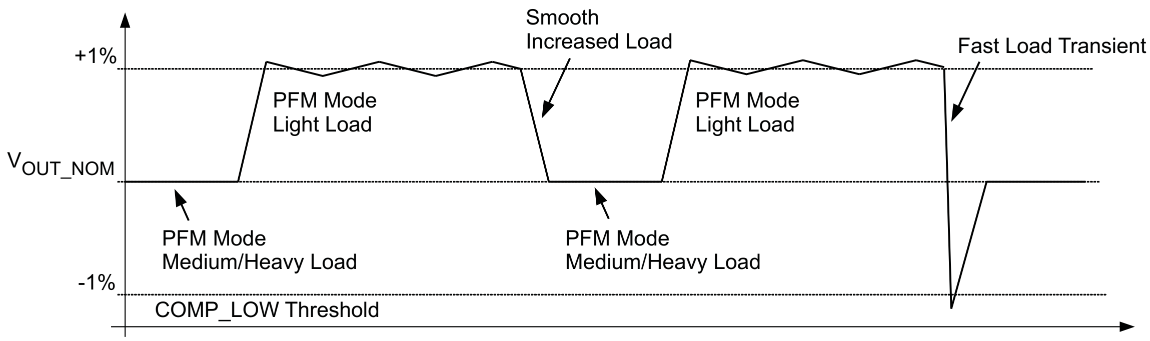


Figure 11. Dynamic Voltage Positioning

8.3.4 Soft Start

The two converters have an internal soft start circuit that limits the inrush current during start-up. During soft start, the output voltage ramp up is controlled as shown in Figure 12.

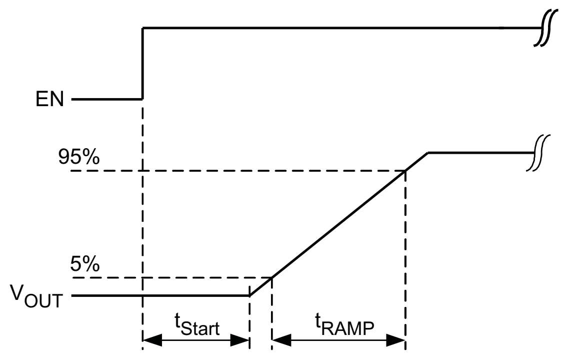


Figure 12. Soft Start

8.3.5 100% Duty Cycle Low Dropout Operation

The converters offer a low input to output voltage difference while still maintaining operation with the use of the 100% duty cycle mode. In this mode, the P-channel switch is constantly turned on. This is useful in battery-powered applications to achieve longest operation time by taking full advantage of the whole battery voltage range (that is, the minimum input voltage to maintain regulation depends on the load current and output voltage) and can be calculated using Equation 3.

$$V_I\,(min) = V_O\,(max) + I_O\,(max) \times (r_{DS(on)}\,(max) + R_L)$$

where

- I_O max = maximum output current plus inductor ripple current.
- $r_{DS(on)}$ max = maximum P-channel switch $r_{DS(on)}$.
- R_L = DC resistance of the inductor.
- V_O (max) = nominal output voltage plus maximum output voltage tolerance. (3)

8.3.6 Undervoltage Lockout

The undervoltage lockout circuit prevents the device from malfunctioning at low input voltages and from excessive discharge of the battery and disables all internal circuitry. The undervoltage lockout threshold, which is sensed at the V_{CC} pin, is typically 1.8 V, 2 V (maximum).

8.3.7 Mode Selection

The MODE pin allows mode selection between forced PWM Mode and Power-Safe Mode for both converters. Connecting this pin to GND enables the automatic PWM and power save mode operation. The converters operates in fixed frequency PWM mode at moderate to heavy loads and in the PFM mode during light loads, maintaining high-efficiency over a wide load current range.

Pulling the MODE pin high forces both converters to operate constantly in the PWM mode even at light load currents. The advantage is the converters operate with a fixed frequency that allows simple filtering of the switching frequency for noise sensitive applications. In this mode, the efficiency is lower compared to the Power-Save Mode during light loads. For additional flexibility, it is possible to switch from Power-Save Mode to forced PWM mode during operation. This allows efficient power management by adjusting the operation of the converter to the specific system requirements.

8.3.8 Enable

To start up each converter independently, the device has a separate enable pin for each DC-DC converter and for each LDO. If EN_DCDC1, EN_DCDC2, EN_LDO1, EN_LDO2, EN_LDO3, EN_LDO4 are set to high, the corresponding converter starts up with soft start as previously described.

Pulling the enable pin low forces the device into shutdown, with a shutdown quiescent current as defined in *Electrical Characteristics*. In this mode, the P and N-Channel MOSFETs are turned off, the and the entire internal control circuitry is switched off. If disabled, the outputs of the LDOs are pulled low by internal 350-Ω resistors, actively discharging the output capacitor. For proper operation, the enable pins must be terminated and must not be left unconnected.

8.3.9 RESET

The TPS65051, TPS65052, TPS65054, and TPS65056 devices contain circuitry that can generate a reset pulse for a processor with a 100-ms delay time. The input voltage at a comparator is sensed at an input called threshold. When the voltage exceeds the threshold, the output goes high with a 100-ms delay time. A hysteresis can be defined with an external resistor connected to the hysteresis input. This circuitry is functional as soon as the supply voltage at V_{CC} exceeds the undervoltage lockout threshold. Therefore, the TPS6505x devices have a shutdown current (all DC-DC converters and LDOs are off) of 9 µA to supply bandgap and comparator.

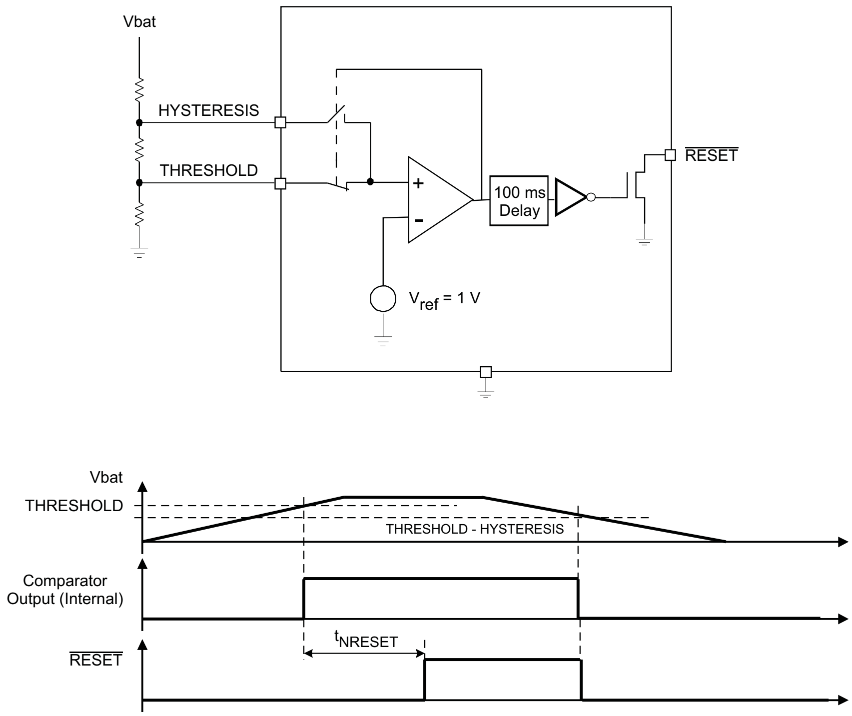


Figure 13. RESET Pulse Circuit

8.3.10 Push-Button ON-OFF (PB-ON-OFF)

The TPS65050 device provides a PB-ON-OFF functionality instead of supervising a voltage with the threshold and hysteresis inputs. The output at PB_OUT is held low after voltage is applied at V_{CC}. Only after the input at PB-IN is pulled high once, the output driver at PB_OUT goes to its inactive state, driven high with its external pullup resistor. Further low-high pulses at PB-IN toggles the status of the PB_OUT output, and can be used to shut down and start the converter with a single push on a button by connecting the PB_OUT output to the enable input of the converters.

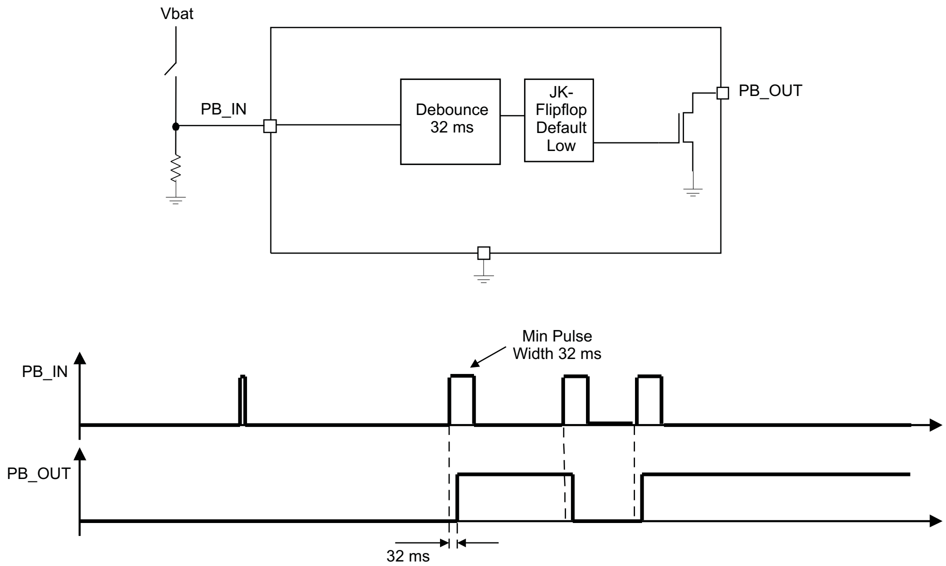


Figure 14. Push-Button Circuit

8.3.11 Short-Circuit Protection

All outputs are short-circuit protected with a maximum output current as defined in the *Electrical Characteristics*.

8.3.12 Thermal Shutdown

As soon as the junction temperature, T_J, exceeds 150°C (typically) for the DC-DC converters, the device goes into thermal shutdown. In this mode, the P and N-Channel MOSFETs are turned off. The device continues its operation when the junction temperature falls below the thermal shutdown hysteresis again. A thermal shutdown for one of the DC-DC converters disables both converters simultaneously.

The thermal shutdown temperature for the LDOs are set to typically 140°C. Therefore, a LDO, which may be used to power an external voltage, never heats up the chip high enough to turn off the DC-DC converters. If one LDO exceeds the thermal shutdown temperature, all LDOs turns off simultaneously.

8.3.13 Low Dropout Voltage Regulators

The low dropout voltage regulators are designed to operate well with small ceramic input and output capacitors. They operate with input voltages down to 1.5 V. The LDOs offer a maximum dropout voltage of 400 mV (LDO1) and 280 mV (LDO2, LDO3, and LDO4) at rated output current. Each LDO supports a current limit feature. The LDOs are enabled by the EN_LDO1, ENLDO2, EN_LDO3 and EN_LDO4 pin. In the TPS65050 and TPS65052 devices, the output voltage of the LDOs is set using 4 pins. The DEFLDO1 to DEFLDO4 pins can either be connected to GND or Vbat (V_{CC}) to define a set of output voltages for LDO1 to LDO4 according to table 1. Connecting the DEFLDOx pins to a voltage different from GND or V_{CC} causes increased leakage current into V_{CC}. In the TPS65051 and TPS65054 devices, the output voltage of the LDOs is set using external resistor dividers.

According to Table 1, The TPS65050 and TPS65052 devices default voltage options adjustable with DEFLDO4…DEFLDO1.

Table 1. Default Options

DEFLDO1	DEFLDO2	DEFLDO3	DEFLDO4	VLDO1	VLDO2	VLDO3	VLDO4
				400 mA LDO	400 mA LDO	200 mA LDO	200 mA LDO
				1.8 V to 5.5 V Input	1.8 V to 5.5 V Input	1.5 V to 5.5 V Input	1.5 V to 5.5 V Input
0	0	0	0	3.3 V	3.3 V	1.85 V	1.85 V
0	0	0	1	3.3 V	3.3 V	1.5 V	1.5 V
0	0	1	0	3.3 V	2.85 V	2.85 V	2.7 V
0	0	1	1	3.3 V	2.85 V	2.85 V	2.5 V
0	1	0	0	3.3 V	2.85 V	2.85 V	1.85 V
0	1	0	1	3.3 V	2.85 V	1.85 V	1.85 V
0	1	1	0	3.3 V	2.85 V	1.5 V	1.5 V
0	1	1	1	3.3 V	2.85 V	1.5 V	1.3 V
1	0	0	0	3.3 V	2.85 V	1.1 V	1.3 V
1	0	0	1	2.85 V	2.85 V	1.85 V	1.85 V
1	0	1	0	2.7 V	3.3 V	1.2 V	1.2 V
1	0	1	1	2.5 V	3.3 V	1.5 V	1.5 V
1	1	0	0	2.5 V	3.3 V	1.5 V	1.3 V
1	1	0	1	1.85 V	1.85 V	1.35 V	1.35 V
1	1	1	0	1.8 V	2.5 V	3.3 V	2.85 V
1	1	1	1	1.2 V	1.8 V	1.1 V	1.3 V

8.4 Device Functional Modes

The TPS6505x devices are either in the ON or the OFF mode. The OFF mode is entered when the voltage on V_{CC} is below the UVLO threshold, 1.8 V (typically). Once the voltage at V_{CC} has increased above UVLO, the device enters ON mode. In the ON mode, the DCDCs and LDOs are available for use.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

This device integrates two step-down converters and four LDOs, which can be used to power the voltage rails needed by a processor or any other application. The PMIC can be controlled through the ENABLE and MODE pins or sequenced from the VIN using RC delay circuits. There is a logic output, RESET, provide the application processor or load a logic signal indicating power good or reset.

9.2 Typical Application

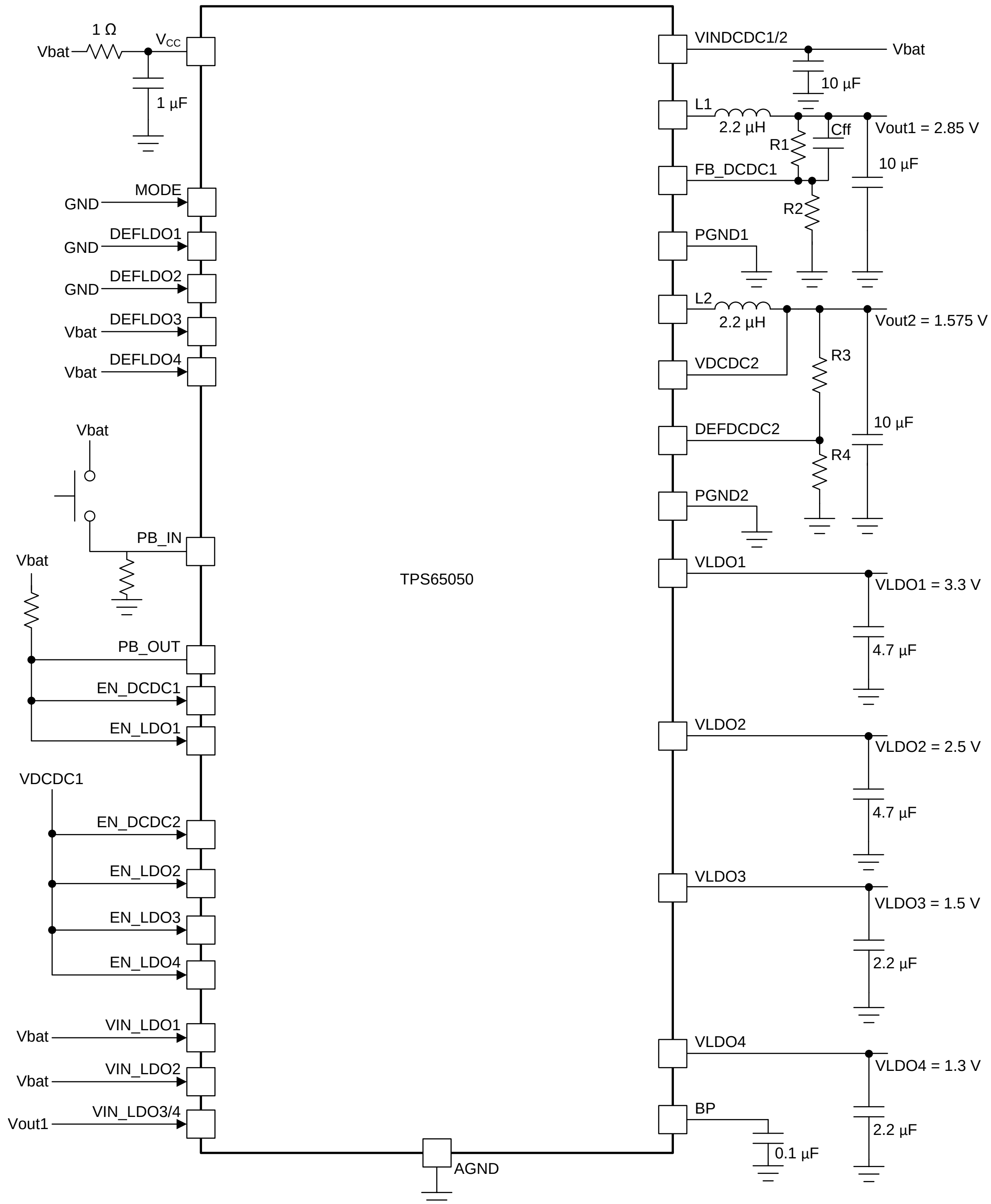


Figure 15. Typical Example Application With PB_ON/OFF Circuit

Typical Application (continued)

9.2.1 Design Requirements

Table 2 lists the design requirements for this example.

Table 2. Design Parameters

PARAMETER	VALUE
DCDC1 and DCDC2 input voltage	2.5 V to 6 V
DCDC1 output voltage	2.85 V
DCDC1 output current	600 mA
DCDC2 output voltage	1.575 V
DCDC2 output current	600 mA
LDO1 output voltage	3.3 V
LDO1 output current	400 mA
LDO2 output voltage	2.5 V
LDO2 output current	400 mA
LDO3 output voltage	1.5 V
LDO3 output current	200 mA
LDO4 output voltage	1.3 V
LDO4 output current	200 mA

9.2.2 Detailed Design Procedure

9.2.2.1 Output Voltage Setting

9.2.2.1.1 Converter 1 (DCDC1)

The output voltage of converter 1 can be set by an external resistor network. The output voltage can be calculated using Equation 4.

$$V_O = V_{ref} \times \left(1 + \frac{R1}{R2}\right) \quad (4)$$

with an internal reference voltage V_{ref}, 0.6 V .

TI recommends setting the total resistance of R1 + R2 to less than 1 MΩ. The resistor network connects to the input of the feedback amplifier, therefore, requiring a small feedforward capacitor in parallel to R1. A typical value of 47 pF is sufficient.

For the TPS65052 and TPS65056 devices, the DCDC1 output voltage is internally fixed to 3.3 V.

9.2.2.1.2 Converter 2 (DCDC2)

The output voltage of converter 2 can be selected as following:

- Adjustable output voltage defined with external resistor network on pin DEFDCDC2. This option is available for the TPS65050 and TPS65051 devices.
- Two default fixed output voltages are selectable by pin DEFDCDC2 (see Table 3). This option is available for the TPS65052, TPS65054, and TPS65056 devices.

Table 3. Default Fixed Output Voltages

Converter 2	DEFDCDC2 = low	DEFDCDC2 = high
TPS65050	—	—
TPS65051	—	—
TPS65052	1 V	1.3 V
TPS65054	1.3 V	1.05 V
TPS65056	1 V	1.3 V

The adjustable output voltage can be calculated similarly to the DCDC1 converter. Setting the total resistance of R3 + R4 to less than 1 MΩ is recommended. Route the DEFDCDC2 line separate from noise sources, such as the inductor or the L2 line. The VDCDC2 line needs to be directly connected to the output capacitor. As the VDCDC2 line is the feedback to the internal amplifier, no feedforward capacitor at R3 is needed.

Using an external resistor divider at DEFDCDC2:

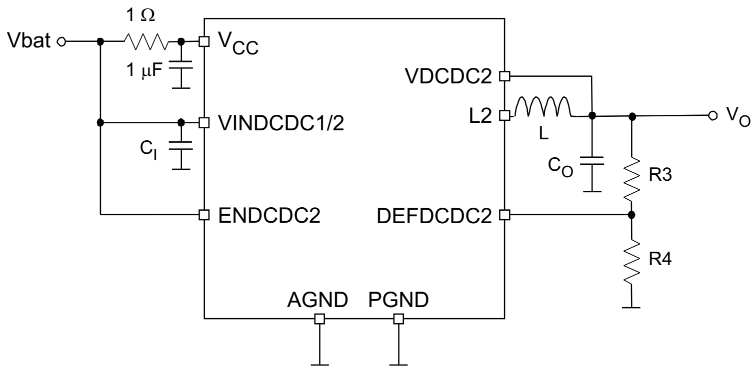


Figure 16. External Resistor Divider

$V_{(DEFDCDC2)} = 0.6\ V$

$$V_O = V_{(DEFDCDC2)} \times \frac{R3 + R4}{R4} \qquad R3 = R4 \times \left(\frac{V_O}{V_{(DEFDCDC2)}} \right) - R4 \tag{5}$$

See Table 4 for typical resistor values:

Table 4. Typical Resistor Values

OUTPUT VOLTAGE	R1	R2	NOMINAL VOLTAGE	Typical CFF
3.3 V	680 kΩ	150 kΩ	3.32 V	47 pF
3 V	510 kΩ	130 kΩ	2.95 V	47 pF
2.85 V	560 kΩ	150 kΩ	2.84 V	47 pF
2.5 V	510 kΩ	160 kΩ	2.51 V	47 pF
1.8 V	300 kΩ	150 kΩ	1.8 v	47 pF
1.6 V	200 kΩ	120 kΩ	1.6 V	47 pF
1.5 V	300 kΩ	200 kΩ	1.5 V	47 pF
1.2 V	330 kΩ	330 kΩ	1.2 V	47 pF

9.2.2.2 Output Filter Design (Inductor and Output Capacitor)

9.2.2.2.1 Inductor Selection

The two converters operate with 2.2-µH output inductor. Larger or smaller inductor values can be used to optimize the performance of the device for specific operation conditions. The selected inductor has to be rated for its DC resistance and saturation current. The DC resistance of the inductance directly influences the efficiency of the converter. Therefore, an inductor with lowest DC resistance should be selected for highest efficiency. The minimum inductor value is 1.5 µH, but an output capacitor of 22 µF minimum is needed in this case. For an output voltage above 2.8 V, TI recommends an inductor value of 3.3 µH (minimum). Lower values result in an increased output voltage ripple in PFM mode.

Use Equation 6 to calculate the maximum inductor current under static load conditions. The saturation current of the inductor should be rated greater than the maximum inductor current as calculated with Equation 6. TI recommends this because during heavy load transient the inductor current rises above the calculated value.

$$\Delta I_L = V_O \times \frac{1 - \frac{V_O}{V_I}}{L \times f} \qquad I_L(max) = I_O(max) + \frac{\Delta I_L}{2}$$

where

- f = Switching Frequency (2.25-MHz typical)
- L = Inductor Value
- ΔI_L = Peak-to-peak inductor ripple current
- $I_L$max = Maximum Inductor current (6)

The highest inductor current occurs at maximum V_I. Open core inductors have a soft saturation characteristic, and they can normally handle greater inductor currents versus a comparable shielded inductor.

A more conservative approach is to select the inductor current rating just for the maximum switch current of the corresponding converter. Consideration must be given to the difference in the core material from inductor to inductor which has an impact on the efficiency especially at high switching frequencies. See Table 5 and the typical applications for possible inductors.

Table 5. Tested Inductors

INDUCTOR TYPE	INDUCTOR VALUE	SUPPLIER
LPS3010	2.2 µH	Coilcraft
LPS3015	3.3 µH	Coilcraft
LPS4012	2.2 µH	Coilcraft
VLF4012	2.2 µH	TDK

9.2.2.2.2 Output Capacitor Selection

The advanced Fast Response voltage mode control scheme of the two converters allows the use of small ceramic capacitors with a value of 22-µF (typical) without having large output voltage undershoots and overshoots during heavy load transients. Ceramic capacitors having low ESR values result in lowest output voltage ripple, and are recommended.

If ceramic output capacitors are used, the capacitor RMS ripple current rating always meets the application requirements. For completeness, the RMS ripple current is calculated as:

$$I_{(RMSCout)} = V_O \times \frac{1 - \frac{V_O}{V_I}}{L \times f} \times \frac{1}{2 \times \sqrt{3}} \qquad (7)$$

At nominal load current, the inductive converters operate in PWM mode, and the overall output voltage ripple is the sum of the voltage spike caused by the output capacitor ESR plus the voltage ripple caused by charging and discharging the output capacitor:

$$\Delta V_O = V_O \times \frac{1 - \frac{V_O}{V_I}}{L \times f} \times \left(\frac{1}{8 \times C_O \times f} + ESR \right)$$

where

- the highest output voltage ripple occurs at the highest input voltage V_I (8)

At light load currents, the converters operate in Power-Save Mode and the output voltage ripple is dependent on the output capacitor value. The output voltage ripple is set by the internal comparator delay and the external capacitor. The typical output voltage ripple is less than 1% of the nominal output voltage.

9.2.2.2.3 Input Capacitor Selection

Because of the nature of the buck converter having a pulsating input current, a low ESR input capacitor is required for best input voltage filtering and minimizing the interference with other circuits caused by high input voltage spikes. The converters need a ceramic input capacitor of 10 μF. The input capacitor can be increased without any limit for better input voltage filtering.

Table 6. Possible Capacitors

CAPACITOR VALUE	SIZE	SUPPLIER	TYPE
2.2 μF	0805	TDK C2012X5R0J226MT	Ceramic
2.2 μF	0805	Taiyo Yuden JMK212BJ226MG	Ceramic
10 μF	0805	Taiyo Yuden JMK212BJ106M	Ceramic
10 μF	0805	TDK C2012X5R0J106M	Ceramic
10 μF	0603	Taiyo Yuden JMK107BJ106MA	Ceramic

9.2.2.3 Low Drop Out Voltage Regulators (LDOs)

The output voltage of all 4 LDOs in the TPS65051, TPS65054, and TPS65056 devices are set by an external resistor network. The output voltage is calculated using Equation 9.

$$V_O = V_{ref} \times \left(1 + \frac{R5}{R6}\right)$$

where

- an internal reference voltage, V_{ref}, 1 V (typical) (9)

TI recommends setting the total resistance of R5 + R6 to less than 1 MΩ. Typically, there is no feedforward capacitor needed at the voltage dividers for the LDOs.

$$V_O = V_{(FB\_LDOs)} \times \frac{R5 + R6}{R6} \qquad R5 = R6 \times \left(\frac{V_O}{V_{(FB\_LDOs)}}\right) - R6 \qquad (10)$$

Typical resistor values:

Table 7. Typical Resistor Values

OUTPUT VOLTAGE	R5	R6	NOMINAL VOLTAGE
3.3 V	300 kΩ	130 kΩ	3.31 V
3 V	300 kΩ	150 kΩ	3 V
2.85 V	240 kΩ	130 kΩ	2.85 V
2.8 V	360 kΩ	200 kΩ	2.8 V
2.5 V	300 kΩ	200 kΩ	2.5 V
1.8 V	240 kΩ	300 kΩ	1.8 v
1.5 V	150 kΩ	300 kΩ	1.5 V
1.3 V	36 kΩ	120 kΩ	1.3 V
1.2 V	100 kΩ	510 kΩ	1.19 V
1.1 V	33 kΩ	330 kΩ	1.1 V

9.2.2.4 PB-ONOFF and Sequencing

The PB-ONOFF output can be used to enable one or several converters. After power up, the PB_OUT pin is low, and pulls down the enable pins connected to PB_OUT; EN_DCDC1, and EN_LDO1 in Figure 15. When PB_IN is pulled to V_{CC} for longer than 32 ms, the PB_OUT pin is turned off, hence the enable pins pulled high using a pullup resistor to V_{CC}. This enables the DCDC1 converter and LDO1. The output voltage of DCDC1 (V_{OUT}1) is used as the enable signal for DCDC2 and LDO2 to LDO4. LDO1 with its output voltage of 3.3 V and LDO2 for an output voltage of 2.5 V are powered from the battery ($V_{(bat)}$) directly. To save power, the input voltage for the lower voltage rails at LDO3 and LDO4 are derived from the output of the step-down converters, keeping the voltage drop at the LDOs low to increase efficiency. As LDO3 and LDO4 are powered from the output of DCDC1, the total output current on V_{OUT}1, LDO3 and LDO4 must not exceed the maximum rating of DCDC1.

Figure 17 shows the power-up timing for this example application.

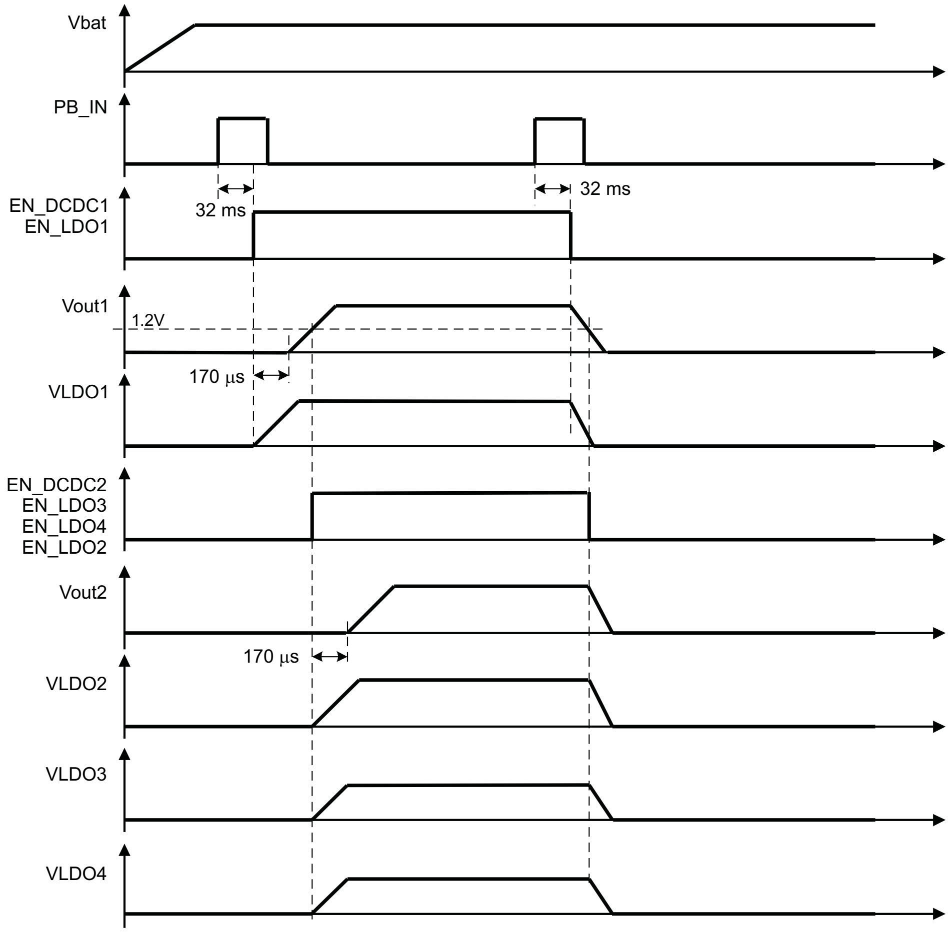


Figure 17. Example Power-up Timing

9.2.2.5 $\overline{\text{RESET}}$

The TPS65051, TPS65052, TPS65054, and TPS65056 devices contain a comparator that is used to supervise a voltage connected to an external voltage divider, and generate a reset signal if the voltage is lower than the threshold. The rising edge is delayed by 100 ms at the open-drain $\overline{\text{RESET}}$ output. The values for the external resistors R13 to R15 are calculated as follows:

V_L = lower voltage threshold (11)

V_L = lower voltage threshold (12)

V_{REF} = reference voltage (1 V) (13)

Example:

- V_L = 3.3 V
- V_H = 3.4 V

Set R15 = 100 kΩ

→ R13 + R14 = 240 kΩ

→ R14 = 3.03 kΩ

→ R13 = 237 kΩ

$$R13 + R14 = R15 \times \left(\frac{V_H}{V_{ref}} - 1 \right)$$

$$R14 = R15 \times \frac{V_H - V_L}{V_L} \quad (14)$$

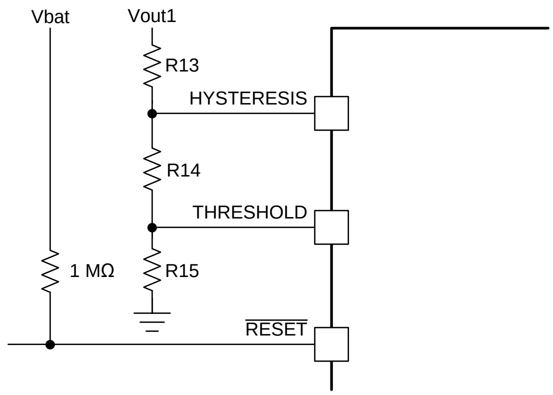


Figure 18. RESET Circuit

9.2.3 Application Curves

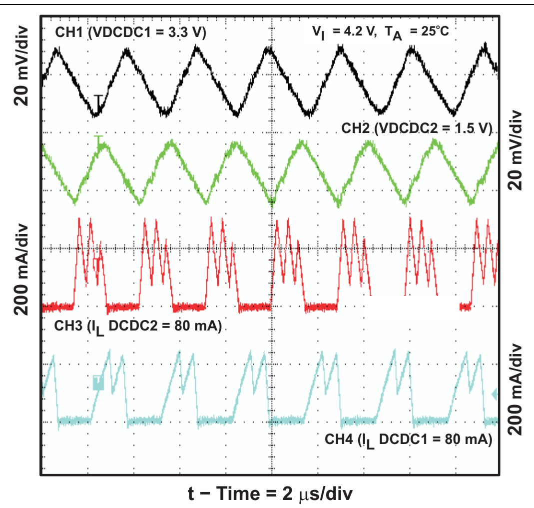


Figure 19. Output Voltage Ripple PWM/PFM Mode = LOW

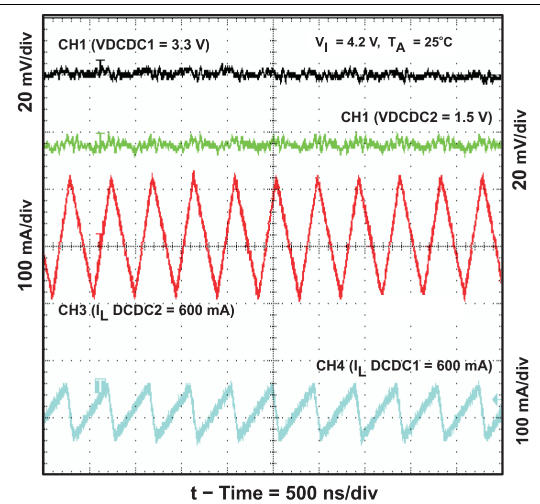


Figure 20. Output Voltage Ripple PWM Mode = HIGH

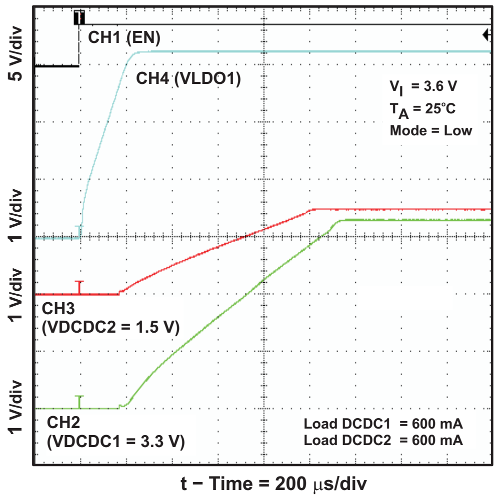


Figure 21. DCDC1 Start-up Timing

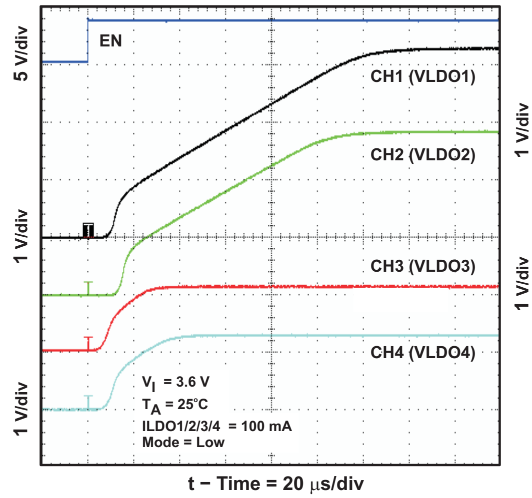


Figure 22. LDO1 to LDO4 Start-up Timing

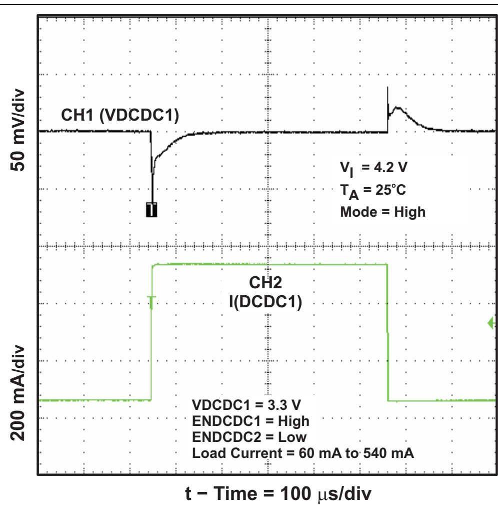


Figure 23. DCDC1 Load Transient Response

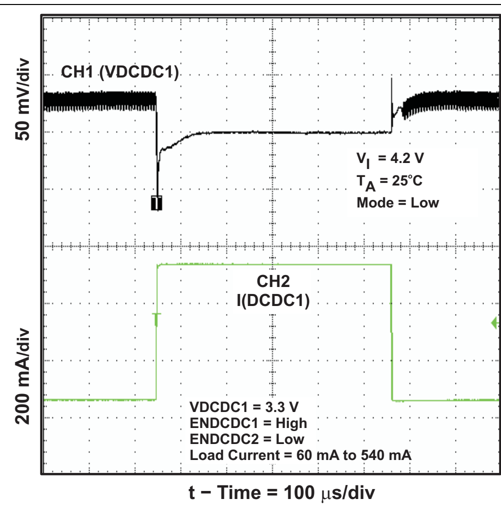


Figure 24. DCDC1 Load Transient Response

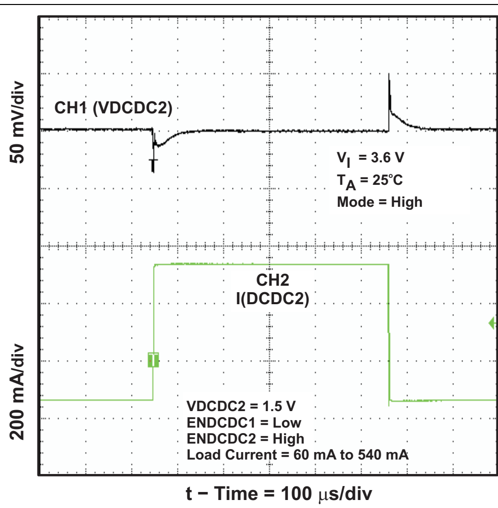


Figure 25. DCDC2 Load Transient Response

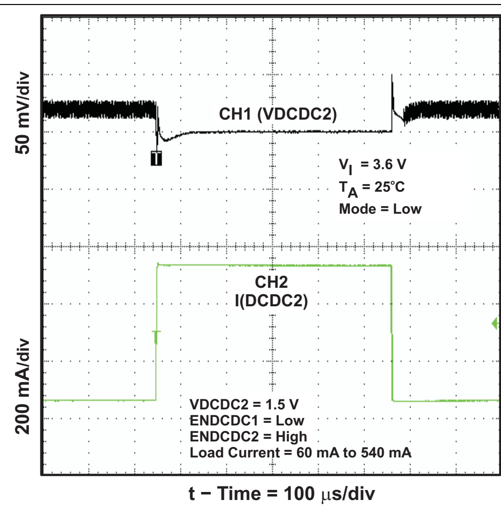


Figure 26. DCDC2 Load Transient Response

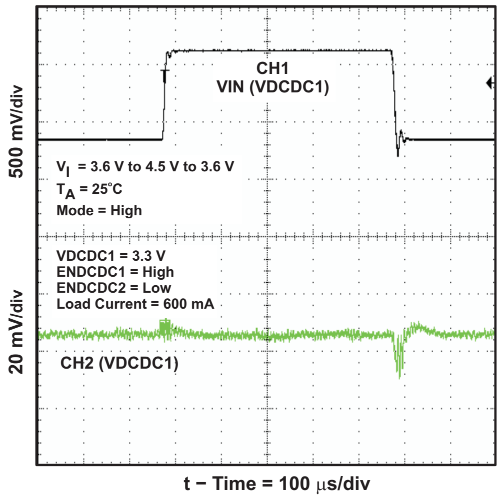


Figure 27. DCDC1 Line Transient Response

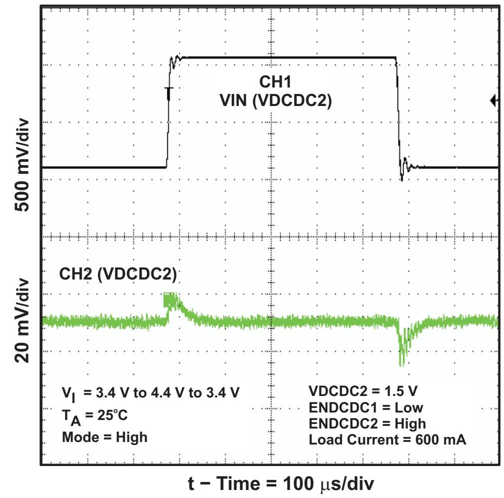


Figure 28. DCDC2 Line Transient Response

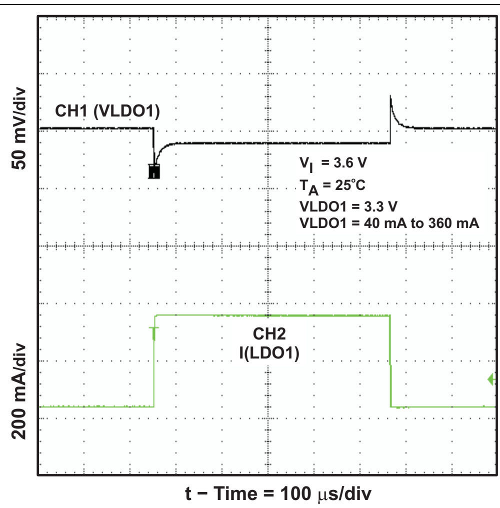


Figure 29. LDO1 Load Transient Response

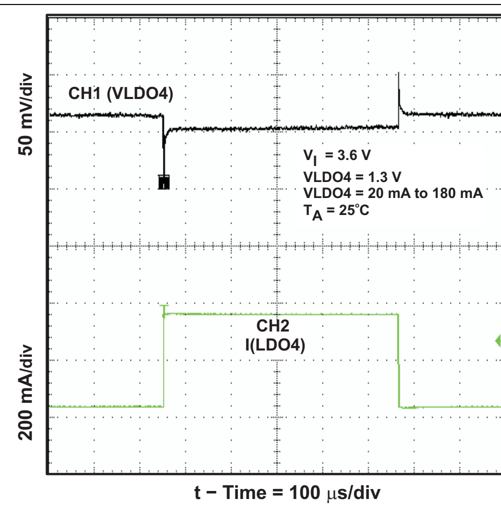


Figure 30. LDO4 Load Transient Response

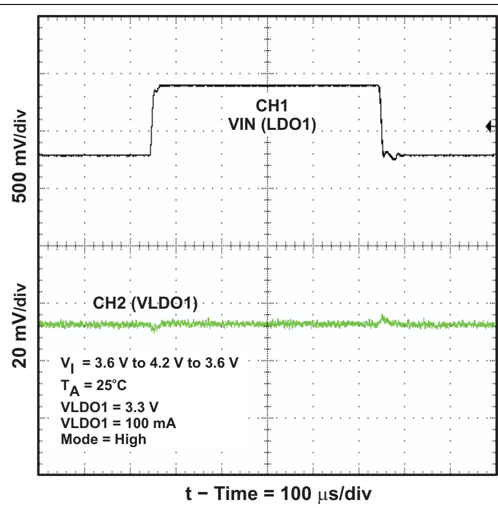


Figure 31. LDO1 Line Transient Response

10 Power Supply Recommendations

In addition to the values listed in the *Recommended Operating Conditions* table, additional recommendations for the power supply are as follows:

- 1-µF bypass capacitor on V_{CC}, located as close as possible to the V_{CC} pin to ground.
- V_{CC} and VINDCDC1/2 must be connected to the same voltage supply with minimal voltage difference.
- Input capacitors must be present on the VINDCDC1/2, VIN_LDO1, VINLDO2, and VIN_LDO3/4 supplies if used.
- Output inductor and capacitors must be used on the outputs of the DC-DC converters if used.
- Output capacitors must be used on the outputs of the LDOs if used.

11 Layout

11.1 Layout Guidelines

- The input capacitors for the DC-DC converters should be placed as close as possible to the VINDCDC1/2 pin and the PGND1 and PGND2 pins.
- The inductor of the output filter should be placed as close as possible to the device to provide the shortest switch node possible, reducing the noise emitted into the system and increasing the efficiency.
- Sense the feedback voltage from the output at the output capacitors to ensure the best DC accuracy. Feedback should be routed away from noisy sources such as the inductor. If possible route on the opposing side as the switch node and inductor and place a GND plane between the feedback and the noisy sources or keepout underneath them entirely.
- Place the output capacitors as close as possible to the inductor to reduce the feedback loop as much as possible. This will ensure best regulation at the feedback point.
- Place the device as close as possible to the most demanding or sensitive load. The output capacitors should be placed close to the input of the load. This will ensure the best AC performance possible.
- The input and output capacitors for the LDOs should be placed close to the device for best regulation performance.
- TI recommends using the common ground plane for the layout of this device. The AGND can be separated from the PGND but, a large low parasitic PGND is required to connect the PGNDx pins to the CIN and external PGND connections. If the AGND and PGND planes are separated, have one connection point to reference the grounds together. Place this connection point close to the IC.

11.2 Layout Example

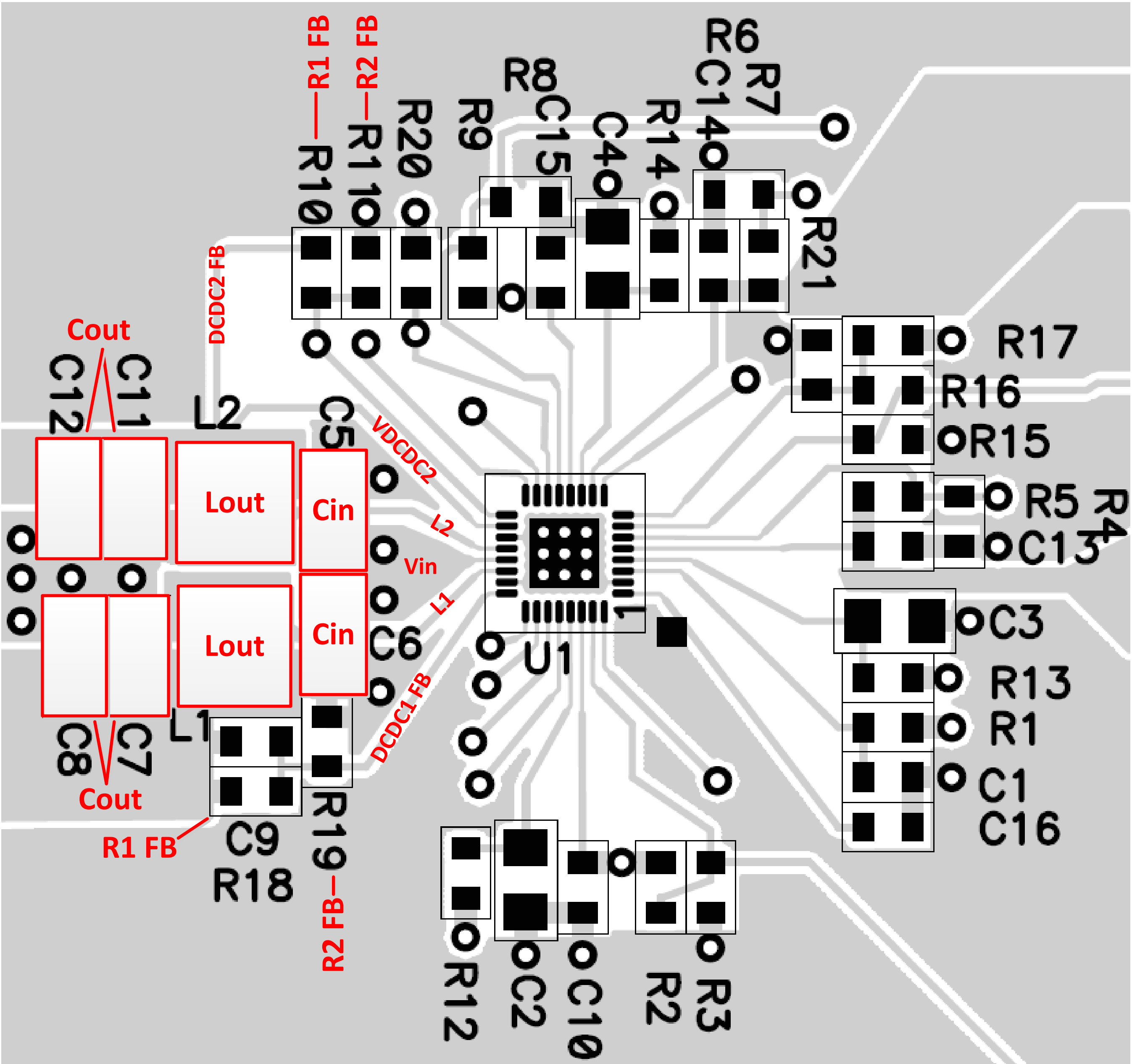


Figure 32. Layout Example from EVM for TPS6505x

12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 8. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS65050	Click here	Click here	Click here	Click here	Click here
TPS65051	Click here	Click here	Click here	Click here	Click here
TPS65052	Click here	Click here	Click here	Click here	Click here
TPS65054	Click here	Click here	Click here	Click here	Click here
TPS65056	Click here	Click here	Click here	Click here	Click here

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Community Resource

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.5 Trademarks

TMS320, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

12.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.7 Glossary

SLYZ022 — *TI Glossary*.
This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS65050RSMR	ACTIVE	VQFN	RSM	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		TPS 65050	Samples
TPS65050RSMT	ACTIVE	VQFN	RSM	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		TPS 65050	Samples
TPS65050RSMTG4	ACTIVE	VQFN	RSM	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		TPS 65050	Samples
TPS65051RSMR	ACTIVE	VQFN	RSM	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 65051	Samples
TPS65051RSMRG4	ACTIVE	VQFN	RSM	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 65051	Samples
TPS65051RSMT	ACTIVE	VQFN	RSM	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 65051	Samples
TPS65051RSMTG4	ACTIVE	VQFN	RSM	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 65051	Samples
TPS65052RSMT	ACTIVE	VQFN	RSM	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 65052	Samples
TPS65054RSMR	ACTIVE	VQFN	RSM	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 65054	Samples
TPS65054RSMT	ACTIVE	VQFN	RSM	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 65054	Samples
TPS65054RSMTG4	ACTIVE	VQFN	RSM	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 65054	Samples
TPS65056RSMR	ACTIVE	VQFN	RSM	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 65056	Samples
TPS65056RSMT	ACTIVE	VQFN	RSM	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 65056	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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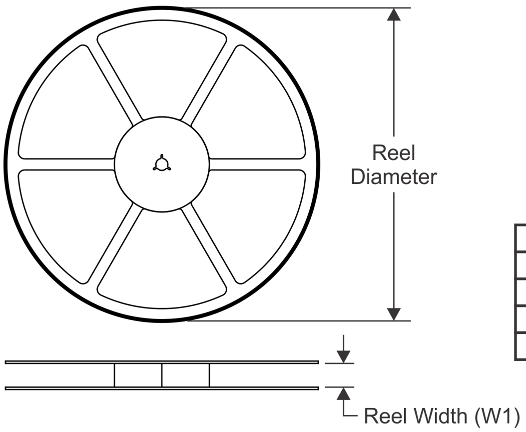
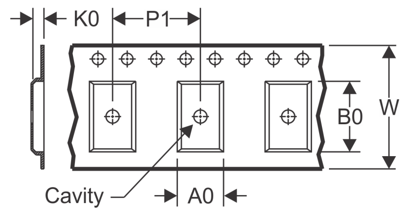
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

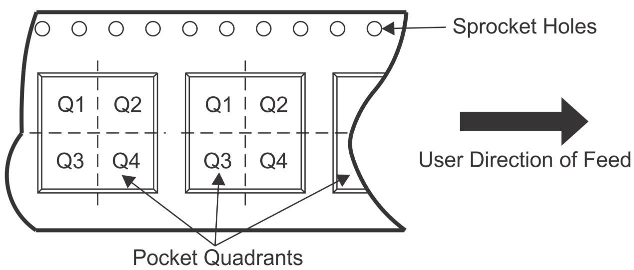


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

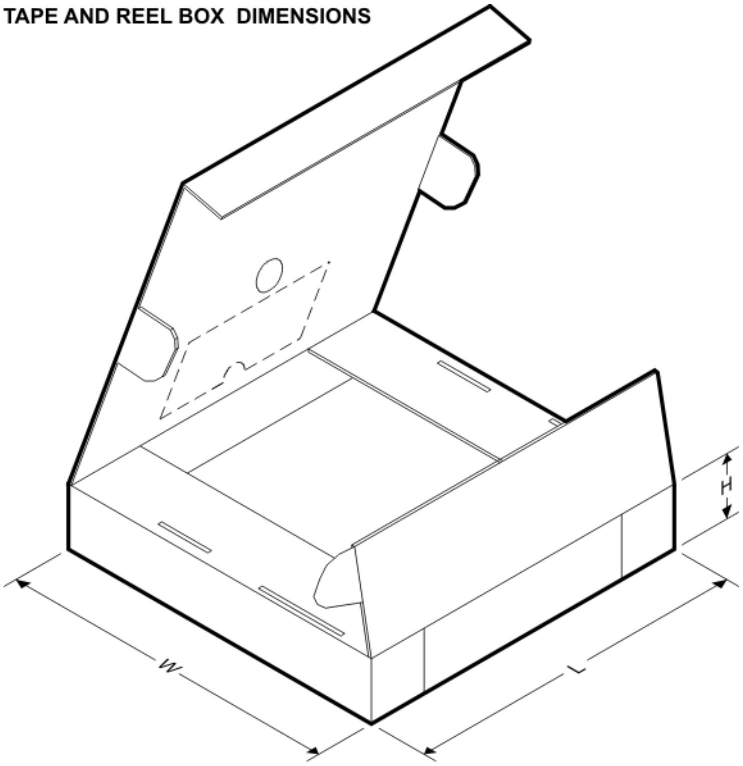
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65050RSMR	VQFN	RSM	32	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS65050RSMT	VQFN	RSM	32	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS65051RSMR	VQFN	RSM	32	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS65051RSMR	VQFN	RSM	32	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS65051RSMT	VQFN	RSM	32	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS65051RSMT	VQFN	RSM	32	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS65052RSMT	VQFN	RSM	32	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS65054RSMR	VQFN	RSM	32	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS65054RSMT	VQFN	RSM	32	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS65056RSMR	VQFN	RSM	32	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS65056RSMT	VQFN	RSM	32	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

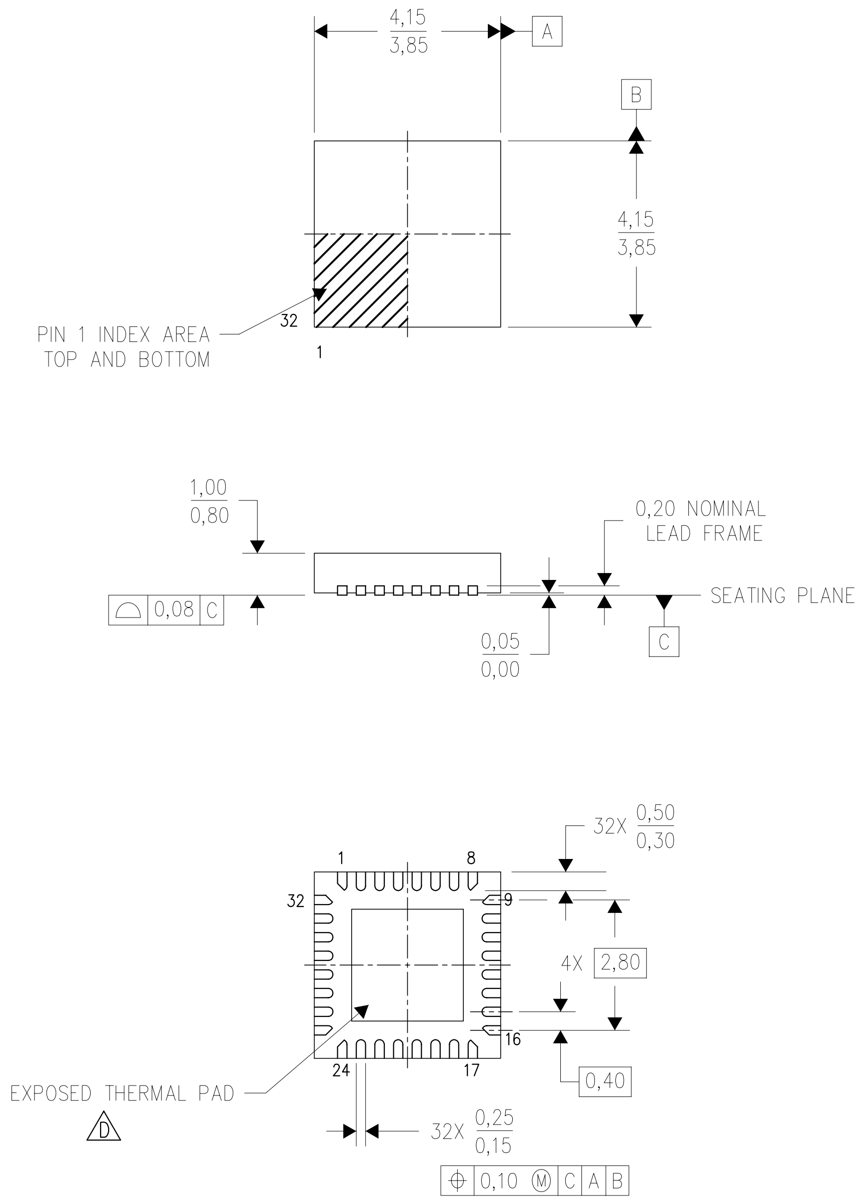
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65050RSMR	VQFN	RSM	32	3000	367.0	367.0	35.0
TPS65050RSMT	VQFN	RSM	32	250	210.0	185.0	35.0
TPS65051RSMR	VQFN	RSM	32	3000	367.0	367.0	35.0
TPS65051RSMR	VQFN	RSM	32	3000	367.0	367.0	35.0
TPS65051RSMT	VQFN	RSM	32	250	210.0	185.0	35.0
TPS65051RSMT	VQFN	RSM	32	250	210.0	185.0	35.0
TPS65052RSMT	VQFN	RSM	32	250	210.0	185.0	35.0
TPS65054RSMR	VQFN	RSM	32	3000	367.0	367.0	35.0
TPS65054RSMT	VQFN	RSM	32	250	210.0	185.0	35.0
TPS65056RSMR	VQFN	RSM	32	3000	367.0	367.0	35.0
TPS65056RSMT	VQFN	RSM	32	250	210.0	185.0	35.0

RSM (S-PVQFN-N32) PLASTIC QUAD FLATPACK NO-LEAD



4207560/B 03/10

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No−Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

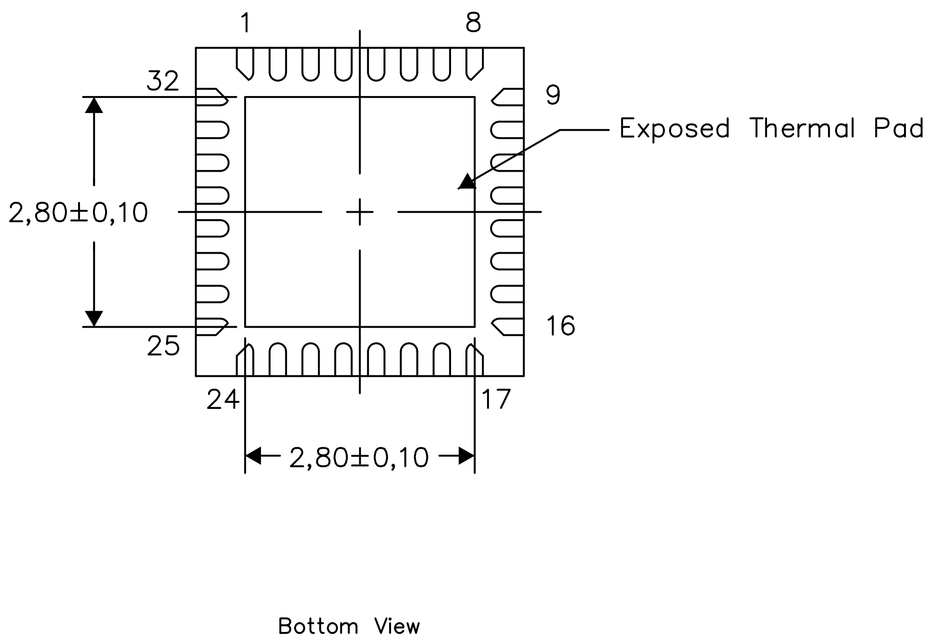
RSM (S-PVQFN-N32) PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

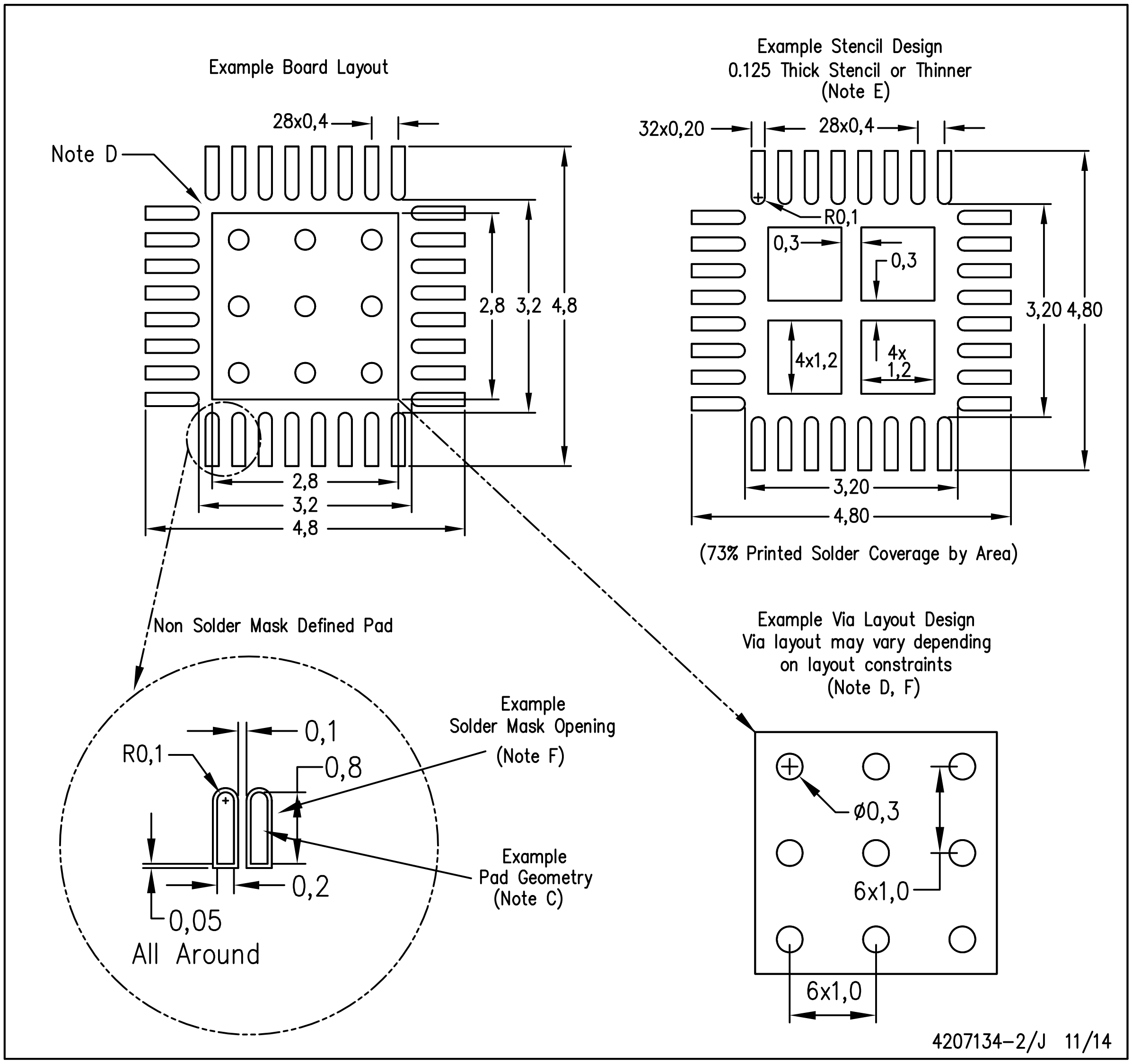


Exposed Thermal Pad Dimensions

4207868-2/I 07/14

NOTE: All linear dimensions are in millimeters

RSM (S−PVQFN−N32) PLASTIC QUAD FLATPACK NO−LEAD



NOTES:

A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC−7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat−Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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