TPS6510x Triple Output LCD Supply With Linear Regulator and VCOM Buffer

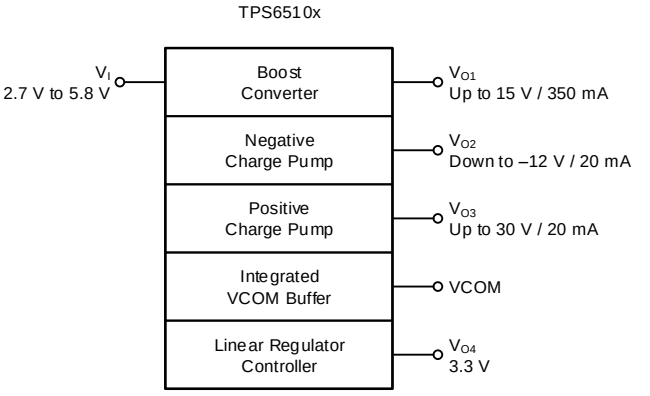
1 Features

- 2.7-V to 5.8-V Input Voltage Range
- 1.6-MHz Fixed Switching Frequency
- 3 Independent Adjustable Outputs
- Boost Converter Output Voltage V_{O1} of up to 15 V With < 1% Output Voltage Accuracy
- Negative Regulated Charge Pump V_{O2}
- Positive Charge Pump V_{O3}
- Integrated VCOM Buffer
- Virtual Synchronous Converter Technology in Boost Converter
- Auxiliary 3.3-V Linear Regulator Controller
- Internal Soft Start
- Internal Power-On Sequencing
- Fault Detection of all Outputs (TPS65100/05)
- No Fault Detection (TPS65101)
- Thermal Shutdown
- Available in TSSOP-24 and VQFN-24 PowerPAD™ Packages

2 Applications

- TFT LCD Displays for Notebooks
- TFT LCD Displays for Monitors
- Portable DVD Players
- Tablet PCs
- Car Navigation Systems
- Industrial Displays

Block Diagram



3 Description

The TPS6510x series offers a compact and small power supply solution that provides all three voltages required by thin film transistor (TFT) LCD displays. The auxiliary linear regulator controller can be used to generate a 3.3-V logic power rail for systems powered by a 5-V supply rail only.

The main output V_{O1}, is a 1.6-MHz, fixed-frequency PWM boost converter providing the source drive voltage for the LCD display. The device is available in two versions with different internal switch current limits to allow the use of a smaller external inductor when lower output power is required. The TPS65100/01 has a typical switch current limit of 2.3 A, and the TPS65105 has a typical switch current limit of 1.37 A. A fully integrated adjustable charge pump doubler/tripler provides the positive LCD gate drive voltage. An externally adjustable negative charge pump provides the negative gate drive voltage. Due to the high 1.6-MHz switching frequency of the charge pumps, inexpensive and small 220-nF capacitors can be used.

The TPS6510x series has an integrated VCOM buffer to power the LCD backplane. For LCD panels powered by 5 V only, the TPS6510x series has a linear regulator controller using an external transistor to provide a regulated 3.3-V output for the digital circuits. For maximum safety, the TPS65100/05 goes into shutdown as soon as one of the outputs is out of regulation. The device can be enabled again by toggling the input or the enable (EN) pin to GND. The TPS65101 does not enter shutdown when one of the outputs is below its power good threshold.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS6510x	HTSSOP (24)	7.80 mm × 4.40 mm
	VQFN (24)	4.00 mm × 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

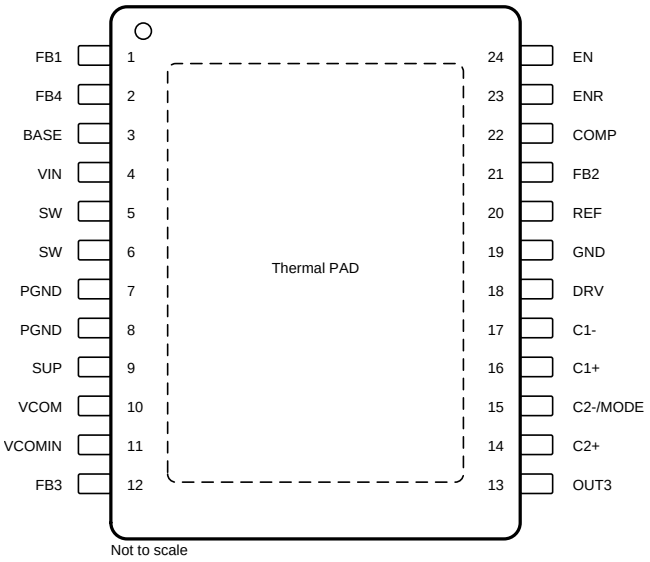
Changes from Revision C (April 2006) to Revision D	Page
• Added *ESD Ratings* table, *Thermal Information* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1
• Deleted *Ordering Information* table, see POA at the end of the datasheet.	1

5 Device Options

LINEAR REGULATOR OUTPUT VOLTAGE	MINIMUM SWITCH CURRENT LIMIT	PACKAGE MARKING
3.3 V	1.6 A	TPS65100
3.3 V	1.6 A	TPS65101
3.3 V	0.96 A	TPS65105

6 Pin Configuration and Functions

PWP Package
24-Pin HTSSOP
(Top View)



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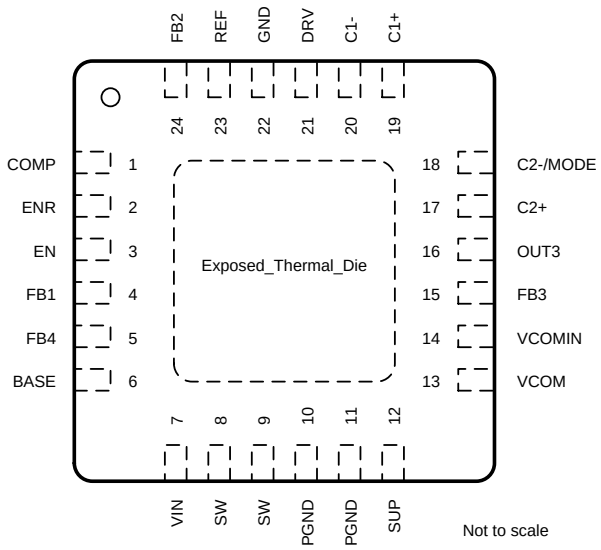
RGE Package
24-Pin VQFN
(Top View)



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Pin Functions

PIN			I/O	DESCRIPTION
NAME	HTSSOP	VQFN		
BASE	3	6	O	Base drive output for the external transistor. If Linear Regulator is not needed pull this pin against VIN.
C1+	16	19	—	Positive terminal of the charge pump flying capacitor
C1-	17	20	—	Negative terminal of the charge pump flying capacitor
C2+	14	17	—	Positive terminal for the charge pump flying capacitor. If the device runs in voltage doubler mode, this pin should be left open.
C2-/MODE	15	18	—	Negative terminal of the charge pump flying capacitor and charge pump MODE pin. If the flying capacitor is connected to this pin, the converter operates in a voltage tripler mode. If the charge pump needs to operate in a voltage doubler mode, the flying capacitor is removed and the C2-/MODE pin should be connected to GND.
COMP	22	1	—	Compensation pin for the main boost converter. A small capacitor is connected to this pin.
DRV	18	21	O	External charge pump driver
EN	24	3	I	Enable pin of the device. This pin should be terminated and not be left floating. A logic high enables the device and a logic low shuts down the device.
ENR	23	2	I	Enable pin of the linear regulator controller. This pin should be terminated and not be left floating. Logic high enables the regulator and a logic low puts the regulator in shutdown.
FB1	1	4	I	Feedback pin of the boost converter
FB2	21	24	I	Feedback pin of negative charge pump
FB3	12	15	I	Feedback pin of positive charge pump
FB4	2	5	I	Feedback pin of the linear regulator controller. The linear regulator controller is set to a fixed output voltage of 3.3 V or 3 V depending on the version.
GND	19	22	—	Ground
OUT3	13	16	O	Positive charge pump output
PGND	7, 8	10, 11	—	Power ground
REF	20	23	O	Internal reference output typically 1.23 V
SUP	9	12	I	Supply pin of the positive, negative charge pump, boost converter gate drive circuit, and VCOM buffer. This pin should be connected to the output of the main boost converter and cannot be connected to any other voltage source. For performance reasons, it is not recommended for a bypass capacitor to be connected directly to this pin.
SW	5, 6	8, 9	—	Switch pin of the boost converter
VCOM	10	13	O	VCOM buffer output
VCOMIN	11	14	I	Positive input terminal of the VCOM buffer. When the VCOM buffer is not used, this terminal can be connected to GND to reduce the overall quiescent current of the IC.
VIN	4	7	I	Input voltage pin of the device
PowerPAD™/ Thermal Die	—	—	—	The PowerPAD or exposed thermal die needs to be connected to the power ground pins (PGND)

7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Voltages on pin VIN(2)	–0.3	6	V
Voltages on pin SUP, PG (2)	–0.3	15.5	V
Voltage on pin FB1, FB2, FB3, FB4	–0.3	5.5	V
Voltages on pin EN, MODE, ENR(2)	–0.3	V_I + 0.3	V
Voltage on VCOMIN	–0.3	14	V
Voltage on pin SW(2)	–0.3	20	V
Voltage on pin DRV	–0.3	15	V
Voltage on pin REF	–0.3	4	V
Voltage on pin BASE	–0.3	5.5	V
Voltage on pin VOUT3	–0.3	30	V
Voltage on pin VCOM	–0.3	15	V
Voltage on pin C1+, C2+	–0.3	30	V
Voltage on pin C1–, C2–	–0.3	15	V
Continuous power dissipation	See *Dissipation Ratings*		
Operating junction temperature, T_J	–40	150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_I	Input voltage	2.7		5.8	V
L	Inductor(1)		4.7		µH
T_A	Operating free-air temperature	–40		85	°C
T_J	Operating junction temperature	–40		125	°C

(1) See the *Detailed Design Procedure* for further information.

7.4 Thermal Information

THERMAL METRIC[1]		TPS6510x		UNIT
		PWP (HTSSOP)	RGE (VQFN)	
		24 PINS	24 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	37.2	33	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	18.9	35.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	16.4	10.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.4	0.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	16.2	10.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.1	1.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

V_I = 3.3 V, EN = V_I, V_{O1} = 10 V, T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
V_I	Input voltage range		2.7		5.8	V
$I_{I(VIN)}$	Quiescent current (VIN)	ENR = VCOMIN = GND, V_{O3} = 2 × V_{O1} Boost converter not switching		0.7	0.9	mA
$I_{I(QCharge)}$	Charge pump quiescent current (SUP)	V_{O1} = SUP = 10 V, V_{O3} = 2 × V_{O1}		1.7	2.7	mA
		V_{O1} = SUP = 10 V, V_{O3} = 3 × V_{O1}		3.9	6	
$I_{I(QVCOM)}$	VCOM quiescent current (SUP)	ENR = GND, V_{O1} = SUP = 10 V		750	1300	µA
$I_{I(QEN)}$	LDO controller quiescent current (VIN)	ENR = V_I, EN = GND		300	800	µA
$I_{I(sd)}$	Shutdown current (VIN)	EN = ENR = GND		1	10	µA
V_{IT-}	Undervoltage lockout threshold	V_I falling		2.2	2.4	V
	Thermal shutdown temperature threshold	T_J rising		160		°C
LOGIC SIGNALS						
V_{IH}	High-level input voltage (EN, ENR)		1.5			V
V_{IL}	Low-level input voltage (EN, ENR)				0.4	V
I_{IH} , I_{IL}	Input leakage current	EN = ENR = GND or V_I		0.01	0.1	µA
MAIN BOOST CONVERTER V_{O1}						
V_{O1}	Output voltage range		5		15	V
$V_{O1} – V_I$	Minimum input to output voltage difference		1			V
$V_{(REF)}$	Reference output voltage (REF)		1.205	1.213	1.219	V
V_{ref}	Feedback regulation voltage (FB1)		1.136	1.146	1.154	V
I_{IB}	Feedback input bias current			10	100	nA
$r_{DS(on)}$	N-MOSFET on-resistance (Q1)	V_{O1} = 10 V, $I_{(sw)}$ = 500 mA		195	290	mΩ
		V_{O1} = 5 V, $I_{(sw)}$ = 500 mA		285	420	
I_{LIM}	N-MOSFET switch current limit (Q1)	TPS65100, TPS65101	1.6	2.3	2.6	A
		TPS65105	0.96	1.37	1.56	A
$r_{DS(on)}$	P-MOSFET on-resistance (Q2)	V_{O1} = 10 V, $I_{(sw)}$ = 100 mA		9	15	Ω
		V_{O1} = 5 V, $I_{(sw)}$ = 100 mA		14	22	

Electrical Characteristics (continued)

V_I = 3.3 V, EN = V_I, V_{O1} = 10 V, T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Maximum P-MOSFET peak switch current				1	A
$I_{(SW)(off)}$	Off-state current (SW)	$V_{(sw)}$ = 15 V		1	10	µA
f_{OSC}	Oscillator frequency	0°C ≤ T_A ≤ 85°C	1.295	1.6	2.1	MHz
		–40°C ≤ T_A ≤ 85°C	1.191	1.6	2.1	
$\Delta V_{O(\Delta VI)}$	Line regulation	2.7 V ≤ V_I ≤ 5.7 V, I_{load} = 100 mA		0.012		%/V
$\Delta V_{O(\Delta IO)}$	Load regulation	0 mA ≤ I_O ≤ 300 mA		0.2		%/A
NEGATIVE CHARGE PUMP V_{O2}						
V_{O2}	Output voltage range		–2			V
$V_{(REF)}$	Reference output voltage (REF)		1.205	1.213	1.219	V
V_{ref}	Feedback regulation voltage (FB2)		–36	0	36	mV
I_{IB}	Feedback input bias current			10	100	nA
$r_{DS(on)}$	Q8 P-Channel switch $r_{DS(ON)}$	I_O = 20 mA		4.3	8	Ω
	Q9 N-Channel switch $r_{DS(ON)}$			2.9	4.4	
I_{OM}	Maximum output current		20			mA
$\Delta V_{O(\Delta VI)}$	Line regulation	7 V ≤ V_{O1} ≤ 15 V, I_O = 10 mA, V_{O2} = –5 V		0.09		%/V
$\Delta V_{O(\Delta IO)}$	Load regulation	1 mA ≤ I_O ≤ 20 mA, V_{O2} = –5 V		0.126		%/mA
POSITIVE CHARGE PUMP V_{O3}						
V_{O3}	Output voltage range				30	V
$V_{(REF)}$	Reference output voltage		1.205	1.213	1.219	V
V_{ref}	Feedback regulation voltage (FB3)		1.187	1.214	1.238	V
I_{IB}	Feedback input bias current			10	100	nA
$r_{DS(on)}$	Q3 P-Channel switch $r_{DS(on)}$	I_O = 20 mA		9.9	15.5	Ω
	Q4 N-Channel switch $r_{DS(on)}$			1.1	1.8	
	Q5 P-Channel switch $r_{DS(on)}$			4.6	8.5	
	Q6 N-Channel switch $r_{DS(on)}$			1.2	2.2	
V_d	D1 – D4 Shottky diode forward voltage	$I_{(D1-D4)}$ = 40 mA		610	720	mV
I_{OM}	Maximum output current		20			mA
$\Delta V_{O(\Delta VI)}$	Line regulation	10 V ≤ V_{O1} ≤ 15 V, I_O = 10 mA, V_{O3} = 27 V		0.56		%/V
$\Delta V_{O(\Delta IO)}$	Load regulation	1 mA ≤ I_O ≤ 20 mA, V_{O3} = 27 V		0.05		%/mA
LINEAR REGULATOR CONTROLLER V_{O4}						
V_{O4}	Output voltage range (FB4)	4.5 V ≤ V_I ≤ 5.5 V, 10 mA ≤ I_O ≤ 500 mA	3.2	3.3	3.4	V
$I_{(BASE)}$	Maximum base drive current	V_I – V_{O4} – V_{BE} ≥ 0.5 V (1)	13.5	19		mA
		V_I – V_{O4} – V_{BE} ≥ 0.75 V (1)	20	27		
$\Delta V_{O(\Delta VI)}$	Line regulation	4.75 V ≤ V_I ≤ 5.5 V, I_O = 500 mA		0.186		%/V
$\Delta V_{O(\Delta IO)}$	Load regulation	1 mA ≤ I_O ≤ 500 mA, V_I = 5 V		0.064		%/A
	Start-up current	V_{O4} ≤ 0.8 V	11	20	25	mA
VCOM BUFFER						
V_{cm}	Common mode input range		2.25		V_{O1}-2	V
V_{Io}	Input offset voltage (IN)	I_O = 0 mA	–25		25	mV

(1) With V_I = supply voltage of the TPS6510x, V_O4 = output voltage of the regulator, V_{BE} = basis emitter voltage of external transistor

Electrical Characteristics (continued)

V_I = 3.3 V, EN = V_I, V_{O1} = 10 V, T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\Delta V_{O(\Delta IO)}$	DC Load regulation	I_O = ±25 mA	–30		37	mV
		I_O = ±50 mA	–45		55	
		I_O = ±100 mA	–72		85	
		I_O = ±150 mA	–97		110	
I_{IB}	Input bias current (IN)		–300	–30	300	nA
I_{OM}	Peak output current	V_{O1} = 15 V	1.2			A
		V_{O1} = 10 V	0.65			A
		V_{O1} = 5 V	0.15			A
FAULT PROTECTION THRESHOLDS						
$V_{(th,\ VO1)}$	Shutdown threshold	V_{O1} Rising	–12% V_{O1}	–8.75% V_{O1}	–6 V_{O1}	V
$V_{(th,\ VO2)}$		V_{O2} Rising	–13 V_{O2}	–9% V_{O2}	–5 V_{O2}	V
$V_{(th,\ VO3)}$		V_{O3} Rising	–11 V_{O3}	–8% V_{O3}	–5 V_{O3}	V

7.6 Dissipation Ratings

PACKAGE	$R\Theta_{JA}$	$T_A \le 25°C$ POWER RATING	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
24-Pin TSSOP	30.13 C°/W (PWP soldered)	3.3 W	1.83 W	1.32 W
24-Pin VQFN	30 C°/W	3.3 W	1.8 W	1.3 W

7.7 Typical Characteristics

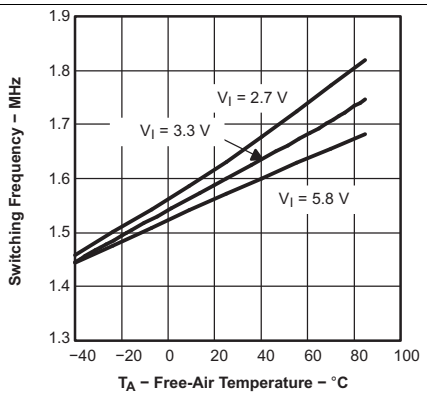


Figure 1. Switching Frequency vs Free-Air Temperature

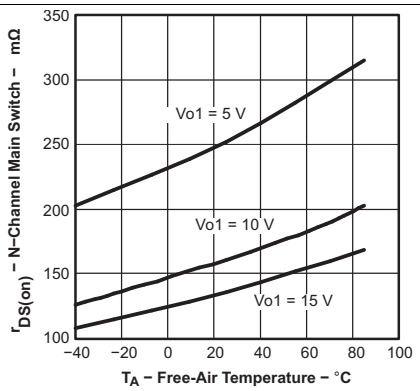


Figure 2. rDS(on) N-Channel Main Switch vs Free-Air Temperature

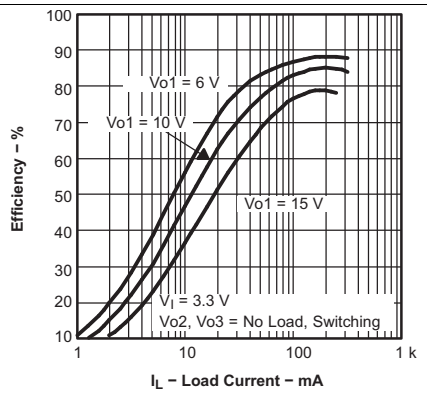


Figure 3. Efficiency vs Load Current

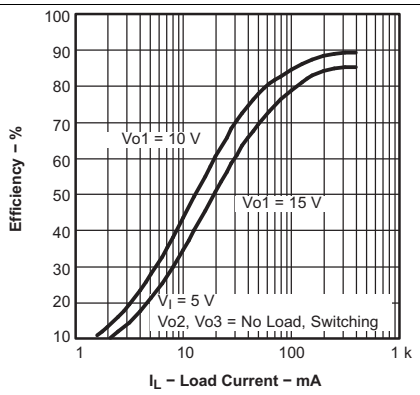


Figure 4. Efficiency vs Load Current

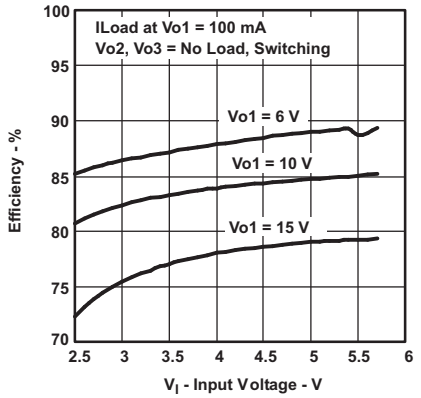


Figure 5. Efficiency vs Input Voltage

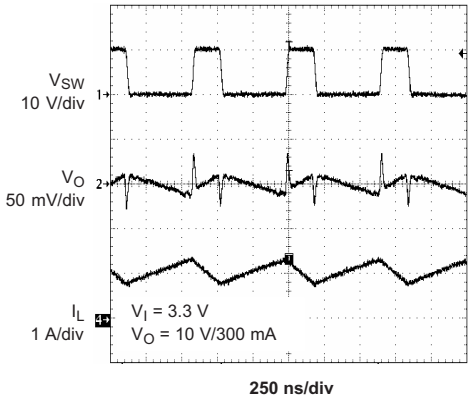


Figure 6. PWM Operation Continuous Mode

Typical Characteristics (continued)

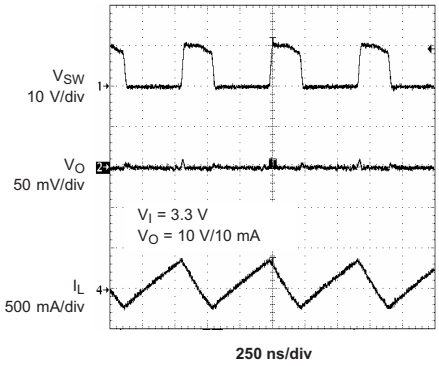


Figure 7. PWM Operation at Light Load

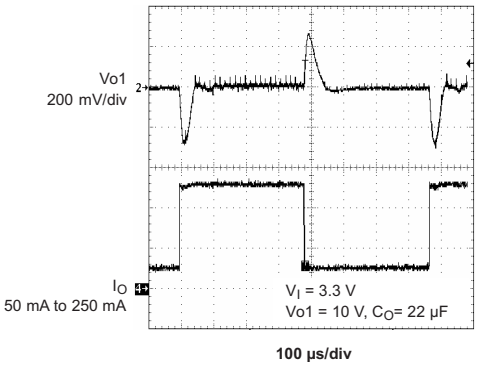


Figure 8. Load Transient Response

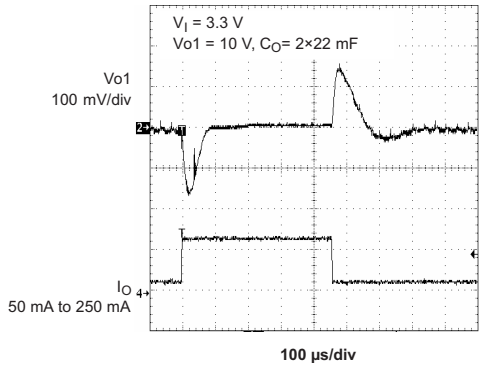


Figure 9. Load Transient Response

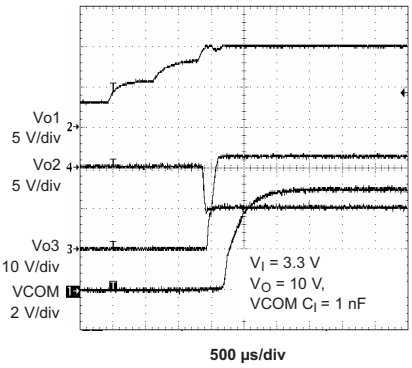


Figure 10. Power-Up Sequencing

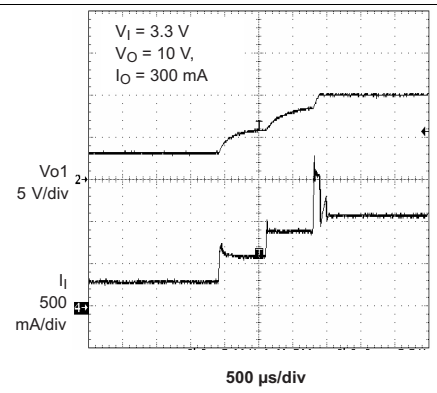


Figure 11. Soft Start VO1

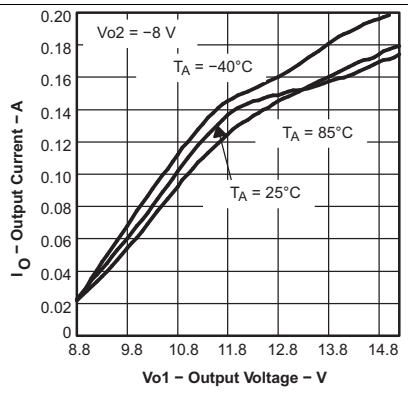


Figure 12. VO2 Maximum Load Current

Typical Characteristics (continued)

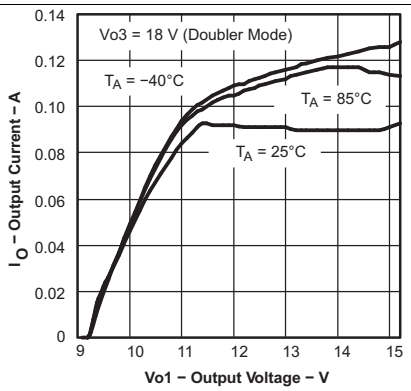


Figure 13. VO3 Maximum Load Current

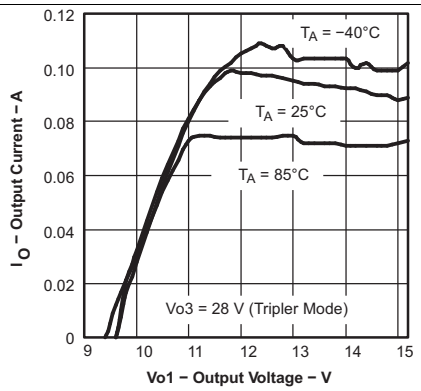


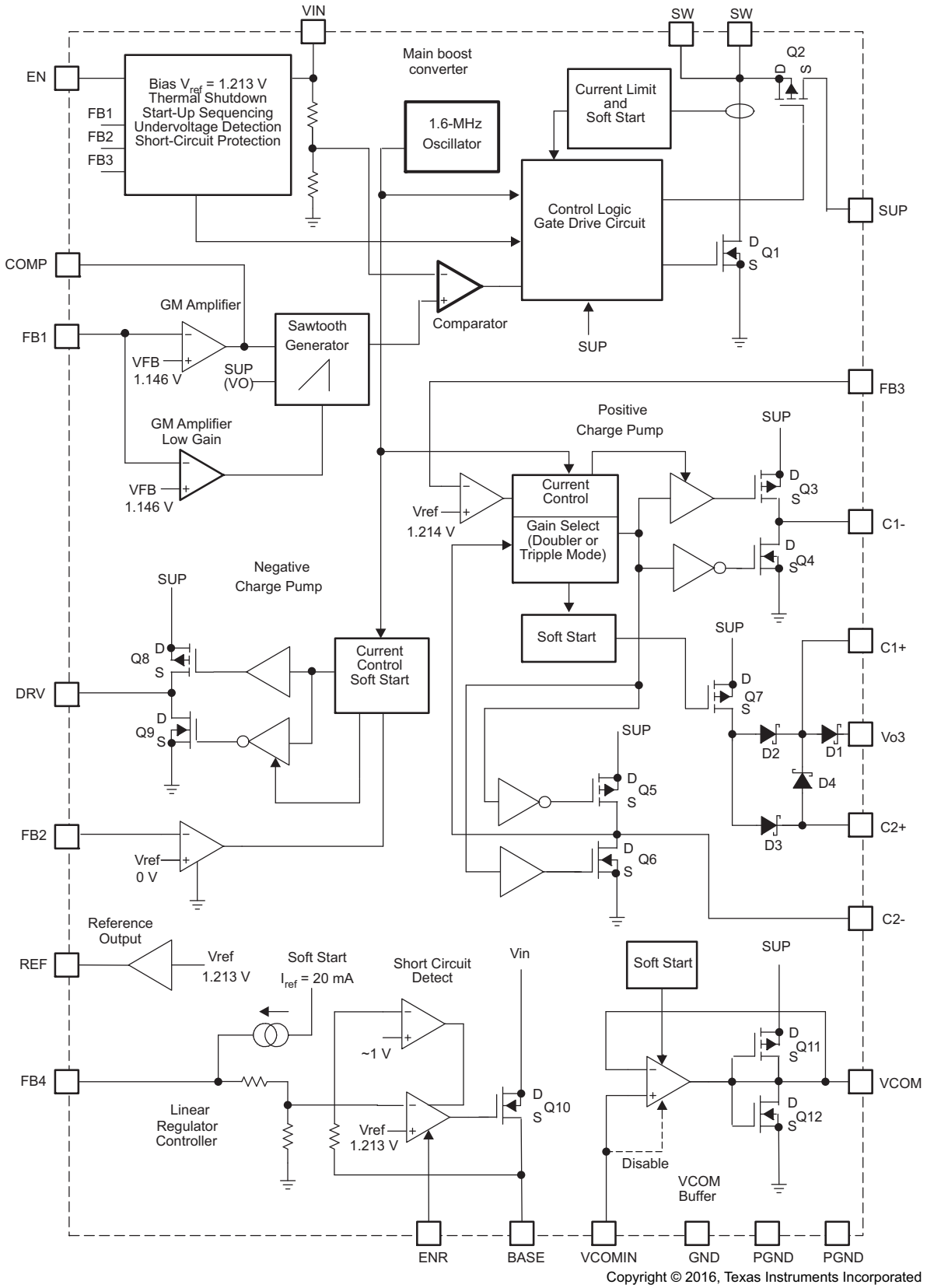
Figure 14. VO3 Maximum Load Current

8 Detailed Description

8.1 Overview

The TPS6510x series consists of a main boost converter operating with a fixed switching frequency of 1.6 MHz to allow for small external components. The boost converter output voltage V_{O1} is also the input voltage, connected through the pin SUP, for the positive and negative charge pumps and the bias supply for the VCOM buffer. The linear regulator controller is independent from this system with its own enable pin. This allows the linear regulator controller to continue to operate while the other supply rails are disabled or in shutdown due to a fault condition on one of their outputs. See *Functional Block Diagram* for more information.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Main Boost Converter

The main boost converter operates with PWM and a fixed switching frequency of 1.6 MHz. The converter uses a unique fast response, voltage mode controller scheme with input voltage feedforward. This achieves excellent line and load regulation (typical is 0.2% A) and allows the use of small external components. To add higher flexibility to the selection of external component values the device uses external loop compensation. Although the boost converter looks like a nonsynchronous boost converter topology operating in discontinuous mode at light load, the TPS6510x series maintains continuous conduction even at light load currents. This is accomplished using the Virtual Synchronous Converter Technology for improved load transient response. This architecture uses an external Schottky diode and an integrated MOSFET in parallel connected between SW and SUP (see the functional block diagram). The integrated MOSFET Q2 allows the inductor current to become negative at light load conditions. For this purpose, a small integrated P-channel MOSFET with typical $r_{DS(on)}$ of around10 Ω is sufficient. When the inductor current is positive, the external Schottky diode with the lower forward voltage conducts the current. This causes the converter to operate with a fixed frequency in continuous conduction mode over the entire load current range. This avoids the ringing on the switch pin as seen with a standard nonsynchronous boost converter and allows a simpler compensation for the boost converter.

8.3.2 VCOM Buffer

VCOMIN is the input of the VCOM buffer. If the VCOM buffer is not required for certain applications, it is possible to shut down the VCOM buffer by statically connecting VCOMIN to ground, reducing the overall quiescent current. The VCOM pin can be left open in this case. The VCOM buffer features soft start avoiding a large voltage drop at V_{O1} during start-up. During operation the VCOMIN cannot be pulled dynamically to ground.

8.3.3 Enable and Power-On Sequencing

The device has two enable pins. These pins should be terminated and not left floating to prevent unpredictable operation. Pulling the enable pin (EN) high enables the device and starts the power on sequencing with the main boost converter V_{O1} coming up first then the negative and positive charge pump and the VCOM buffer. If the VCOMIN pin is low, the VCOM buffer remains disabled. The linear regulator has an independent enable pin (ENR). Pulling this pin low disables the regulator, and pulling this pin high enables this regulator.

If the enable pin EN is pulled high, the device starts its power on sequencing. The main boost converter starts up first with its soft start. If the output voltage has reached 91.25% of its output voltage, the negative charge pump comes up next. The negative charge pump starts with a soft start and when the output voltage has reached 91% of the nominal value, the positive charge pump comes up with a soft start. The VCOM buffer is enabled as soon as the positive charge pump has reached its nominal value and VCOMIN is greater than typically 1.0 V. Pulling the enable pin low shuts down the device. Depended on load current and output capacitance, each of the outputs goes down.

8.3.4 Positive Charge Pump

The TPS6510x series has a fully regulated integrated positive charge pump generating V_{O3}. The input voltage for the charge pump is applied to the SUP pin that is equal to the output of the main boost converter V_{O1}. The charge pump is capable of supplying a minimum load current of 20 mA. Depending on the voltage difference between V_{O1} and V_{O3} higher load currents are possible.

8.3.5 Negative Charge Pump

The TPS6510x series has a regulated negative charge pump using two external Schottky diodes. The input voltage for the charge pump is applied to the SUP pin that is connected to the output of the main boost converter V_{O1}. The charge pump inverts the main boost converter output voltage and is capable of supplying a minimum load current of 20 mA. Depending on the voltage difference between V_{O1} and V_{O1}, higher load currents are possible. See Figure 12.

Feature Description (continued)

8.3.6 Linear Regulator Controller

The TPS6510x series includes a linear regulator controller to generate a 3.3-V rail which is useful when the system is powered from a 5-V supply. The regulator is independent from the other voltage rails of the device and has its own enable (ENR). Since most of the systems require this voltage rail to come up first it is recommended to use a R-C delay on EN. This delays the start-up of the main boost converter which will reduce the inrush current as well. If the linear regulator is not used then it is recommended to pull ENR pin to GND and to pull BASE and FB4 pin to VIN.

8.3.7 Soft Start

The main boost converter as well as the charge pumps, linear regulator, and VCOM buffer have an internal soft start. This avoids heavy voltage drops at the input voltage rail or at the output of the main boost converter V_{O1} during start-up caused by high inrush currents. See Figure 10 and Figure 11. During soft start of the main boost converter V_{O1} the internal current limit threshold is increased in three steps. The device starts with the first step where the current limit is set to 2/5 of the typical current limit (2/5 of 2.3A) for 1024 clock cycles then increased to 3/5 of the current limit for 1024 clock cycles and the 3rd step is the full current limit. The TPS65101 has an extended soft-start time where each step is 2048 clock cycles.

8.3.8 Fault Protection

All the outputs of the TPS65100 and TPS65105 have short-circuit detection where the device enters shutdown. The TPS65101, as an exception, does not enter shutdown in case one of the outputs falls below its power good threshold. The main boost converter has overvoltage and undervoltage protection. If the output voltage V_{O1} rises above the overvoltage protection threshold of typically 5% of V_{O1}, then the device stops switching but remains operational. When the output voltage falls below this threshold again, then the converter continues operation. When the output voltage falls below power good threshold of typically 8.75% of V_{O1}, in case of a short-circuit condition, then the TPS65100 and TPS65105 goes into shutdown. Because there is a direct pass from the input to the output through the diode, the short-circuit condition remains. If this condition needs to be avoided, a fuse at the input or an output disconnect using a single transistor and resistor is required. The negative and positive charge pumps have an undervoltage lockout to protect the LCD panel of possible latch-up conditions in case of a short-circuit condition or faulty operation. When the negative output voltage is typically above 9.5% of its output voltage (closer to ground), then the device enters shutdown. When the positive charge pump output voltage V_{O3} is below 8% typical of its output voltage, then the device goes into shutdown as well.

See the fault protection thresholds section in the *Electrical Characteristics* table. The device can be enabled again by toggling the enable pin EN below 0.4 V or by cycling the input voltage below the undervoltage threshold of 2.2 V. The linear regulator reduces the output current to typical 20 mA under a short-circuit condition when the output voltage is typically < 1 V. See the *Functional Block Diagram*. The linear regulator does not go into shutdown under a short-circuit condition.

8.3.9 Thermal Shutdown

A thermal shutdown is implemented to prevent damage due to excessive heat and power dissipation. Typically, the thermal shutdown threshold is 160°C. If this temperature is reached, the device goes into shutdown. The device can be enabled by toggling the enable pin to low and back to high or by cycling the input voltage to GND and back to V_I again.

8.3.10 Linear Regulator Controller

The TPS6510x series includes a linear regulator controller to generate a 3.3-V rail when the system is powered from a 5-V supply. Because an external NPN transistor is required, the input voltage of the TPS6510x series applied to V_I needs to be higher than the output voltage of the regulator. To provide a minimum base drive current of 13.5 mA, a minimum internal voltage drop of 500 mV from V_I to $V_{(BASE)}$ is required.

This can be translated into a minimum input voltage on V_I for a certain output voltage as Equation 1 shows:

$$V_{I(min)} = V_{O4} + V_{BE} + 0.5\ V \quad (1)$$

Feature Description (continued)

The base drive current together with the h_{FE} of the external transistor determines the possible output current. Using a standard NPN transistor like the BCP68 allows an output current of 1 A and using the BCP54 allows a load current of 337 mA for an input voltage of 5 V. Other transistors can be used as well depending on the required output current, power dissipation, and PCB space. The device is stable with a 4.7-µF ceramic output capacitor. Larger output capacitor values can be used to improve the load transient response when higher load currents are required.

8.4 Device Functional Modes

8.4.1 Enable and Disable

$V_I \geq V_{IT+}$: When the input voltage is above the undervoltage lockout threshold, the device is turned on and the power-on sequencing starts.

$V_I \leq V_{IT-}$: When the input voltage is below the undervoltage lockout threshold, the device turns off and all functions are disabled.

8.4.2 Fault Mode

8.4.2.1 Overvoltage Protection

V_{O1} > 105% of V_{O1} (typical): device stops switching but remains operational. When the output falls below this threshold, the converter continues operation.

8.4.2.2 Short-Circuit Protection

V_{O1} < 91.25% of V_{O1} (typical): device goes into shutdown. Because there is a direct pass from input to output through the diode, the short-circuit condition remains. A fuse at the input or an output disconnect can avoid this condition.

V_{O2} < 91% of V_{O2} (typical): device goes into shutdown. The device can be enabled by toggling the enable pin (EN) below 0.4 V or by cycling the input voltage below V_{IT-}.

V_{O3} < 92% of V_{O3} (typical): device goes into shutdown. The device can be enabled by toggling the enable pin (EN) below 0.4 V or by cycling the input voltage below V_{IT-}.

V_{O4} < 1 V (typical): linear regulator reduces output current to typical 20 mA. It does not go into shutdown.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS6510x series provides all three voltages that are required for (TFT) LCD displays. The auxiliary linear regulator controller can be used to generate a 3.3-V logic power rail for systems powered by a 5-V supply rail only. Additionally it has an integrated VCOM buffer to power the LCD backplane.

9.2 Typical Applications

Figure 15 shows a typical application circuit for a display panel power by a 5-V supply rail. It generates up to 350 mA at 15 V to drive the source driver and 20 mA at 30 V and –12 V to drive the gate drivers.

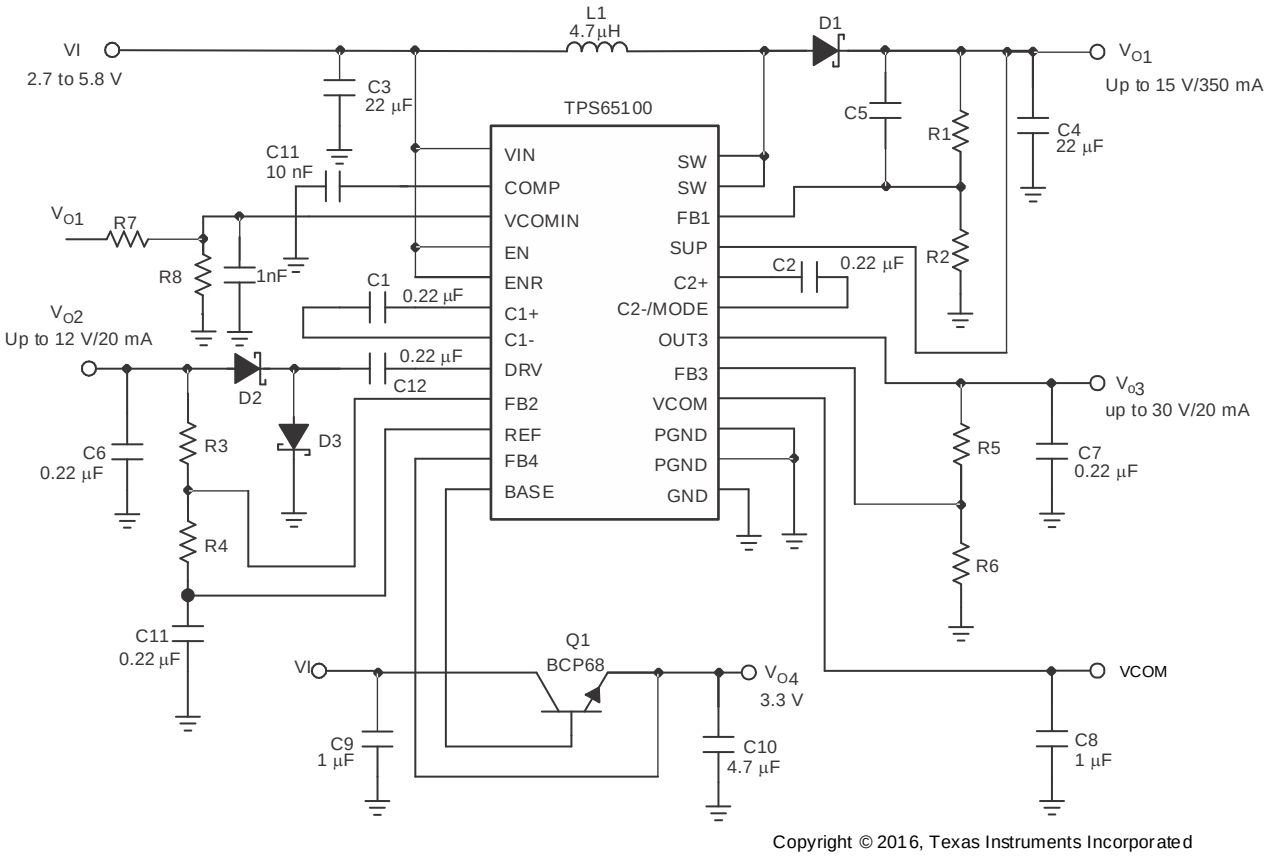


Figure 15. Typical Application Circuit

Typical Applications (continued)

9.2.1 Design Requirements

Table 1 shows the design parameters for this example.

Table 1. Design Parameters

PARAMETER		VALUE
V_I	Input supply voltage	3.3 V
V_{O1}	Boost converter output voltage and current	10 V at 300 mA
$V_{O1(PP)}$	Boost converter peak-to-peak output voltage ripple	1% = 10 mV
$V_{(SW)}$	Switch voltage drop	0.5 V
V_F	Schottky diode forward voltage drop	0.8 V
V_{O2}	Positive charge pump output voltage and current	23 V at 20 mA
$V_{O2(PP)}$	Positive charge pump peak-to-peak output voltage ripple	100 mV
V_{O3}	Negative charge pump output voltage and current	–5 V at 20 mA
$V_{O3(PP)}$	Negative charge pump peak-to-peak output voltage ripple	100 mV

9.2.2 Detailed Design Procedure

9.2.2.1 Boost Converter Design Procedure

The first step in the design procedure is to calculate the maximum possible output current of the main boost converter = 10 V.

1. Duty cycle:

$$D = \frac{V_{O1} + V_F - V_I}{V_{O1} + V_F - V_{SW}} = \frac{10\ V + 0.8\ V - 3.3\ V}{10\ V + 0.8\ V - 0.5\ V} = 0.73 \quad (2)$$

2. Average inductor current:

$$I_L = \frac{I_{O1}}{1 - D} = \frac{300\ mA}{1 - 0.73} = 1.1\ A \quad (3)$$

3. Inductor peak-to-peak ripple current:

$$\Delta i_L = \frac{(V_I - V_{SW}) \times D}{f_{osc} \times L} = \frac{(3.3\ V - 0.5\ V) \times 0.73}{1.6\ MHz \times 4.7\ \mu H} = 271\ mA \quad (4)$$

4. Peak switch current:

$$I_{(SW)M} = I_L + \frac{\Delta i_L}{2} = 1.1\ A + \frac{271\ mA}{2} = 1.24\ A \quad (5)$$

The integrated switch, the inductor and the external Schottky diode must be able to handle the peak switch current. The calculated peak switch current has to be equal or lower than the minimum N-MOSFET switch current limit (Q1) as specified in the electrical characteristics table (1.6 A for the TPS65100/01 and 0.96 A for the TPS65105).

If the peak switch current is higher, then the converter cannot support the required load current. This calculation must be done for the minimum input voltage where the peak switch current is highest. The calculation includes conduction losses like switch $r_{DS(on)}$ and diode forward drop voltage losses. Additional switching losses, inductor core and winding losses, etc., require a slightly higher peak switch current in the actual application. The above calculation still allows an estimate for a good design and component selection.

9.2.2.1.1 Inductor Selection

Several inductors work with the TPS6510x series. Especially with the external compensation, the performance can be adjusted to the specific application requirements. The main parameter for inductor selection is the saturation current of the inductor which should be higher than the peak switch current as calculated above with additional margin to cover for heavy load transients and extreme start-up conditions. Another method is to choose the inductor with a saturation current at least as high as the minimum switch current limit of 1.6 A for the TPS65100/01 and 0.96 A for the TPS65105. The different switch current limits allow selection of a physically smaller inductor when less output current is required. The second important parameter is inductor DC resistance.

Usually, the lower the DC resistance, the higher the efficiency. However, inductor DC resistance, is not the only parameter determining the efficiency. Especially for a boost converter where the inductor is the energy storage element the type and material of the inductor influences the efficiency as well. Especially at the high switching frequency of 1.6 MHz, inductor core losses, proximity effects, and skin effects become more important. Usually, an inductor with a larger form factor yields higher efficiency. The efficiency difference between different inductors can vary between 2% to 10%.

For the TPS6510x series, inductor values between 3.3 μH and 6.8 μH are a good choice but other values can be used as well. Possible inductors are shown in Table 2.

Table 2. Inductor Selection

DEVICE	INDUCTOR VALUE	COMPONENT SUPPLIER	DIMENSIONS / mm	I_{SAT} / DCR
TPS65100	4.7 μH	Coilcraft DO1813P-472HC	8,89 x 6,1 x 5	2.6 A/54 mΩ
	4.2 μH	Sumida CDRH5D28 4R2	5,7 x 5,7 x 3	2.2 A/23 mΩ
	4.7 μH	Sumida CDC5D23 4R7	6 x 6 x 2,5	1.6 A/48 mΩ
	3.3 μH	Wuerth Elektronik 744042003	4,8 x 4,8 x 2	1.8 A/65 mΩ
	4.2 μH	Sumida CDRH6D12 4R2	6,5 x 6,5 x 1,5	1.8 A/60 mΩ
	3.3 μH	Sumida CDRH6D12 3R3	6,5 x 6,5 x 1,5	1.9 A/50 mΩ
TPS65105	3.3 μH	Sumida CDPH4D19 3R3	5,1 x 5,1 x 2	1.5 A/26 mΩ
	3.3 μH	Coilcraft DO1606T-332	6,5 x 5,2 x 2	1.4 A/120 mΩ
	3.3 μH	Sumida CDRH2D18/HP 3R3	3,2 x 3,2 x 2	1.45 A/69 mΩ
	4.7 μH	Wuerth Elektronik 744010004	5,5 x 3,5 x 1	1.0 A/260 mΩ
	3.3 μH	Coilcraft LPO6610-332M	6,6 x 5,5 x 1	1.3 A/160 mΩ

9.2.2.1.2 Output Capacitor Selection

For the best output voltage filtering, a low ESR output capacitor is recommended. Ceramic capacitors have a low ESR value, but depending on the application, tantalum capacitors can be used as well. A 22-μF ceramic output capacitor works for most of the applications. Higher capacitor values can be used to improve the load transient regulation. See Table 3 for selection of the output capacitor. The output voltage ripple can be calculated as:

$$\Delta V_{O1} = \frac{I_{O1}}{C_O} \times \left(\frac{1}{f_{OSC}} - \frac{I_{(SW)M} \times L}{V_{O1} + V_F - V_I} \right) + I_{(SW)M} \times ESR$$

where

- $I_{(SW)M}$ = Peak switch current as calculated in the previous section with $I_{(SW)M}$
- L = Selected inductor value
- I_O = Normal load current
- f_{osc} = Switching frequency
- V_F = Rectifier diode forward voltage (typical 0.3 V)
- C_O = Selected output capacitor
- ESR = Output capacitor ESR value (6)

9.2.2.1.3 Input Capacitor Selection

For good input voltage filtering, low ESR ceramic capacitors are recommended. A 22-μF ceramic input capacitor is sufficient for most of the applications. For better input voltage filtering, this value can be increased. See Table 3 for input capacitor recommendations.

Table 3. Input and Output Capacitors Selection

CAPACITOR	VOLTAGE RATING	COMPONENT SUPPLIER	COMMENTS
22 µF/1210	16 V	Taiyo Yuden EMK325BY226MM	output capacitor C_O
22 µF/1206	6.3 V	Taiyo Yuden JMK316BJ226	input capacitor C_I

9.2.2.1.4 Rectifier Diode Selection

A Schottky diode is recommended to achieve good efficiency as the forward voltage drop is lower than of silicon diodes. The following table shows criteria which should be considered when choosing the rectifier diode:

Table 4. Rectifier Diode Selection Requirements

PARAMETER	VALUE	Comment
Voltage Rating	≥ $V_{O1(M)}$	Higher than maximum output voltage of boost converter
Average Forward Current	≥ I_O	Higher than the output current
Peak Current	> $I_{L(PP)}$	Higher than the inductor peak current
Forward voltage drop, reverse leakage current	Low as possible	For good efficiency

Possible diodes are: On Semiconductor MBRM120L, Microsemi UPS120E, and Fairchild Semiconductor MBRS130L.

9.2.2.1.5 Converter Loop Design and Stability

The TPS6510x series converter loop can be externally compensated and allows access to the internal transconductance error amplifier output at the COMP pin. A small feedforward capacitor across the upper feedback resistor divider speeds up the circuit as well. To test the converter stability and load transient performance of the converter, a load step from 50 mA to 250 mA is applied, and the output voltage of the converter is monitored. Applying load steps to the converter output is a good tool to judge the stability of such a boost converter. Please refer to SLVA381 to understand the relationship between the phase margin in an AC loop response and the ringing in a load-step

9.2.2.1.6 Design Procedure Quick Steps

1. Select the feedback resistor divider to set the output voltage.
2. Select the feedforward capacitor to place a zero at 50 kHz.
3. Select the compensation capacitor on pin COMP. The smaller the value, the higher the low frequency gain.
4. Use a 50-kΩ potentiometer in series to C_c and monitor V_{O1} during load transients. Fine tune the load transient by adjusting the potentiometer. Select a resistor value that comes closest to the potentiometer resistor value. This needs to be done at the highest V_I and highest load current since the stability is most critical at these conditions.

9.2.2.1.7 Setting the Output Voltage and Selecting the Feedforward Capacitor

The output voltage is set by the external resistor divider and is calculated as:

$$V_{O1} = V_{ref} \times \left(1 + \frac{R_1}{R_2}\right) \quad (7)$$

Across the upper resistor a bypass capacitor is required to speed up the circuit during load transients as shown in Figure 16.

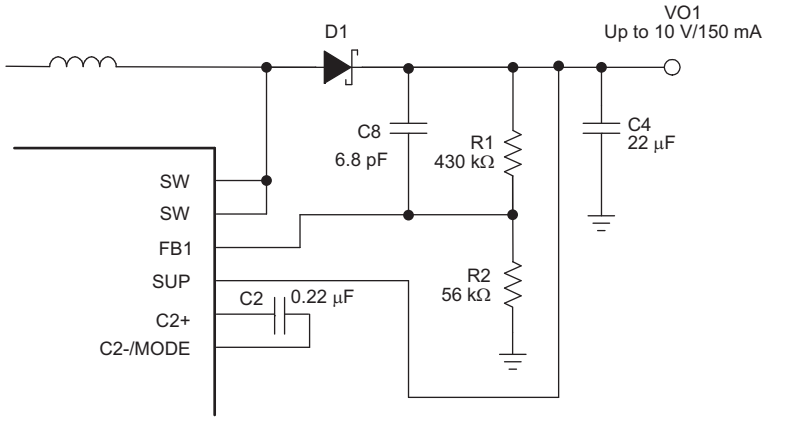


Figure 16. Feedforward Capacitor

Together with R1 the bypass capacitor C8 sets a zero in the control loop at approximately 50 kHz:

$$f_Z = \frac{1}{20 \times \pi \times C8 \times R1} \quad (8)$$

A value closest to the calculated value should be used. Larger feedforward capacitor values reduce the load regulation of the converter and cause DC voltage changes as shown in Figure 17.

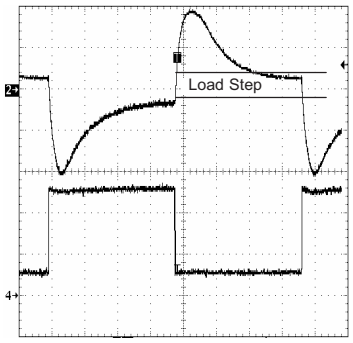


Figure 17. Load Regulation Caused by a Too Large Feedforward Capacitor Value

9.2.2.2 Negative Charge Pump

The negative charge pump provides a regulated output voltage by inverting the main output voltage V_{O1}. The negative charge pump output voltage is set with external feedback resistors.

The maximum load current of the negative charge pump depends on the voltage drop across the external Schottky diodes, the internal on resistance of the charge pump MOSFETS Q8 and Q9, and the impedance of the flying capacitor C12. When the voltage drop across these components is larger than the voltage difference from V_{O1} to V_{O2}, the charge pump is in dropout, providing the maximum possible output current.

Therefore, the higher the voltage difference between V_{O1} and V_{O2}, the higher the possible load current. See Figure 12 for the possible output current versus boost converter voltage V_{O1}.

$$V_{O2(max)} = -(V_{O1} - 2V_F - I_O(2 \times r_{DS(on)Q8} + 2 \times r_{DS(on)Q9})) \quad (9)$$

Setting the output voltage:

$$V_{O2} = -1.213\ V \times \left(\frac{R_3}{R_4}\right)$$

$$R3 = R4 \times \left(\frac{|V_{O2}|}{1.213\ V} \right)$$

The lower feedback resistor value R4 should be in a range between 40 kΩ to 120 kΩ or the overall feedback resistance should be within 500 kΩ to 1 MΩ. Smaller values load the reference too heavily and larger values may cause stability problems. The negative charge pump requires two external Schottky diodes. The peak current rating of the Schottky diode has to be twice the load current of the output. For a 20-mA output current, the dual Schottky diode BAT54 or similar is a good choice.

9.2.2.3 Positive Charge Pump

The positive charge pump can be operated in a voltage doubler mode or a voltage tripler mode depending on the configuration of the C2+ and C2-/MODE pins. To operate in a voltage doubler leave the C2+ pin open and connect C2-/MODE to GND. To operate the charge pump in the voltage tripler mode, a flying capacitor needs to be connected between C2+ and C2-/MODE.

The maximum load current of the positive charge pump depends on the voltage drop across the internal Schottky diodes, the internal on resistance of the charge pump MOSFETS, and the impedance of the flying capacitor. When the voltage drop across these components is larger than the voltage difference V_{O1} x 2 to V_{O3} (doubler mode) or V_{O1} x 3 to V_{O3} (tripler mode), then the charge pump is in dropout, providing the maximum possible output current. Therefore, the higher the voltage difference between 2 x V_{O1} or 3 x V_{O1} to V_{O3}, the higher the possible load current. See Figure 13 and Figure 14 for the output current versus boost converter voltage V_{O1} and the following calculations. The following graph shows voltage ranges of a doubler and tripler depending of the boost converter voltage V_{O1}.

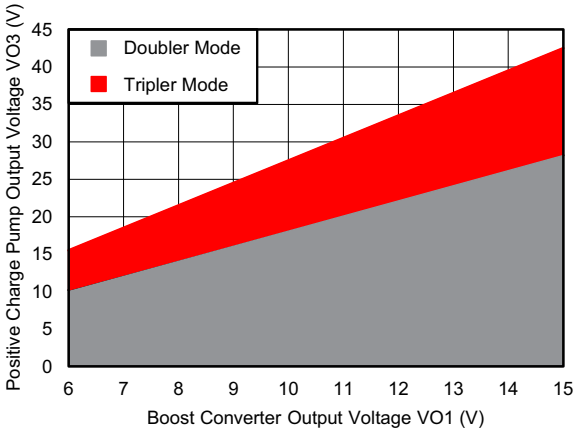


Figure 18. Positive Charge Pump – Output Ranges for I_O = 20 mA

Table 5 gives first order formulas to calculate the minimum and maximum output voltages of the positive charge pump.

Table 5. Voltage Limitation Positive Charge Pump

MODE		EQUATION
Doubler	Minimum output voltage	$V_{O3(min\_d)} = V_{O1}$
	Maximum output voltage	$V_{O3(max\_d)} = 2 \times V_{O1} - (2 \times V_F + 2 \times I_O \cdot (2 \times r_{DS(on)Q5} + r_{DS(on)Q3} + r_{DS(on)Q4}))$
Tripler	Minimum output voltage	$V_{O3(min\_t)} = V_{O3(max\_d)}$
	Maximum output voltage	$V_{O3(max\_t)} = 3 \times V_{O1} - (4 \times V_F + 2 \times I_O (3 \times r_{DS(on)Q5} + r_{DS(on)Q3} + r_{DS(on)Q4}))$

The output voltage is set by the external resistor divider and is calculated as:

$$V_{O3} = 1.214\ V \times \left(1 + \frac{R5}{R6}\right) \quad (10)$$

$$R5 = R6 \times \left(\frac{|V_{O3}|}{1.214\ V} - 1\right) \quad (11)$$

9.2.2.4 VCOM Buffer

The VCOM buffer is typically used to drive the backplane of a TFT panel. The VCOM output voltage is typically set to half of the main output voltage V_{O1} plus a small shift to implement the specific compensation voltage. The TFT video signal gets coupled through the TFT storage capacitor plus the LCD cell capacitance to the output of the VCOM buffer. Because of these, short current pulses in the positive and negative direction appear at the output of the VCOM buffer. To minimize the output voltage ripple caused by the current pulses, a transconductance amplifier having a current source output and an output capacitor is used. The output capacitor supports the high frequency part of the current pulses drawn from the LCD panel. The VCOM buffer only needs to handle the low frequency portion of the current pulses. A 1-µF ceramic output capacitor is sufficient for most of the applications.

The VCOM buffer has an integrated soft start to avoid voltage drops on V_{O1} during start-up. The soft start is implemented as such that the VCOMIN is held low until the VCOM buffer is fully biased and the common mode range is reached. Then the positive input is released and the VCOM buffer output slowly comes up. Usually a 1-nF capacitor on VCOMIN to GND is used to filter high frequency noise coupled in from V_{O1}. The size of this capacitor together with the upper feedback resistor value determines the start-up time. The larger the capacitor from VCOMIN to GND, the slower the start-up time.

9.2.3 Application Curves

Table 6 lists the application curves.

Table 6. Table of Graphs

			FIGURE
MAIN BOOST CONVERTER (V_{OUT1})			
	PWM operation at light load		Figure 7
	Load transient response, C_O = 22 µF		Figure 8
	Load transient response, C_O = 2 x 22 µF		Figure 9
	Power-up sequencing		Figure 10
	Soft start V_{O1}		Figure 11
NEGATIVE CHARGE PUMP			
I_{OM}	V_{O2} Maximum load current	vs Output voltage V_{O1}	Figure 12
POSITIVE CHARGE PUMP			
I_{OM}	V_{O3} Maximum load current	vs Output voltage V_{O1} (doubler mode)	Figure 13
I_{OM}	V_{O3} Maximum load current	vs Output voltage V_{O1} (tripler mode)	Figure 14

9.3 System Examples

9.3.1 Notebook Supply

Figure 19 shows a typical application circuit suitable to supply (TFT) LCD displays in notebook applications. The circuit is designed to operate from a single-cell Li-Ion battery and generates output voltages for the source driver VO1 of 10 V, for the gate driver VO2 of –5 V and VO3 of 23 V and a VCOM voltage of VO1/2.

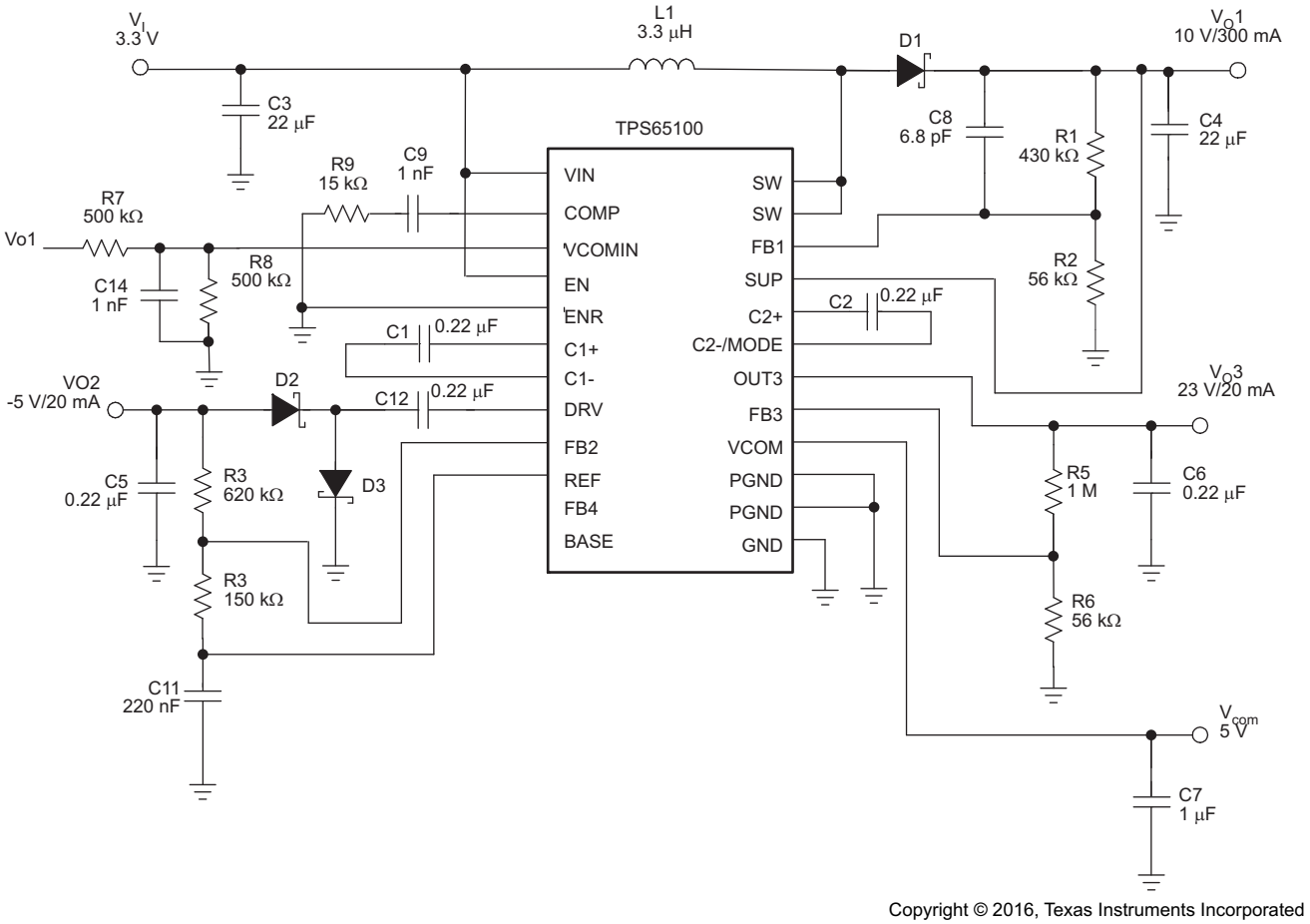


Figure 19. Typical Application, Notebook Supply Diagram

System Examples (continued)

9.3.2 Monitor Supply

Figure 20 shows a typical application circuit suitable to supply (TFT) LCD displays in monitor applications. The circuit is designed to operate by a 5-V power rail and generates output voltages for the source driver VO1 of 13.5 V, for the gate driver VO2 of –7 V and VO3 of 23 V and a VCOM voltage of VO1/2. Additionally monitor applications also require a supply voltage for the digital part that is provided from VO4 of 3.3 V.

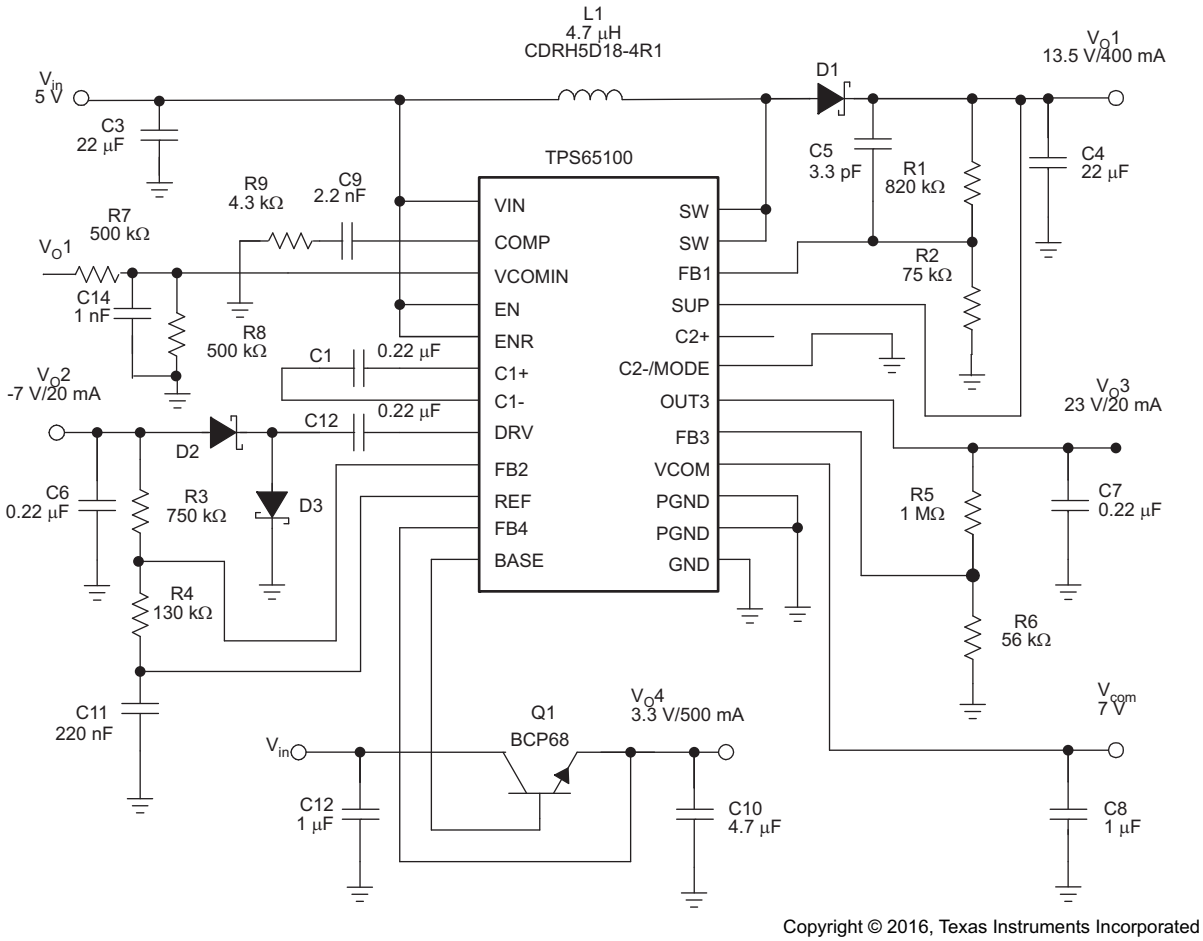


Figure 20. Typical Application, Monitor Supply Diagram

10 Power Supply Recommendations

The TPS6510x devices are designed to operate from an input voltage supply range from 2.7 V to 5.8 V. This input supply must be well regulated.

11 Layout

11.1 Layout Guidelines

For all switching power supplies, the layout is an important step in the design, especially at high-peak currents and switching frequencies. If the layout is not carefully designed, the regulator might show stability and EMI problems. Therefore, the traces carrying high-switching currents should be routed first using wide and short traces. The input filter capacitor should be placed as close as possible to the input pin VIN of the IC. TI recommends the following PCB layout guidelines for the TPS6510x devices:

1. Connect PGND and AGND together on the same ground plane
2. Connect all capacitor grounds and PGND together on a common ground plane.
3. Place the input capacitor as close as possible to the input pin of the IC.
4. Place the rectifier diode as close as possible to the IC
5. Route first the traces carrying high-switching current with wide and short traces
6. Isolate analog signal paths from power paths.
7. If vias are necessary, try to use more than one in parallel to decrease parasitics, especially for power traces.
8. Solder the thermal pad to the PCB for good thermal performance.

11.2 Layout Example

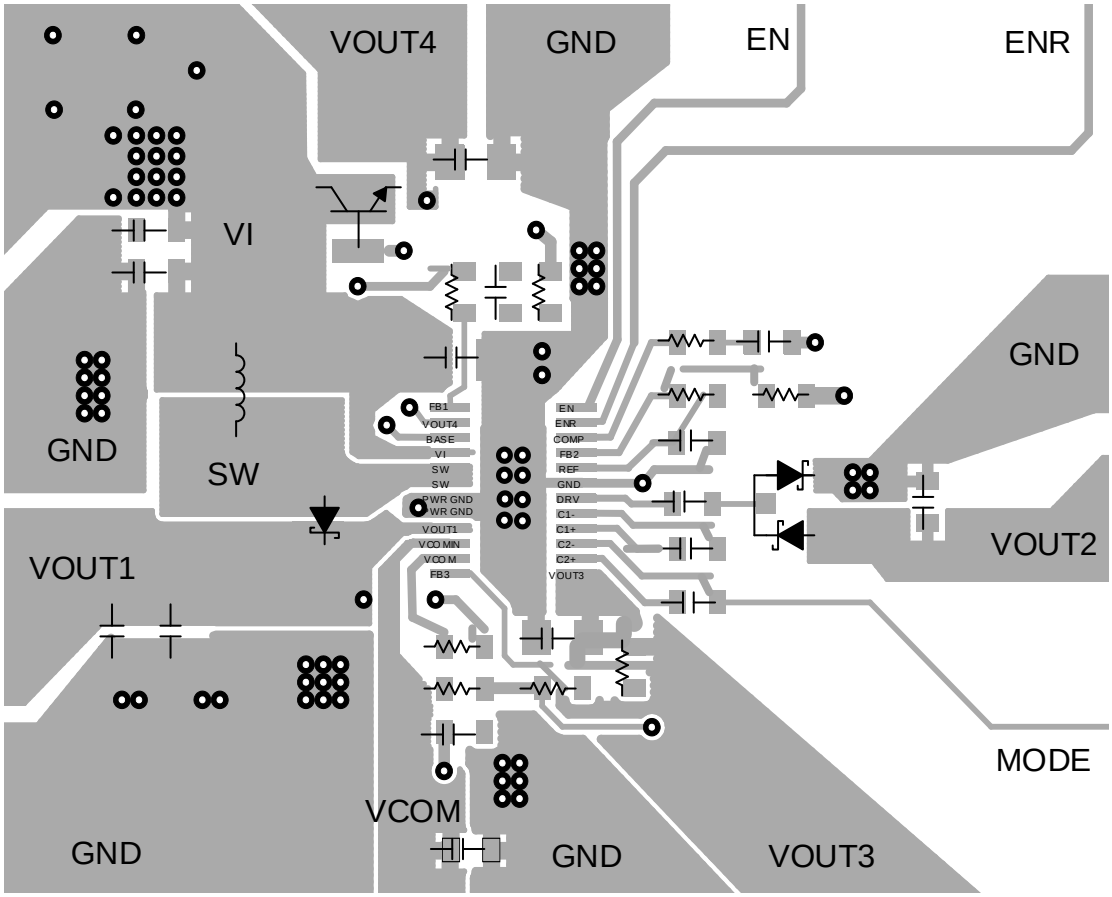


Figure 21. TPS6510x Layout Example

11.3 Thermal Performance

An influential component of thermal performance of a package is board design. To take full advantage of the heat dissipation abilities of the PowerPAD or VQFN package with exposed thermal die, a board that acts similar to a heat sink and allows the use of an exposed (and solderable) deep downset pad should be used. For further information, see the Texas Instruments application notes *PowerPAD Thermally Enhanced Package* and *PowerPAD Made Easy*. For the VQFN package, see the *QFN/SON PCB Attachement* application report. Especially for the VQFN package it is required to solder down the Thermal Pad to achieve the required thermal resistance.

12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

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12.2 Documentation Support

12.2.1 Related Documentation

For related documentation see the following:

- *PowerPAD Thermally Enhanced Package* (SLMA002)
- *QFN/SON PCB Attachement* (SLUA271)
- *PowerPAD Made Easy* (SLMA004)
- *How to Compensate the TPS6510x* (SLVA813)
- *Simplifying Stability Checks* (SLVA381)

12.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 7. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS65100	Click here	Click here	Click here	Click here	Click here
TPS65101	Click here	Click here	Click here	Click here	Click here
TPS65105	Click here	Click here	Click here	Click here	Click here

12.4 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.5 Community Resource

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.6 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

12.7 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.8 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS65100PWP	ACTIVE	HTSSOP	PWP	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS65100	Samples
TPS65100PWPG4	ACTIVE	HTSSOP	PWP	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS65100	Samples
TPS65100PWPR	ACTIVE	HTSSOP	PWP	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS65100	Samples
TPS65100RGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 65100	Samples
TPS65101PWP	ACTIVE	HTSSOP	PWP	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS65101	Samples
TPS65101PWPR	ACTIVE	HTSSOP	PWP	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS65101	Samples
TPS65101RGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 65101	Samples
TPS65105PWP	ACTIVE	HTSSOP	PWP	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS65105	Samples
TPS65105PWPG4	ACTIVE	HTSSOP	PWP	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS65105	Samples
TPS65105PWPR	ACTIVE	HTSSOP	PWP	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS65105	Samples
TPS65105RGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 65105	Samples
TPS65105RGERG4	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 65105	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TPS65100 :

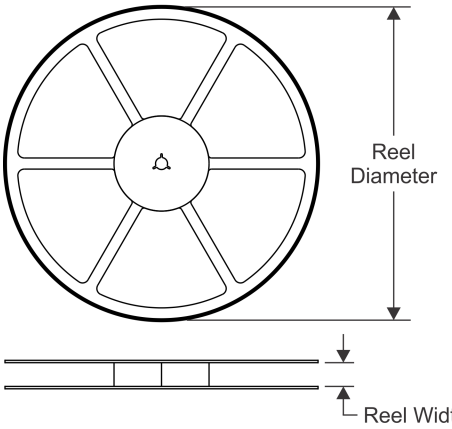
- Automotive: TPS65100-Q1

NOTE: Qualified Version Definitions:

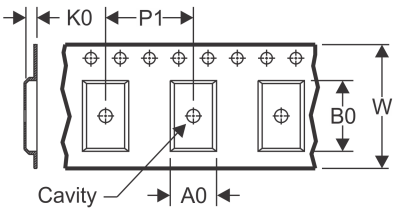
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

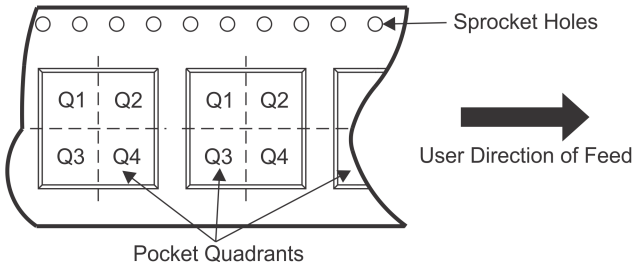


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

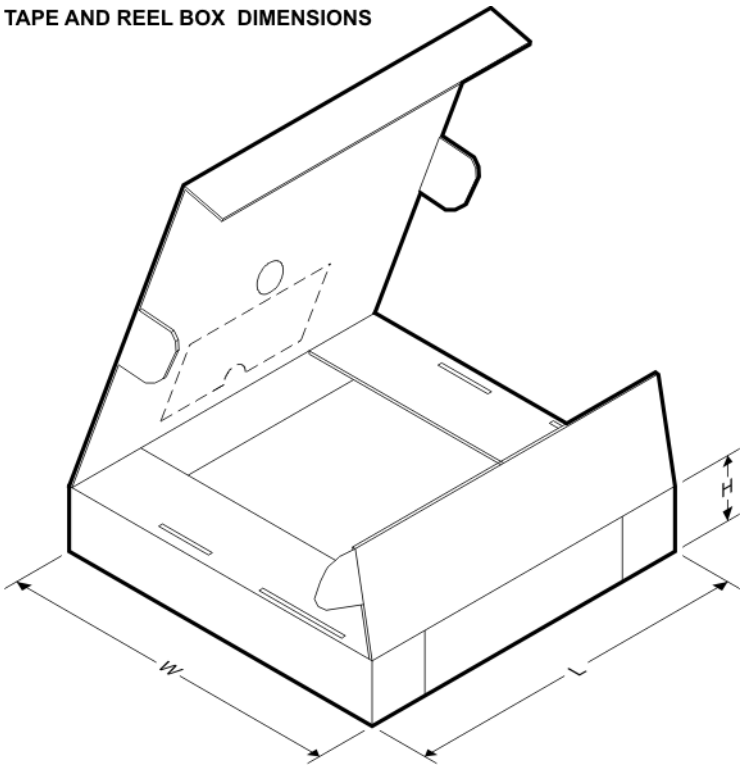
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65100PWPR	HTSSOP	PWP	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
TPS65100RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS65101PWPR	HTSSOP	PWP	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
TPS65101RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS65105PWPR	HTSSOP	PWP	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
TPS65105RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

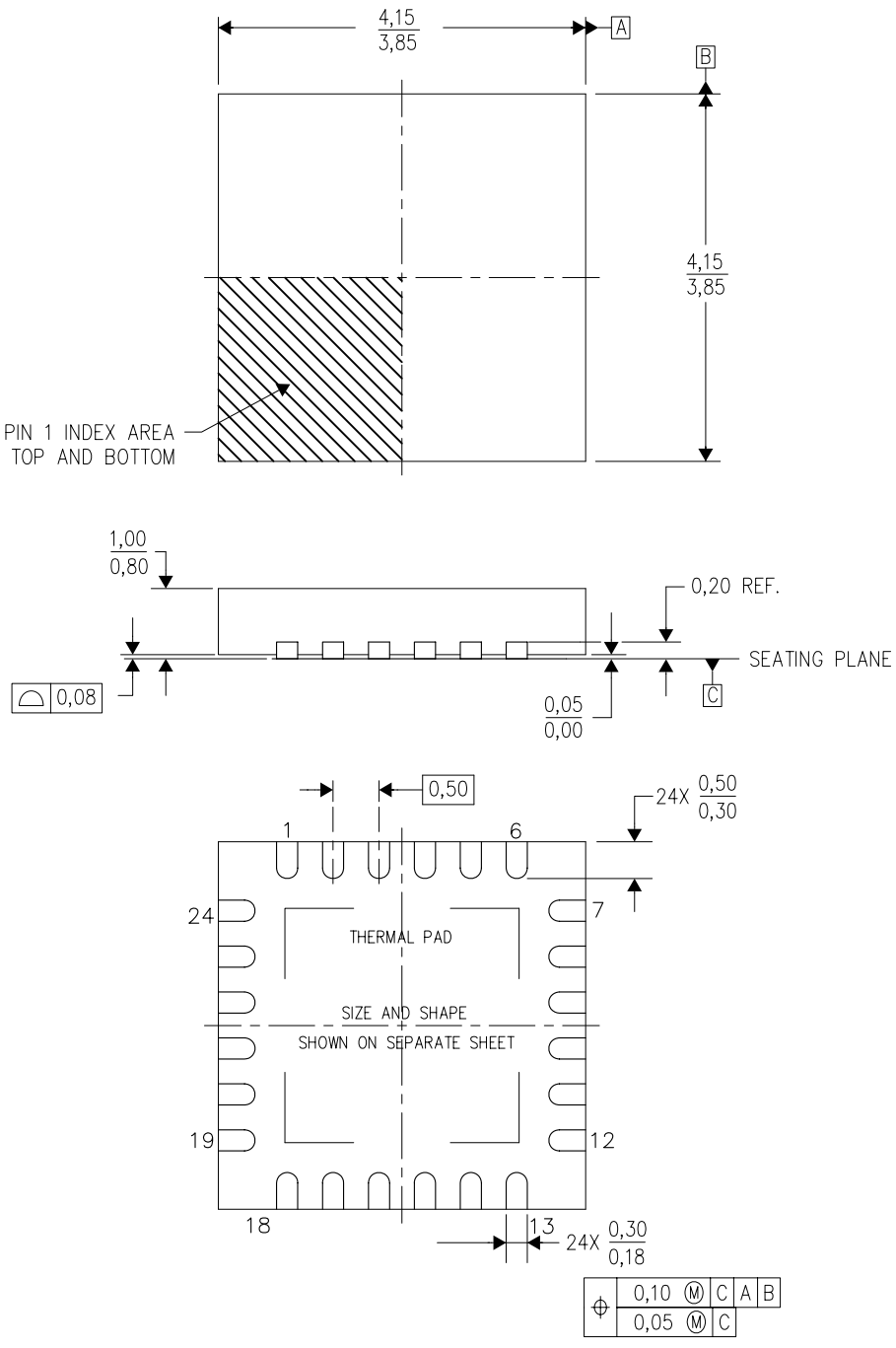
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65100PWPR	HTSSOP	PWP	24	2000	367.0	367.0	38.0
TPS65100RGER	VQFN	RGE	24	3000	367.0	367.0	35.0
TPS65101PWPR	HTSSOP	PWP	24	2000	367.0	367.0	38.0
TPS65101RGER	VQFN	RGE	24	3000	367.0	367.0	35.0
TPS65105PWPR	HTSSOP	PWP	24	2000	367.0	367.0	38.0
TPS65105RGER	VQFN	RGE	24	3000	367.0	367.0	35.0

RGE (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–Leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

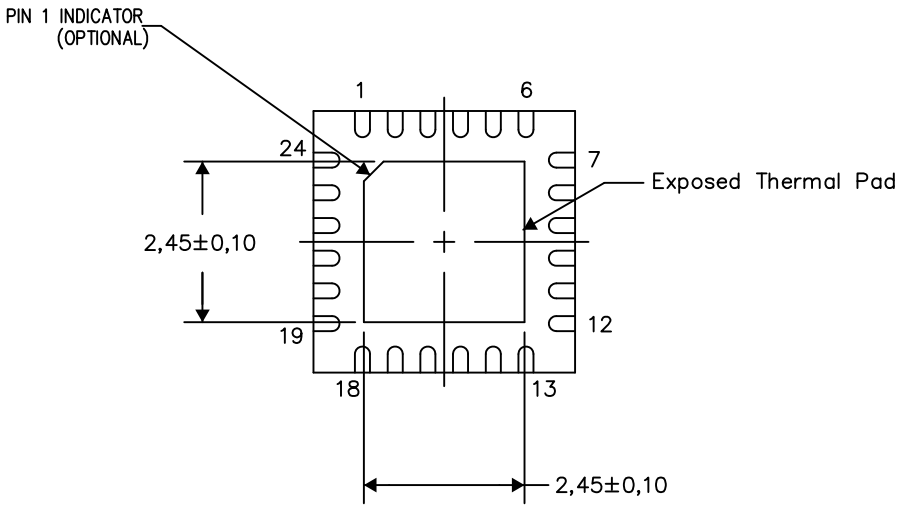
RGE (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



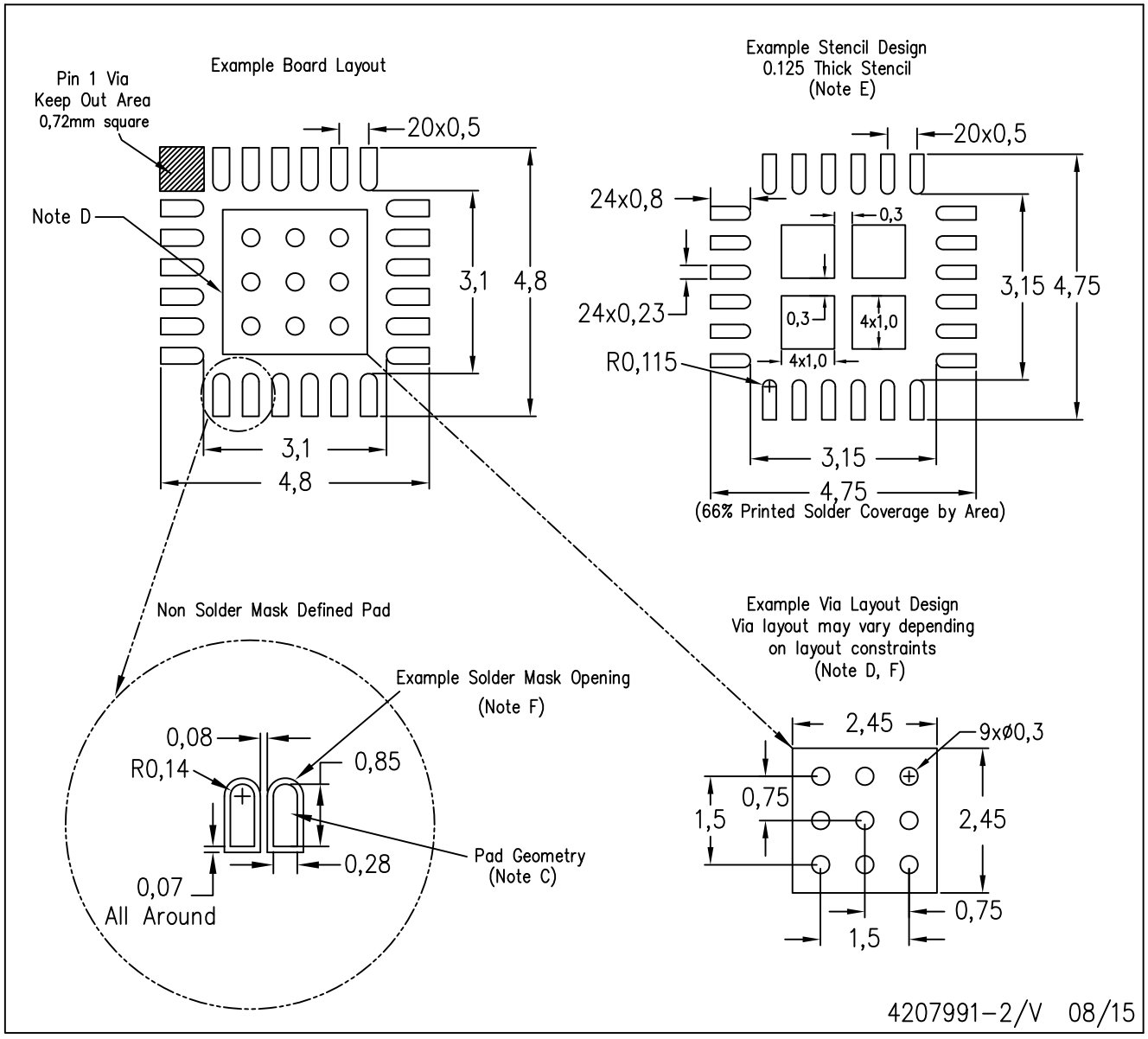
Bottom View

Exposed Thermal Pad Dimensions

4206344–3/AK 08/15

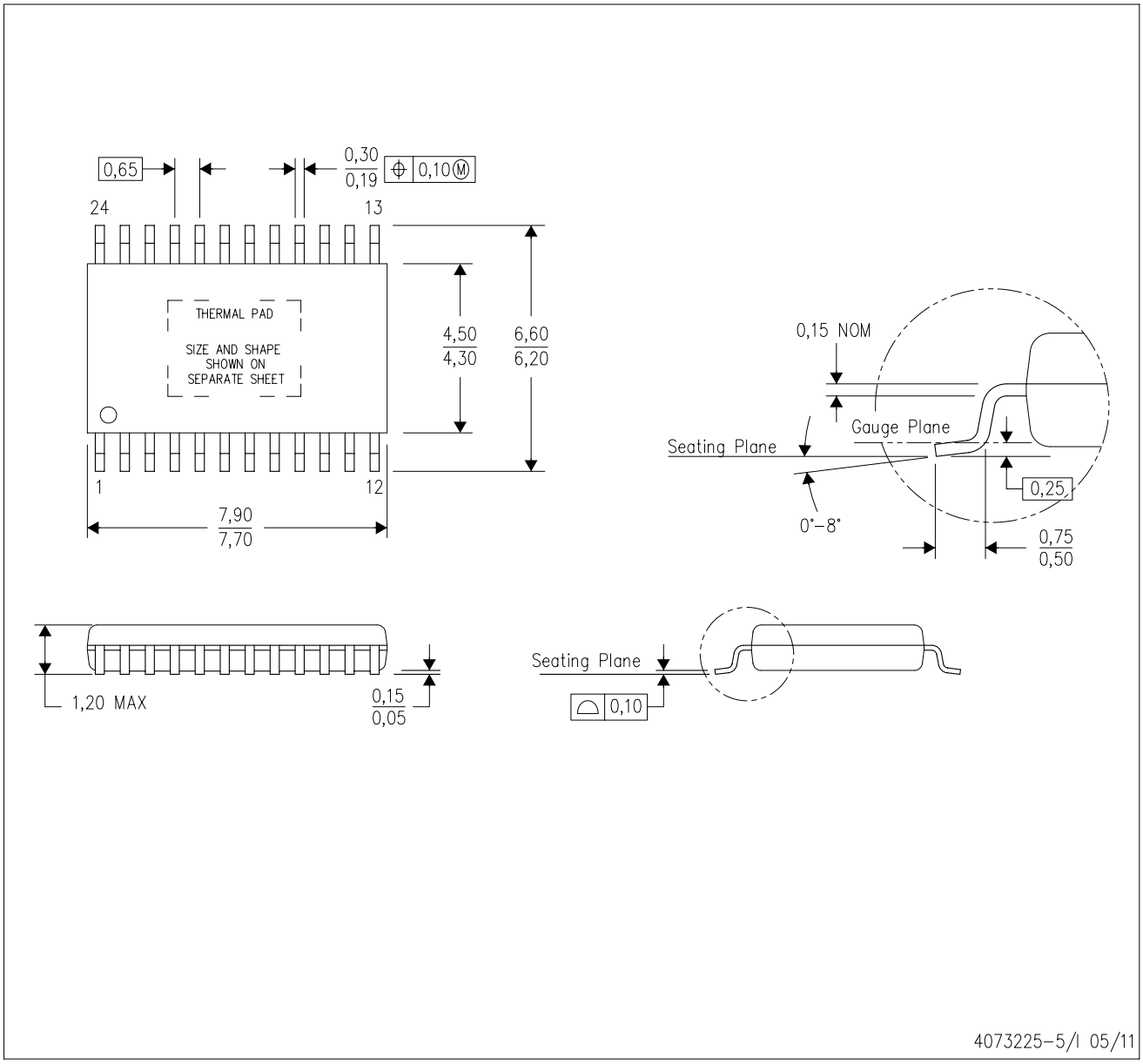
NOTES: A. All linear dimensions are in millimeters

RGE (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

PWP (R–PDSO–G24) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

PowerPAD is a trademark of Texas Instruments.

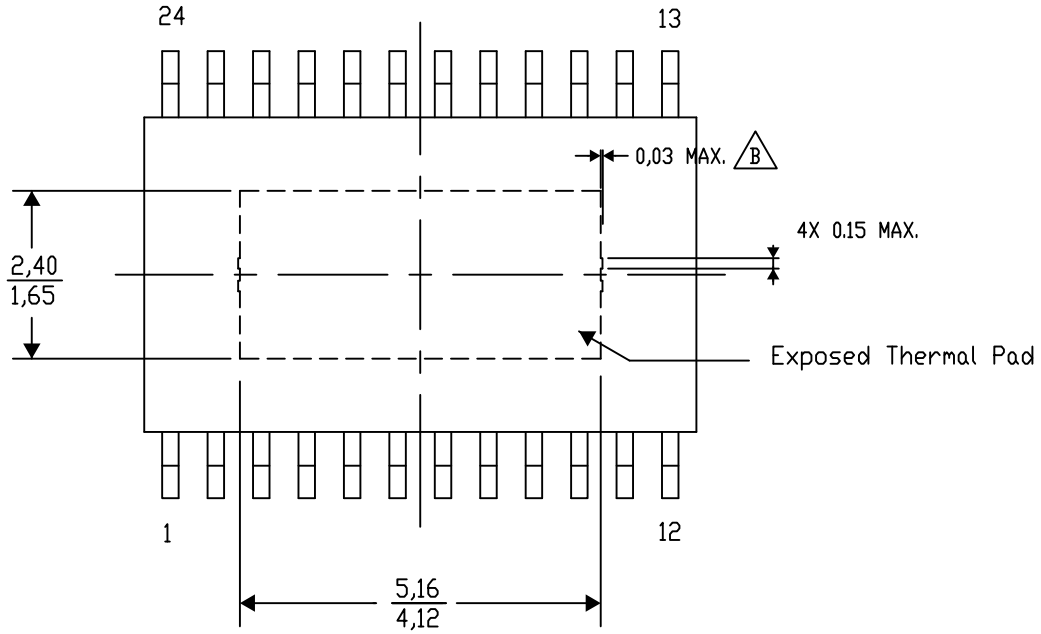
PWP (R–PDSO–G24) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

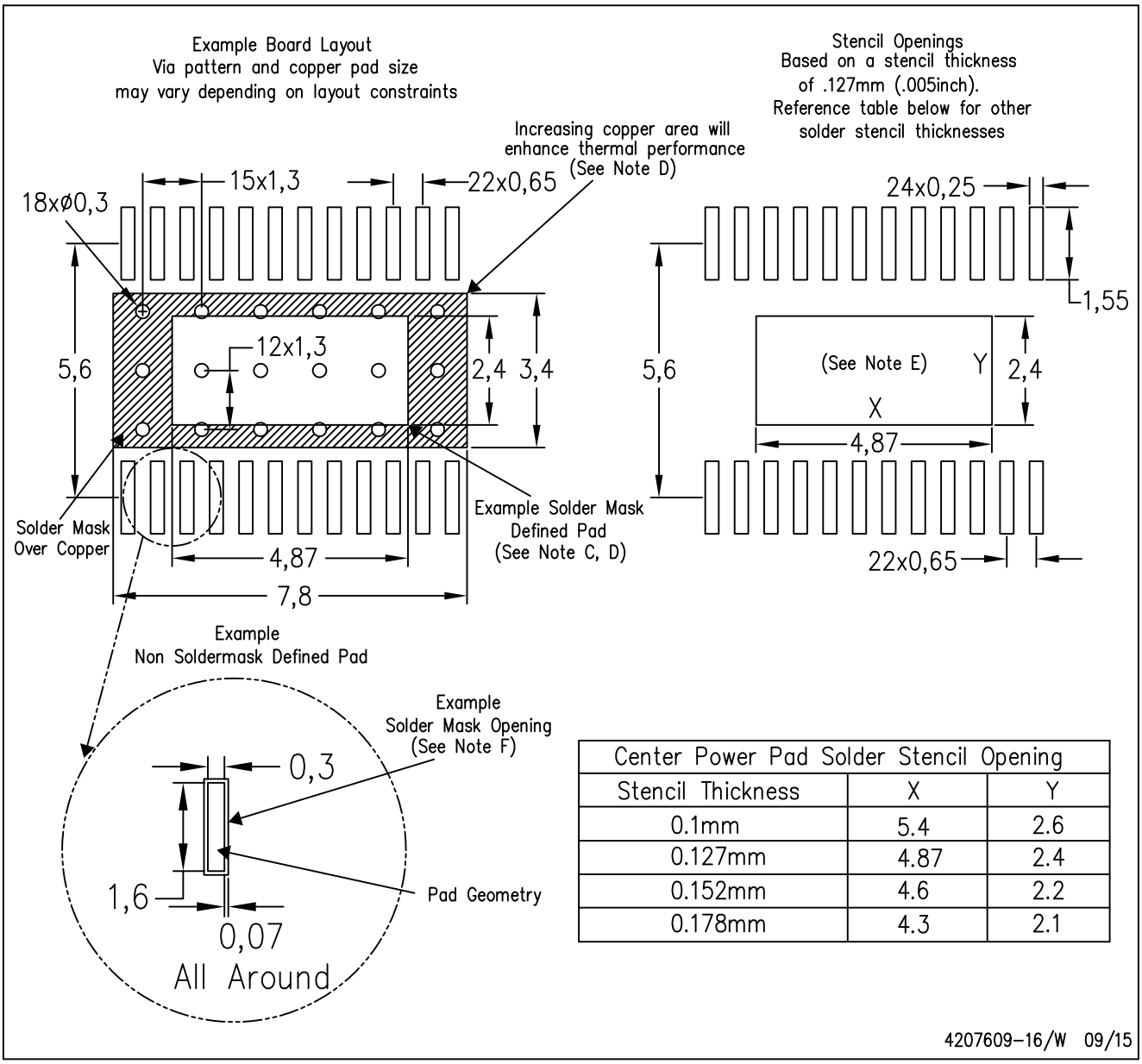
4206332–29/AO 01/16

NOTE: A. All linear dimensions are in millimeters

B. Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PWP (R–PDSO–G24) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	5.4	2.6
0.127mm	4.87	2.4
0.152mm	4.6	2.2
0.178mm	4.3	2.1

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.

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