LOW INPUT VOLTAGE, 1-A LOW-DROPOUT LINEAR REGULATORS WITH SUPERVISOR

Check for Samples: TPS72501, TPS72515, TPS72516, TPS72518, TPS72525

FEATURES

- **1-A Output Current**
- **Available in 1.5-V, 1.6-V, 1.8-V, 2.5-V Fixed-Output and Adjustable Versions (1.2-V to 5.5-V)**
- **Input Voltage Down to 1.8 V**
- **Low 170-mV Dropout Voltage at 1 A (TPS72525)**
- **Stable With Any Type/Value Output Capacitor**
- **Integrated Supervisor (SVS) With 50-ms $\overline{\text{RESET}}$ Delay Time**
- **Low 210-µA Ground Current at Full Load (TPS72525)**
- **Less than 1-µA Standby Current**
- **±2% Output Voltage Tolerance Over Line, Load, and Temperature (-40°C to 125°C)**
- **Integrated UVLO**
- **Thermal and Overcurrent Protection**
- **5-Lead SOT223-5 or DDPAK and 8-Pin SOP (TPS72501 only) Surface Mount Package**

APPLICATIONS

- **PCI Cards**
- **Modem Banks**
- **Telecom Boards**
- **DSP, FPGA, and Microprocessor Power Supplies**
- **Portable, Battery-Powered Applications**

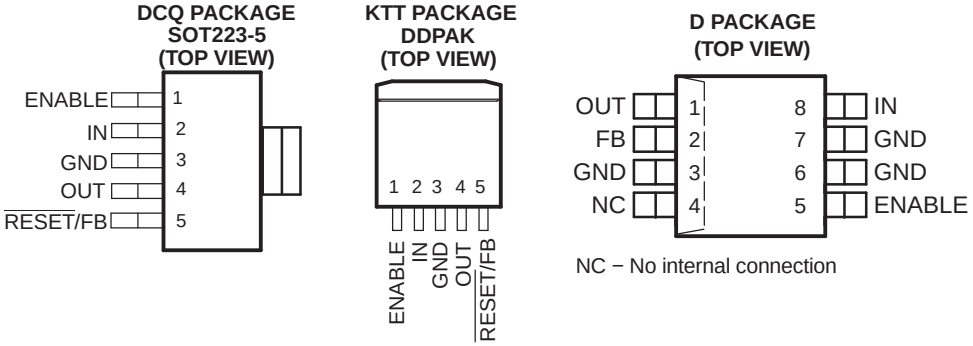
DESCRIPTION

The TPS725xx family of 1-A low-dropout (LDO) linear regulators has fixed voltage options available that are commonly used to power the latest DSPs, FPGAs, and microcontrollers. An adjustable option ranging from 1.22 V to 5.5 V is also available. The integrated supervisory circuitry provides an active low $\overline{\text{RESET}}$ signal when the output falls out of regulation. The no capacitor/any capacitor feature allows the customer to tailor output transient performance as needed. Therefore, compared to other regulators capable of providing the same output current, this family of regulators can provide a stand-alone power supply solution or a post regulator for a switch mode power supply.

These regulators are ideal for higher current applications. The family operates over a wide range of input voltages (1.8 V to 6 V) and has very low dropout (170 mV at 1-A).

Ground current is typically 210 µA at full load and drops to less than 80 µA at no load. Standby current is less than 1 µA.

Each regulator option is available in either a SOT223-5, D (TPS72501 only), or DDPAK package. With a low input voltage and properly heatsinked package, the regulator dissipates more power and achieves higher efficiencies than similar regulators requiring 2.5 V or more minimum input voltage and higher quiescent currents. These features make it a viable power supply solution for portable, battery-powered equipment.



NOTE: TPS72501 replaces RESET with FB. Tab is GND for the DCK and KTT packages.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DESCRIPTION (CONTINUED)

Although an output capacitor is not required for stability, transient response and output noise are improved with a 10-µF output capacitor.

Unlike some regulators that have a minimum current requirement, the TPS725 family is stable with no output load current. The low noise capability of this family, coupled with its high current operation and ease of power dissipation, make it ideal for telecom boards, modem banks, and other noise-sensitive applications.

ORDERING INFORMATION

T_J	VOLTAGE(1)	SOT223-5(2)	SYMBOL	DDPAK(3)	D(4)	SYMBOL
-40°C to 125°C	Adjustable (1.2 V to 5 V)	TPS72501DCQ	PS72501	TPS72501KTT	TPS72501D	TPS72501
	1.5 V	TPS72515DCQ	PS72515	TPS72515KTT	—	TPS72515
	1.6 V	TPS72516DCQ	PS72516	TPS72516KTT	—	TPS72516
	1.8 V	TPS72518DCQ	PS72518	TPS72518KTT	—	TPS72518
	2.5 V	TPS72525DCQ	PS72525	TPS72525KTT	—	TPS72525

(1) Other voltage options are available upon request from the manufacturer.
(2) To order a taped and reeled part, add the suffix **R** to the part number (e.g., TPS72501DCQ**R**).
(3) To order a 50-piece reel, add the suffix **T** (e.g., TPS72501KTT**T**); to order a 500-piece reel, add the suffix **R** (e.g., TPS72501KTT**R**).
(4) To order a taped and reeled part, add the suffix **R** or **T** (2500 or 500) to the part number (e.g. TPS72501D**R**)

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

		UNIT
Input voltage, V_I (2)	-0.3 to 7	V
Voltage range at EN, FB	-0.3 to V_I + 0.3	V
Voltage on OUT, $\overline{\text{RESET}}$	6	V
ESD rating, HBM	2	kV
Continuous total power dissipation	See Dissipation Ratings Table	
Operating junction temperature range, T_J	-50 to 150	°C
Maximum junction temperature range, T_J	150	°C
Storage temperature, T_{stg}	-65 to 150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Input voltage, V_I (1)	1.8		6	V
Continuous output current, I_O	0		1	A
Operating junction temperature, T_J	-40		125	°C

(1) Minimum $V_I = V_O$ (nom) + V_{DO}.

PACKAGE DISSIPATION RATINGS

PACKAGE	BOARD	$R_{\theta JC}$	$R_{\theta JA}$
DDPAK	High K(1)	2 °C/W	23 °C/W
SOT223	Low K(2)	15 °C/W	53 °C/W
D-8	High K(1)	39.4 °C/W	55 °C/W

(1) The JEDEC high-K (2s2p) board design used to derive this data was a 3-inch x 3-inch (7.5-cm x 7.5-cm), multilayer board with 1 ounce internal power and ground planes and 2 ounce copper traces on top and bottom of the board.
(2) The JEDEC low-K (1s) board design used to derive this data was a 3-inch x 3-inch (7.5-cm x 7.5-cm), two-layer board with 2 ounce copper traces on top of the board.

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range $V_I = V_{O(typ)} + 1$ V, I_O= 1 mA, EN = IN, C_o = 1 µF, C_i = 1 µF (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
	Bandgap voltage reference				1.177	1.220	1.263	V
V_O	Output voltage	TPS72501 Adjustable	0 µA < I_O < 1 A(1)	1.22 V ≤ V_O ≤ 5.5 V	0.965 V_O		1.035 V_O	V
		TPS72515	T_J = 25°C			1.5		
			0 µA< I_O < 1 A	1.8 V ≤ V_I ≤ 5.5 V	1.47		1.53	
		TPS72516	T_J = 25°C			1.6		
			0 µA < I_O < 1 A	2.6 V ≤ V_I ≤ 5.5 V	1.568		1.632	
		TPS72518	T_J = 25°C			1.8		
			0 µA < I_O < 1 A	2.8 V ≤ V_I ≤ 5.5 V	1.764		1.836	
		TPS72525	T_J = 25°C			2.5		
			0 µA < I_O < 1 A	3.5 V ≤ V_I ≤ 5.5 V	2.45		2.55	
I	Ground current		I_O = 0 µA			75	120	µA
			I_O = 1 A			210	300	
	Standby current		EN < 0.4 V	T_J = 25°C		0.2		µA
			EN < 0.4 V				1	
V_n	Output noise voltage		BW = 200 Hz to 100 kHz, T_J = 25°C	C_o = 10 µF, I_O = 1 mA		150		µV
PSRR	Ripple rejection		f = 1 kHz, C_o = 10 µF	T_J = 25°C		60		dB
	Current limit(2)				1.1	1.6	2.3	A
	Output voltage line regulation ($\Delta V_O/V_O$)(3)		V_O + 1 V < V_I≤ 5.5 V		-0.15	0.02	0.15	%/V
	Output voltage load regulation		0 µA < I_O < 1 A		-0.25	0.05	0.25	%/A
V_{IH}	EN high level input(2)				1.3			V
V_{IL}	EN low level input(2)				-0.2		0.4	
I_I	EN input current		EN = 0 V or V_I			0.01	100	nA
$I_{(FB)}$	Feedback current		TPS72501	$V_{(FB)}$ = 1.22	-100		100	nA
	UVLO threshold		V_{CC} rising		1.45	1.57	1.70	V
	UVLO hysteresis		T_J = 25°C, V_{CC} rising			50		mV
	UVLO deglitch		T_J = 25°C, V_{CC} rising			10		µs
	UVLO delay		T_J = 25°C, V_{CC} rising			100		µs

(1) Minimum IN operating voltage used for testing is $V_{O(typ)}$ + 1 V.
(2) Test condition includes output voltage V_O = V_O - 15% and pulse duration = 10 ms.
(3) V_{Imin} = (V_O + 1) or 1.8 V whichever is greater.

$$\text{Line regulation (mV)} = (\%/V) \times \frac{V_O\left(5.5\ V - V_{Imin}\right)}{100} \times 1000$$

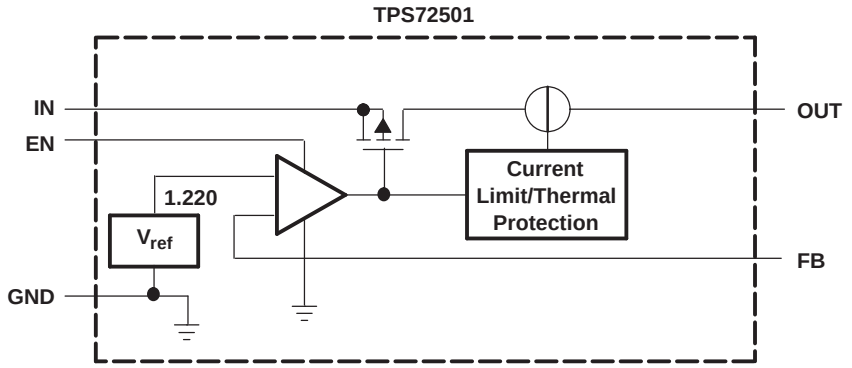
ELECTRICAL CHARACTERISTICS (continued)

over recommended operating free-air temperature range $V_I = V_{O(typ)} + 1$ V, I_O= 1 mA, EN = IN, C_o = 1 µF, C_i = 1 µF (unless otherwise noted)

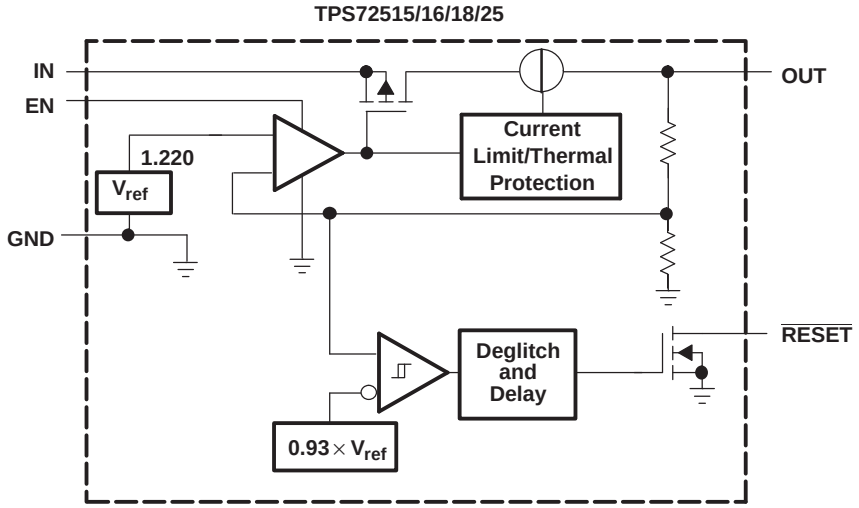
PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{DO}	Dropout voltage	TPS72525 (4)	I_O = 1 A	T_J = 25°C		170		mV
			I_O = 1 A				280	
		TPS72518 (5)	I_O = 1 A	T_J = 25°C		210		
			I_O = 1 A				320	
$\overline{RESET}$	Minimum input voltage for valid $\overline{RESET}$				1.3			V
	Trip threshold voltage				90	93	96	$\%V_O$
	Hysteresis voltage					10		mV
	$t_{(RESET)}$ delay time				25	50	75	ms
	Rising edge deglitch					10		µs
	Output low voltage (at 700 µA)				-0.3		0.4	V
	Leakage current						100	nA

(4) Dropout voltage is defined as the differential voltage between V_O and V_I when V_O drops 100 mV below the value measured with $V_I = V_O + 1$ V.
(5) Dropout voltage is defined as the differential voltage between V_O and V_I when V_O drops 100 mV below the value measured with $V_I = V_O + 1$ V.

FUNCTIONAL BLOCK DIAGRAM—ADJUSTABLE VERSION



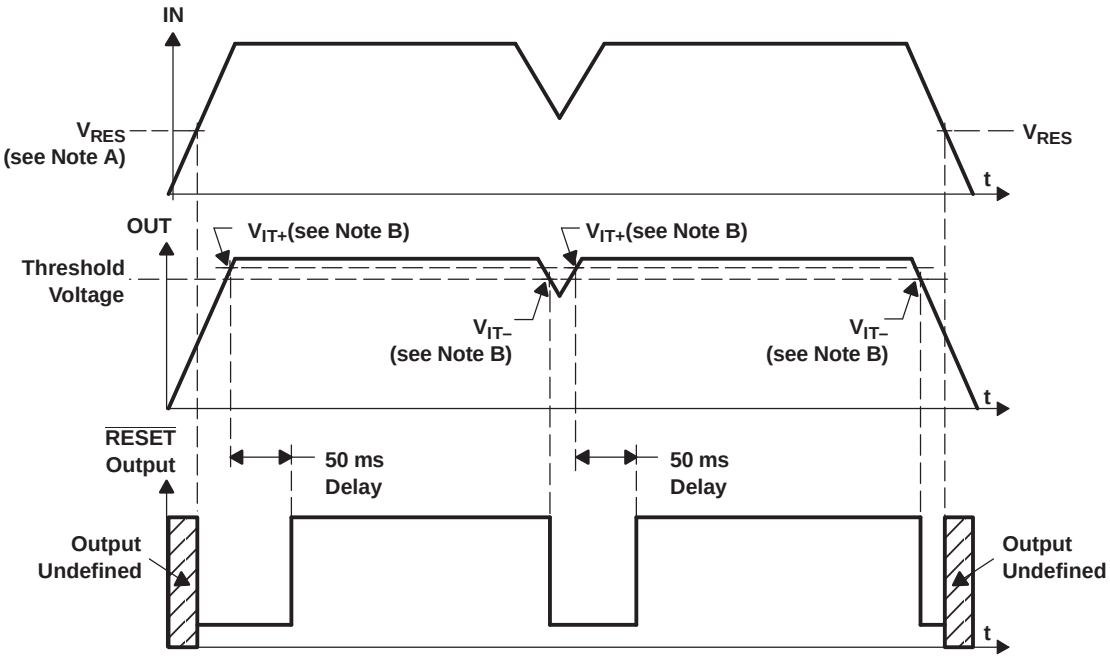
FUNCTIONAL BLOCK DIAGRAM—FIXED VERSION



TERMINAL FUNCTIONS

TERMINAL			I/O	DESCRIPTION
NAME	NO. D	NO.D CQ & KTT		
ENABLE	5	1	I	Enable input
FB	2			Feedback
GND	3, 6, 7	3		Ground
IN	8	2	I	Input supply voltage
$\overline{\text{RESET}}$/FB	—	5	O/I	This terminal is the feedback point for the adjustable option TPS72501. For all other options, this terminal is the $\overline{\text{RESET}}$ output terminal. When used with a pullup resistor, this open-drain output provides the active low $\overline{\text{RESET}}$ signal when the regulator output voltage drops more than 5% below its nominal output voltage. The $\overline{\text{RESET}}$ delay time is typically 50 ms.
NC	4	—		No connection
OUT	1	4	O	Regulated output voltage

$\overline{\text{RESET}}$ TIMING DIAGRAM



NOTES:A. V_{RES} is the minimum input voltage for a valid $\overline{\text{RESET}}$. The symbol V_{RES} is not currently listed within EIA or JEDEC standards for semiconductor symbology.

B. V_{IT} –Trip voltage is typically 7% lower than the output voltage (93%V_O) V_{IT-} to V_{IT+} is the hysteresis voltage.

TYPICAL CHARACTERISTICS

TPS72518
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

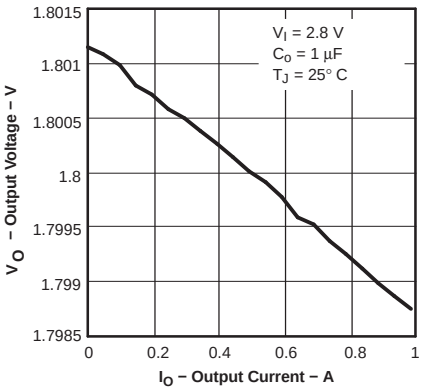


Figure 1.

TPS72518
OUTPUT VOLTAGE
vs
JUNCTION TEMPERATURE

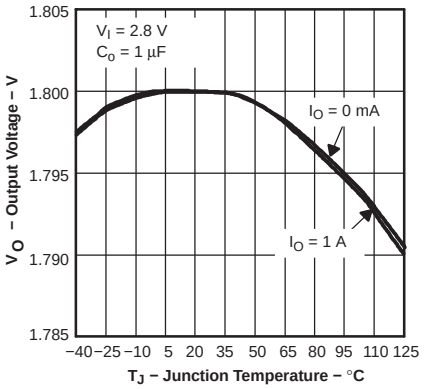


Figure 2.

TPS72518
GROUND CURRENT
vs
JUNCTION TEMPERATURE

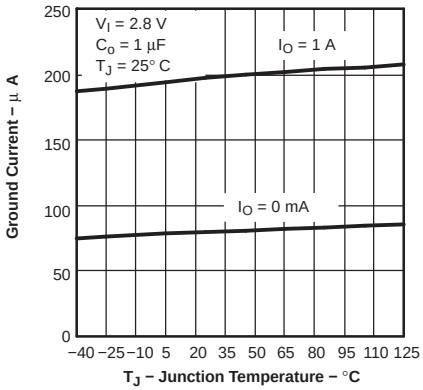


Figure 3.

TYPICAL CHARACTERISTICS (continued)

TPS72518
GROUND CURRENT
vs
OUTPUT CURRENT

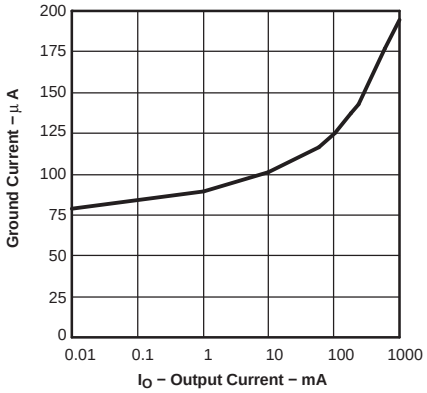


Figure 4.

TPS72525
DC DROPOUT VOLTAGE
vs
OUTPUT CURRENT

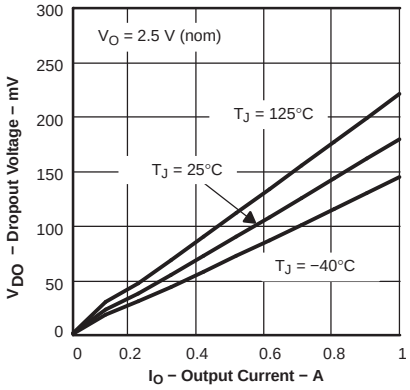


Figure 5.

TPS72518
DROPOUT VOLTAGE
vs
JUNCTION TEMPERATURE

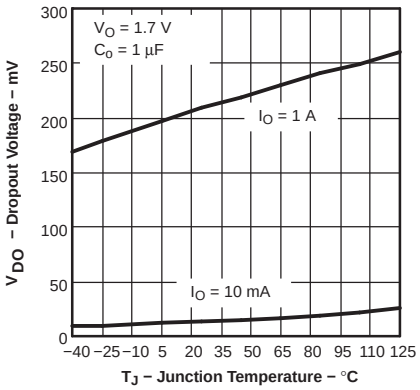


Figure 6.

MINIMUM REQUIRED
INPUT VOLTAGE
vs
OUTPUT VOLTAGE

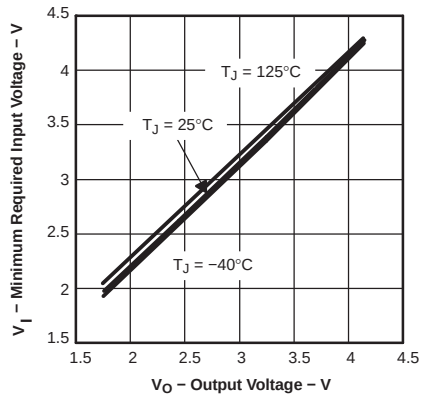


Figure 7.

TPS72518
LINE TRANSIENT RESPONSE

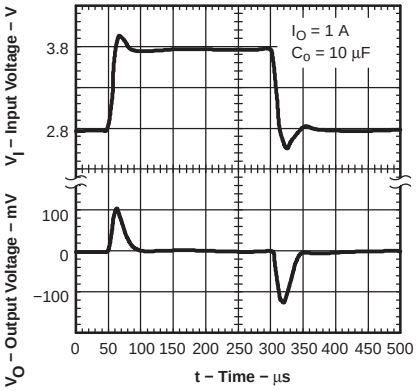


Figure 8.

TPS72518
LOAD TRANSIENT RESPONSE

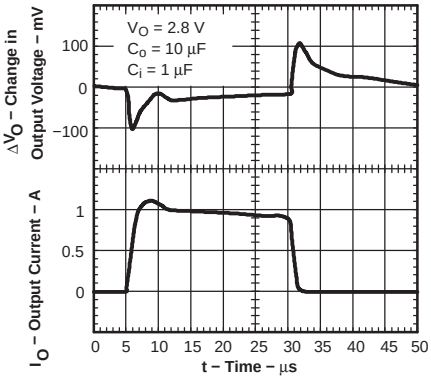


Figure 9.

TYPICAL CHARACTERISTICS (continued)

TPS72518 LOAD TRASIENT RESPONSE

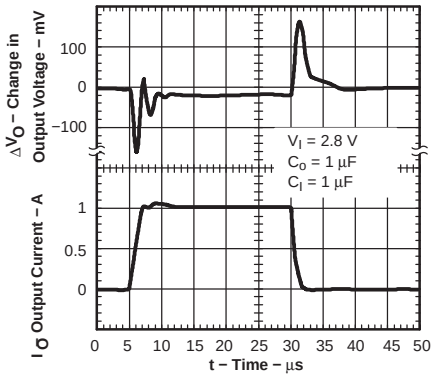


Figure 10.

TPS72518 OUTPUT VOLTAGE, ENABLE VOLTAGE vs TIME (START-UP)

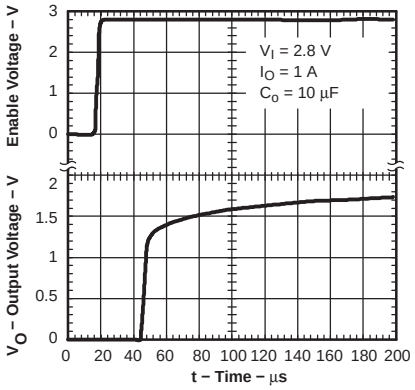


Figure 11.

TPS72518 POWER UP/POWER DOWN

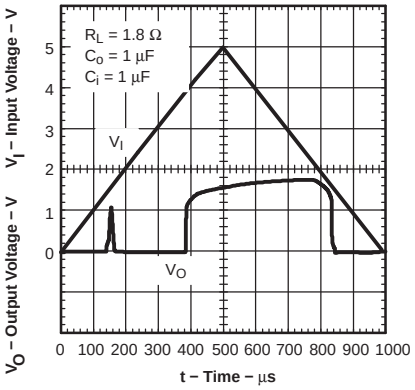


Figure 12.

TPS72518 OUTPUT SPECTRAL NOISE DENSITY vs FREQUENCY

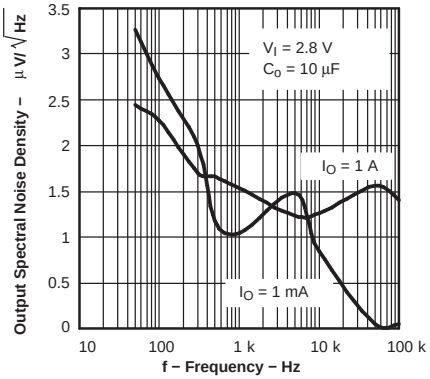


Figure 13.

TPS72518 RIPPLE REJECTION vs FREQUENCY

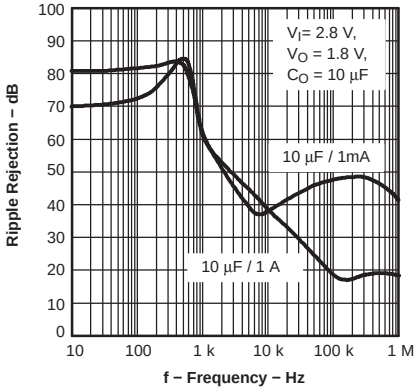


Figure 14.

CURRENT LIMIT vs INPUT VOLTAGE

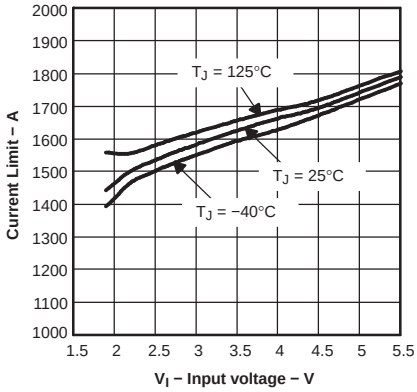


Figure 15.

TPS72515 GROUND CURRENT vs INPUT VOLTAGE

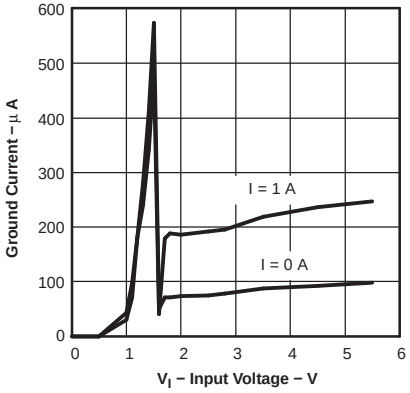


Figure 16.

DROPOUT VOLTAGE vs INPUT VOLTAGE

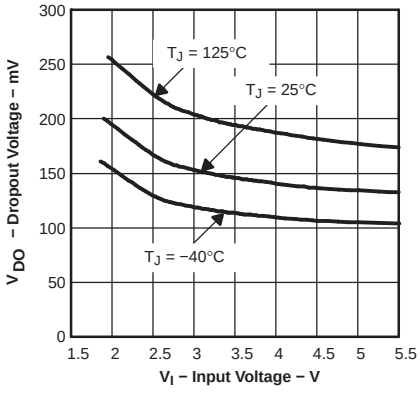


Figure 17.

APPLICATION INFORMATION

The TPS725xx family of low-dropout (LDO) regulators has numerous features that make it applicable to a wide range of applications. The family operates with very low input voltage (≥1.8 V) and low dropout voltage (typically 200 mV at full load), making it an efficient stand-alone power supply or post regulator for battery or switch mode power supplies. Both the active low $\overline{\text{RESET}}$ and 1-A output current make the TPS725xx family ideal for powering processor and FPGA supplies. The TPS725xx family also has low output noise (typically 150 μV_{RMS} with 10-µF output capacitor), making it ideal for use in telecom equipment.

External Capacitor Requirements

A 1-µF or larger ceramic input bypass capacitor, connected between IN and GND and located close to the TPS725xx, is required for stability. To improve transient response, noise rejection, and ripple rejection, an additional 10-µF or larger, low ESR capacitor is recommended. A higher-value, low ESR input capacitor may be necessary if large, fast-rise-time load transients are anticipated and the device is located several inches from the power source, especially if the minimum input voltage of 1.8 V is used.

Although an output capacitor is not required for stability, transient response and output noise are improved with a 10-µF output capacitor.

Programming the TPS72501 Adjustable LDO Regulator

The output voltage of the TPS72501 adjustable regulator is programmed using an external resistor divider as shown in Figure 18. The output voltage is calculated using:

$$V_O = V_{ref} \times \left(1 + \frac{R1}{R2}\right) \quad (1)$$

Where:

- $V_{FB} = V_{REF} = 1.22$ V typical (see the electrical characteristics for V_{REF} range)

Resistors R1 and R2 should be chosen for approximately 10-µA divider current. Lower value resistors offer no inherent advantage and waste more power. Higher values should be avoided as leakage currents at FB increase the output voltage error. The recommended design procedure is to choose R2 = 120 kΩ to set the divider current at 10 µA and then calculate R1 using:

$$R1 = \left(\frac{V_O}{V_{ref}} - 1\right) \times R2 \quad (2)$$

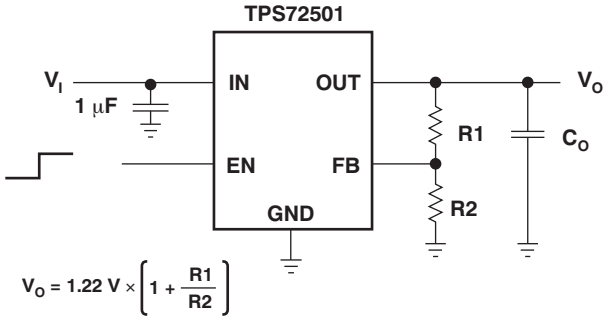


Figure 18. TPS72501 Adjustable Typical Application Diagram

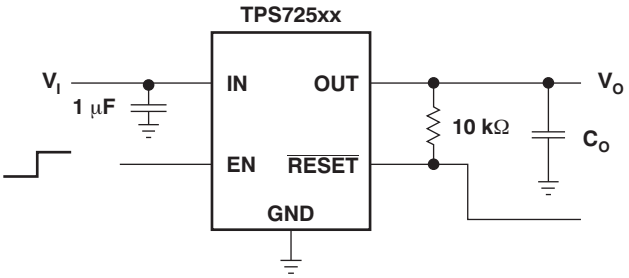


Figure 19. TPS72501 Fixed Output Typical Application Diagram

Table 1. Output Voltage Programming Guide (Standard 1% Resistor Values)

PROGRAM VOLTAGE	R1 (kΩ)	R2 (kΩ)	ACTUAL VOLTAGE
1.8 V	56.2	118	1.801
2.5 V	127	121	2.5
3.3 V	196	115	3.299
3.6 V	205	105	3.602

Regulator Protection

The TPS725xx pass element has a built-in back diode that safely conducts reverse current when the input voltage drops below the output voltage (e.g., during power down). Current is conducted from the output to the input and is not internally limited. If extended reverse voltage is anticipated, external limiting might be appropriate.

The TPS725xx also features internal current limiting and thermal protection. During normal operation, the TPS725xx limits output current to approximately 1.6 A. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds 165°C, thermal-protection circuitry shuts it down. Once the device has cooled down to below 145°C, regulator operation resumes.

THERMAL INFORMATION

The amount of heat that an LDO linear regulator generates is directly proportional to the amount of power it dissipates during operation. All integrated circuits have a maximum allowable junction temperature ($T_J$max) above which normal operation is not assured. A system designer must design the operating environment so that the operating junction temperature (T_J) does not exceed the maximum junction temperature ($T_J$max). The two main environmental variables that a designer can use to improve thermal performance are air flow and external heatsinks. The purpose of this information is to aid the designer in determining the proper operating environment for a linear regulator that is operating at a specific power level.

In general, the maximum expected power ($P_{D(max)}$) consumed by a linear regulator is computed as:

$$P_D max = \left(V_{I(avg)} - V_{O(avg)}\right) \times I_{O(avg)} + V_{I(avg)} \times I_{(Q)} \quad (3)$$

Where:

- $V_{I(avg)}$ is the average input voltage.
- $V_{O(avg)}$ is the average output voltage.
- $I_{O(avg)}$ is the average output current.
- $I_{(Q)}$ is the quiescent current.

For most TI LDO regulators, the quiescent current is insignificant compared to the average output current; therefore, the term $V_{I(avg)} \times I_{(Q)}$ can be neglected. The operating junction temperature is computed by adding the ambient temperature (T_A) and the increase in temperature due to the regulator's power dissipation. The temperature rise is computed by multiplying the maximum expected power dissipation by the sum of the thermal resistances between the junction and the case ($R_{\theta JC}$), the case to heatsink ($R_{\theta CS}$), and the heatsink to ambient ($R_{\theta SA}$). Thermal resistances are measures of how effectively an object dissipates heat. Typically, the larger the device, the more surface area available for power dissipation and the lower the object's thermal resistance.

Figure 20 illustrates these thermal resistances for (a) a SOT223 package mounted in a JEDEC low-K board, and (b) a DDPAK package mounted on a JEDEC high-K board.

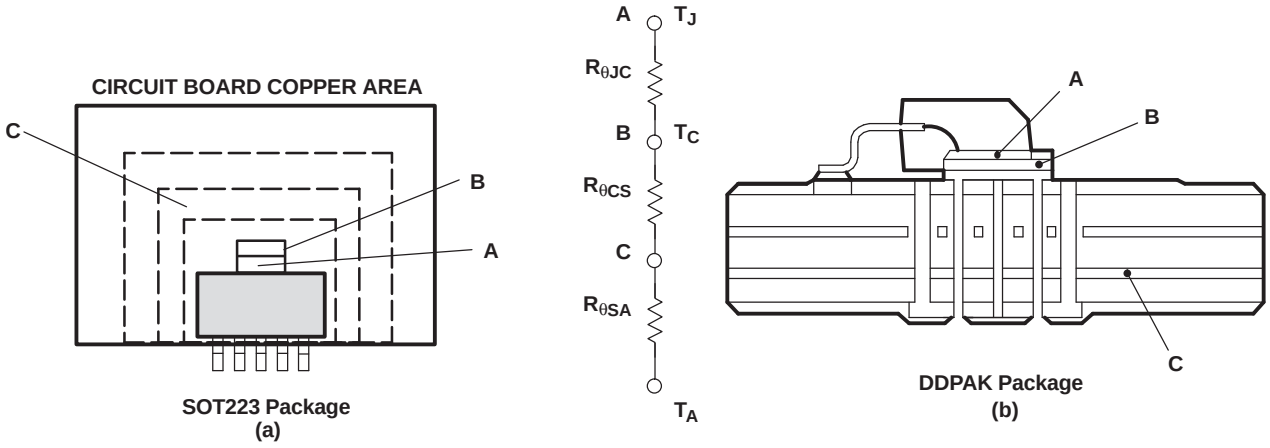


Figure 20. Thermal Resistances

Equation 4 summarizes the computation:

$$T_J = T_A + P_D max \times \left(R_{\theta JC} + R_{\theta CS} + R_{\theta SA}\right) \quad (4)$$

The $R_{\theta JC}$ is specific to each regulator as determined by its package, lead frame, and die size provided in the regulator's data sheet. The $R_{\theta SA}$ is a function of the type and size of heatsink. For example, *black body radiator* type heatsinks can have $R_{\theta CS}$ values ranging from 5°C/W for very large heatsinks to 50°C/W for very small heatsinks. The $R_{\theta CS}$ is a function of how the package is attached to the heatsink. For example, if a thermal compound is used to attach a heatsink to a SOT223 package, $R_{\theta CS}$of 1°C/W is reasonable.

Even if no external *black body radiator* type heatsink is attached to the package, the board on which the regulator is mounted provides some heatsinking through the pin solder connections. Some packages, like the DDPAK and SOT223 packages, use a copper plane underneath the package or the circuit board's ground plane for additional heatsinking to improve their thermal performance. Computer-aided thermal modeling can be used to compute very accurate approximations of an integrated circuit's thermal performance in different operating environments (e.g., different types of circuit boards, different types and sizes of heatsinks, different air flows, etc.). Using these models, the three thermal resistances can be combined into one thermal resistance between junction and ambient ($R_{\theta JA}$). This $R_{\theta JA}$is valid only for the specific operating environment used in the computer model.

Equation 4 simplifies into Equation 5:

$$T_J = T_A + P_D\text{max} \times R_{\theta JA} \quad (5)$$

Rearranging Equation 5 gives Equation 6:

$$R_{\theta JA} = \frac{T_J - T_A}{P_D\text{max}} \quad (6)$$

Using Equation 5 and the computer model generated curves shown in Figure 21 and Figure 24, a designer can quickly compute the required heatsink thermal resistance/board area for a given ambient temperature, power dissipation, and operating environment.

DDPAK Power Dissipation

The DDPAK package provides an effective means of managing power dissipation in surface mount applications. The DDPAK package dimensions are provided in the *Mechanical Data* section at the end of the data sheet. The addition of a copper plane directly underneath the DDPAK package enhances the thermal performance of the package.

To illustrate, the TPS72525 in a DDPAK package was chosen. For this example, the average input voltage is 5 V, the output voltage is 2.5 V, the average output current is 1 A, the ambient temperature 55°C, the air flow is 150 LFM, and the operating environment is the same as documented below. Neglecting the quiescent current, the maximum average power is:

$$P_D\text{max} = (5 - 2.5)\ \text{V} \times 1\ \text{A} = 2.5\ \text{W} \quad (7)$$

Substituting $T_J$max for T_J into Equation 6 gives Equation 8:

$$R_{\theta JA}\text{max} = (125 - 55)°\text{C}/2.5\ \text{W} = 28°\text{C/W} \quad (8)$$

From Figure 21, DDPAK Thermal Resistance vs Copper Heatsink Area, the ground plane needs to be 1 cm^2 for the part to dissipate 2.5 W. The operating environment used in the computer model to construct Figure 21 consisted of a standard JEDEC High-K board (2S2P) with a 1 oz. internal copper plane and ground plane. The package is soldered to a 2 oz. copper pad. The pad is tied through thermal vias to the 1 oz. ground plane. Figure 22 shows the side view of the operating environment used in the computer model.

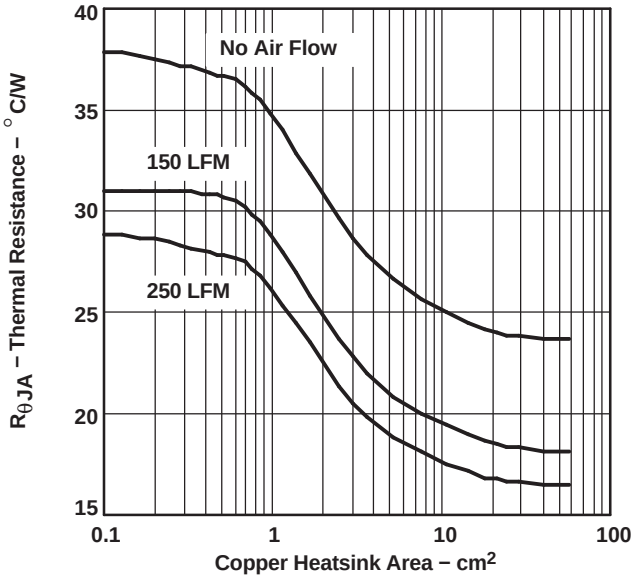


Figure 21. DDPAK Thermal Resistance vs Copper Heatsink Area

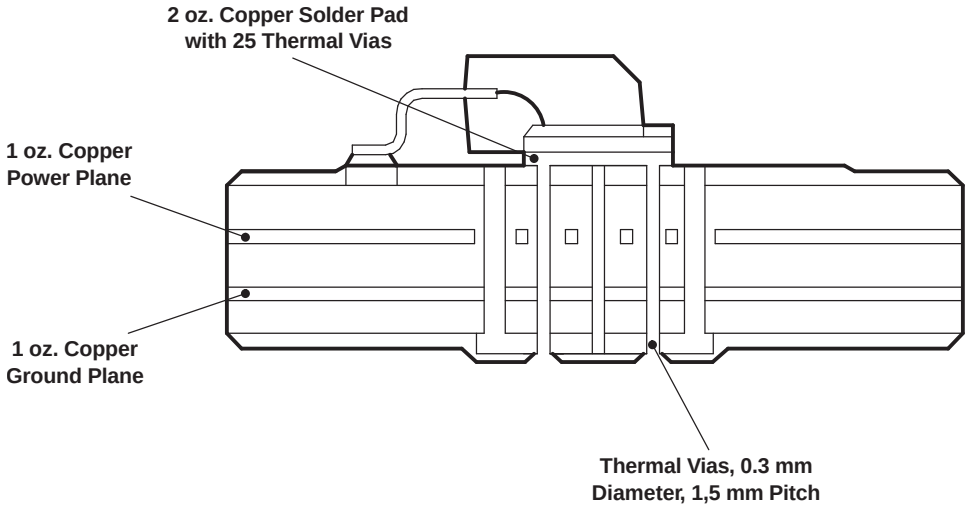


Figure 22. DDPAK Thermal Resistance

From the data in Figure 23 and rearranging Equation 6, the maximum power dissipation for a different ground plane area and a specific ambient temperature can be computed.

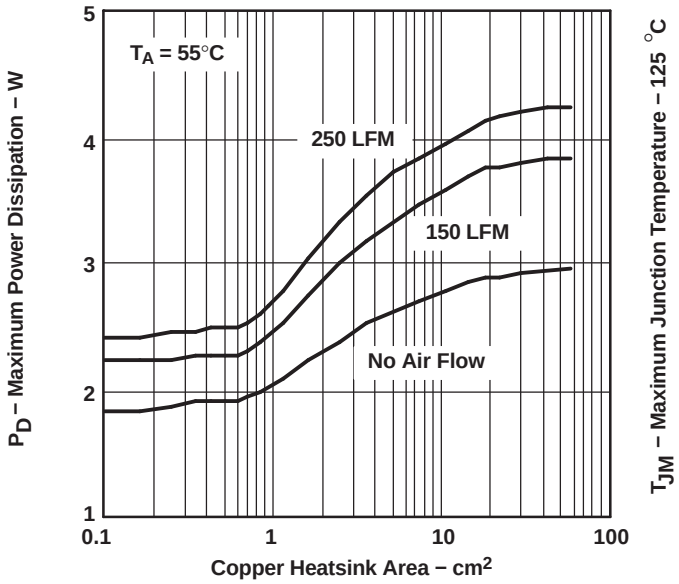


Figure 23. Maximum Power Dissipation vs Copper Heatsink Area

SOT223 Power Dissipation

The SOT223 package provides an effective means of managing power dissipation in surface mount applications. The SOT223 package dimensions are provided in the *Mechanical Data* section at the end of the data sheet. The addition of a copper plane directly underneath the SOT223 package enhances the thermal performance of the package.

To illustrate, the TPS72525 in a SOT223 package was chosen. For this example, the average input voltage is 3.3 V, the output voltage is 2.5 V, the average output current is 1 A, the ambient temperature 55°C, no air flow is present, and the operating environment is the same as documented below. Neglecting the quiescent current, the maximum average power is:

$$P_D\text{max} = (3.3 - 2.5)\ \text{V} \times 1\ \text{A} = 800\ \text{mW} \quad (9)$$

Substituting $T_J$max for T_J into Equation 6 gives Equation 10:

$$R_{\theta JA}\text{max} = (125 - 55)°\text{C}/800\ \text{mW} = 87.5°\text{C/W} \quad (10)$$

From Figure 24, $R_{\Theta JA}$ vs PCB Copper Area, the ground plane needs to be 0.55 in^2 for the part to dissipate 800 mW. The operating environment used to construct Figure 24 consisted of a board with 1 oz. copper planes. The package is soldered to a 1 oz. copper pad on the top of the board. The pad is tied through thermal vias to the 1 oz. ground plane.

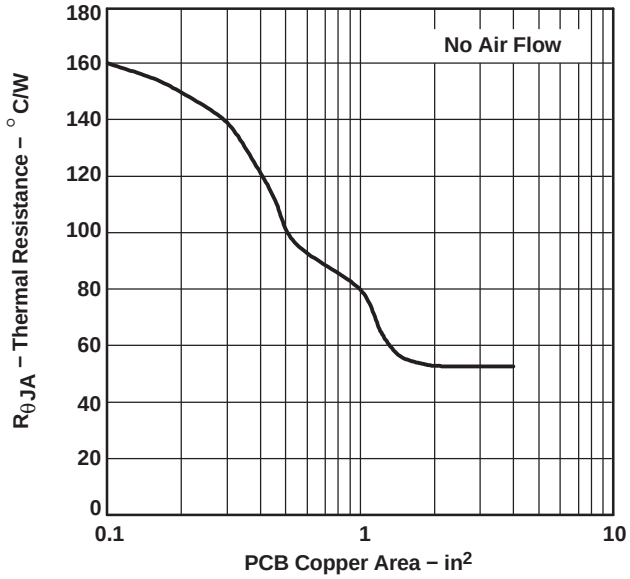


Figure 24. SOT223 Thermal Resistance vs PCB AREA

From the data in Figure 24 and rearranging Equation 6, the maximum power dissipation for a different ground plane area and a specific ambient temperature can be computed (as shown in Figure 25).

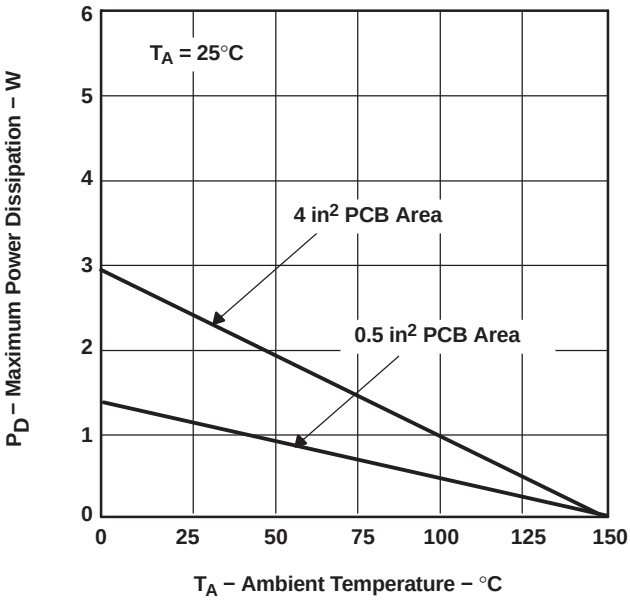


Figure 25. SOT223 Power Dissipation

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (March 2004) to Revision E	Page
• Deleted Figure 14, *Output Impedance vs Frequency*	8
• Updated Figure 18	9
• Added Figure 19	10
• Added Table 1, *Output Voltage Programming Guide*	10

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS72501DCQ	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS72501	Samples
TPS72501DCQG4	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS72501	Samples
TPS72501DCQR	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS72501	Samples
TPS72501DCQRG4	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS72501	Samples
TPS72501DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 72501	Samples
TPS72501DT	ACTIVE	SOIC	D	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 72501	Samples
TPS72501DTG4	ACTIVE	SOIC	D	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 72501	Samples
TPS72501KTTR	ACTIVE	DDPAK/ TO-263	KTT	5	500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	TPS 72501	Samples
TPS72501KTTRG3	ACTIVE	DDPAK/ TO-263	KTT	5	500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	TPS 72501	Samples
TPS72501KTTT	ACTIVE	DDPAK/ TO-263	KTT	5	50	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	TPS 72501	Samples
TPS72515DCQ	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS72515	Samples
TPS72515DCQG4	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS72515	Samples
TPS72515DCQR	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS72515	Samples
TPS72515DCQRG4	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS72515	Samples
TPS72515KTTR	ACTIVE	DDPAK/ TO-263	KTT	5	500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR		TPS 72515	Samples
TPS72515KTTT	ACTIVE	DDPAK/ TO-263	KTT	5	50	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	TPS 72515	Samples
TPS72515KTTTG3	ACTIVE	DDPAK/ TO-263	KTT	5	50	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	TPS 72515	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS72516DCQ	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS72516	Samples
TPS72516DCQR	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS72516	Samples
TPS72516DCQRG4	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS72516	Samples
TPS72516KTTT	ACTIVE	DDPAK/ TO-263	KTT	5	50	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	TPS 72516	Samples
TPS72518DCQ	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS72518	Samples
TPS72518DCQG4	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS72518	Samples
TPS72518DCQR	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS72518	Samples
TPS72518DCQRG4	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS72518	Samples
TPS72518KTTR	ACTIVE	DDPAK/ TO-263	KTT	5	500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR		TPS 72518	Samples
TPS72518KTTRG3	ACTIVE	DDPAK/ TO-263	KTT	5	500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR		TPS 72518	Samples
TPS72518KTTT	ACTIVE	DDPAK/ TO-263	KTT	5	50	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	TPS 72518	Samples
TPS72518KTTTG3	ACTIVE	DDPAK/ TO-263	KTT	5	50	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	TPS 72518	Samples
TPS72525DCQ	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS72525	Samples
TPS72525DCQG4	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS72525	Samples
TPS72525DCQR	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS72525	Samples
TPS72525DCQRG4	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS72525	Samples
TPS72525KTTR	ACTIVE	DDPAK/ TO-263	KTT	5	500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR		TPS 72525	Samples
TPS72525KTTRG3	ACTIVE	DDPAK/ TO-263	KTT	5	500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR		TPS 72525	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS72525KTTT	ACTIVE	DDPAK/ TO-263	KTT	5	50	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	TPS 72525	Samples
TPS72525KTTTG3	ACTIVE	DDPAK/ TO-263	KTT	5	50	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	TPS 72525	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

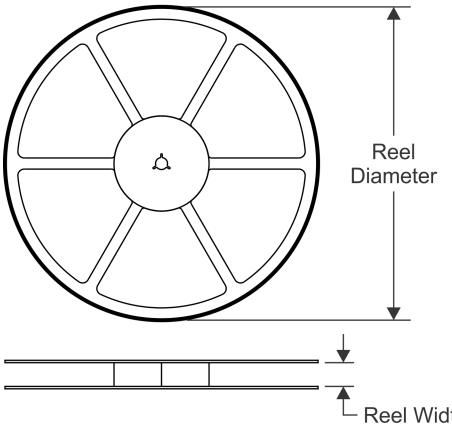
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

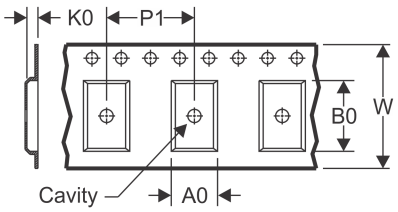
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

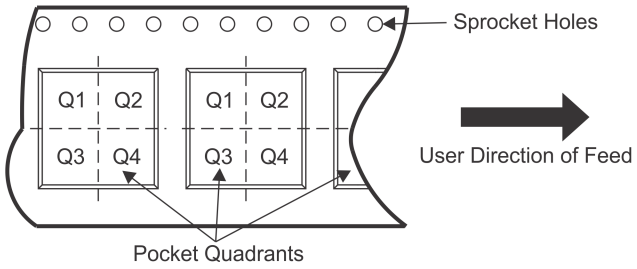


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

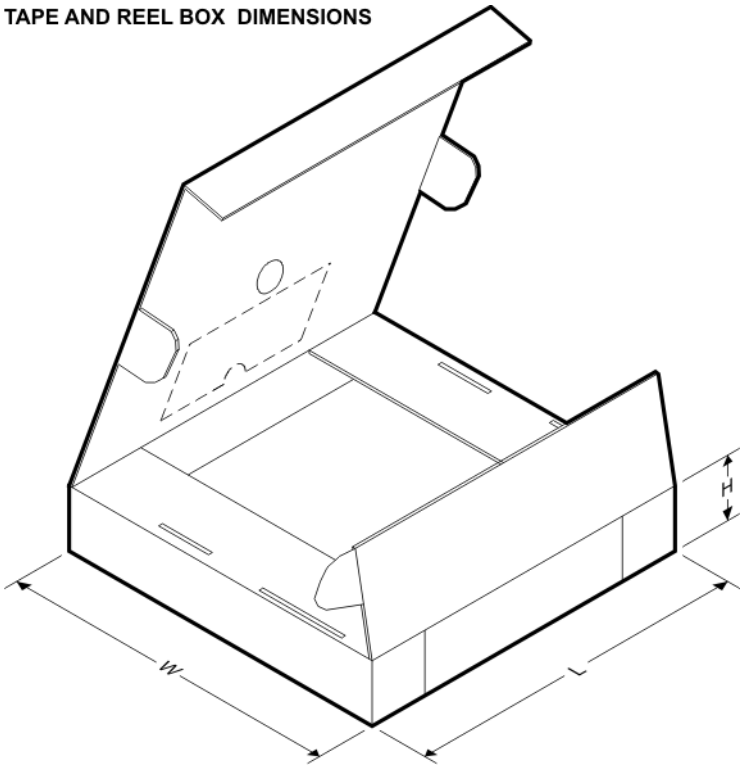


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS72501DCQR	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3
TPS72501DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS72501DT	SOIC	D	8	250	180.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS72501KTTR	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.6	15.6	4.9	16.0	24.0	Q2
TPS72501KTTT	DDPAK/ TO-263	KTT	5	50	330.0	24.4	10.6	15.6	4.9	16.0	24.0	Q2
TPS72515DCQR	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3
TPS72515KTTR	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.6	15.6	4.9	16.0	24.0	Q2
TPS72515KTTT	DDPAK/ TO-263	KTT	5	50	330.0	24.4	10.6	15.6	4.9	16.0	24.0	Q2
TPS72516DCQR	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3
TPS72516KTTT	DDPAK/ TO-263	KTT	5	50	330.0	24.4	10.6	15.6	4.9	16.0	24.0	Q2
TPS72518DCQR	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3
TPS72518KTTR	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.6	15.6	4.9	16.0	24.0	Q2
TPS72518KTTT	DDPAK/ TO-263	KTT	5	50	330.0	24.4	10.6	15.6	4.9	16.0	24.0	Q2

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS72525DCQR	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3
TPS72525KTTR	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.6	15.6	4.9	16.0	24.0	Q2
TPS72525KTTT	DDPAK/ TO-263	KTT	5	50	330.0	24.4	10.6	15.6	4.9	16.0	24.0	Q2

TAPE AND REEL BOX DIMENSIONS

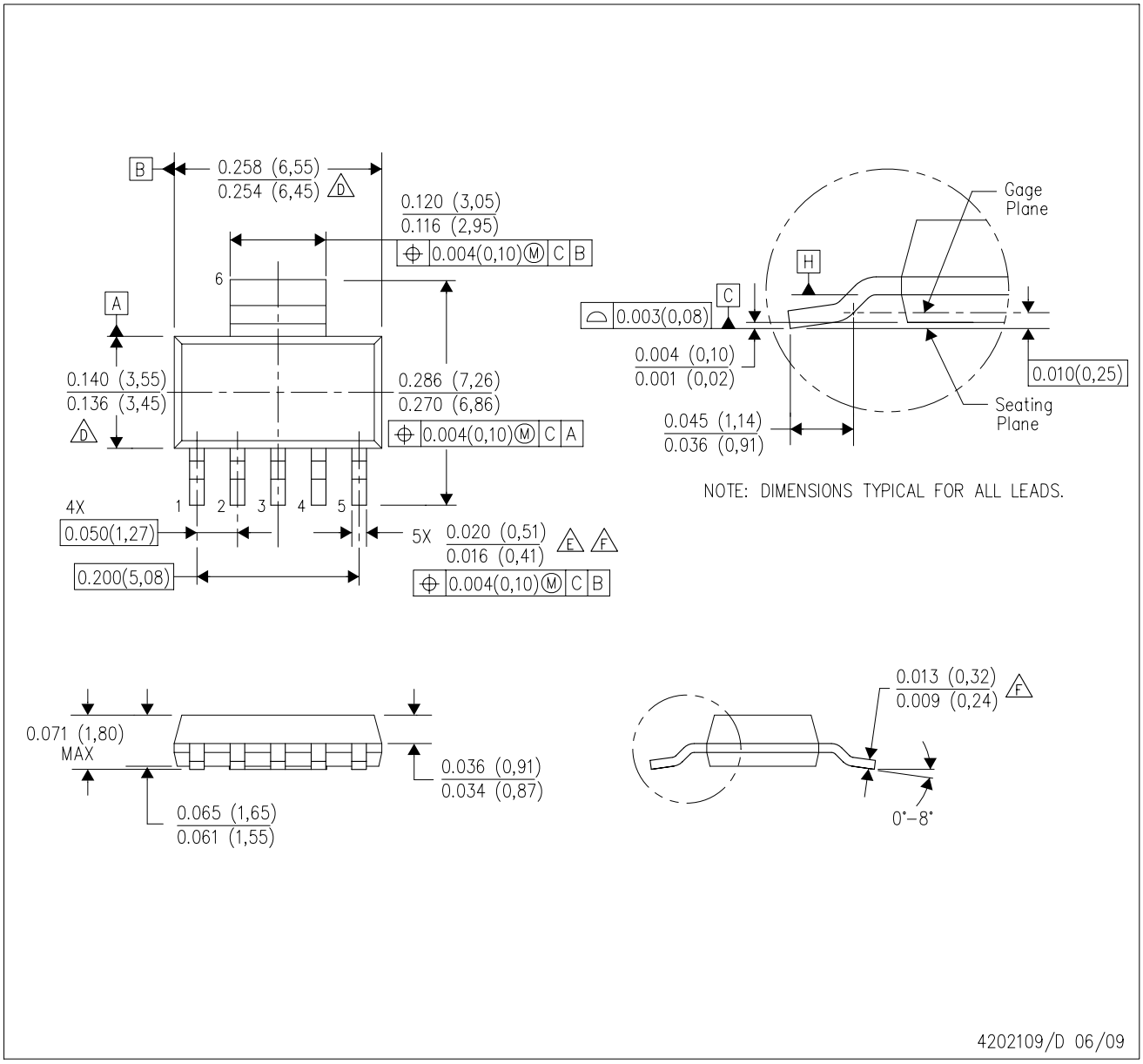


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS72501DCQR	SOT-223	DCQ	6	2500	358.0	335.0	35.0
TPS72501DR	SOIC	D	8	2500	367.0	367.0	35.0
TPS72501DT	SOIC	D	8	250	210.0	185.0	35.0
TPS72501KTTR	DDPAK/TO-263	KTT	5	500	367.0	367.0	45.0
TPS72501KTTT	DDPAK/TO-263	KTT	5	50	367.0	367.0	45.0
TPS72515DCQR	SOT-223	DCQ	6	2500	358.0	335.0	35.0
TPS72515KTTR	DDPAK/TO-263	KTT	5	500	367.0	367.0	45.0
TPS72515KTTT	DDPAK/TO-263	KTT	5	50	367.0	367.0	45.0
TPS72516DCQR	SOT-223	DCQ	6	2500	346.0	346.0	41.0
TPS72516KTTT	DDPAK/TO-263	KTT	5	50	367.0	367.0	45.0
TPS72518DCQR	SOT-223	DCQ	6	2500	358.0	335.0	35.0
TPS72518KTTR	DDPAK/TO-263	KTT	5	500	367.0	367.0	45.0

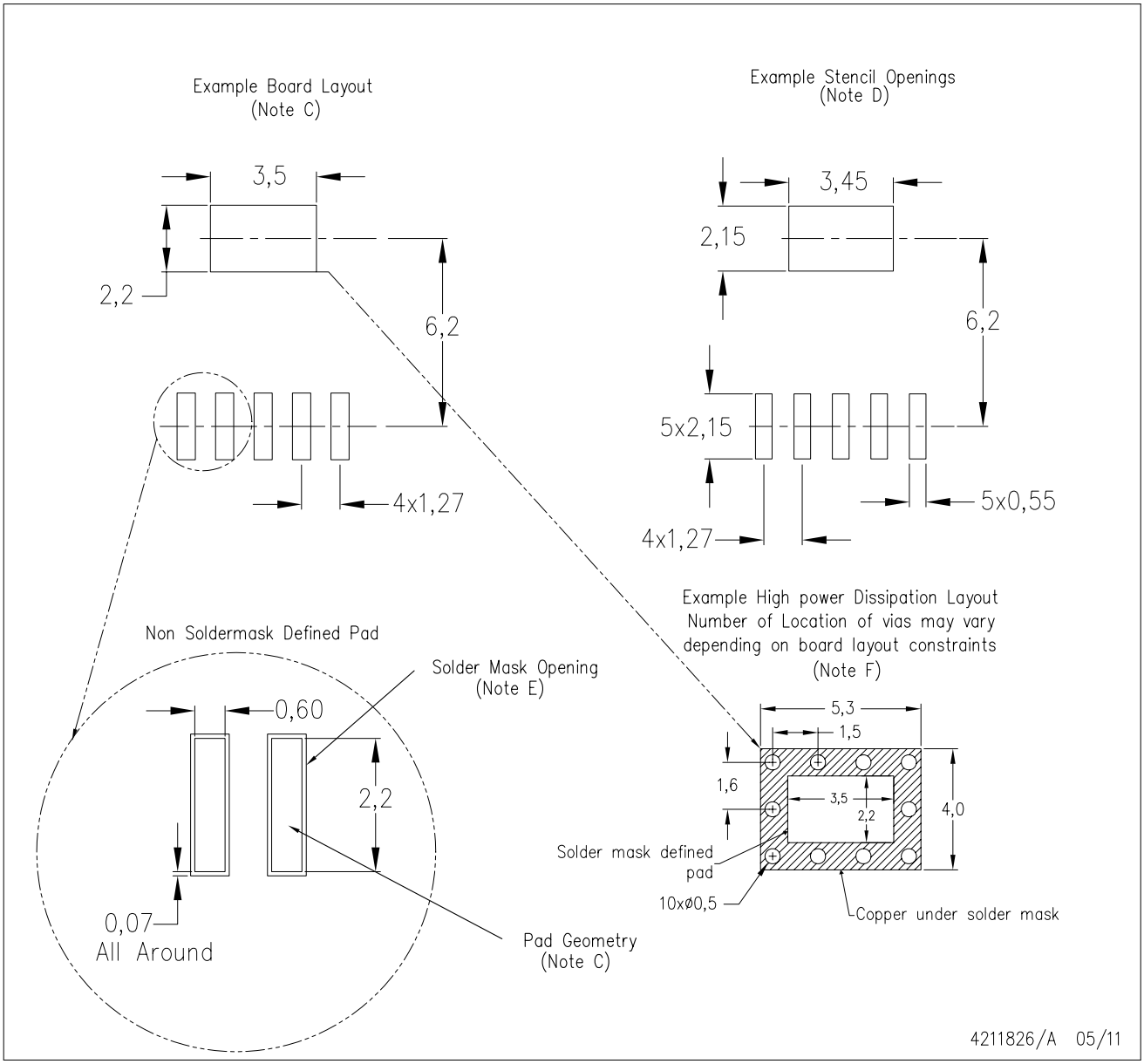
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS72518KTTT	DDPAK/TO-263	KTT	5	50	367.0	367.0	45.0
TPS72525DCQR	SOT-223	DCQ	6	2500	358.0	335.0	35.0
TPS72525KTTR	DDPAK/TO-263	KTT	5	500	367.0	367.0	45.0
TPS72525KTTT	DDPAK/TO-263	KTT	5	50	367.0	367.0	45.0

DCQ (R–PDSO–G6) PLASTIC SMALL–OUTLINE



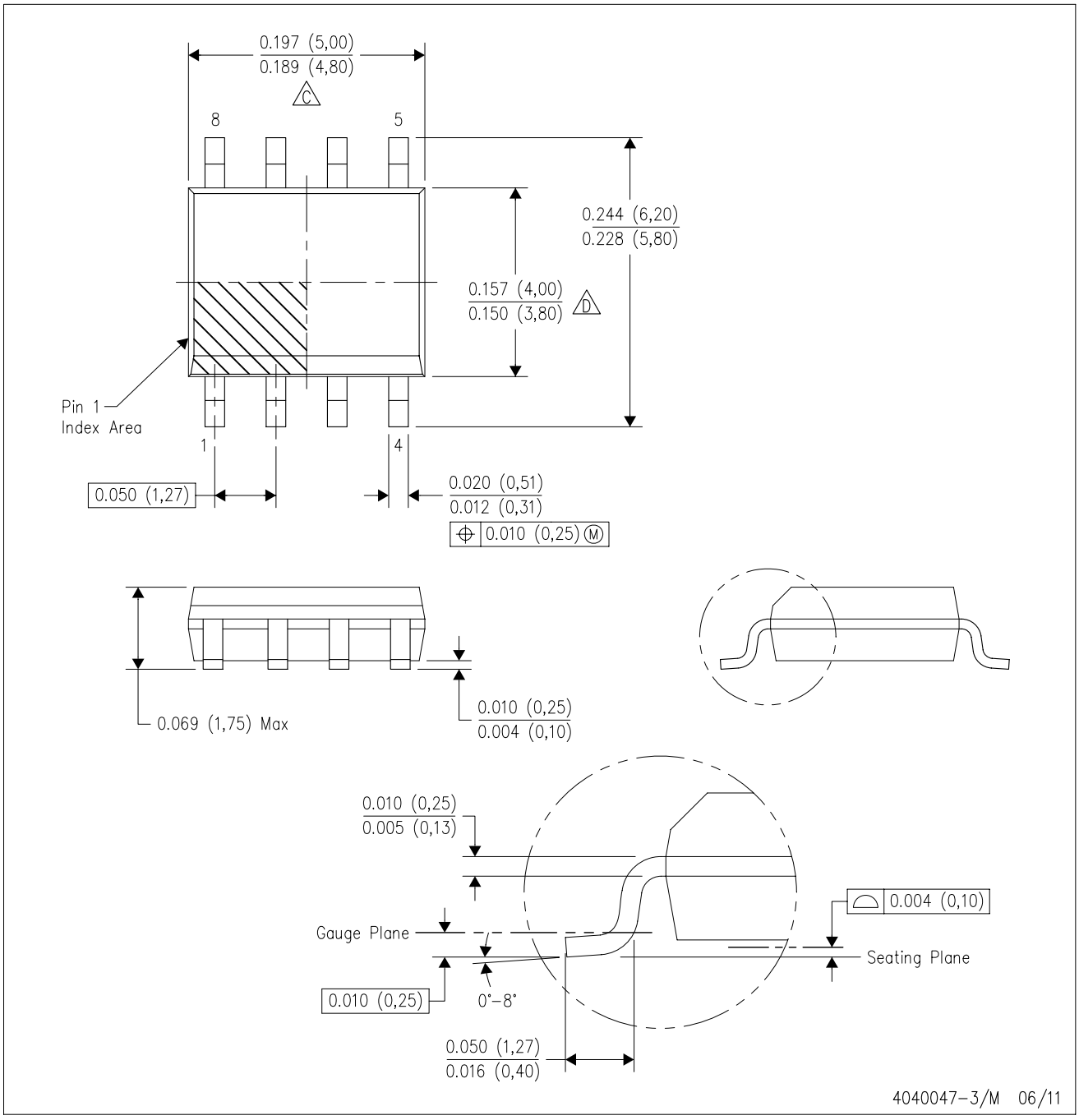
NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Controlling dimension in inches.
- D. Body length and width dimensions are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs, and interlead flash, but including any mismatch between the top and the bottom of the plastic body.
- E. Lead width dimension does not include dambar protrusion.
- F. Lead width and thickness dimensions apply to solder plated leads.
- G. Interlead flash allow 0.008 inch max.
- H. Gate burr/protrusion max. 0.006 inch.
- I. Datums A and B are to be determined at Datum H.

DCQ (R–PDSO–G6) PLASTIC SMALL OUTLINE



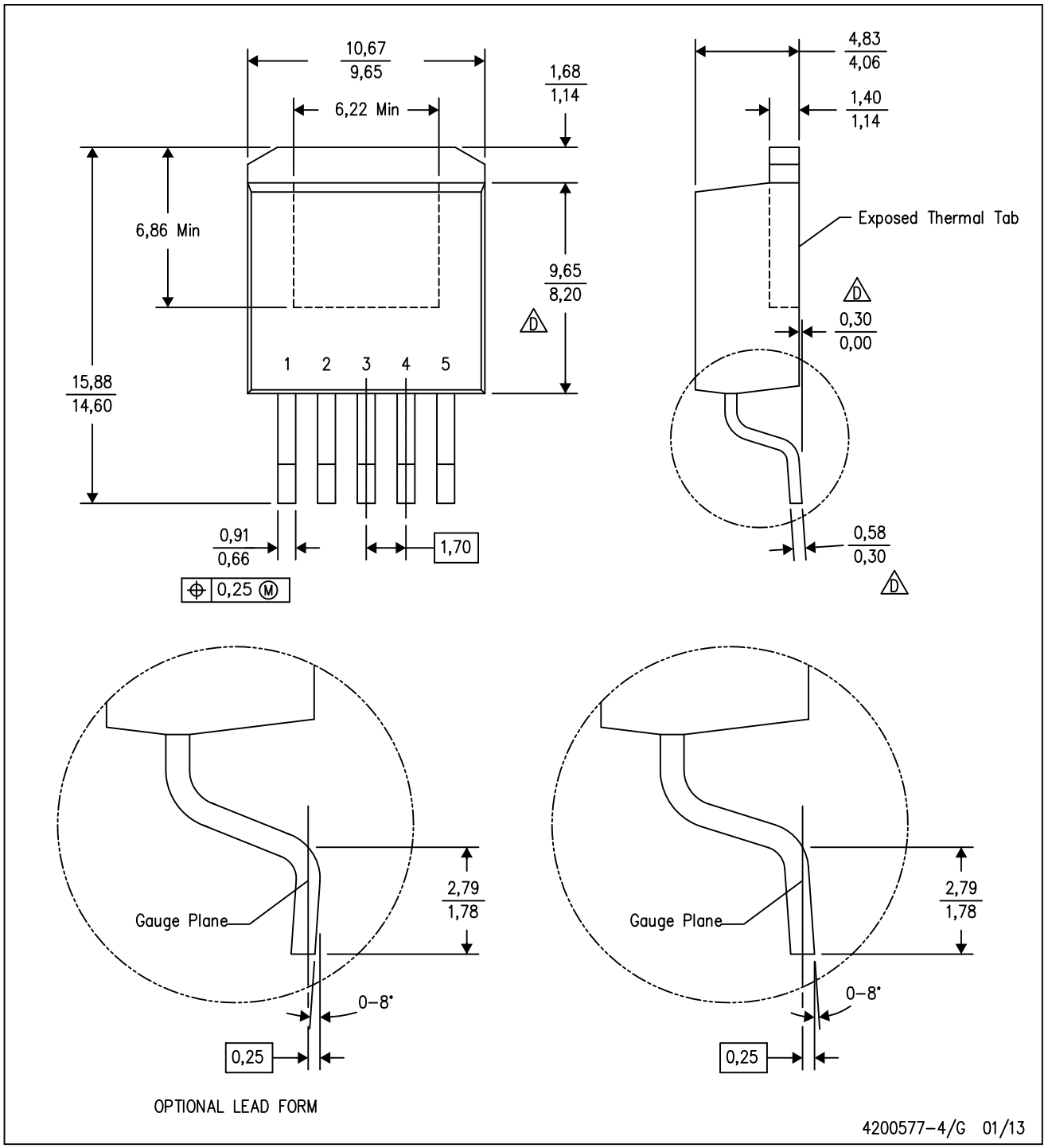
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–SM–782 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
F. Please refer to the product data sheet for specific via and thermal dissipation requirements.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



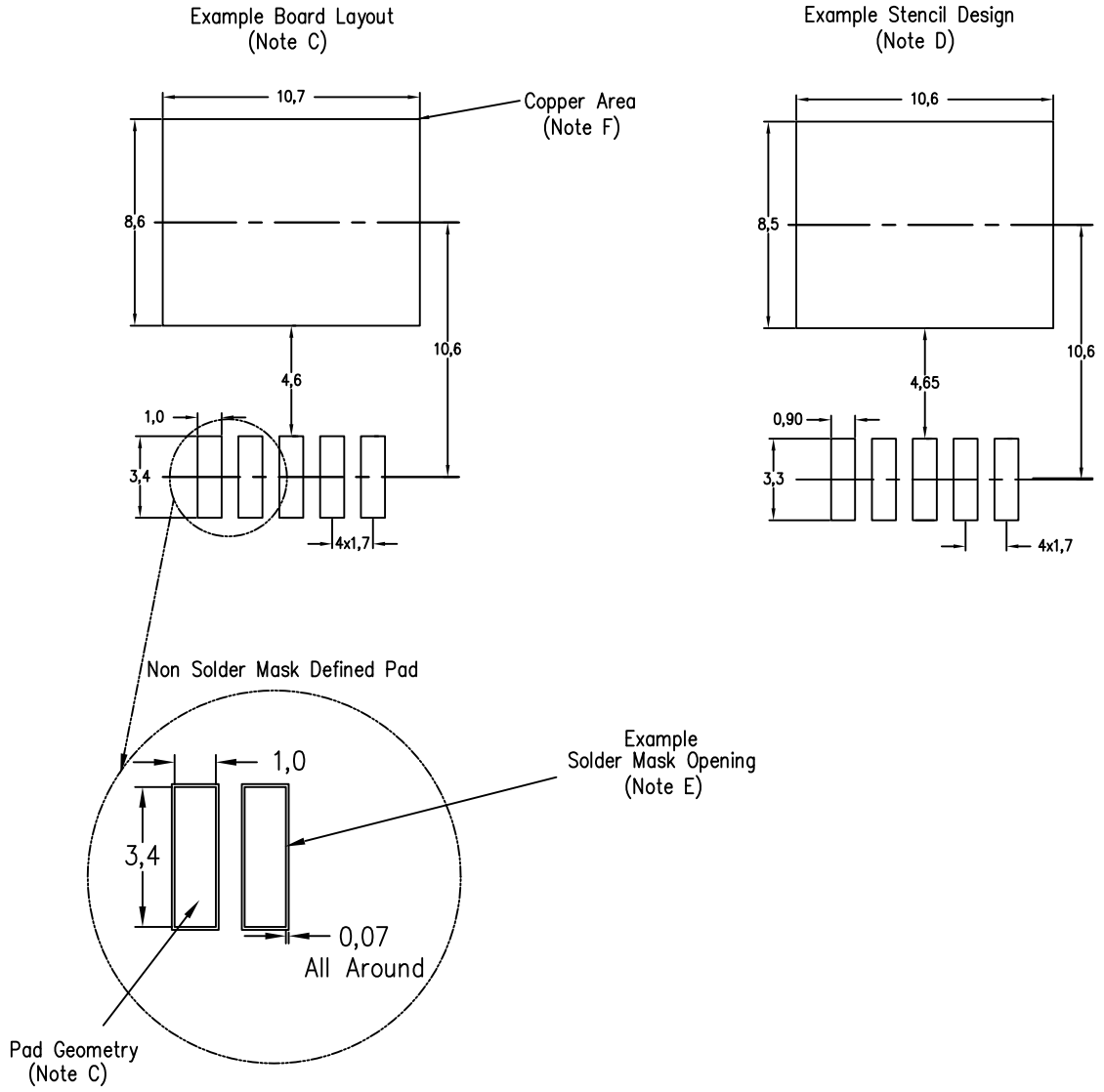
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

KTT (R–PSFM–G5) PLASTIC FLANGE–MOUNT PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash or protrusion not to exceed 0.005 (0,13) per side.
D. Falls within JEDEC TO–263 variation BA, except minimum lead thickness, maximum seating height, and minimum body length.

KTT (R–PSFM–G5) PLASTIC FLANGE–MOUNT PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–SM–782 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
F. This package is designed to be soldered to a thermal pad on the board. Refer to the Product Datasheet for specific thermal information, via requirements, and recommended thermal pad size. For thermal pad sizes larger than shown a solder mask defined pad is recommended in order to maintain the solderable pad geometry while increasing copper area.

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