

TPS799 200-mA, Low-Quiescent Current, Ultralow Noise, High-PSRR Low-Dropout Linear Regulator

1 Features

- 200-mA Low-Dropout Regulator With EN
- Multiple Output Voltage Versions Available:
 - Fixed Outputs of 1.2 V to 4.5 V Using Innovative Factory EEPROM Programming
 - Adjustable Outputs from 1.20 V to 6.5 V
- Inrush Current Protection with EN Toggle
- Low I_Q : 40 μ A
- High PSRR: 66 dB at 1 kHz
- Stable with a Low-ESR, 2- μ F Typical Output Capacitance
- Excellent Load and Line Transient Response
- 2% Overall Accuracy (Load, Line, and Temperature)
- Very Low Dropout: 100 mV
- Package: 5-Bump, Thin, 1-mm x 1.37-mm DSBGA

2 Applications

- Cellular Phones
- Wireless LAN, *Bluetooth*[®]
- VCOs, RF
- Handheld Organizers, PDAs

3 Description

The TPS799 family of low-dropout (LDO), low-power linear regulators offers excellent ac performance with very low ground current. High power-supply rejection ratio (PSRR), low noise, fast start-up, and excellent line and load transient response are provided while consuming a very low 40- μ A (typical) ground current.

The TPS799 is stable with ceramic capacitors and uses an advanced BiCMOS fabrication process to yield a dropout voltage of typically 100 mV at a 200-mA output. The TPS799 uses a precision voltage reference and feedback loop to achieve an overall accuracy of 2% over all load, line, process, and temperature variations. The TPS799 features inrush current protection when the EN toggle is used to start the device, immediately clamping the current.

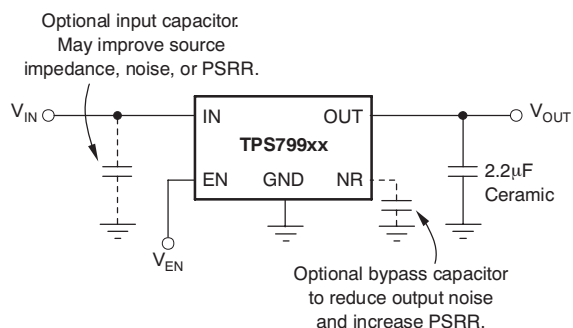
All devices are fully specified over the temperature range of $T_J = -40^\circ\text{C}$ to 125°C , and offered in a low-profile, die-sized ball grid array (DSBGA) package, ideal for wireless handsets and WLAN cards.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS799	SOT (5)	2.90 mm x 1.60 mm
	SON (6)	2.00 x 2.00 mm
	DSBGA (5)	1.57 mm x 1.20 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Circuit Fixed Voltage Versions



Typical Application Circuit Adjustable Voltage Version

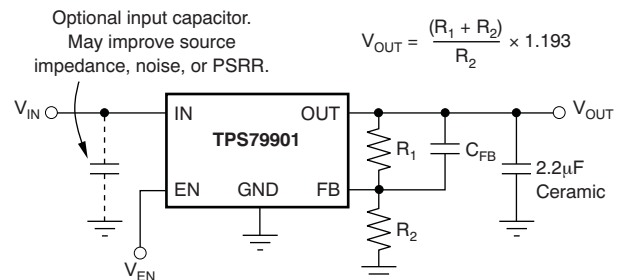


Table of Contents

<p>1 Features 1</p> <p>2 Applications 1</p> <p>3 Description 1</p> <p>4 Revision History 2</p> <p>5 Pin Configuration and Functions 3</p> <p> 5.1 Fixed Voltage Versions 3</p> <p> 5.2 Adjustable Voltage Versions 3</p> <p>6 Specifications 5</p> <p> 6.1 Absolute Maximum Ratings 5</p> <p> 6.2 ESD Ratings 5</p> <p> 6.3 Recommended Operating Conditions 5</p> <p> 6.4 Thermal Information 5</p> <p> 6.5 Electrical Characteristics 6</p> <p> 6.6 Typical Characteristics 7</p> <p>7 Detailed Description 12</p> <p> 7.1 Overview 12</p> <p> 7.2 Functional Block Diagram 12</p> <p> 7.3 Feature Description 13</p>	<p> 7.4 Device Functional Modes 13</p> <p>8 Application and Implementation 14</p> <p> 8.1 Application Information 14</p> <p> 8.2 Typical Applications 14</p> <p> 8.3 Do's and Don'ts 16</p> <p>9 Power Supply Recommendations 16</p> <p>10 Layout 16</p> <p> 10.1 Layout Guidelines 16</p> <p> 10.2 Layout Example 17</p> <p> 10.3 Thermal Information 17</p> <p>11 Device and Documentation Support 18</p> <p> 11.1 Device Support 18</p> <p> 11.2 Documentation Support 18</p> <p> 11.3 Trademarks 18</p> <p> 11.4 Electrostatic Discharge Caution 18</p> <p> 11.5 Glossary 18</p> <p>12 Mechanical, Packaging, and Orderable Information 18</p>
---	---

4 Revision History

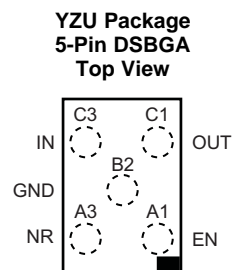
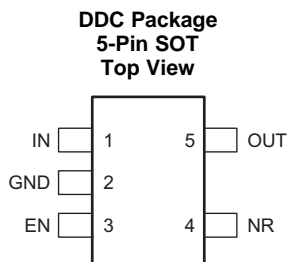
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision J (August 2010) to Revision K	Page
• Added <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section	1
• Changed Features list	1
• Changed Description section.....	1
• Changed figure on front page; replaced device pinouts with application circuits.....	1
• Changed Pin Configuration and Functions section; updated table format, renamed pin packages to meet new standards	3
• Changed "free-air" to "junction" temperature in condition statement for <i>Absolute Maximum Ratings</i>	5
• Changed <i>free-air</i> to <i>junction</i> in Recommended Operating Conditions table conditions.....	5
• Added thermal information for additional device packages	5

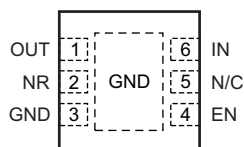
Changes from Revision I (November 2007) to Revision J	Page
• Replaced the <i>Dissipation Ratings</i> table with the <i>Thermal Information</i> table	5

5 Pin Configuration and Functions

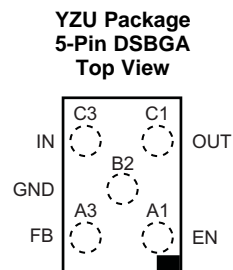
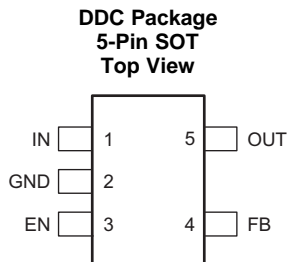
5.1 Fixed Voltage Versions



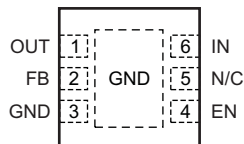
DRV Package
6-Pin SON With Exposed Thermal Pad
Top View



5.2 Adjustable Voltage Versions



DRV Package
6-Pin SON With Exposed Thermal Pad
Top View



Pin Functions

PIN				I/O	DESCRIPTION
NAME	DDC	YZY	DRV		
IN	1	C3	6	I	Input supply.
GND	2	B2	3, Pad	—	Ground. The pad must be tied to GND.
EN	3	A1	4	I	Driving this pin high turns on the regulator. Driving this pin low puts the regulator into shutdown mode. EN can be connected to IN if not used.
NR	4	A3	2	—	Fixed voltage versions only. Noise reduction; connecting this pin to an external capacitor bypasses noise generated by the internal band gap. This capacitor allows output noise to be reduced to very low levels.
FB	4	A3	2	I	Adjustable voltage version only. Feedback; this pin is the input to the control loop error amplifier, and sets the output voltage of the device.
OUT	5	C1	1	O	Output of the regulator. To assure stability, a small ceramic capacitor (total typical capacitance $\geq 2 \mu\text{F}$) is required from this pin to ground.
N/C	—	—	5	—	Not internally connected. This pin must either be left open, or tied to GND.

6 Specifications

6.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted) ⁽¹⁾

		MIN	MAX	UNIT
Voltage ⁽²⁾	IN	-0.3	7.0	V
	EN	-0.3	$V_{IN} + 0.3$	V
	OUT	-0.3	$V_{IN} + 0.3$	V
Current	OUT	Internally limited		mA
Temperature	Operating virtual junction, T_J	-55	150	°C
	Storage temperature range, T_{stg}	-55	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to network ground terminal.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	±2000
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	±500

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	2.7		6.5	V
I_{OUT}	Output current	0.5		200	mA
T_J	Operating junction temperature	-40		125	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TPS799			UNIT
		DDC (SOT)	DRV (SON)	YZU (DSBGA)	
		5 PINS	6 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	225.3	74.2	143.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	39.3	58.8	1.1	
$R_{\theta JB}$	Junction-to-board thermal resistance	47.3	145.9	84.7	
Ψ_{JT}	Junction-to-top characterization parameter	0.5	0.2	3.8	
Ψ_{JB}	Junction-to-board characterization parameter	46.7	54.4	84.4	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	7.2	N/A	

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

6.5 Electrical Characteristics

Over operating temperature range ($T_J = -40^\circ\text{C}$ to 125°C), $V_{IN} = V_{OUT(nom)} + 0.3\text{ V}$ or 2.7 V , whichever is greater; $I_{OUT} = 1\text{ mA}$, $V_{EN} = V_{IN}$, $C_{OUT} = 2.2\ \mu\text{F}$, $C_{NR} = 0.01\ \mu\text{F}$, unless otherwise noted. For TPS79901, $V_{OUT} = 3.0\text{ V}$. Typical values are at $T_J = 25^\circ\text{C}$.

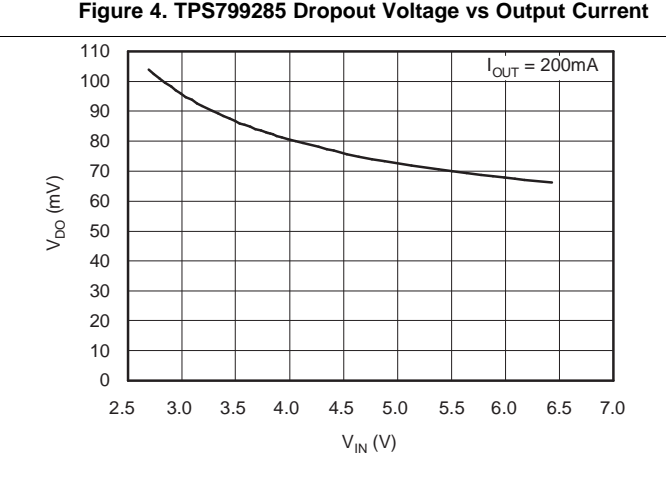
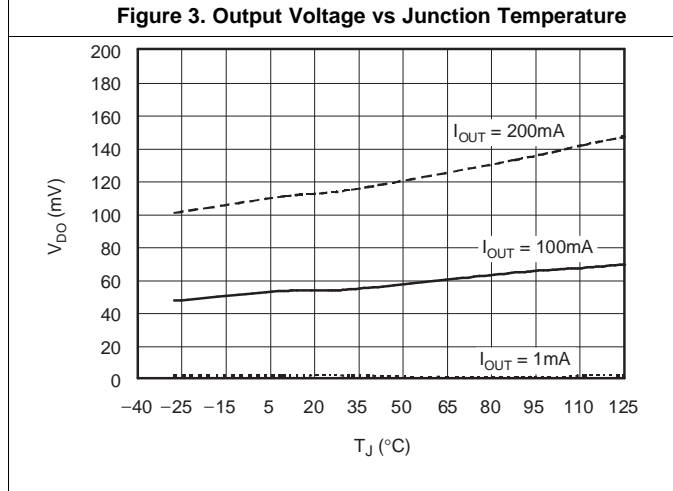
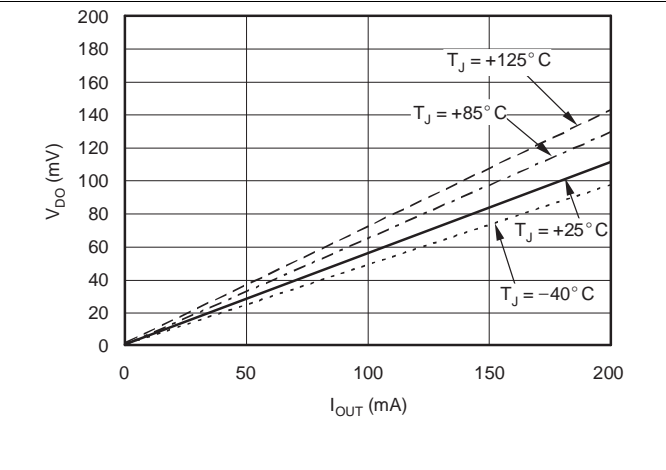
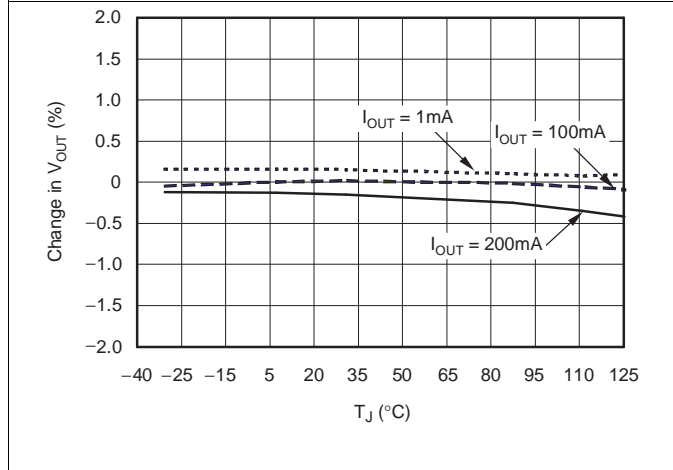
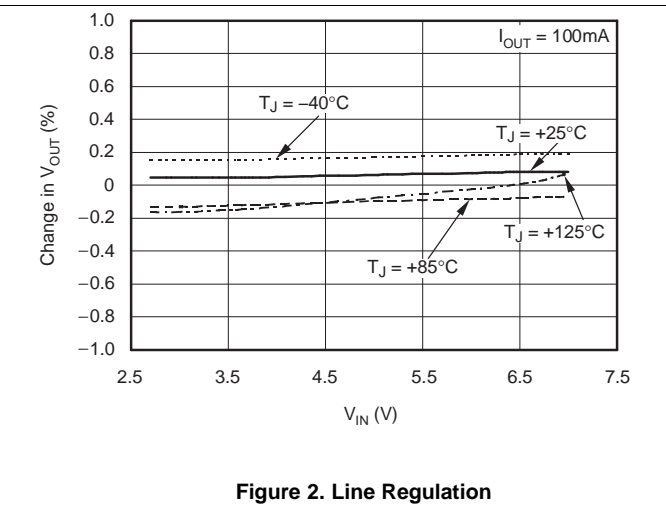
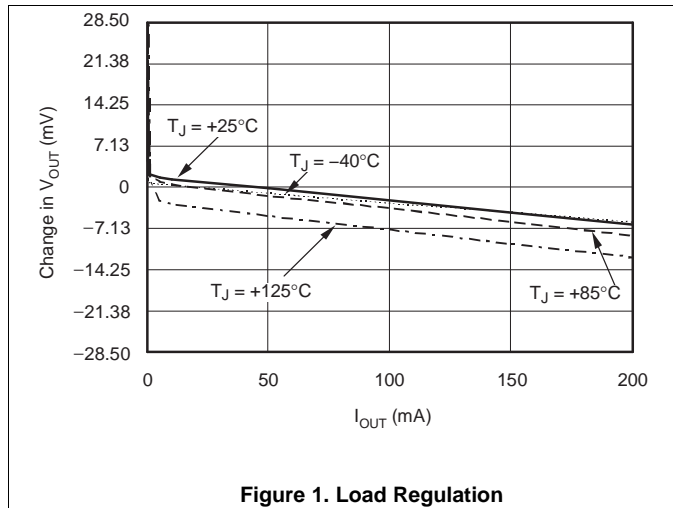
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range ⁽¹⁾		2.7		6.5	V
V_{FB}	Internal reference (TPS79901)		1.169	1.193	1.217	V
V_{OUT}	Output voltage range (TPS79901)		V_{FB}	$6.5 - V_{DO}$		V
V_{OUT}	Output accuracy, nominal	$T_J = 25^\circ\text{C}$	-1%		1%	
	Output accuracy ⁽¹⁾ Over V_{IN} , I_{OUT} , temperature	$V_{OUT} + 0.3\text{ V} \leq V_{IN} \leq 6.5\text{ V}$ $500\ \mu\text{A} \leq I_{OUT} \leq 200\text{ mA}$	-2%	$\pm 1\%$	2%	
$\Delta V_{O(\Delta VI)}$	Line regulation ⁽¹⁾	$V_{OUT(NOM)} + 0.3\text{ V} \leq V_{IN} \leq 6.5\text{ V}$		0.02		%/V
$\Delta V_{O(\Delta IO)}$	Load regulation	$500\ \mu\text{A} \leq I_{OUT} \leq 200\text{ mA}$		0.002		%/mA
V_{DO}	Dropout voltage ⁽²⁾ ($V_{IN} = V_{OUT(nom)} - 0.1\text{ V}$)	$I_{OUT} = 200\text{ mA}$	$V_{OUT(nom)} \leq 3.3\text{ V}$	100	175	mV
			$V_{OUT(nom)} \geq 3.3\text{ V}$	90	160	mV
I_{CL}	Output current limit	$V_{OUT} = 0.9 \times V_{OUT(nom)}$	220	400	600	mA
I_{GND}	Ground pin current	$500\ \mu\text{A} \leq I_{OUT} \leq 200\text{ mA}$		40	60	μA
I_{SHDN}	Shutdown current (I_{GND})	$V_{EN} \leq 0.4\text{ V}$, $2.7\text{ V} \leq V_{IN} \leq 6.5\text{ V}$		0.15	1	μA
I_{FB}	Feedback pin current (TPS79901)		-0.5		0.5	μA
PSRR	Power-supply rejection ratio	$V_{IN} = 3.85\text{ V}$, $V_{OUT} = 2.85\text{ V}$, $C_{NR} = 0.01\ \mu\text{F}$, $I_{OUT} = 100\text{ mA}$	$f = 100\text{ Hz}$	70		dB
			$f = 1\text{ kHz}$	66		dB
			$f = 10\text{ kHz}$	51		dB
			$f = 100\text{ kHz}$	38		dB
V_n	Output noise voltage	BW = 10 Hz to 100 kHz, $V_{OUT} = 2.85\text{ V}$	$C_{NR} = 0.01\ \mu\text{F}$	$10.5 \times V_{OUT}$		μV_{RMS}
			$C_{NR} = \text{none}$	$94 \times V_{OUT}$		μV_{RMS}
	Start-up time	$V_{OUT} = 2.85\text{ V}$, $R_L = 14\ \Omega$, $C_{OUT} = 2.2\ \mu\text{F}$	$C_{NR} = 0.001\ \mu\text{F}$	45		μs
			$C_{NR} = 0.047\ \mu\text{F}$	45		μs
			$C_{NR} = 0.01\ \mu\text{F}$	50		μs
			$C_{NR} = \text{none}$	50		μs
$V_{EN(HI)}$	Enable high (enabled)		1.2		V_{IN}	V
$V_{EN(LO)}$	Enable low (shutdown)		0		0.4	V
$I_{EN(HI)}$	Enable pin current, enabled	$V_{EN} = V_{IN} = 6.5\text{ V}$		0.03	1	μA
T_{sd}	Thermal shutdown temperature	Shutdown, temperature increasing		165		$^\circ\text{C}$
		Reset, temperature decreasing		145		$^\circ\text{C}$
T_J	Operating junction temperature		-40		125	$^\circ\text{C}$
UVLO	Undervoltage lockout	V_{IN} rising	1.90	2.20	2.65	V
	Hysteresis	V_{IN} falling		70		mV

(1) Minimum $V_{IN} = V_{OUT} + V_{DO}$ or 2.7 V , whichever is greater.

(2) V_{DO} is not measured for devices with $V_{OUT(nom)} < 2.8\text{ V}$ because minimum $V_{IN} = 2.7\text{ V}$.

6.6 Typical Characteristics

Over operating temperature range ($T_J = -40^\circ\text{C}$ to 125°C), $V_{IN} = V_{OUT(nom)} + 0.3\text{ V}$ or 2.7 V , whichever is greater; $I_{OUT} = 1\text{ mA}$, $V_{EN} = V_{IN}$, $C_{OUT} = 2.2\ \mu\text{F}$, and $C_{NR} = 0.01\ \mu\text{F}$, unless otherwise noted. For TPS79901, $V_{OUT} = 3.0\text{ V}$. Typical values are at $T_J = 25^\circ\text{C}$.



Typical Characteristics (continued)

Over operating temperature range ($T_J = -40^\circ\text{C}$ to 125°C), $V_{IN} = V_{OUT(nom)} + 0.3\text{ V}$ or 2.7 V , whichever is greater; $I_{OUT} = 1\text{ mA}$, $V_{EN} = V_{IN}$, $C_{OUT} = 2.2\ \mu\text{F}$, and $C_{NR} = 0.01\ \mu\text{F}$, unless otherwise noted. For TPS79901, $V_{OUT} = 3.0\text{ V}$. Typical values are at $T_J = 25^\circ\text{C}$.

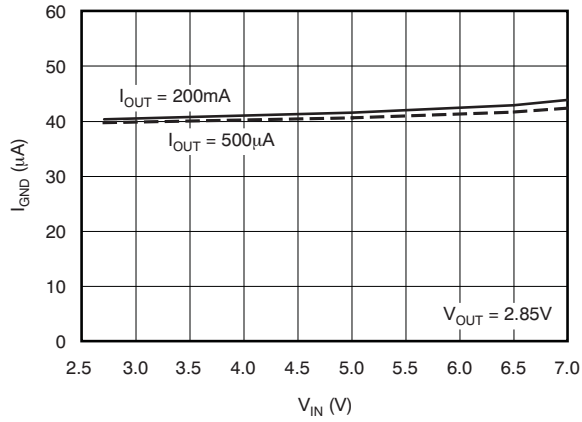


Figure 7. Ground Pin Current vs Input Voltage

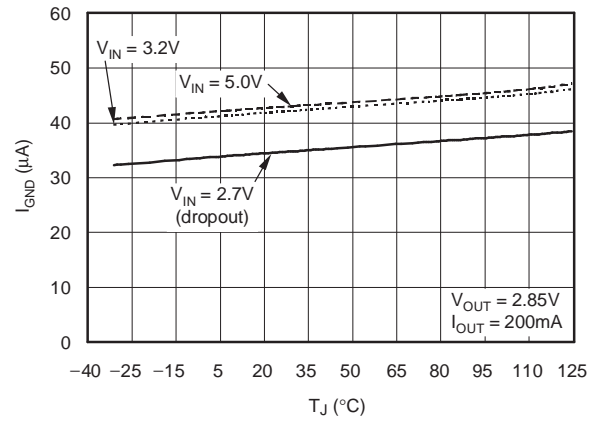


Figure 8. TPS799285 Ground Pin Current vs Junction Temperature

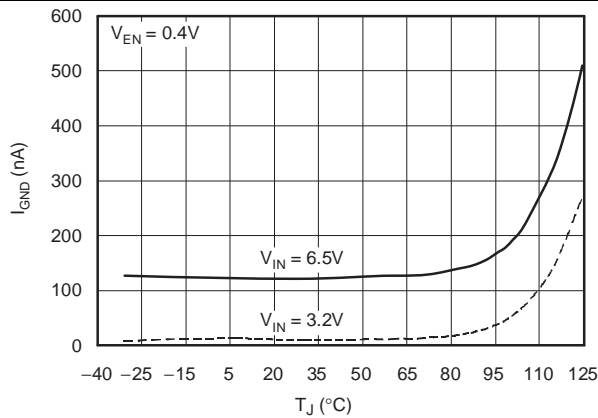


Figure 9. Ground Pin Current (Disabled) vs Junction Temperature

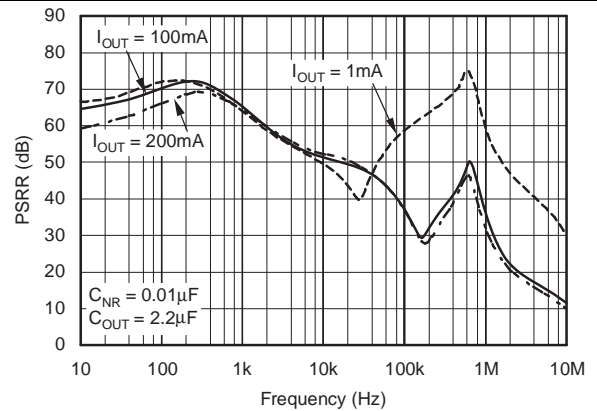


Figure 10. TPS799285 Power-Supply Ripple Rejection vs Frequency ($V_{IN} - V_{OUT} = 1.0\text{ V}$)

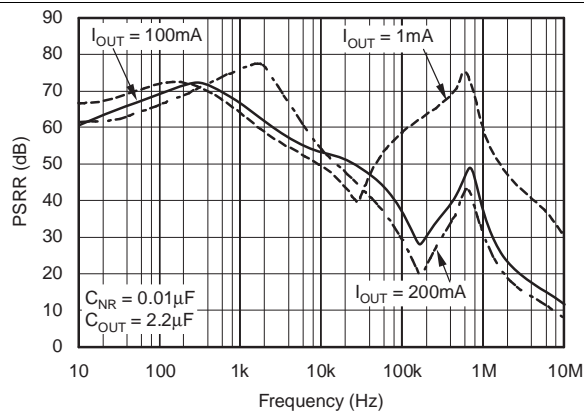


Figure 11. TPS799285 Power-Supply Ripple Rejection vs Frequency ($V_{IN} - V_{OUT} = 0.5\text{ V}$)

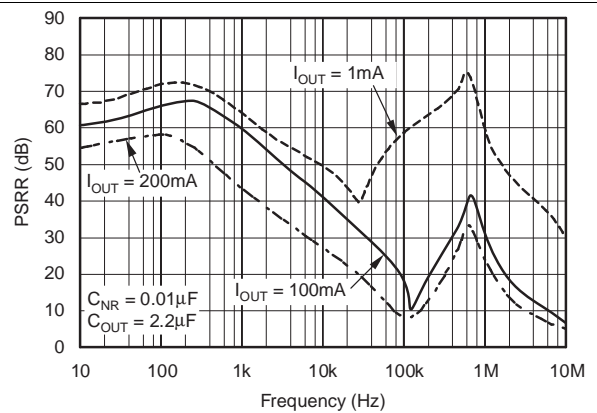


Figure 12. TPS799285 Power-Supply Ripple Rejection vs Frequency ($V_{IN} - V_{OUT} = 0.25\text{ V}$)

Typical Characteristics (continued)

Over operating temperature range ($T_J = -40^{\circ}\text{C}$ to 125°C), $V_{IN} = V_{OUT(nom)} + 0.3\text{ V}$ or 2.7 V , whichever is greater; $I_{OUT} = 1\text{ mA}$, $V_{EN} = V_{IN}$, $C_{OUT} = 2.2\ \mu\text{F}$, and $C_{NR} = 0.01\ \mu\text{F}$, unless otherwise noted. For TPS79901, $V_{OUT} = 3.0\text{ V}$. Typical values are at $T_J = 25^{\circ}\text{C}$.

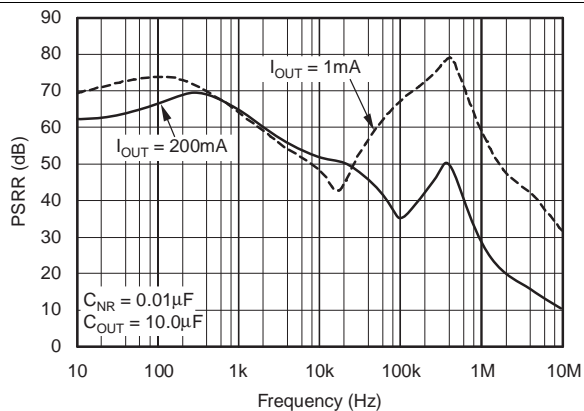


Figure 13. TPS799285 Power-Supply Ripple Rejection vs Frequency ($V_{IN} - V_{OUT} = 1.0\text{ V}$)

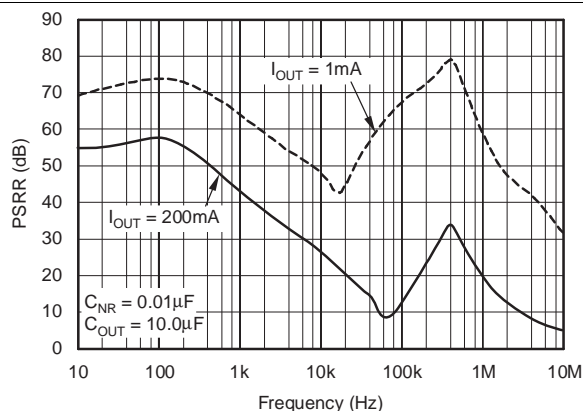


Figure 14. TPS799285 Power-Supply Ripple Rejection vs Frequency ($V_{IN} - V_{OUT} = 0.25\text{ V}$)

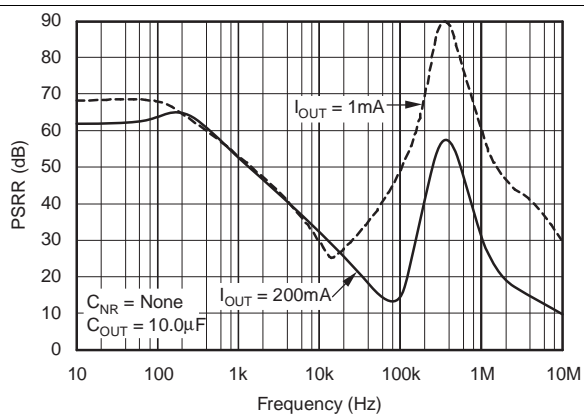


Figure 15. TPS799285 Power-Supply Ripple Rejection vs Frequency ($V_{IN} - V_{OUT} = 1.0\text{ V}$)

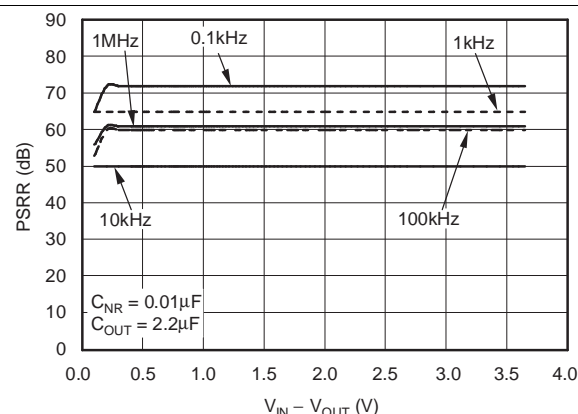


Figure 16. Power-Supply Ripple Rejection vs $V_{IN} - V_{OUT}$, $I_{OUT} = 1\text{ mA}$

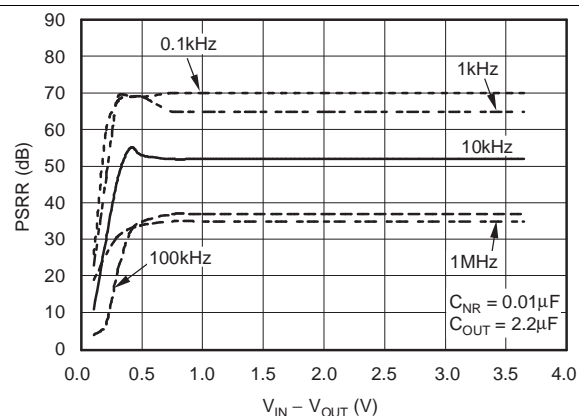


Figure 17. Power-Supply Ripple Rejection vs $V_{IN} - V_{OUT}$, $I_{OUT} = 100\text{ mA}$

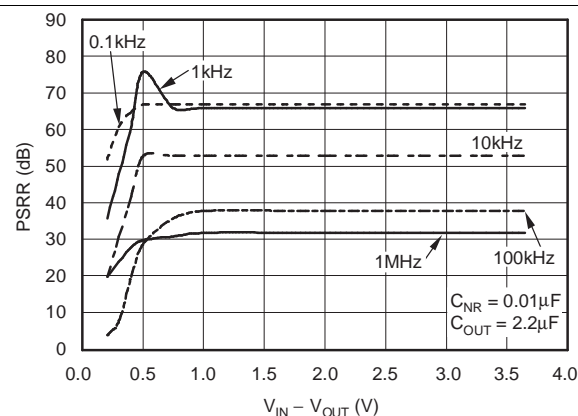


Figure 18. Power-Supply Ripple Rejection vs $V_{IN} - V_{OUT}$, $I_{OUT} = 200\text{ mA}$

Typical Characteristics (continued)

Over operating temperature range ($T_J = -40^\circ\text{C}$ to 125°C), $V_{IN} = V_{OUT(nom)} + 0.3\text{ V}$ or 2.7 V , whichever is greater; $I_{OUT} = 1\text{ mA}$, $V_{EN} = V_{IN}$, $C_{OUT} = 2.2\ \mu\text{F}$, and $C_{NR} = 0.01\ \mu\text{F}$, unless otherwise noted. For TPS79901, $V_{OUT} = 3.0\text{ V}$. Typical values are at $T_J = 25^\circ\text{C}$.

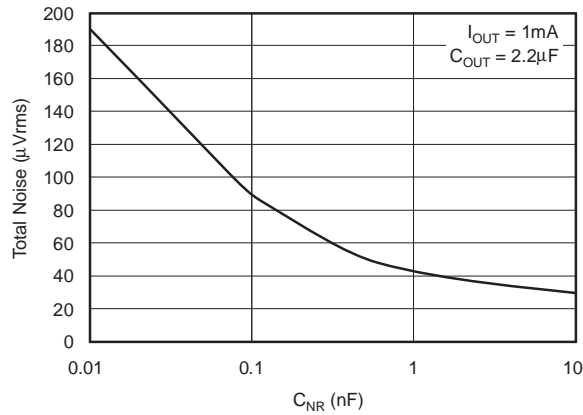


Figure 19. TPS799285 Total Noise vs C_{NR}

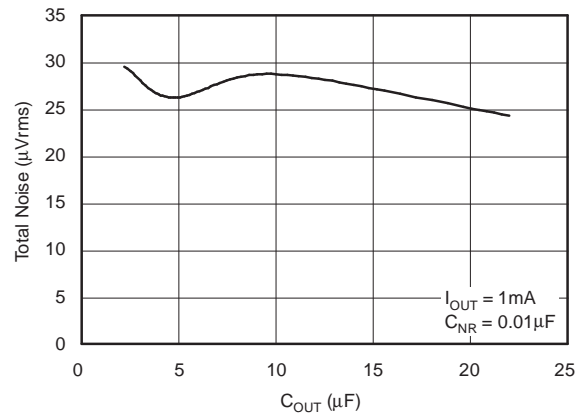


Figure 20. TPS799285 Total Noise vs C_{OUT}

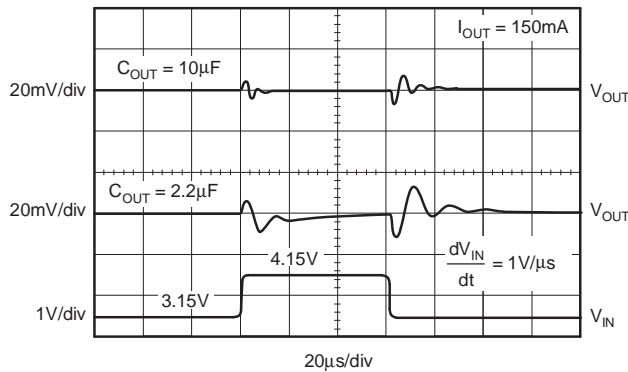


Figure 21. TPS799285 Line Transient Response

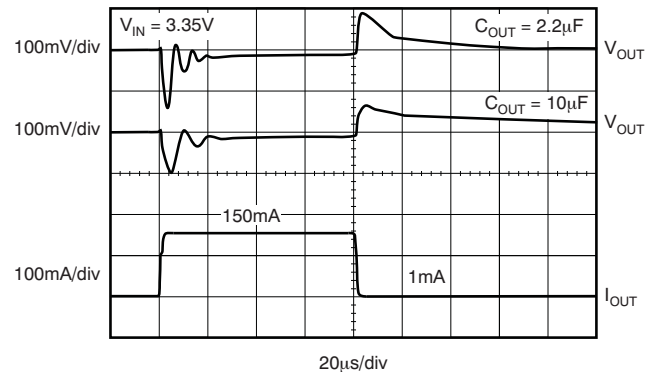


Figure 22. TPS799285 Load Transient Response

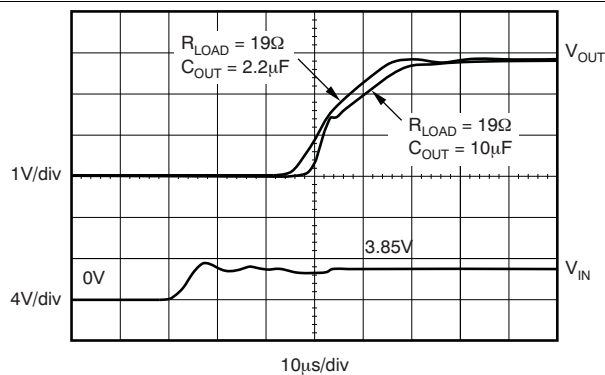


Figure 23. TPS799285 Turn-On Response ($V_{EN} = V_{IN}$)

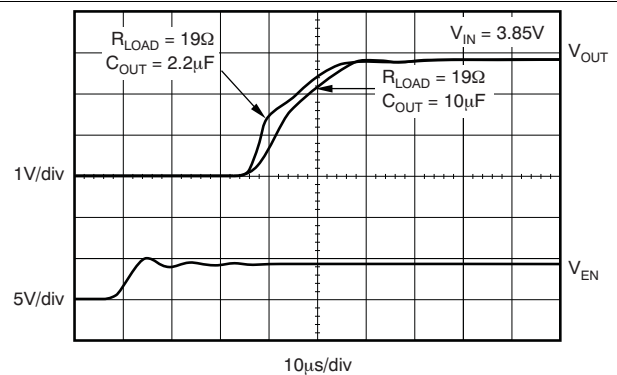


Figure 24. TPS799285 Enable Response

Typical Characteristics (continued)

Over operating temperature range ($T_J = -40^{\circ}\text{C}$ to 125°C), $V_{IN} = V_{OUT(nom)} + 0.3\text{ V}$ or 2.7 V , whichever is greater; $I_{OUT} = 1\text{ mA}$, $V_{EN} = V_{IN}$, $C_{OUT} = 2.2\text{ }\mu\text{F}$, and $C_{NR} = 0.01\text{ }\mu\text{F}$, unless otherwise noted. For TPS79901, $V_{OUT} = 3.0\text{ V}$. Typical values are at $T_J = 25^{\circ}\text{C}$.

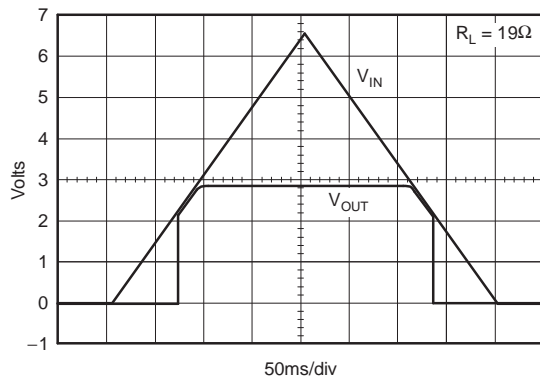


Figure 25. TPS799285 Power-Up/Power-Down

7 Detailed Description

7.1 Overview

The TPS799 family of low-dropout (LDO) regulators combines the high performance required of many RF and precision analog applications with ultralow current consumption. High PSRR is provided by a high-gain, high-bandwidth error loop with good supply rejection at very low headroom ($V_{IN} - V_{OUT}$). A noise-reduction pin is provided to bypass noise generated by the band-gap reference and to improve PSRR, while a quick-start circuit quickly charges this capacitor at start-up. The combination of high performance and low ground current also make these devices an excellent choice for portable applications. All versions have thermal and overcurrent protection, and are fully specified from -40°C to 125°C .

The TPS799 family also features inrush current protection with an EN toggle start-up, and overshoot detection at the output. When the EN toggle is used to start the device, current limit protection is immediately activated, restricting the inrush current to the device. If voltage at the output overshoots 5% from the nominal value, a pulldown resistor reduces the voltage to normal operating conditions, as shown in the [Functional Block Diagram](#).

7.2 Functional Block Diagram

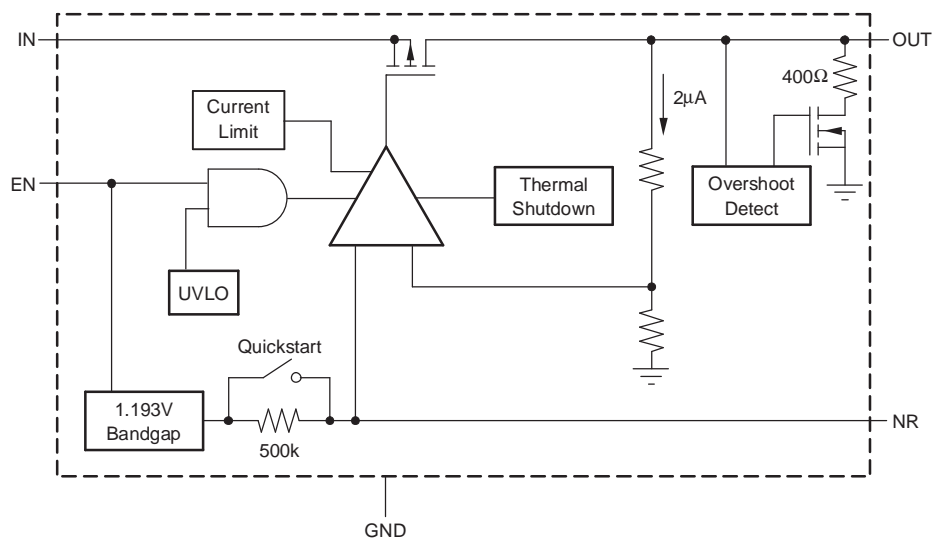


Figure 26. Fixed-Voltage Versions

Functional Block Diagram (continued)

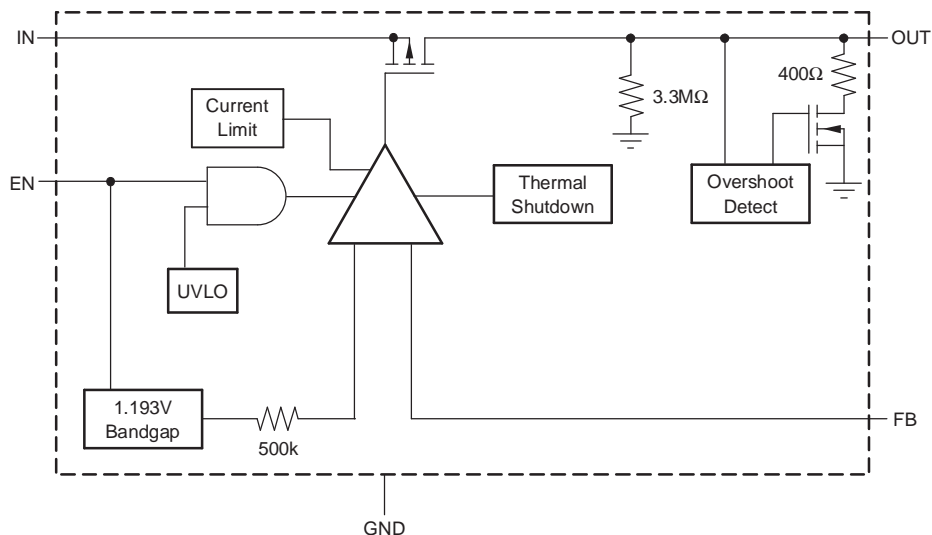


Figure 27. Adjustable-Voltage Versions

7.3 Feature Description

7.3.1 Internal Current Limit

The TPS799 internal current limit helps protect the regulator during fault conditions. In current limit mode, the output sources a fixed amount of current that is largely independent of the output voltage. For reliable operation, do not operate the device in a current-limit state for extended periods of time.

The PMOS pass element in the TPS799 has a built-in body diode that conducts current when the voltage at OUT exceeds the voltage at IN. This current is not limited; therefore, if extended reverse voltage operation is anticipated, external limiting may be required.

7.3.2 Shutdown

The enable pin (EN) is active high and is compatible with standard and low-voltage TTL-CMOS levels. When shutdown capability is not required, EN can be connected to IN.

7.3.3 Start Up

The TPS799 uses a start-up circuit to quickly charge the noise reduction capacitor, C_{NR} , if present (see the [Functional Block Diagram](#)). This circuit allows for the combination of very low output noise and fast start-up times. The NR pin is high impedance so a low leakage C_{NR} capacitor must be used; most ceramic capacitors are appropriate for this configuration.

Note that for fastest start-up, apply V_{IN} first, and then drive the enable pin (EN) high. If EN is tied to IN, start-up is somewhat slower. The start-up switch is closed for approximately 135 μ s. To ensure that C_{NR} is fully charged during start-up, use a 0.01- μ F or smaller capacitor.

7.3.4 Undervoltage Lockout (UVLO)

The TPS799 uses an undervoltage lockout circuit to keep the output shut off until internal circuitry is operating properly. The UVLO circuit has a deglitch feature so that undershoot transients are typically ignored on the input if these transients are less than 50 μ s in duration.

7.4 Device Functional Modes

Driving EN over 1.2 V turns on the regulator. Driving EN below 0.4 V puts the regulator into shutdown mode, thus reducing the operating current to 150 nA, nominal.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS799 family of LDO regulators provides high PSRR while maintaining ultralow current consumption. The family also features inrush current protection and overshoot detection at the output.

8.2 Typical Applications

Figure 28 and Figure 29 show the basic circuit connections.

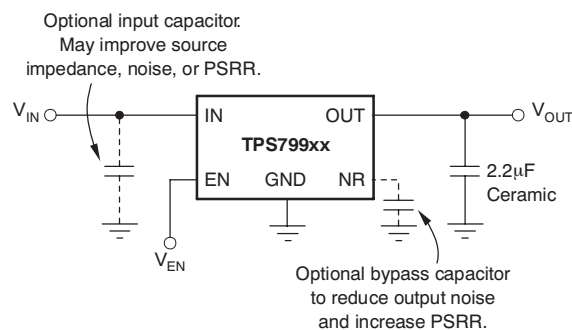


Figure 28. Typical Application Circuit for Fixed Voltage Versions

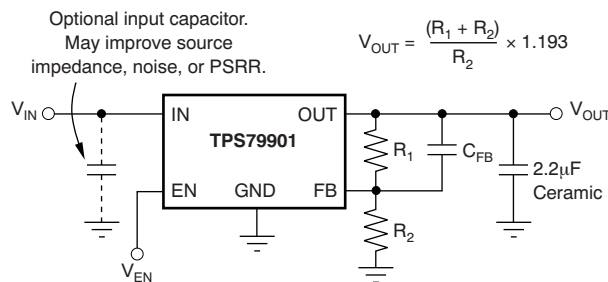


Figure 29. Typical Application Circuit for Adjustable Voltage Version

8.2.1 Design Requirements

Select the desired device based on the output voltage.

Provide an input supply with adequate headroom to account for dropout and output current to account for the GND terminal current, and power the load.

8.2.2 Detailed Design Procedure

8.2.2.1 Input and Output Capacitor Requirements

Although an input capacitor is not required for stability, good analog design practice is to connect a 0.1-µF to 1-µF low ESR capacitor across the input supply near the regulator. This capacitor counteracts reactive input sources and improves transient response, noise rejection, and ripple rejection. A higher-value capacitor may be necessary if large, fast rise-time load transients are anticipated, or if the device is located several inches from the power source. If source impedance is not sufficiently low, a 0.1-µF input capacitor may be necessary to ensure stability.

Typical Applications (continued)

The TPS799 is designed to be stable with standard ceramic capacitors with values of 2.2 μF or greater. X5R- and X7R-type capacitors are best because they have minimal variation in value and ESR over temperature. Maximum ESR must be less than 1.0 Ω .

8.2.2.2 Output Noise

In most LDOs, the band gap is the dominant noise source. If a noise-reduction capacitor (C_{NR}) is used with the TPS799, the band gap does not contribute significantly to noise. Instead, noise is dominated by the output resistor divider and the error amplifier input. To minimize noise in a given application, use a 0.01- μF noise reduction capacitor. To further optimize noise, equivalent series resistance of the output capacitor can be set to approximately 0.2 Ω . This configuration maximizes phase margin in the control loop, reducing total output noise by up to 10%.

Noise can be referred to the feedback point; with $C_{\text{NR}} = 0.01 \mu\text{F}$ total noise is approximately given by [Equation 1](#):

$$V_N = \frac{10.5 \mu\text{V}_{\text{RMS}}}{V} \times V_{\text{OUT}} \quad (1)$$

8.2.2.3 Dropout Voltage

The TPS799 uses a PMOS pass transistor to achieve a low dropout voltage. When ($V_{\text{IN}} - V_{\text{OUT}}$) is less than the dropout voltage (V_{DO}), the PMOS pass device is in its linear region of operation and $r_{\text{DS(on)}}$ of the PMOS pass element is the input-to-output resistance. Because the PMOS device behaves like a resistor in dropout, V_{DO} approximately scales with the output current.

As with any linear regulator, PSRR degrades as ($V_{\text{IN}} - V_{\text{OUT}}$) approaches dropout. This effect is illustrated in [Figure 10](#) through [Figure 18](#) in the [Typical Characteristics](#) section.

8.2.2.4 Transient Response

As with any regulator, increasing the size of the output capacitor reduces over- and undershoot magnitude, but increases the duration of the transient response. The transient response of the TPS799 is enhanced by an active pulldown device that engages when the output overshoots by approximately 5% or more when the device is enabled. When enabled, the pulldown device behaves like a 350- Ω resistor to ground.

8.2.2.5 Minimum Load

The TPS799 is stable with no output load. To meet the specified accuracy, a minimum load of 500 μA is required. With loads less than 500 μA at junction temperatures near 125°C, the output can drift up enough to cause the output pulldown device to turn on. The output pulldown device limits voltage drift to 5% typically; however, ground current can increase by approximately 50 μA . In typical applications, the junction cannot reach high temperatures at light loads because there is no noticeable dissipated power. The specified ground current is then valid at no load in most applications.

8.2.2.6 Feedback Capacitor Requirements (TPS79901 Only)

The feedback capacitor, C_{FB} , shown in [Figure 29](#) is required for stability. For a parallel combination of R_1 and R_2 equal to 250 k Ω , any value from 3 pF to 1 nF can be used. Fixed voltage versions have an internal 30-pF feedback capacitor which is quick-charged at start-up. The adjustable version does not have this quick-charge circuit, so values below 5 pF should be used to ensure fast startup; values above 47 pF can be used to implement an output voltage soft-start. Larger value capacitors also improve noise slightly. The TPS79901 is stable in unity-gain configuration (OUT tied to FB) without C_{FB} .

Typical Applications (continued)

8.2.3 Application Curve

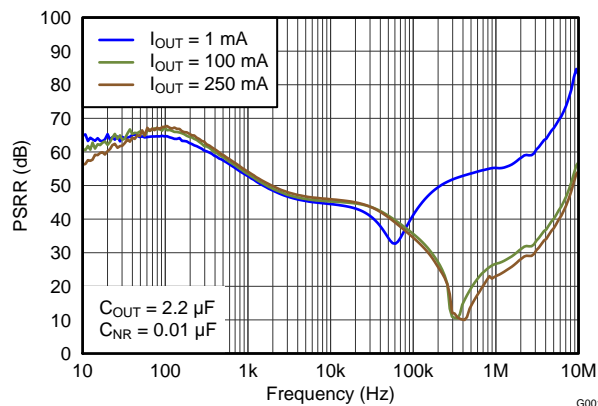


Figure 30. Power-Supply Rejection Ratio vs Frequency

8.3 Do's and Don'ts

Do place at least one 2.2- μ F ceramic capacitor as close as possible to the OUT pin of the regulator.

Do not place the output capacitor more than 10 mm away from the regulator.

Do connect a 0.1- μ F to 1- μ F low equivalent series resistance (ESR) capacitor across the IN pin and GND input of the regulator.

Do not exceed the absolute maximum ratings.

9 Power Supply Recommendations

These devices are designed to operate from an input voltage supply range between 2.7 V and 6.5 V. The input voltage range provides adequate headroom in order for the device to have a regulated output. This input supply is well-regulated and stable. If the input supply is noisy, additional input capacitors with low ESR can help improve the output noise performance.

10 Layout

10.1 Layout Guidelines

10.1.1 Board Layout Recommendations to Improve PSRR and Noise Performance

To improve ac performance (such as PSRR, output noise, and transient response), design the board with separate ground planes for V_{IN} and V_{OUT} , with each ground plane connected only at the GND pin of the device. In addition, connect the bypass capacitor directly to the GND pin of the device.

10.2 Layout Example

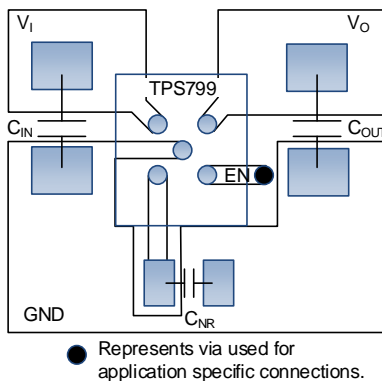


Figure 31. Layout Example

10.3 Thermal Information

10.3.1 Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately 165°C, allowing the device to cool. When the junction temperature cools to approximately 145°C the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage resulting from overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, limit junction temperature to 125°C maximum. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection triggers at least 35°C above the maximum expected ambient condition of a particular application. This configuration produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS799 is designed to protect against overload conditions. This circuitry is not intended to replace proper heatsinking. Continuously running the device into thermal shutdown degrades device reliability.

10.3.2 Power Dissipation

The ability to remove heat from the die is different for each package type, presenting different considerations in the PCB layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Performance data for JEDEC low- and high-K boards are given in the [Thermal Information](#) table near the front of this data sheet. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers also improves heatsink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation is equal to the product of the output current times the voltage drop across the output pass element, as shown in [Equation 2](#):

$$P_D = (V_{IN} - V_{OUT}) \cdot I_{OUT} \quad (2)$$

10.3.3 Package Mounting

Solder pad footprint recommendations for the TPS799 are available from the TI's website at www.ti.com.

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 Evaluation Modules

An evaluation module (EVM) is available to assist in the initial circuit performance evaluation using the TPS799. This EVM, the TPS799 evaluation module, can be requested at the Texas Instruments web site through the product folders or purchased [directly from the TI eStore](#).

11.1.1.2 Spice Models

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. A SPICE model for the TPS799 is available through the product folders under simulation models.

11.1.2 Device Nomenclature

Table 1. Device Nomenclature⁽¹⁾

PRODUCT	V _{OUT}
TPS799xx(x) yyy z	xx(x) is nominal output voltage (for example, 28 = 2.8 V, 285 = 2.85 V, 01 = Adjustable). yyy is package designator. z is package quantity.

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation, see the following:

- Application report: *Using New Thermal Metrics*, [SBVA025](#).
- Application report: *IC Package Thermal Metrics*, [SPRA953](#)
- *TPS799xxEVM-105 User's Guide*, [SLVU130](#)

11.3 Trademarks

Bluetooth is a registered trademark of Bluetooth SIG, Inc.

All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS79901DDCR	ACTIVE	SOT-23-THIN	DDC	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AWT	Samples
TPS79901DDCRG4	ACTIVE	SOT-23-THIN	DDC	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AWT	Samples
TPS79901DDCT	ACTIVE	SOT-23-THIN	DDC	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AWT	Samples
TPS79901DDCTG4	ACTIVE	SOT-23-THIN	DDC	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AWT	Samples
TPS79901DRVR	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AWT	Samples
TPS79901DRVRG4	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AWT	Samples
TPS79901DRVT	ACTIVE	WSON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AWT	Samples
TPS79901DRVTG4	ACTIVE	WSON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AWT	Samples
TPS79901YZUR	ACTIVE	DSBGA	YZU	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	E9	Samples
TPS79901YZUT	ACTIVE	DSBGA	YZU	5	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	E9	Samples
TPS799125YZUR	ACTIVE	DSBGA	YZU	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	YZ	Samples
TPS799125YZUT	ACTIVE	DSBGA	YZU	5	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	YZ	Samples
TPS79912DDCR	ACTIVE	SOT-23-THIN	DDC	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CCF	Samples
TPS79912DDCRG4	ACTIVE	SOT-23-THIN	DDC	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CCF	Samples
TPS79912DDCT	ACTIVE	SOT-23-THIN	DDC	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CCF	Samples
TPS79912DDCTG4	ACTIVE	SOT-23-THIN	DDC	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CCF	Samples
TPS79912DRVR	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CCF	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS79912DRV1T	ACTIVE	WSON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CCF	Samples
TPS79912DRV1TG4	ACTIVE	WSON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CCF	Samples
TPS79912YZUR	ACTIVE	DSBGA	YZU	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	F8	Samples
TPS79912YZUT	ACTIVE	DSBGA	YZU	5	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	F8	Samples
TPS79913DDCR	ACTIVE	SOT-23-THIN	DDC	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	BUJ	Samples
TPS79913DDCT	ACTIVE	SOT-23-THIN	DDC	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	BUJ	Samples
TPS79913DDCTG4	ACTIVE	SOT-23-THIN	DDC	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	BUJ	Samples
TPS79913YZUR	ACTIVE	DSBGA	YZU	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	F9	Samples
TPS79913YZUT	ACTIVE	DSBGA	YZU	5	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	F9	Samples
TPS79915DDCR	ACTIVE	SOT-23-THIN	DDC	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AWU	Samples
TPS79915DDCRG4	ACTIVE	SOT-23-THIN	DDC	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AWU	Samples
TPS79915DDCT	ACTIVE	SOT-23-THIN	DDC	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AWU	Samples
TPS79915DDCTG4	ACTIVE	SOT-23-THIN	DDC	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AWU	Samples
TPS79915YZUR	ACTIVE	DSBGA	YZU	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	EA	Samples
TPS79915YZUT	ACTIVE	DSBGA	YZU	5	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	EA	Samples
TPS799185DDCR	ACTIVE	SOT-23-THIN	DDC	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CGP	Samples
TPS799185DDCRG4	ACTIVE	SOT-23-THIN	DDC	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CGP	Samples
TPS799185DDCT	ACTIVE	SOT-23-THIN	DDC	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CGP	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS799185YZUR	ACTIVE	DSBGA	YZU	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	ZA	Samples
TPS799185YZUT	ACTIVE	DSBGA	YZU	5	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	ZA	Samples
TPS79918DDCR	ACTIVE	SOT-23-THIN	DDC	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AWV	Samples
TPS79918DDCRG4	ACTIVE	SOT-23-THIN	DDC	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AWV	Samples
TPS79918DDCT	ACTIVE	SOT-23-THIN	DDC	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AWV	Samples
TPS79918DDCTG4	ACTIVE	SOT-23-THIN	DDC	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AWV	Samples
TPS79918DRVR	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AWV	Samples
TPS79918DRVRG4	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AWV	Samples
TPS79918DRVT	ACTIVE	WSON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AWV	Samples
TPS79918DRVTG4	ACTIVE	WSON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AWV	Samples
TPS79918YZUR	ACTIVE	DSBGA	YZU	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	EB	Samples
TPS79918YZUT	ACTIVE	DSBGA	YZU	5	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	EB	Samples
TPS799195DRVR	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	BTP	Samples
TPS799195DRVRG4	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	BTP	Samples
TPS799195DRVT	ACTIVE	WSON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	BTP	Samples
TPS799195DRVTG4	ACTIVE	WSON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	BTP	Samples
TPS799195YZUR	ACTIVE	DSBGA	YZU	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	AO	Samples
TPS799195YZUT	ACTIVE	DSBGA	YZU	5	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	AO	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS79919YZUR	ACTIVE	DSBGA	YZU	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	F6	Samples
TPS79919YZUT	ACTIVE	DSBGA	YZU	5	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	F6	Samples
TPS79920YZUR	ACTIVE	DSBGA	YZU	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	GA	Samples
TPS79920YZUT	ACTIVE	DSBGA	YZU	5	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	GA	Samples
TPS79921YZUR	ACTIVE	DSBGA	YZU	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	G7	Samples
TPS79921YZUT	ACTIVE	DSBGA	YZU	5	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	G7	Samples
TPS79925DDCR	ACTIVE	SOT-23-THIN	DDC	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AWW	Samples
TPS79925DDCRG4	ACTIVE	SOT-23-THIN	DDC	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AWW	Samples
TPS79925DDCT	ACTIVE	SOT-23-THIN	DDC	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AWW	Samples
TPS79925DDCTG4	ACTIVE	SOT-23-THIN	DDC	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AWW	Samples
TPS79925YZUR	ACTIVE	DSBGA	YZU	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	EC	Samples
TPS79925YZUT	ACTIVE	DSBGA	YZU	5	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	EC	Samples
TPS79926YZUR	ACTIVE	DSBGA	YZU	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	F3	Samples
TPS79926YZUT	ACTIVE	DSBGA	YZU	5	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	F3	Samples
TPS799275YZUR	ACTIVE	DSBGA	YZU	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	G2	Samples
TPS799275YZUT	ACTIVE	DSBGA	YZU	5	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	G2	Samples
TPS79927DDCR	ACTIVE	SOT-23-THIN	DDC	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	BWE	Samples
TPS79927DDCT	ACTIVE	SOT-23-THIN	DDC	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	BWE	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS79927DRVR	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	BPM	Samples
TPS79927DRVT	ACTIVE	WSON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	BPM	Samples
TPS79927DRVTG4	ACTIVE	WSON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	BPM	Samples
TPS79927YZUT	ACTIVE	DSBGA	YZU	5	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	F5	Samples
TPS799285DDCR	ACTIVE	SOT-23-THIN	DDC	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AXY	Samples
TPS799285DDCRG4	ACTIVE	SOT-23-THIN	DDC	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AXY	Samples
TPS799285DDCT	ACTIVE	SOT-23-THIN	DDC	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AXY	Samples
TPS799285DDCTG4	ACTIVE	SOT-23-THIN	DDC	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AXY	Samples
TPS799285DRVR	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	BST	Samples
TPS799285DRVT	ACTIVE	WSON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	BST	Samples
TPS799285YZUR	ACTIVE	DSBGA	YZU	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	EE	Samples
TPS79928DDCR	ACTIVE	SOT-23-THIN	DDC	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AWX	Samples
TPS79928DDCRG4	ACTIVE	SOT-23-THIN	DDC	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AWX	Samples
TPS79928DDCT	ACTIVE	SOT-23-THIN	DDC	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AWX	Samples
TPS79928DDCTG4	ACTIVE	SOT-23-THIN	DDC	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AWX	Samples
TPS79928DRVR	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AWX	Samples
TPS79928DRVRG4	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AWX	Samples
TPS79928DRVT	ACTIVE	WSON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AWX	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS79928DRV TG4	ACTIVE	WSO N	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AWX	Samples
TPS79928YZUR	ACTIVE	DSBGA	YZU	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	ED	Samples
TPS79928YZUT	ACTIVE	DSBGA	YZU	5	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	ED	Samples
TPS79930DDCR	ACTIVE	SOT-23-THIN	DDC	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AXZ	Samples
TPS79930DDCRG4	ACTIVE	SOT-23-THIN	DDC	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AXZ	Samples
TPS79930DDCT	ACTIVE	SOT-23-THIN	DDC	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AXZ	Samples
TPS79930DDCTG4	ACTIVE	SOT-23-THIN	DDC	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AXZ	Samples
TPS79930YZUR	ACTIVE	DSBGA	YZU	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	EF	Samples
TPS79930YZUT	ACTIVE	DSBGA	YZU	5	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	EF	Samples
TPS799315DDCR	ACTIVE	SOT-23-THIN	DDC	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CGQ	Samples
TPS799315DDCRG4	ACTIVE	SOT-23-THIN	DDC	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CGQ	Samples
TPS799315DDCT	ACTIVE	SOT-23-THIN	DDC	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CGQ	Samples
TPS799315YZUR	ACTIVE	DSBGA	YZU	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	GP	Samples
TPS799315YZUT	ACTIVE	DSBGA	YZU	5	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	GP	Samples
TPS79932YZUR	ACTIVE	DSBGA	YZU	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	(F4 ~ FY)	Samples
TPS79932YZUT	ACTIVE	DSBGA	YZU	5	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	(F4 ~ FY)	Samples
TPS79933DDCR	ACTIVE	SOT-23-THIN	DDC	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AXX	Samples
TPS79933DDCRG4	ACTIVE	SOT-23-THIN	DDC	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AXX	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS79933DDCT	ACTIVE	SOT-23-THIN	DDC	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AXX	Samples
TPS79933DDCTG4	ACTIVE	SOT-23-THIN	DDC	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AXX	Samples
TPS79933DRVR	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AXX	Samples
TPS79933DRVRG4	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AXX	Samples
TPS79933DRVT	ACTIVE	WSON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AXX	Samples
TPS79933DRVTG4	ACTIVE	WSON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AXX	Samples
TPS79933YZUR	ACTIVE	DSBGA	YZU	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	EG	Samples
TPS79933YZUT	ACTIVE	DSBGA	YZU	5	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	EG	Samples
TPS79942DDCR	ACTIVE	SOT-23-THIN	DDC	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CJQ	Samples
TPS79942DDCRG4	ACTIVE	SOT-23-THIN	DDC	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CJQ	Samples
TPS79942DDCT	ACTIVE	SOT-23-THIN	DDC	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CJQ	Samples
TPS79945YZUR	ACTIVE	DSBGA	YZU	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	FK	Samples
TPS79945YZUT	ACTIVE	DSBGA	YZU	5	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	FK	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS799 :

- Automotive: [TPS799-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



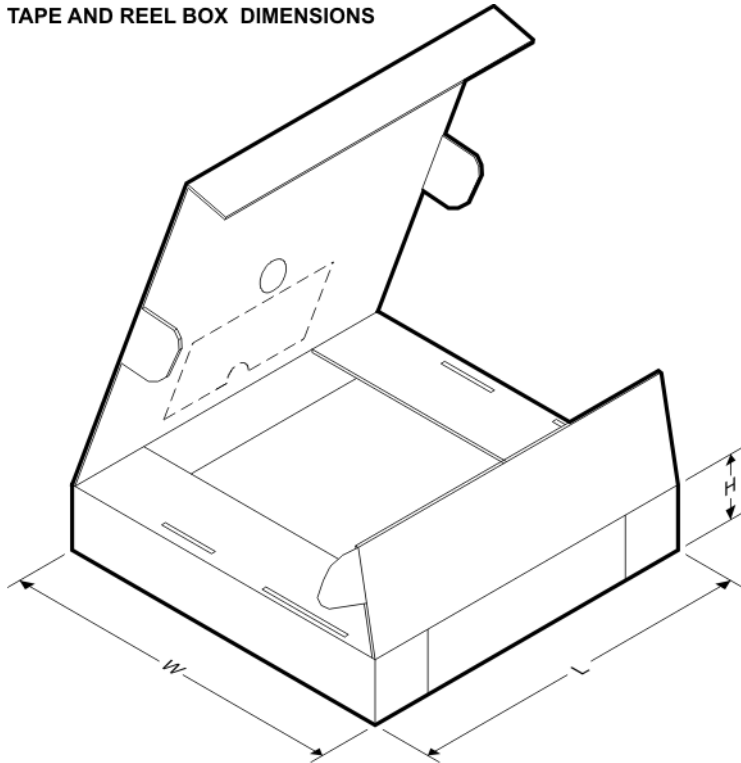
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS79901DDCR	SOT-23-THIN	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS79901DDCR	SOT-23-THIN	DDC	5	3000	180.0	8.4	3.1	3.05	1.1	4.0	8.0	Q3
TPS79901DDCT	SOT-23-THIN	DDC	5	250	180.0	8.4	3.1	3.05	1.1	4.0	8.0	Q3
TPS79901DDCT	SOT-23-THIN	DDC	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS79901DRVR	WSO	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS79901DRVT	WSO	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS79901YZUR	DSBGA	YZU	5	3000	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1
TPS79901YZUT	DSBGA	YZU	5	250	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1
TPS799125YZUR	DSBGA	YZU	5	3000	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1
TPS799125YZUT	DSBGA	YZU	5	250	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1
TPS79912DDCR	SOT-23-THIN	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS79912DDCT	SOT-23-THIN	DDC	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS79912DRVR	WSO	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS79912DRVT	WSO	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS79912YZUR	DSBGA	YZU	5	3000	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1
TPS79912YZUT	DSBGA	YZU	5	250	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1
TPS79913DDCR	SOT-23-THIN	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS79913DDCT	SOT-23-THIN	DDC	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS79913YZUR	DSBGA	YZU	5	3000	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1
TPS79913YZUT	DSBGA	YZU	5	250	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1
TPS79915DDCR	SOT-23-THIN	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS79915DDCT	SOT-23-THIN	DDC	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS79915YZUR	DSBGA	YZU	5	3000	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1
TPS79915YZUT	DSBGA	YZU	5	250	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1
TPS799185DDCR	SOT-23-THIN	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS799185DDCT	SOT-23-THIN	DDC	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS799185YZUR	DSBGA	YZU	5	3000	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1
TPS799185YZUT	DSBGA	YZU	5	250	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1
TPS79918DDCR	SOT-23-THIN	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS79918DDCT	SOT-23-THIN	DDC	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS79918DRV	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS79918DRVT	WSON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS79918YZUR	DSBGA	YZU	5	3000	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1
TPS79918YZUT	DSBGA	YZU	5	250	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1
TPS799195DRV	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS799195DRVT	WSON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS799195YZUR	DSBGA	YZU	5	3000	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1
TPS799195YZUT	DSBGA	YZU	5	250	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1
TPS79919YZUR	DSBGA	YZU	5	3000	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1
TPS79919YZUT	DSBGA	YZU	5	250	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1
TPS79920YZUR	DSBGA	YZU	5	3000	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1
TPS79920YZUT	DSBGA	YZU	5	250	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1
TPS79921YZUR	DSBGA	YZU	5	3000	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1
TPS79921YZUT	DSBGA	YZU	5	250	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1
TPS79925DDCR	SOT-23-THIN	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS79925DDCT	SOT-23-THIN	DDC	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS79925YZUR	DSBGA	YZU	5	3000	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1
TPS79925YZUT	DSBGA	YZU	5	250	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1
TPS79926YZUR	DSBGA	YZU	5	3000	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1
TPS79926YZUT	DSBGA	YZU	5	250	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS799275YZUR	DSBGA	YZU	5	3000	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1
TPS799275YZUT	DSBGA	YZU	5	250	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1
TPS79927DDCR	SOT-23-THIN	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS79927DDCT	SOT-23-THIN	DDC	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS79927DRVR	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS79927DRVT	WSON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS79927YZUT	DSBGA	YZU	5	250	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1
TPS799285DDCR	SOT-23-THIN	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS799285DDCT	SOT-23-THIN	DDC	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS799285DRVR	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS799285DRVT	WSON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS799285YZUR	DSBGA	YZU	5	3000	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1
TPS79928DDCR	SOT-23-THIN	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS79928DDCT	SOT-23-THIN	DDC	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS79928DRVR	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS79928DRVT	WSON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS79928YZUR	DSBGA	YZU	5	3000	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1
TPS79928YZUT	DSBGA	YZU	5	250	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1
TPS79930DDCR	SOT-23-THIN	DDC	5	3000	180.0	8.4	3.1	3.05	1.1	4.0	8.0	Q3
TPS79930DDCR	SOT-23-THIN	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS79930DDCT	SOT-23-THIN	DDC	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS79930YZUR	DSBGA	YZU	5	3000	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1
TPS79930YZUT	DSBGA	YZU	5	250	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1
TPS799315DDCR	SOT-23-THIN	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS799315DDCT	SOT-23-THIN	DDC	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS799315YZUR	DSBGA	YZU	5	3000	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1
TPS799315YZUT	DSBGA	YZU	5	250	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1
TPS79932YZUR	DSBGA	YZU	5	3000	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1
TPS79932YZUT	DSBGA	YZU	5	250	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1
TPS79933DDCR	SOT-23-THIN	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS79933DDCR	SOT-23-THIN	DDC	5	3000	180.0	8.4	3.1	3.05	1.1	4.0	8.0	Q3
TPS79933DDCT	SOT-23-THIN	DDC	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS79933DDCT	SOT-	DDC	5	250	180.0	8.4	3.1	3.05	1.1	4.0	8.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
	23-THIN											
TPS79933DRVR	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS79933DRVT	WSON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS79933YZUR	DSBGA	YZU	5	3000	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1
TPS79933YZUT	DSBGA	YZU	5	250	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1
TPS79942DDCR	SOT-23-THIN	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS79942DDCT	SOT-23-THIN	DDC	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS79945YZUR	DSBGA	YZU	5	3000	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1
TPS79945YZUT	DSBGA	YZU	5	250	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

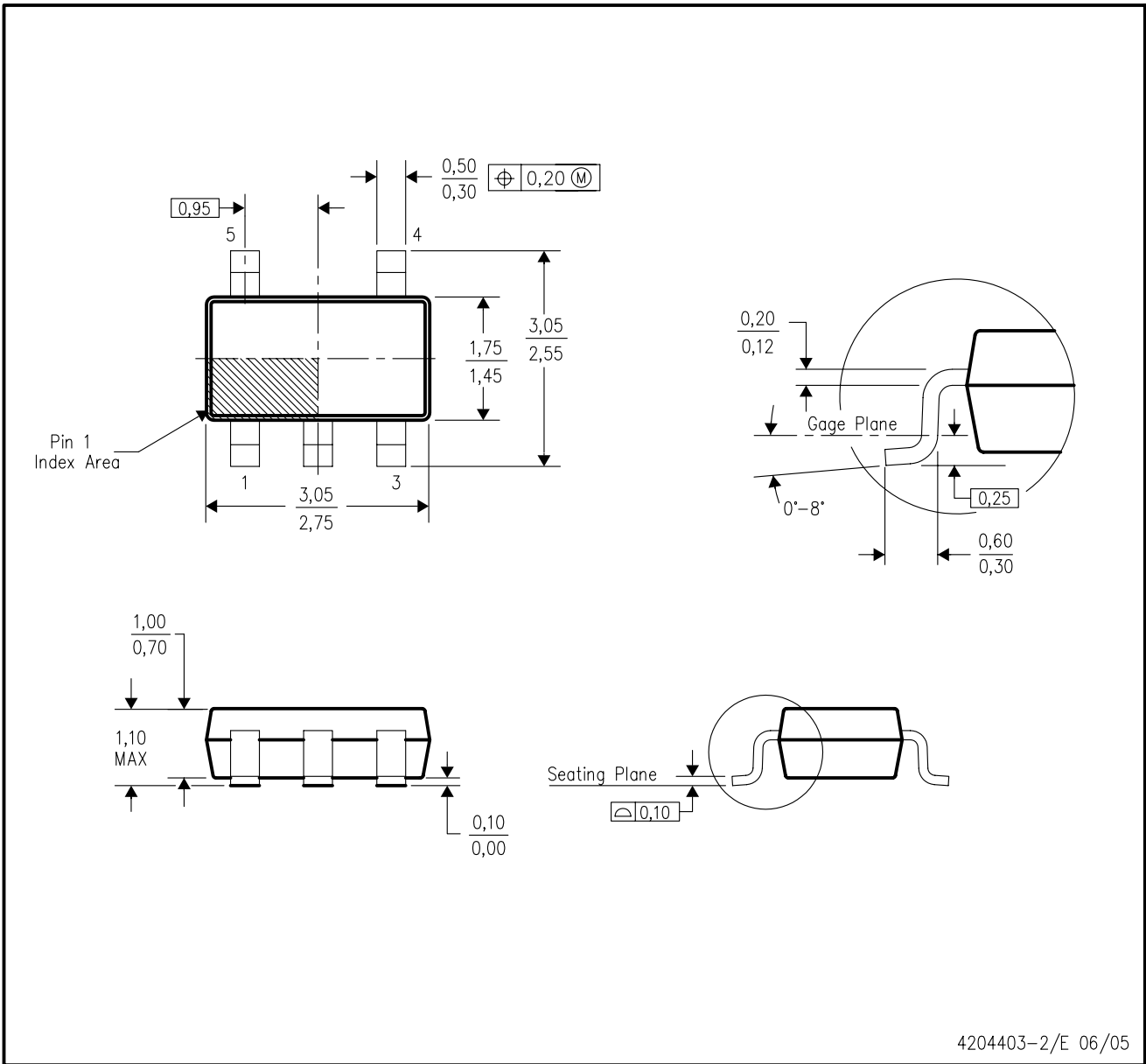
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS79901DDCR	SOT-23-THIN	DDC	5	3000	203.0	203.0	35.0
TPS79901DDCR	SOT-23-THIN	DDC	5	3000	202.0	201.0	28.0
TPS79901DDCT	SOT-23-THIN	DDC	5	250	202.0	201.0	28.0
TPS79901DDCT	SOT-23-THIN	DDC	5	250	203.0	203.0	35.0
TPS79901DRVR	WSON	DRV	6	3000	203.0	203.0	35.0
TPS79901DRVT	WSON	DRV	6	250	203.0	203.0	35.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS79901YZUR	DSBGA	YZU	5	3000	210.0	185.0	35.0
TPS79901YZUT	DSBGA	YZU	5	250	210.0	185.0	35.0
TPS799125YZUR	DSBGA	YZU	5	3000	182.0	182.0	20.0
TPS799125YZUT	DSBGA	YZU	5	250	182.0	182.0	20.0
TPS79912DDCR	SOT-23-THIN	DDC	5	3000	203.0	203.0	35.0
TPS79912DDCT	SOT-23-THIN	DDC	5	250	203.0	203.0	35.0
TPS79912DRVR	WSON	DRV	6	3000	203.0	203.0	35.0
TPS79912DRVT	WSON	DRV	6	250	203.0	203.0	35.0
TPS79912YZUR	DSBGA	YZU	5	3000	210.0	185.0	35.0
TPS79912YZUT	DSBGA	YZU	5	250	210.0	185.0	35.0
TPS79913DDCR	SOT-23-THIN	DDC	5	3000	203.0	203.0	35.0
TPS79913DDCT	SOT-23-THIN	DDC	5	250	203.0	203.0	35.0
TPS79913YZUR	DSBGA	YZU	5	3000	210.0	185.0	35.0
TPS79913YZUT	DSBGA	YZU	5	250	210.0	185.0	35.0
TPS79915DDCR	SOT-23-THIN	DDC	5	3000	203.0	203.0	35.0
TPS79915DDCT	SOT-23-THIN	DDC	5	250	203.0	203.0	35.0
TPS79915YZUR	DSBGA	YZU	5	3000	210.0	185.0	35.0
TPS79915YZUT	DSBGA	YZU	5	250	210.0	185.0	35.0
TPS799185DDCR	SOT-23-THIN	DDC	5	3000	203.0	203.0	35.0
TPS799185DDCT	SOT-23-THIN	DDC	5	250	203.0	203.0	35.0
TPS799185YZUR	DSBGA	YZU	5	3000	182.0	182.0	20.0
TPS799185YZUT	DSBGA	YZU	5	250	182.0	182.0	20.0
TPS79918DDCR	SOT-23-THIN	DDC	5	3000	203.0	203.0	35.0
TPS79918DDCT	SOT-23-THIN	DDC	5	250	203.0	203.0	35.0
TPS79918DRVR	WSON	DRV	6	3000	203.0	203.0	35.0
TPS79918DRVT	WSON	DRV	6	250	203.0	203.0	35.0
TPS79918YZUR	DSBGA	YZU	5	3000	182.0	182.0	20.0
TPS79918YZUT	DSBGA	YZU	5	250	182.0	182.0	20.0
TPS799195DRVR	WSON	DRV	6	3000	203.0	203.0	35.0
TPS799195DRVT	WSON	DRV	6	250	203.0	203.0	35.0
TPS799195YZUR	DSBGA	YZU	5	3000	182.0	182.0	20.0
TPS799195YZUT	DSBGA	YZU	5	250	182.0	182.0	20.0
TPS79919YZUR	DSBGA	YZU	5	3000	210.0	185.0	35.0
TPS79919YZUT	DSBGA	YZU	5	250	210.0	185.0	35.0
TPS79920YZUR	DSBGA	YZU	5	3000	210.0	185.0	35.0
TPS79920YZUT	DSBGA	YZU	5	250	210.0	185.0	35.0
TPS79921YZUR	DSBGA	YZU	5	3000	210.0	185.0	35.0
TPS79921YZUT	DSBGA	YZU	5	250	210.0	185.0	35.0
TPS79925DDCR	SOT-23-THIN	DDC	5	3000	203.0	203.0	35.0
TPS79925DDCT	SOT-23-THIN	DDC	5	250	203.0	203.0	35.0
TPS79925YZUR	DSBGA	YZU	5	3000	210.0	185.0	35.0
TPS79925YZUT	DSBGA	YZU	5	250	210.0	185.0	35.0
TPS79926YZUR	DSBGA	YZU	5	3000	182.0	182.0	20.0
TPS79926YZUT	DSBGA	YZU	5	250	182.0	182.0	20.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS799275YZUR	DSBGA	YZU	5	3000	210.0	185.0	35.0
TPS799275YZUT	DSBGA	YZU	5	250	210.0	185.0	35.0
TPS79927DDCR	SOT-23-THIN	DDC	5	3000	203.0	203.0	35.0
TPS79927DDCT	SOT-23-THIN	DDC	5	250	203.0	203.0	35.0
TPS79927DRVR	WSON	DRV	6	3000	203.0	203.0	35.0
TPS79927DRVT	WSON	DRV	6	250	203.0	203.0	35.0
TPS79927YZUT	DSBGA	YZU	5	250	210.0	185.0	35.0
TPS799285DDCR	SOT-23-THIN	DDC	5	3000	203.0	203.0	35.0
TPS799285DDCT	SOT-23-THIN	DDC	5	250	203.0	203.0	35.0
TPS799285DRVR	WSON	DRV	6	3000	203.0	203.0	35.0
TPS799285DRVT	WSON	DRV	6	250	203.0	203.0	35.0
TPS799285YZUR	DSBGA	YZU	5	3000	210.0	185.0	35.0
TPS79928DDCR	SOT-23-THIN	DDC	5	3000	203.0	203.0	35.0
TPS79928DDCT	SOT-23-THIN	DDC	5	250	203.0	203.0	35.0
TPS79928DRVR	WSON	DRV	6	3000	203.0	203.0	35.0
TPS79928DRVT	WSON	DRV	6	250	203.0	203.0	35.0
TPS79928YZUR	DSBGA	YZU	5	3000	210.0	185.0	35.0
TPS79928YZUT	DSBGA	YZU	5	250	210.0	185.0	35.0
TPS79930DDCR	SOT-23-THIN	DDC	5	3000	202.0	201.0	28.0
TPS79930DDCR	SOT-23-THIN	DDC	5	3000	203.0	203.0	35.0
TPS79930DDCT	SOT-23-THIN	DDC	5	250	203.0	203.0	35.0
TPS79930YZUR	DSBGA	YZU	5	3000	210.0	185.0	35.0
TPS79930YZUT	DSBGA	YZU	5	250	210.0	185.0	35.0
TPS799315DDCR	SOT-23-THIN	DDC	5	3000	203.0	203.0	35.0
TPS799315DDCT	SOT-23-THIN	DDC	5	250	203.0	203.0	35.0
TPS799315YZUR	DSBGA	YZU	5	3000	210.0	185.0	35.0
TPS799315YZUT	DSBGA	YZU	5	250	210.0	185.0	35.0
TPS79932YZUR	DSBGA	YZU	5	3000	210.0	185.0	35.0
TPS79932YZUT	DSBGA	YZU	5	250	210.0	185.0	35.0
TPS79933DDCR	SOT-23-THIN	DDC	5	3000	203.0	203.0	35.0
TPS79933DDCR	SOT-23-THIN	DDC	5	3000	202.0	201.0	28.0
TPS79933DDCT	SOT-23-THIN	DDC	5	250	203.0	203.0	35.0
TPS79933DDCT	SOT-23-THIN	DDC	5	250	202.0	201.0	28.0
TPS79933DRVR	WSON	DRV	6	3000	203.0	203.0	35.0
TPS79933DRVT	WSON	DRV	6	250	203.0	203.0	35.0
TPS79933YZUR	DSBGA	YZU	5	3000	210.0	185.0	35.0
TPS79933YZUT	DSBGA	YZU	5	250	210.0	185.0	35.0
TPS79942DDCR	SOT-23-THIN	DDC	5	3000	203.0	203.0	35.0
TPS79942DDCT	SOT-23-THIN	DDC	5	250	203.0	203.0	35.0
TPS79945YZUR	DSBGA	YZU	5	3000	210.0	185.0	35.0
TPS79945YZUT	DSBGA	YZU	5	250	210.0	185.0	35.0

DDC (R-PDSO-G5)

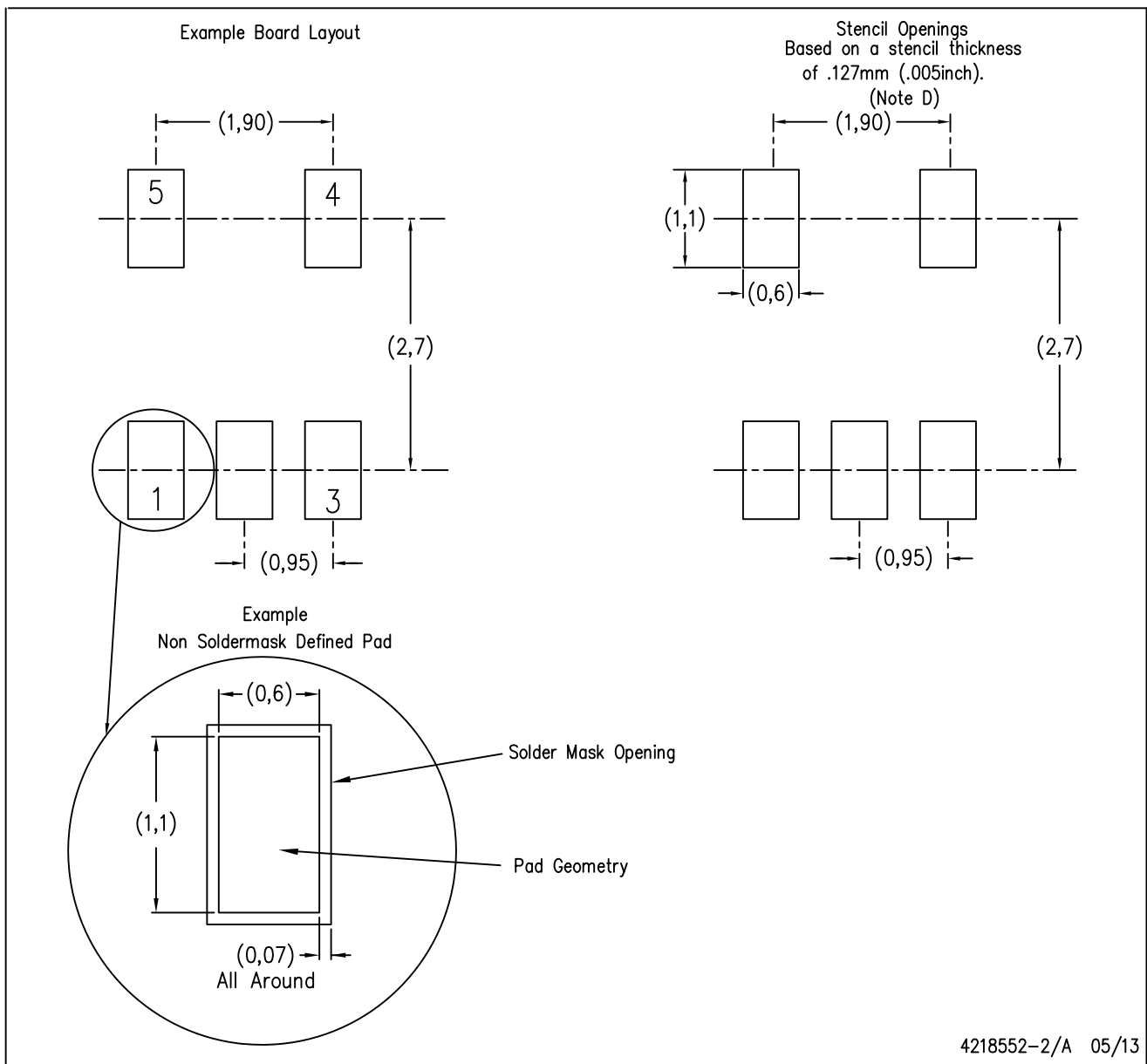
PLASTIC SMALL-OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion.
 - D. Falls within JEDEC MO-193 variation AB (5 pin).

DDC (R-PDSO-G5)

PLASTIC SMALL OUTLINE

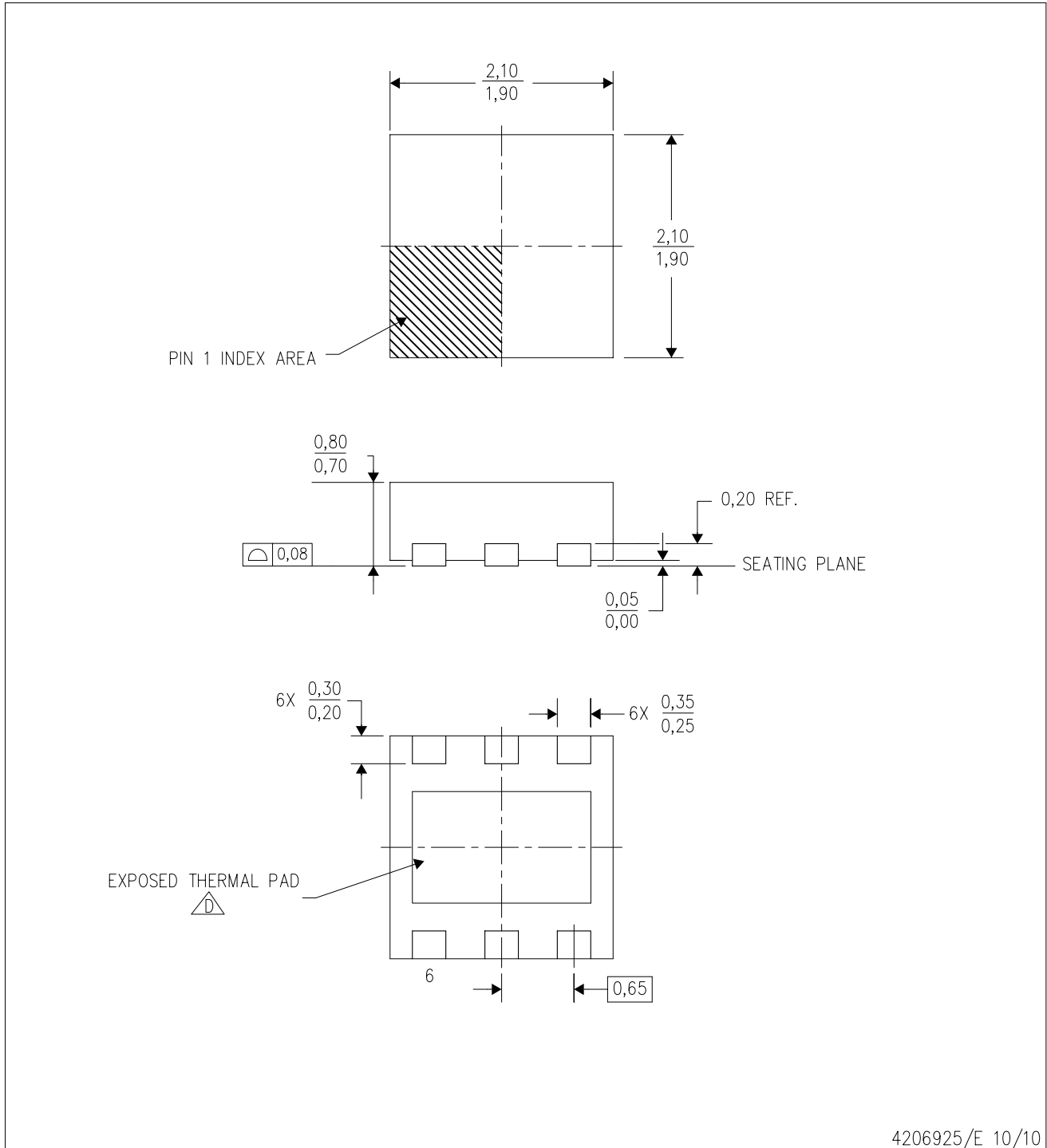


- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

MECHANICAL DATA

DRV (S-PWSON-N6)

PLASTIC SMALL OUTLINE NO-LEAD



4206925/E 10/10

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - Small Outline No-Lead (SON) package configuration.
- D** The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

THERMAL PAD MECHANICAL DATA

DRV (S-PWSON-N6)

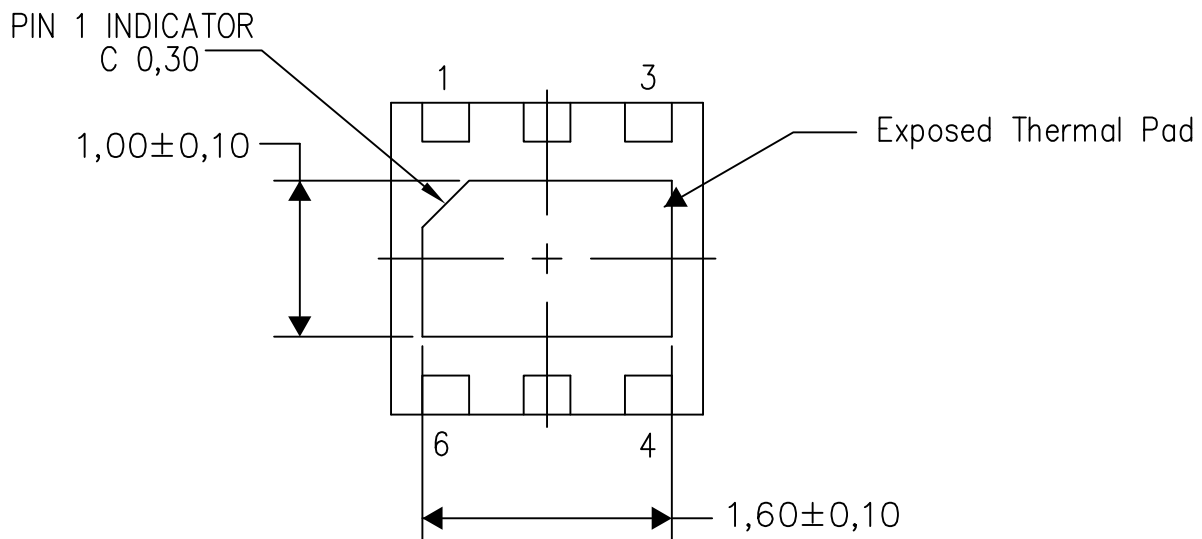
PLASTIC SMALL OUTLINE NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

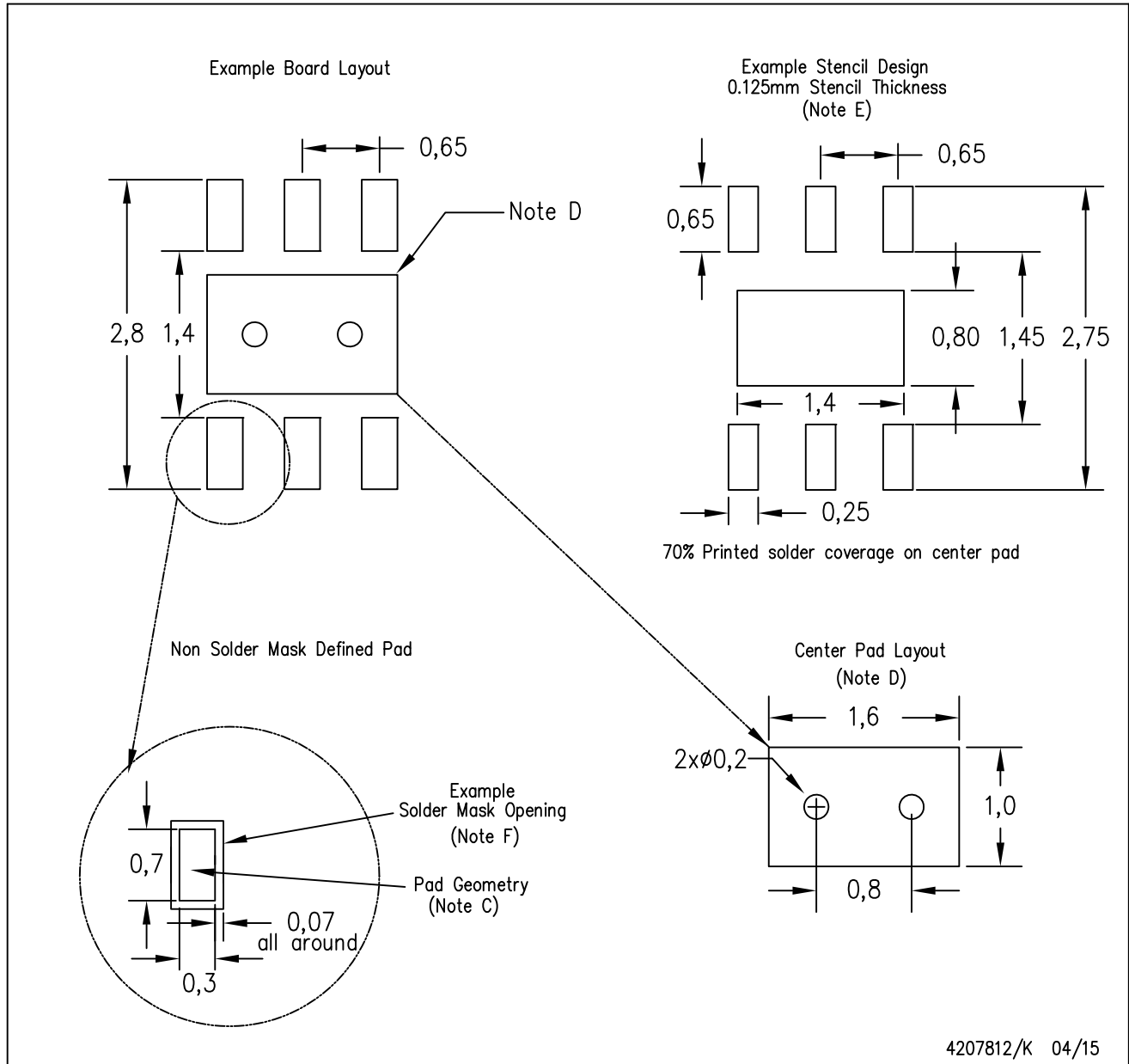
Exposed Thermal Pad Dimensions

4206926/Q 04/15

NOTE: All linear dimensions are in millimeters

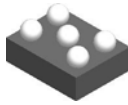
DRV (S-PWSON-N6)

PLASTIC SMALL OUTLINE NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - F. Customers should contact their board fabrication site for solder mask tolerances.

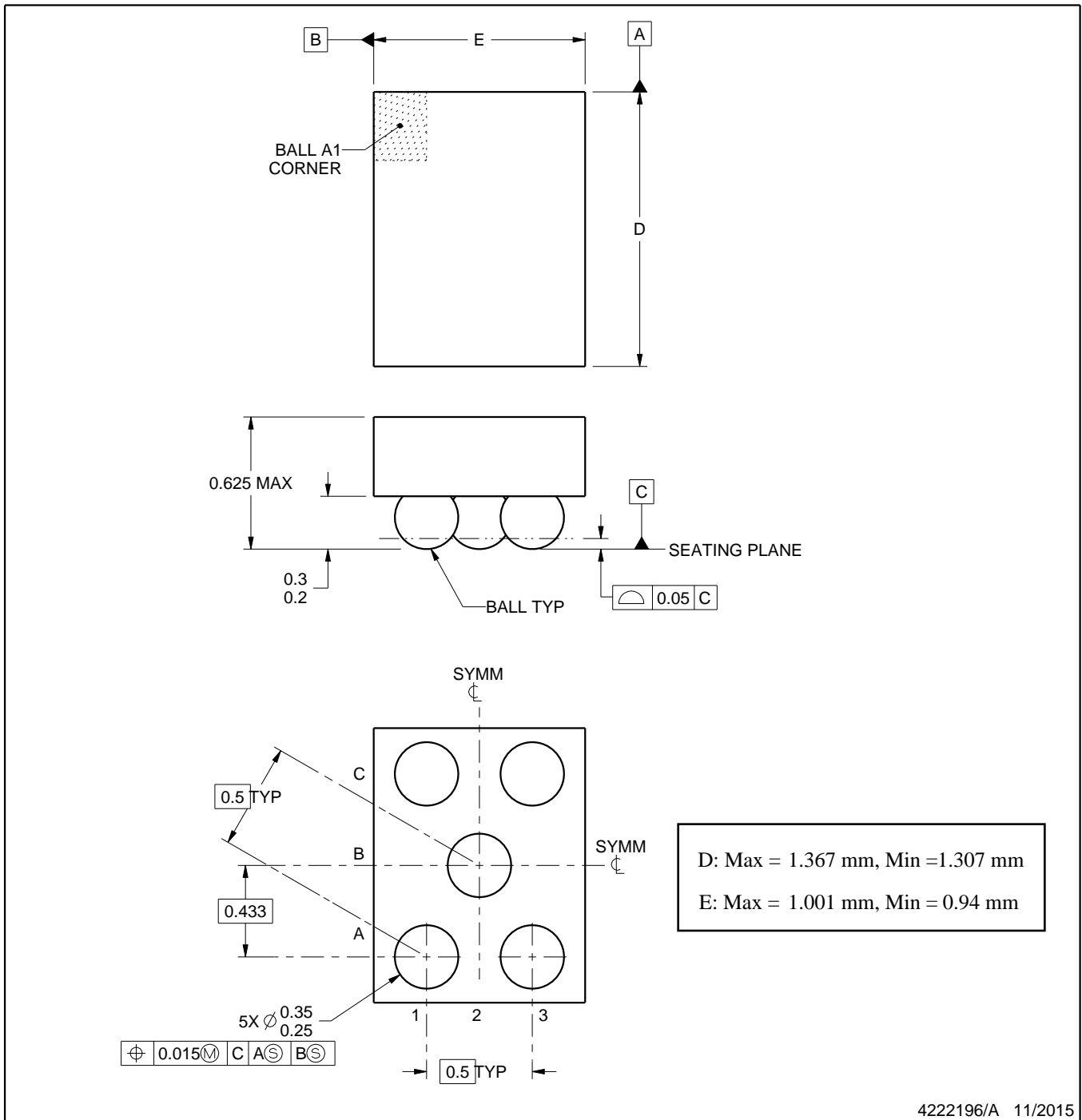
YZU0005



PACKAGE OUTLINE

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



4222196/A 11/2015

NOTES:

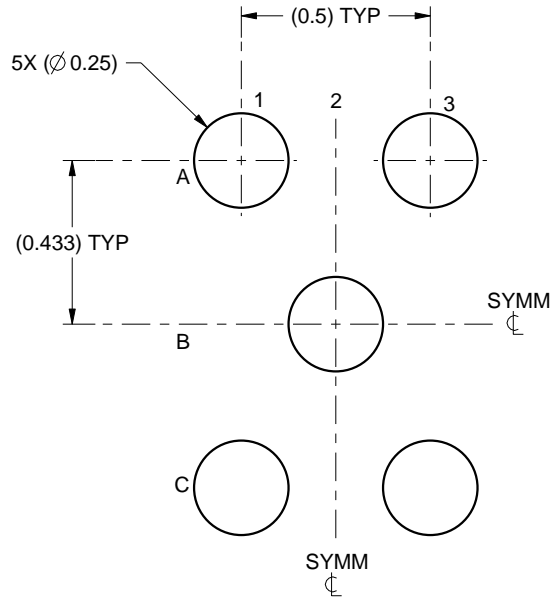
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

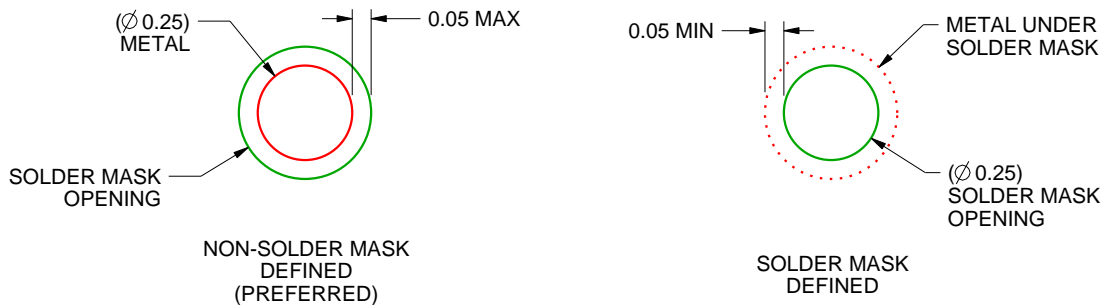
YZU0005

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
SCALE:50X



SOLDER MASK DETAILS
NOT TO SCALE

4222196/A 11/2015

NOTES: (continued)

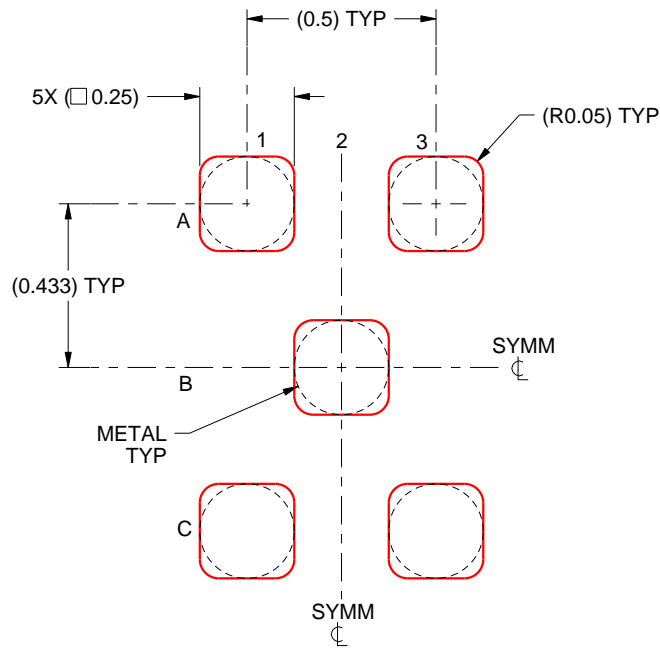
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. Refer to Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YZU0005

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:50X

4222196/A 11/2015

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.