TPS7A16xx-Q1 60-V, 5-µA I_Q, 100-mA, Low-Dropout Voltage Regulator With Enable and Power-Good

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 1: –40°C to 125°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level H2
  - Device CDM ESD Classification Level C3B
- Wide Input Voltage Range: 3 V to 60 V
- Ultralow Quiescent Current: 5 µA
- Quiescent Current at Shutdown: 1 µA
- Output Current: 100 mA
- Low Dropout Voltage: 60 mV at 20 mA
- Accuracy: 2%
- Available in:
  - Fixed Output Voltage: 3.3 V, 5 V
  - Adjustable Version From Approximately 1.2 to 18.5 V
- Power-Good With Programable Delay
- Current-Limit and Thermal Shutdown Protections
- Stable With Ceramic Output Capacitors: ≥ 2.2 µF
- Package: High-Thermal-Performance MSOP-8 PowerPAD™ Package

2 Applications

- High Cell-Count Battery Packs for Power Tools and Other Battery-Powered Microprocessor and Microcontroller Systems
- Car Audio, Navigation, Infotainment, and Other Automotive Systems
- Power Supplies for Notebook PCs, Digital TVs, and Private LAN Systems
- Smoke or CO_2 Detectors and Battery-Powered Alarm or Security Systems

3 Description

The TPS7A16xx-Q1 ultralow-power, low-dropout (LDO) voltage regulators offer the benefits of ultralow quiescent current, high input voltage, and miniaturized, high-thermal-performance packaging.

The TPS7A16xx-Q1 devices are designed for continuous or sporadic (power backup) battery-powered applications where ultralow quiescent current is critical to extending system battery life.

The TPS7A16xx-Q1 devices offer an enable pin (EN) compatible with standard CMOS logic and an integrated open-drain active-high power-good output (PG) with a user-programmable delay. These pins are intended for use in microcontroller-based, battery-powered applications where power-rail sequencing is required.

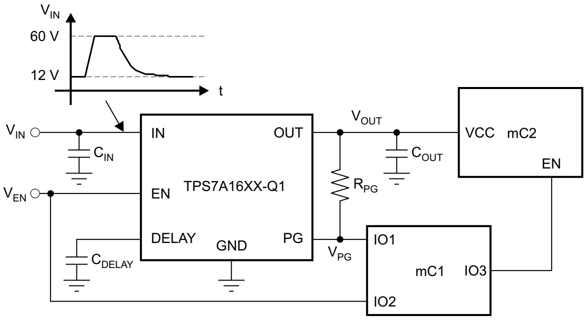
In addition, the TPS7A16xx-Q1 devices are ideal for generating a low-voltage supply from multicell solutions ranging from high-cell-count power-tool packs to automotive applications; not only can these devices supply a well-regulated voltage rail, but they can also withstand and maintain regulation during voltage transients. These features translate to simpler and more cost-effective, electrical surge-protection circuitry.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS7A1601-Q1	HVSSOP (8)	3.00 mm x 3.00 mm
TPS7A1633-Q1		
TPS7A1650-Q1		

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Typical Application Schematic



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (August 2014) to Revision D — Page

- Changed data sheet title 1
- Changed pinout drawing 3
- Changed *Handling Ratings* table to *ESD Ratings*; moved storage temperature to *Absolute Maximum Ratings* 4
- Changed maximum EN pin voltage and added a row for EN slew rate 4
- Changed UNIT for accuracy on V_{OUT} 5
- Changed *Ground current* to *Quiescent current* 5
- Changed Figure 2 6
- Changed caption of Figure 3 6
- Changed and added text in *Enable (EN)* 9
- Moved three paragraphs of text from *Layout Example* to *Layout Guidelines* 17

Changes from Revision B (May 2012) to Revision C — Page

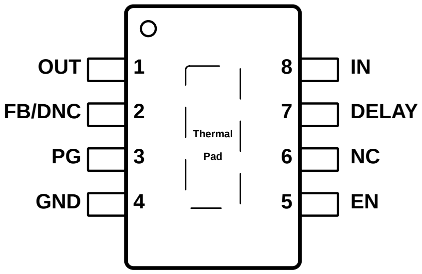
- Added *Handling Rating* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section 4

Changes from Revision A (March 2012) to Revision B — Page

- Changed to AEC-Q100 Qualified With the Following Results 1

5 Pin Configuration and Functions

DGN Package
8-Pin HVSSOP With Exposed Thermal Pad
Top View



NC – No internal connection

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
DELAY	7	O	Delay pin. Connect a capacitor to GND to adjust the PG delay time; leave open if the reset function is not needed.
EN	5	I	Enable pin. This pin turns the regulator on or off. If $V_{EN} \geq V_{EN\_HI}$, the regulator is enabled. If $V_{EN} \leq V_{EN\_LO}$, the regulator is disabled. If not used, the EN pin can be connected to IN. Make sure that $V_{EN} \leq V_{IN}$ at all times.
FB/DNC	2	I	For the adjustable version (TPS7A1601-Q1), the feedback pin is the input to the control-loop error amplifier. This pin is used to set the output voltage of the device when the regulator output voltage is set by external resistors. For the fixed voltage versions: **Do not connect** to this pin. Do not route this pin to any electrical net, not even GND or IN.
GND	4	—	Ground pin
IN	8	I	Regulator input supply pin. A capacitor > 0.1 µF must be tied from this pin to ground to assure stability. It is recommended to connect a 10-µF ceramic capacitor from IN to GND (as close to the device as possible) to reduce circuit sensitivity to printed-circuit-board (PCB) layout, especially when long input tracer or high source impedances are encountered.
NC	6	---	This pin can be left open or tied to any voltage between GND and IN.
OUT	1	O	Regulator output pin. A capacitor > 2.2 µF must be tied from this pin to ground to assure stability. It is recommended to connect a 10-µF ceramic capacitor from OUT to GND (as close to the device as possible) to maximize ac performance.
PG	3	O	Power-good pin. Open-collector output; leave open or connect to GND if the power-good function is not needed.
Thermal pad		---	Solder to printed circuit board (PCB) to enhance thermal performance. Although it can be left floating, it is highly recommended to connect the thermal pad to the GND plane.

6 Specifications

6.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Voltage	IN pin to GND pin	–0.3	62	V
	OUT pin to GND pin	–0.3	20	
	OUT pin to IN pin	–62	0.3	
	FB pin to GND pin	–0.3	3	
	FB pin to IN pin	–62	0.3	
	EN pin to IN pin	–62	0.3	
	EN pin to GND pin	–0.3	62	
	PG pin to GND pin	–0.3	5.5	
	DELAY pin to GND pin	–0.3	5.5	
Current	Peak output	Internally limited		
Temperature	Operating virtual junction, T_J, absolute maximum range (2)	–40	150	°C
	Storage temperature range	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Permanent damage does not occur to the part operating within this range, though electrical performance is not guaranteed outside the operating ambient temperature range.

6.2 ESD Ratings

				MIN	MAX	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 (1)		–2	2	kV
		Charged device model (CDM), per AEC Q100-011	Corner pins (OUT, GND, IN, and EN)	–750	750	V
			Other pins	–500	500	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Unregulated input	3		60	V
V_{OUT}	Regulated output	1.2		18	V
EN	Voltage	0		V_{IN}	V
	Slew rate, voltage ramp-up			1.5	V/µs
DELAY		0		5	V
PG		0		5	V
T_J	Operating junction temperature range	–40		150	°C

6.4 Thermal Information

THERMAL METRIC (1)		TPS7A16xx-Q1 DGN (HVSSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	66.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	45.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	34.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	34.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

Thermal Information (continued)

THERMAL METRIC[1]		TPS7A16xx-Q1 DGN (HVSSOP) 8 PINS	UNIT
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	14.9	°C/W

6.5 Electrical Characteristics

At T_A= –40°C to 125°C, $V_{IN} = V_{OUT(NOM)}$ + 0.5 V or V_{IN} = 3 V (whichever is greater), $V_{EN} = V_{IN}$, I_{OUT} = 10 µA, C_{IN} = 1 µF, C_{OUT} = 2.2 µF, and FB tied to OUT, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range		3		60	V
V_{REF}	Internal reference	T_A = 25°C, $V_{FB} = V_{REF}$, V_{IN} = 3 V, I_{OUT} = 10 µA	1.169	1.193	1.217	V
V_{UVLO}	Undervoltage lockout threshold			2.7		V
V_{OUT}	Output voltage range	$V_{IN} \geq V_{OUT(NOM)}$ + 0.5 V	V_{REF}		18.5	V
	Nominal accuracy	T_A = 25°C, V_{IN} = 3 V, I_{OUT} = 10 µA	–2%		2%	
	Overall accuracy	$V_{OUT(NOM)}$ + 0.5 V ≤ V_{IN} ≤ 60 V[1] 10 µA ≤ I_{OUT} ≤ 100 mA	–2%		2%	
$\Delta V_{O(\Delta VI)}$	Line regulation	3 V ≤ V_{IN} ≤ 60 V		±1		$\%V_{OUT}$
$\Delta V_{O(\Delta IO)}$	Load regulation	10 µA ≤ I_{OUT} ≤ 100 mA		±1		$\%V_{OUT}$
V_{DO}	Dropout voltage	V_{IN} = 4.5 V, $V_{OUT(NOM)}$ = 5 V, I_{OUT} = 20 mA		60		mV
		V_{IN} = 4.5 V, $V_{OUT(NOM)}$ = 5 V, I_{OUT} = 100 mA		265	500	mV
I_{LIM}	Current limit	V_{OUT} = 90% $V_{OUT(NOM)}$, V_{IN} = 3.0 V	101	225	400	mA
I_Q	Quiescent current	3 V ≤ V_{IN} ≤ 60 V, I_{OUT} = 10 µA		5	15	µA
		I_{OUT} = 100 mA		5		µA
I_{SHDN}	Shutdown supply current	V_{EN} = 0.4 V		0.59	5.0	µA
I_{FB}	Feedback current[2]		–1	0.0	1	µA
I_{EN}	Enable current	3 V ≤ V_{IN} ≤ 12 V, $V_{IN} = V_{EN}$	–1	0.01	1	µA
V_{EN_HI}	Enable high-level voltage		1.2			V
V_{EN_LO}	Enable low- level voltage				0.3	V
V_{IT}	PG trip threshold	OUT pin floating, V_{FB} increasing, $V_{IN} \geq V_{IN\_MIN}$	85		95	$\%V_{OUT}$
		OUT pin floating, V_{FB} decreasing, $V_{IN} \geq V_{IN\_MIN}$	83		93	$\%V_{OUT}$
V_{HYS}	PG trip hysteresis			2.3	4	$\%V_{OUT}$
$V_{PG,\ LO}$	PG output low voltage	OUT pin floating, V_{FB} = 80% V_{REF}, I_{PG}= 1mA			0.4	V
$I_{PG,\ LKG}$	PG leakage current	$V_{PG}= V_{OUT(NOM)}$	–1		1	µA
I_{DELAY}	DELAY pin current			1	2	µA
PSRR	Power-supply rejection ratio	V_{IN} = 3 V, $V_{OUT(NOM)} = V_{REF}$, C_{OUT} = 10 µF, f = 100 Hz		50		dB
T_{SD}	Thermal shutdown temperature	Shutdown, temperature increasing		170		°C
		Reset, temperature decreasing		150		°C
T_A	Operating ambient temperature range		–40		125	°C

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[1] Maximum input voltage is limited to 24 V because of the package power dissipation limitations at full load ($P \approx (V_{IN} - V_{OUT}) \times I_{OUT} = (24\ V - V_{REF}) \times 50\ mA \approx 1.14\ W$). The device is capable of sourcing a maximum current of 50 mA at higher input voltages as long as the power dissipated is within the thermal limits of the package plus any external heatsinking.

[2] I_{FB} > 0 flows out of the device.

6.6 Typical Characteristics

At T_A = –40°C to 125°C, $V_{IN} = V_{OUT(NOM)}$ + 0.5 V or V_{IN} = 3 V (whichever is greater), $V_{EN} = V_{IN}$, I_{OUT} = 10 µA, C_{IN} = 1 µF, C_{OUT} = 2.2 µF, and FB tied to OUT, unless otherwise noted.

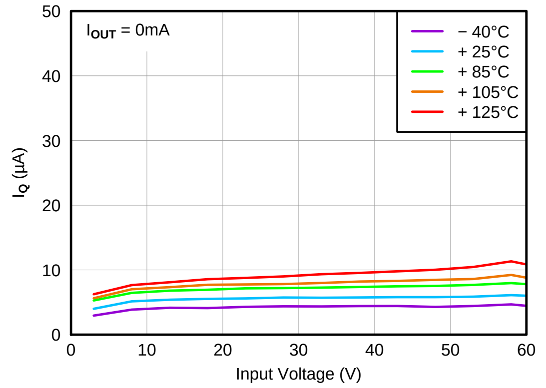


Figure 1. Quiescent Current vs Input Voltage

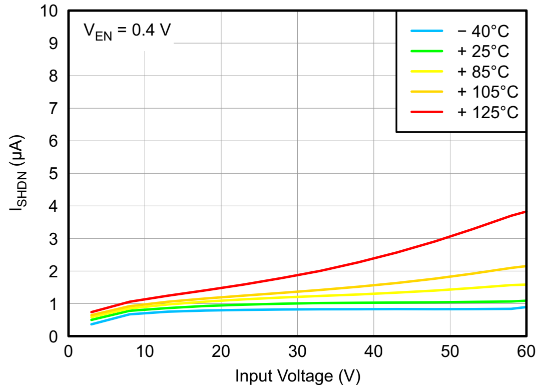


Figure 2. Shutdown Current vs Input Voltage

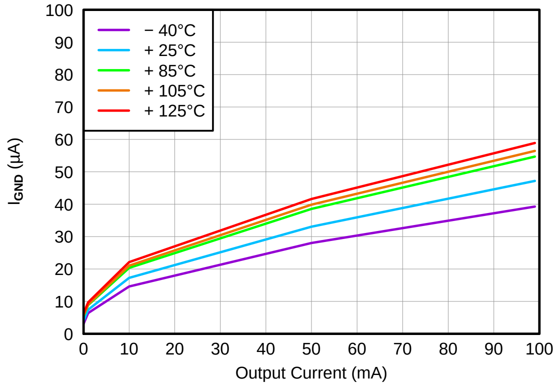


Figure 3. Quiescent Current vs Output Current

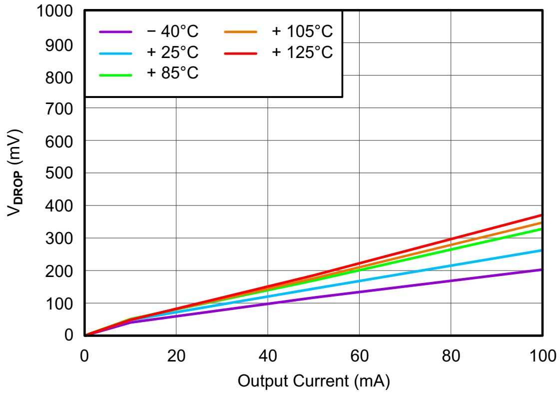


Figure 4. Dropout Voltage vs Output Current

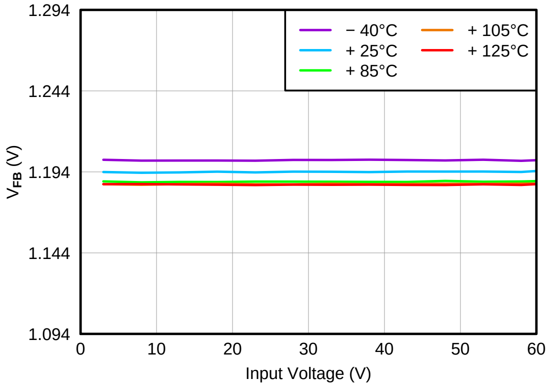


Figure 5. Feedback Voltage vs Input Voltage

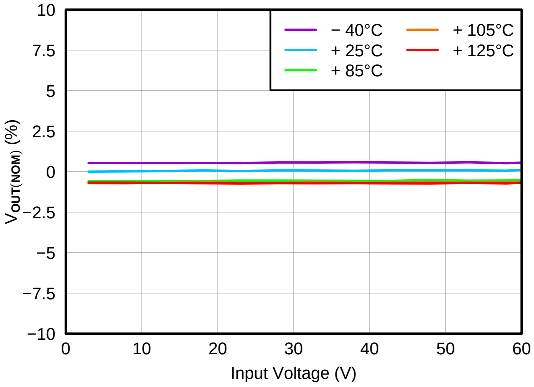


Figure 6. Line Regulation

Typical Characteristics (continued)

At T_A = –40°C to 125°C, $V_{IN} = V_{OUT(NOM)}$ + 0.5 V or V_{IN} = 3 V (whichever is greater), $V_{EN} = V_{IN}$, I_{OUT} = 10 µA, C_{IN} = 1 µF, C_{OUT} = 2.2 µF, and FB tied to OUT, unless otherwise noted.

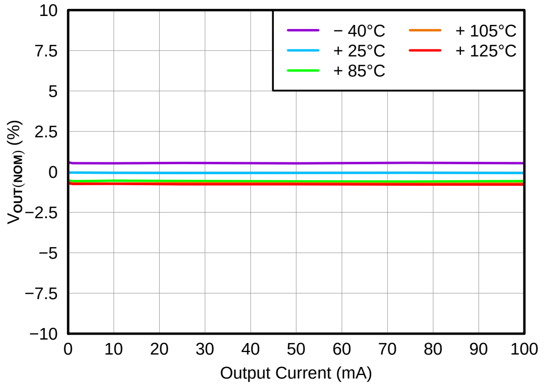


Figure 7. Load Regulation

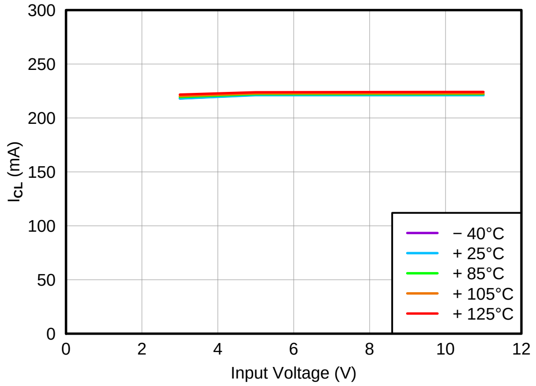


Figure 8. Current Limit vs Input Voltage

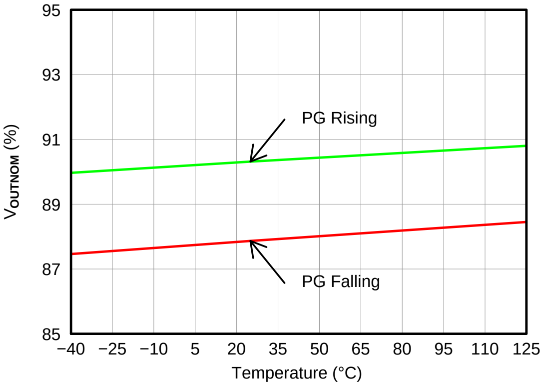


Figure 9. Power-Good Threshold Voltage vs Temperature

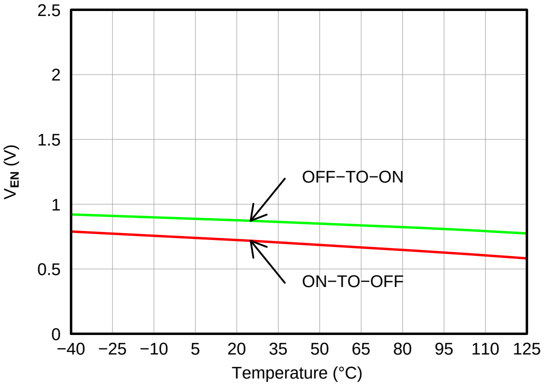


Figure 10. Enable Threshold Voltage vs Temperature

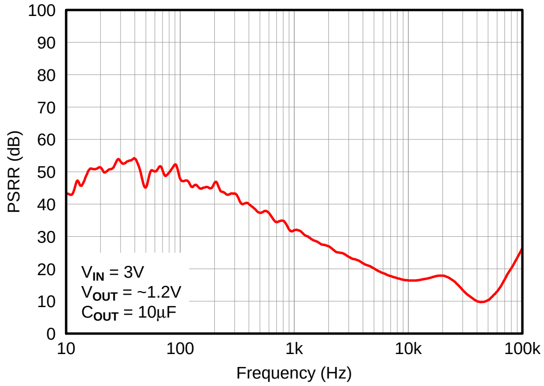


Figure 11. Power-Supply Rejection Ratio

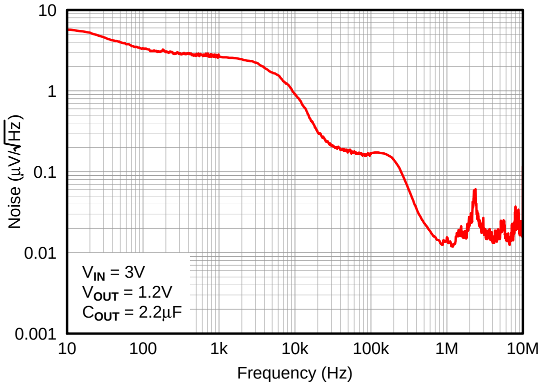


Figure 12. Output Spectral Noise Density

Typical Characteristics (continued)

At T_A = –40°C to 125°C, $V_{IN} = V_{OUT(NOM)}$ + 0.5 V or V_{IN} = 3 V (whichever is greater), $V_{EN} = V_{IN}$, I_{OUT} = 10 µA, C_{IN} = 1 µF, C_{OUT} = 2.2 µF, and FB tied to OUT, unless otherwise noted.

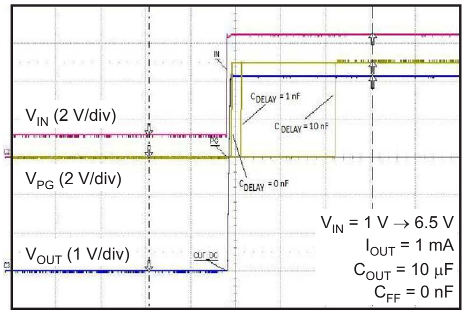


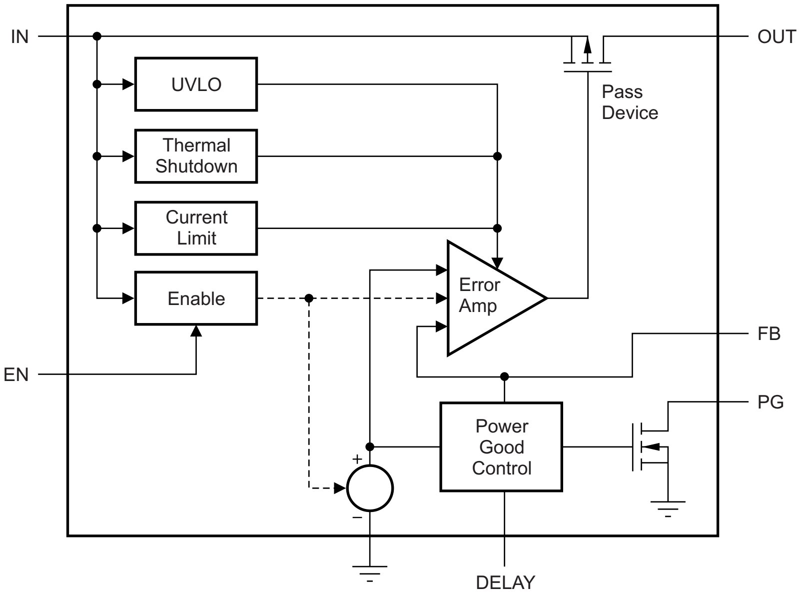
Figure 13. Power-Good Delay

7 Detailed Description

7.1 Overview

The TPS7A16xx-Q1 family of devices is ultra low power, low-dropout (LDO) voltage regulators that offers the benefits of ultra-low quiescent current, high input voltage, and miniaturized, high thermal-performance packaging. TPS7A16xx-Q1 family also offers an enable pin (EN) and integrated open-drain active-high power-good output (PG) with a user-programmable delay.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Enable (EN)

The enable terminal is a high-voltage-tolerant terminal. A high input on EN actives the device and turns on the regulator. For self-bias applications, connect this input to the V_{IN} terminal. Ensure that $V_{EN} \leq V_{IN}$ at all times.

When the enable signal is PWM pulses, the slew rate of the rising and falling edges must be less than 1.5 V/µs. Adding a 0.1-µF capacitor from the EN pin to GND is recommended.

7.3.2 Regulated Output (V_{OUT})

The V_{OUT} terminal is the regulated output based on the required voltage. The output has current limitation. During initial power up, the regulator has a soft start incorporated to control the initial current through the pass element. In the event that the regulator drops out of regulation, the output tracks the input minus a drop based on the load current. When the input voltage drops below the UVLO threshold, the regulator shuts down until the input voltage recovers above the minimum start-up level.

7.3.3 PG Delay Timer (DELAY)

The power-good delay time (t_{DELAY}) is defined as the time period from when V_{OUT} exceeds the PG trip threshold voltage (V_{IT}) to when the PG output is high. This power-good delay time is set by an external capacitor (C_{DELAY}) connected from the DELAY pin to GND; this capacitor is charged from 0 V to ~1.8 V by the DELAY pin current (I_{DELAY}) once V_{OUT} exceeds the PG trip threshold (V_{IT}).

7.4 Device Functional Modes

7.4.1 Power-Good

The power-good (PG) pin is an open-drain output and can be connected to any 5.5-V or lower rail through an external pullup resistor. When no C_{DELAY} is used, the PG output is high-impedance when V_{OUT} is greater than the PG trip threshold (V_{IT}). If V_{OUT} drops below V_{IT}, the open-drain output turns on and pulls the PG output low. If output voltage monitoring is not needed, the PG pin can be left floating or connected to GND.

To ensure proper operation of the power-good feature, maintain $V_{IN} \geq 3$ V (V_{IN_MIN}).

7.4.1.1 Power-Good Delay and Delay Capacitor

The power-good delay time (t_{DELAY}) is defined as the time period from when V_{OUT} exceeds the PG trip threshold voltage (V_{IT}) to when the PG output is high. This power-good delay time is set by an external capacitor (C_{DELAY}) connected from the DELAY pin to GND; this capacitor is charged from 0 V to ap 1.8 V by the DELAY pin current (I_{DELAY}) once V_{OUT} exceeds the PG trip threshold (V_{IT}).

When C_{DELAY} is used, the PG output is high-impedance when V_{OUT} exceeds V_{IT}, and V_{DELAY} exceeds V_{REF}.

The power-good delay time can be calculated using: $t_{DELAY} = (C_{DELAY} \times V_{REF})/I_{DELAY}$. For example, when C_{DELAY} = 10 nF, the PG delay time is approximately 12 ms; that is, (10 nF × 1.193 V)/1 µA = 11.93 ms.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS7A16xx-Q1 family of ultralow-power voltage regulators offers the benefit of ultralow quiescent current, high input voltage, and miniaturized, high-thermal-performance packaging.

The TPS7A16xx-Q1 are designed for continuous or sporadic (power backup) battery-operated applications where ultralow quiescent current is critical to extending system battery life.

8.2 Typical Applications

8.2.1 TPS7A1601-Q1 Circuit as an Adjustable Regulator

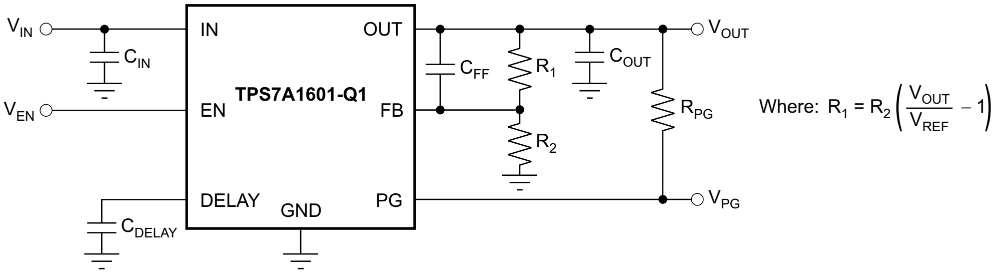


Figure 14. TPS7A1601-Q1 Circuit as an Adjustable Regulator Schematic

8.2.1.1 Design Requirements

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	5.5 V to 40 V
Output voltage	5 V
Output current rating	100 mA
Output capacitor range	2.2 µF to 100 µF
Delay capacitor range	100 pF to 100 nF

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Adjustable Voltage Operation

The TPS7A1601-Q1 has an output voltage range from 1.194 V to 20 V. The nominal output of the device is set by two external resistors, as shown in Figure 15:

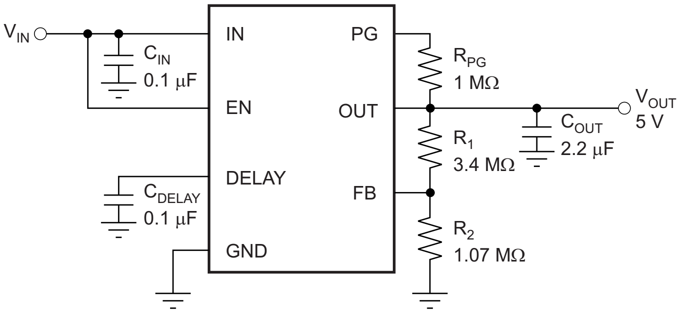


Figure 15. Adjustable Operation

R_1 and R_2 can be calculated for any output voltage range using the formula shown in Equation 1:

$$R_1 = R_2 \left(\frac{V_{OUT}}{V_{REF}} - 1 \right) \quad (1)$$

8.2.1.2.1.1 *Resistor Selection*

It is recommended to use resistors in the order of MΩ to keep the overall quiescent current of the system as low as possible (by making the current used by the resistor divider negligible compared to the quiescent current of the device).

If greater voltage accuracy is required, take into account the voltage offset contributions as a result of feedback current and use 0.1% tolerance resistors.

Table 2 shows the resistor combination to achieve an output for a few of the most common rails using commercially available 0.1% tolerance resistors to maximize nominal voltage accuracy, while adhering to the formula shown in Equation 1.

Table 2. Selected Resistor Combinations

V_{OUT}	R_1	R_2	$V_{OUT}/(R_1 + R_2) \ll I_Q$	NOMINAL ACCURACY
1.194 V	0 Ω	∞	0 µA	±2%
1.8 V	1.18 MΩ	2.32 MΩ	514 nA	±(2% + 0.14%)
2..5 V	1.5 MΩ	1.37 MΩ	871 nA	±(2% + 0.16%)
3.3 V	2 MΩ	1.13 MΩ	1056 nA	±(2% + 0.35%)
5 V	3.4 MΩ	1.07 MΩ	1115 nA	±(2% + 0.39%)
10 V	7.87 MΩ	1.07 MΩ	1115 nA	±(2% + 0.42%)
12 V	14.3 MΩ	1.58 MΩ	755 nA	±(2% + 0.18%)
15 V	42.2 MΩ	3.65 MΩ	327 nA	±(2% + 0.19%)
18 V	16.2 MΩ	1.15 MΩ	1038 nA	±(2% + 0.26%)

Close attention must be paid to board contamination when using high-value resistors; board contaminants may significantly impact voltage accuracy. If board cleaning measures cannot be ensured, consider using a fixed-voltage version of the TPS7A16 or using resistors in the order of hundreds or tens of kΩ.

8.2.1.2.2 Capacitor Recommendations

Low equivalent-series-resistance (ESR) capacitors should be used for the input, output, and feed-forward capacitors. Ceramic capacitors with X7R and X5R dielectrics are preferred. These dielectrics offer more stable characteristics. Ceramic X7R capacitors offer improved overtemperature performance, while ceramic X5R capacitors are the most cost-effective and are available in higher values.

Note that high-ESR capacitors may degrade PSRR.

8.2.1.2.3 Input and Output Capacitor Requirements

The TPS7A16xx-Q1 ultralow-power, high-voltage linear regulators achieve stability with a minimum input capacitance of 0.1 µF and output capacitance of 2.2 µF; however, it is recommended to use a 10-µF ceramic capacitor to maximize ac performance.

8.2.1.2.4 Feed-Forward Capacitor (Only for Adjustable Version)

Although a feed-forward capacitor (C_{FF}) from OUT to FB is not needed to achieve stability, it is recommended to use a 0.01-µF feed-forward capacitor to maximize ac performance.

8.2.1.2.5 Transient Response

As with any regulator, increasing the size of the output capacitor reduces over/undershoot magnitude but increases the duration of the transient response.

8.2.1.3 Application Curves

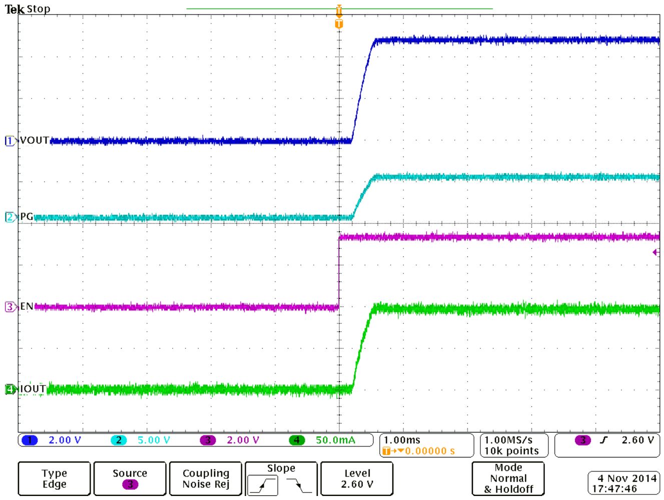


Figure 16. CH1 is VOUT, CH2 is PG, CH4 is Iout, VIN is 12 V and Ready Before EN

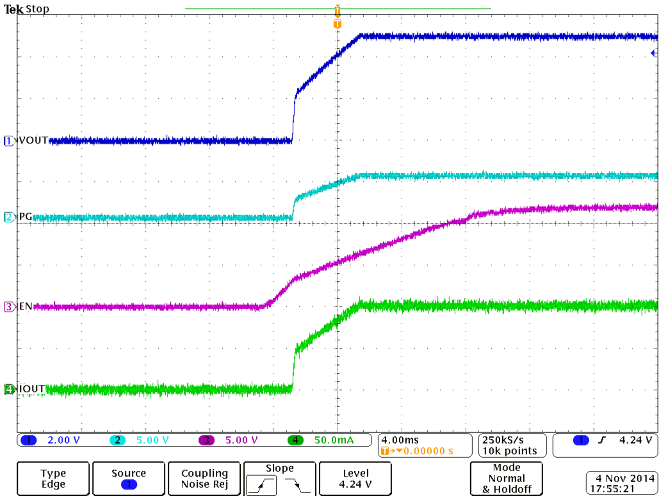


Figure 17. CH1 is VOUT, CH2 is PG, CH3 is EN, CH4 is Iout, VIN is 12 V Connected to EN

8.2.2 Automotive Applications

The TPS7A16xx-Q1 maximum input voltage of 60 V makes it ideal for use in automotive applications where high-voltage transients are present.

Events such as load-dump overvoltage (where the battery is disconnected while the alternator is providing current to a load) may cause voltage spikes from 25 V to 60 V. In order to prevent any damage to sensitive circuitry, local transient voltage suppressors can be used to cap voltage spikes to lower, more manageable voltages.

The TPS7A16xx-Q1 can be used to simplify and lower costs in such cases. The very high voltage range allows this regulator not only to withstand the voltages coming out of these local transient voltage suppressors, but even replace them, thus lowering system cost and complexity.

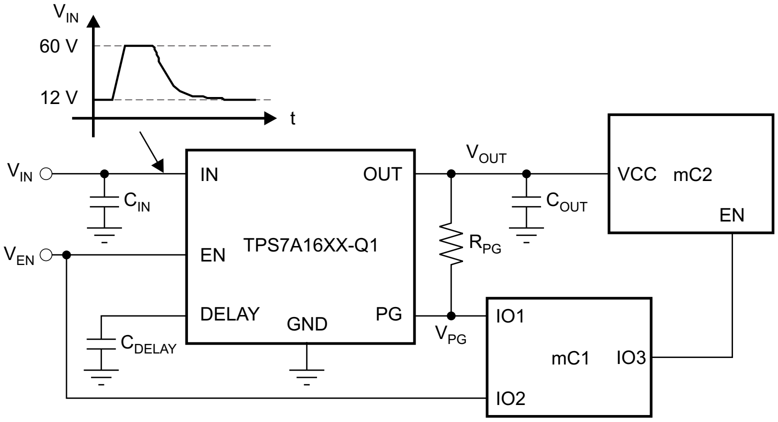


Figure 18. Low-Power Microcontroller Rail Sequencing in Automotive Applications Subjected to Load-Dump Transients

8.2.2.1 *Design Requirements*

Table 3. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	5.5 V to 60 V
Output voltage	5 V
Output current rating	100 mA
Output capacitor range	2.2 µF to 100 µF
Delay capacitor range	100 pF to 100 nF

8.2.2.2 *Detailed Design Procedure*

See *Capacitor Recommendations* and *Input and Output Capacitor Requirements*.

8.2.2.2.1 Device Recommendations

The output is fixed, so choose TPS7A1650-Q1.

8.2.2.3 *Application Curves*

See Figure 16 and Figure 17.

8.2.3 Multicell Battery Packs

Currently, battery packs can employ up to a dozen cells in series that, when fully charged, may have voltages of up to 55 V. Internal circuitry in these battery packs is used to prevent overcurrent and overvoltage conditions that may degrade battery life or even pose a safety risk; this internal circuitry is often managed by a low-power microcontroller, such as TI's MSP430™. See the overview for microcontrollers (MCU) for more information.

The microcontroller continuously monitors the battery itself, whether the battery is in use or not. Although this microcontroller could be powered by an intermediate voltage taken from the multicell array, this approach unbalances the battery pack itself, degrading its life or adding cost to implement more complex cell balancing topologies.

The best approach to power this microcontroller is to regulate down the voltage from the entire array to discharge every cell equally and prevent any balancing issues. This approach reduces system complexity and cost.

TPS7A16xx-Q1 is the ideal regulator for this application because it can handle very high voltages (from the entire multicell array) and has very low quiescent current (to maximize battery life).

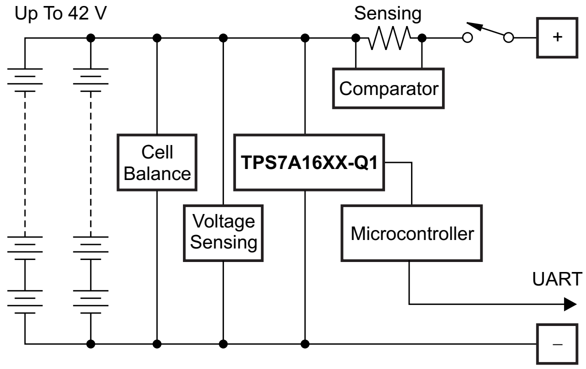


Figure 19. Protection Based on Low-Power Microcontroller Power From Multicell Battery Packs

8.2.3.1 Design Requirements

Table 4. Device Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	5.5 V to 55 V
Output voltage	5 V
Output current rating	100 mA
Output capacitor range	2.2 µF to 100 µF
Delay capacitor range	100 pF to 100 nF

8.2.3.2 Detailed Design Procedure

See *Device Recommendations*, *Capacitor Recommendations*, and *Input and Output Capacitor Requirements*.

8.2.3.3 Application Curves

See Figure 16 and Figure 17.

8.2.4 Battery-Operated Power Tools

High-voltage multicell battery packs support high-power applications, such as power tools, with high current drain when in use, highly intermittent use cycles, and physical separation between battery and motor.

In these applications, a microcontroller or microprocessor controls the motor. This microcontroller must be powered with a low-voltage rail coming from the high-voltage, multicell battery pack; as mentioned previously, powering this microcontroller or microprocessor from an intermediate voltage from the multicell array causes battery-pack life degradation or added system complexity because of cell balancing issues. In addition, this microcontroller or microprocessor must be protected from the high-voltage transients because of the motor inductance.

The TPS7A16xx-Q1 can be used to power the motor-controlled microcontroller or microprocessor; its low quiescent current maximizes battery shelf life, and its very high-voltage capabilities simplify system complexity by replacing voltage suppression filters, thus lowering system cost.

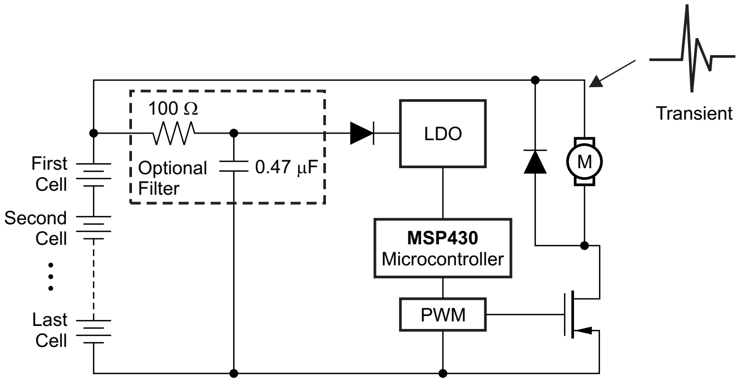


Figure 20. Low Power Microcontroller Power From Multi-Cell Battery Packs in Power Tools

8.2.4.1 Design Requirements

Table 5. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	5.5 V to 60 V
Output voltage	5 V
Output current rating	100 mA
Output capacitor range	2.2 µF to 100 µF
Delay capacitor range	100 pF to 100 nF

8.2.4.2 Detailed Design Procedure

See *Device Recommendations*, *Capacitor Recommendations*, and *Input and Output Capacitor Requirements*.

8.2.4.3 Application Curves

See Figure 16 and Figure 17.

9 Power Supply Recommendations

Design of the device is for operation from an input voltage supply with a range between 3 V and 60 V. This input supply must be well regulated. TPS7A16xx-Q1 ultralow-power, high-voltage linear regulators achieve stability with a minimum input capacitance of 0.1 μF and output capacitance of 2.2 μF; however, it is recommended to use a 10-μF ceramic capacitor to maximize AC performance.

10 Layout

10.1 Layout Guidelines

To improve ac performance such as PSRR, output noise, and transient response, it is recommended that the board be designed with separate ground planes for IN and OUT, with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the output capacitor should connect directly to the GND pin of the device.

Equivalent series inductance (ESL) and ESR must be minimized in order to maximize performance and ensure stability. Every capacitor must be placed as close as possible to the device and on the same side of the PCB as the regulator itself.

Do not place any of the capacitors on the opposite side of the PCB from where the regulator is installed. The use of vias and long traces is strongly discouraged because they may impact system performance negatively and even cause instability.

If possible, and to ensure the maximum performance denoted in this product data sheet, use the same layout pattern used for TPS7A16xx-Q1 evaluation board, available at www.ti.com.

Layout is a critical part of good power-supply design. There are several signal paths that conduct fast-changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power-supply performance. To help eliminate these problems, the IN pin should be bypassed to ground with a low-ESR ceramic bypass capacitor with X5R or X7R dielectric.

It may be possible to obtain acceptable performance with alternative PCB layouts; however, the layout and the schematic have been shown to produce good results and are meant as a guideline.

Figure 21 shows the schematic for the suggested layout. Figure 22 and Figure 23 show the top and bottom printed circuit board (PCB) layers for the suggested layout.

10.1.1 Additional Layout Considerations

The high impedance of the FB pin makes the regulator sensitive to parasitic capacitances that may couple undesirable signals from nearby components (especially from logic and digital ICs, such as microcontrollers and microprocessors); these capacitively-coupled signals may produce undesirable output voltage transients. In these cases, it is recommended to use a fixed-voltage version of the TPS7A16xx-Q1, or to isolate the FB node by flooding the local PCB area with ground-plane copper to minimize any undesirable signal coupling.

10.2 Layout Example

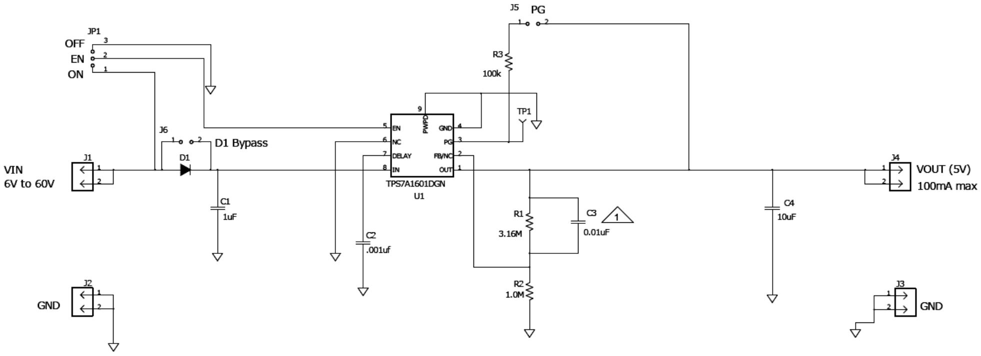


Figure 21. Schematic for Suggested Layout

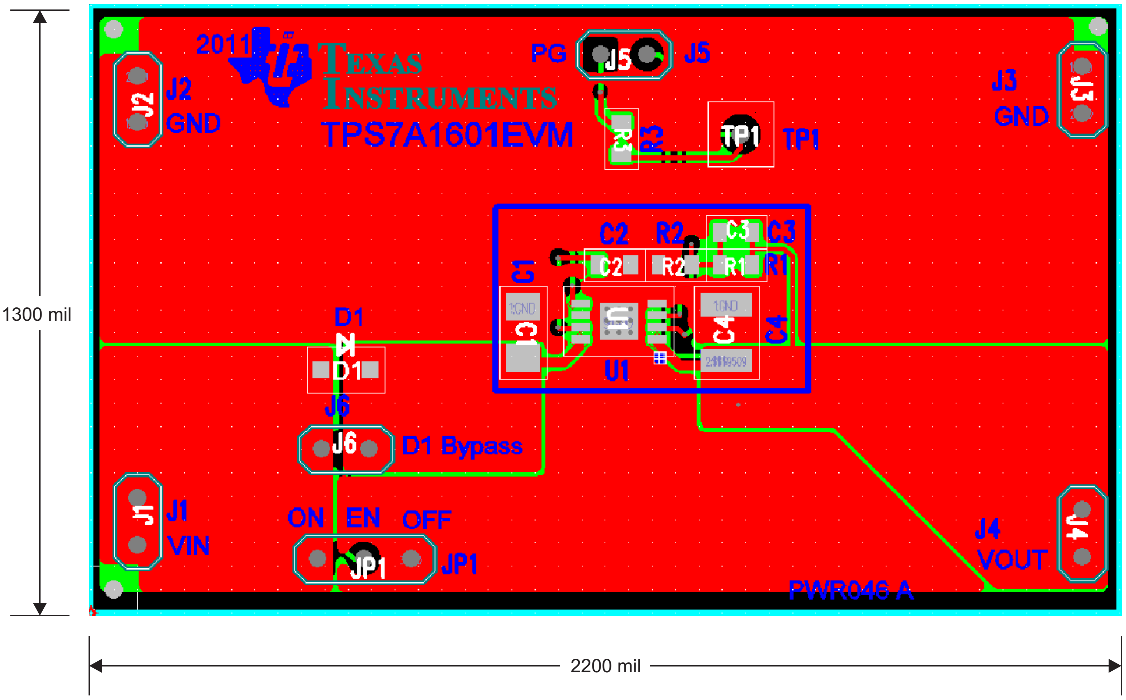


Figure 22. Suggested Layout: Top Layer

Layout Example (continued)

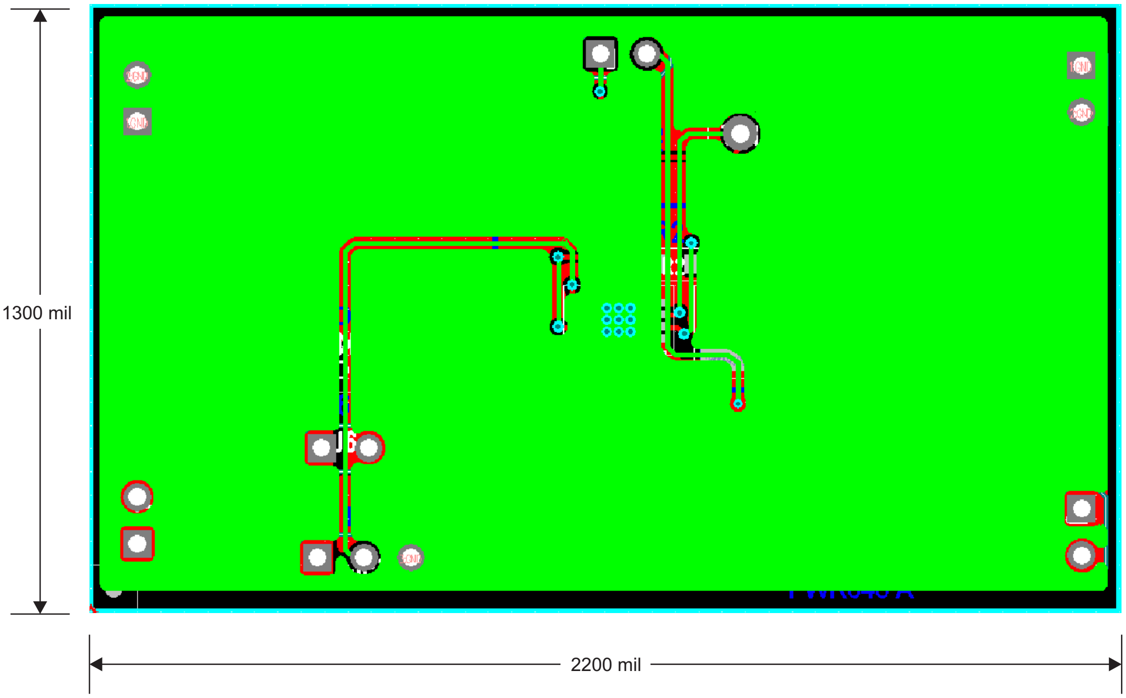


Figure 23. Suggested Layout: Bottom Layer

10.3 Power Dissipation

The ability to remove heat from the die is different for each package type, presenting different considerations in the PCB layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Using heavier copper increases the effectiveness of removing heat from the device. The addition of plated through-holes to heat dissipating layers also improves the heatsink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation (P_D) is equal to the product of the output current times the voltage drop across the output pass element, as shown in Equation 2:

$$P_D = (V_{IN} - V_{OUT})\ I_{OUT} \quad (2)$$

10.4 Thermal Considerations

Thermal protection disables the output when the junction temperature rises to approximately 170°C, allowing the device to cool. When the junction temperature cools to approximately 150°C, the output circuitry is enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heat-spreading area. For reliable operation, junction temperature should be limited to a maximum of 125°C at the worst case ambient temperature for a given application. To estimate the margin of safety in a complete design (including the copper heat-spreading area), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection should trigger at least 45°C above the maximum expected ambient condition of the particular application. This configuration produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS7A16xx-Q1 has been designed to protect against overload conditions. It was not intended to replace proper heatsinking. Continuously running the TPS7A16xx-Q1 into thermal shutdown degrades device reliability.

11 Device and Documentation Support

11.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 6. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS7A1601-Q1	Click here	Click here	Click here	Click here	Click here
TPS7A1633-Q1	Click here	Click here	Click here	Click here	Click here
TPS7A1650-Q1	Click here	Click here	Click here	Click here	Click here

11.2 Trademarks

PowerPAD, MSP430 are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated devices. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS7A1601QDGNRQ1	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PXZQ	Samples
TPS7A1633QDGNRQ1	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PXYQ	Samples
TPS7A1650QDGNRQ1	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PYAQ	Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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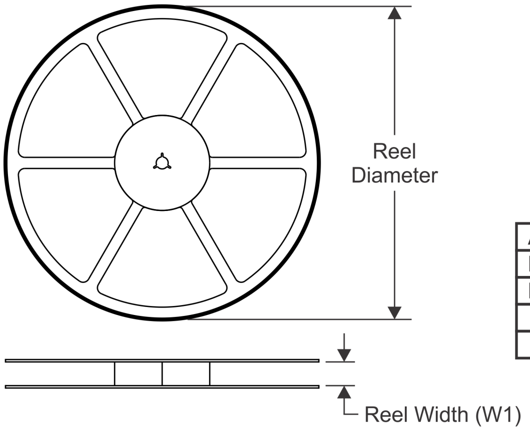
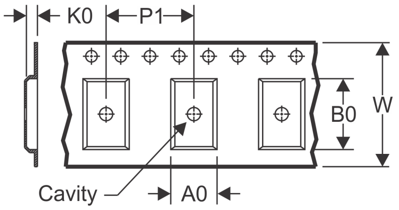
TAPE AND REEL INFORMATION

REEL DIMENSIONS

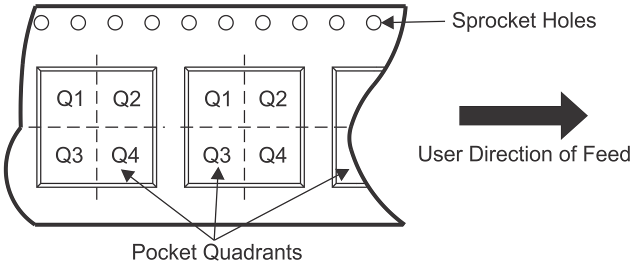


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

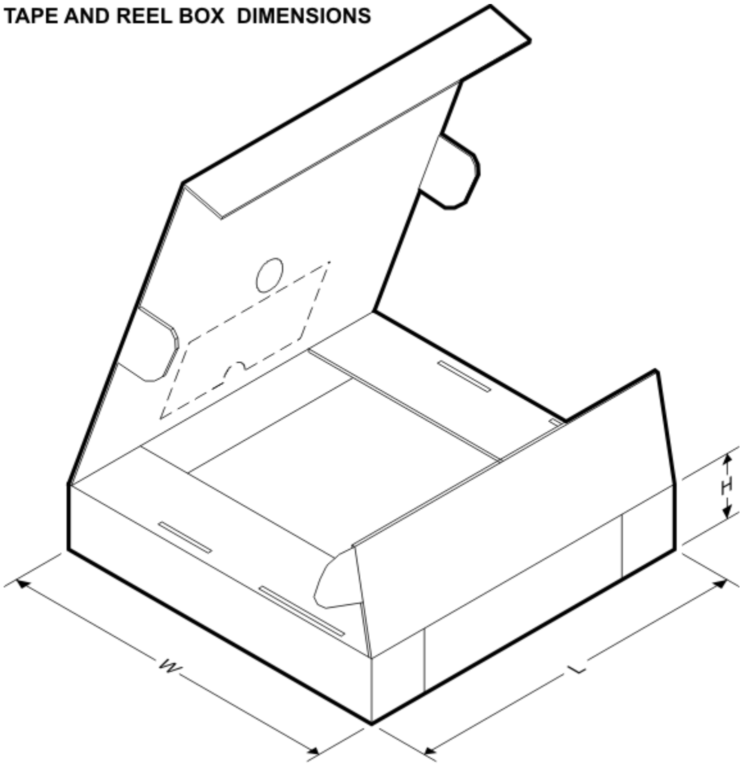
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7A1601QDGNRQ1	MSOP-PowerPAD	DGN	8	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
TPS7A1633QDGNRQ1	MSOP-PowerPAD	DGN	8	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
TPS7A1650QDGNRQ1	MSOP-PowerPAD	DGN	8	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1

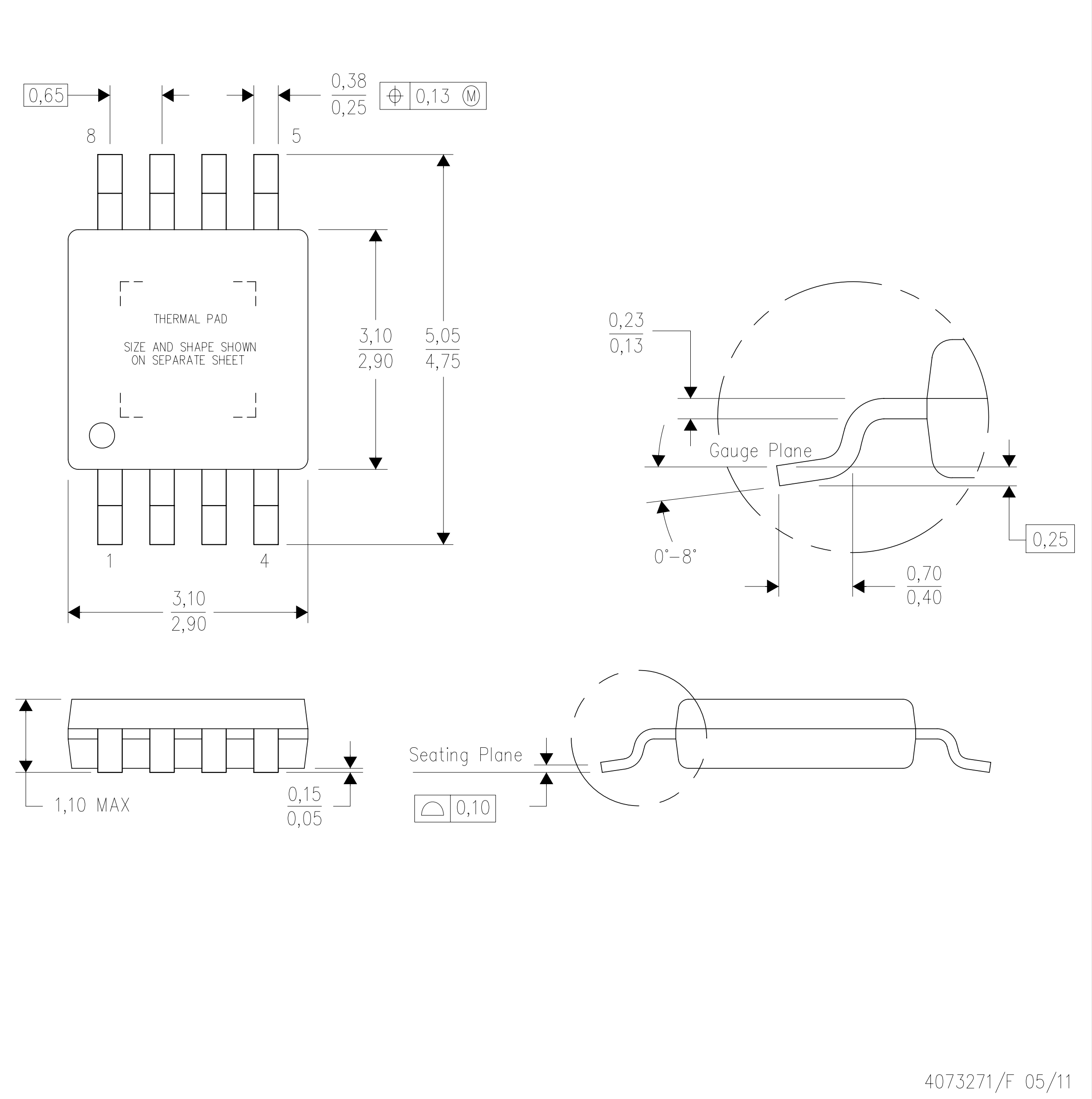
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7A1601QDGNRQ1	MSOP-PowerPAD	DGN	8	2500	370.0	355.0	55.0
TPS7A1633QDGNRQ1	MSOP-PowerPAD	DGN	8	2500	370.0	355.0	55.0
TPS7A1650QDGNRQ1	MSOP-PowerPAD	DGN	8	2500	370.0	355.0	55.0

DGN (S-PDSO-G8) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F. Falls within JEDEC MO-187 variation AA-T

PowerPAD is a trademark of Texas Instruments.

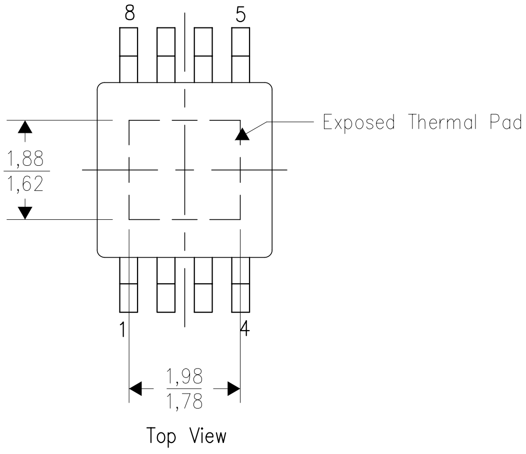
DGN (S-PDSO-G8) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



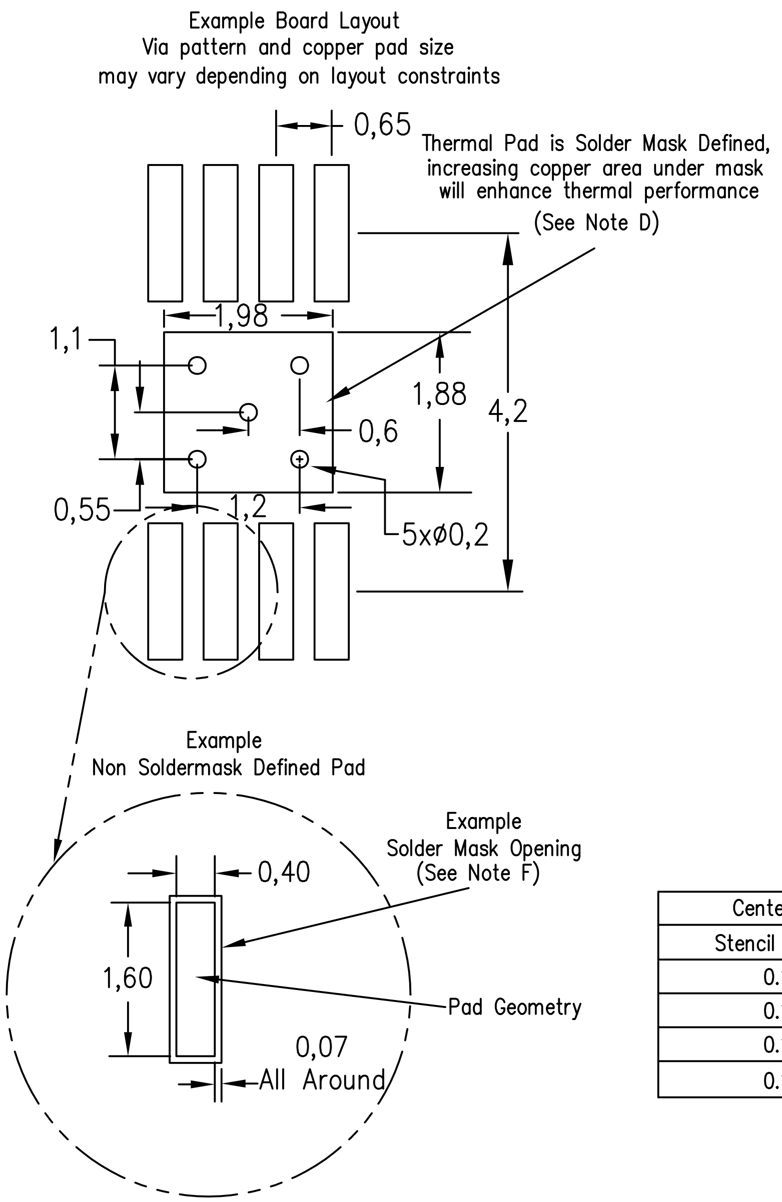
Exposed Thermal Pad Dimensions

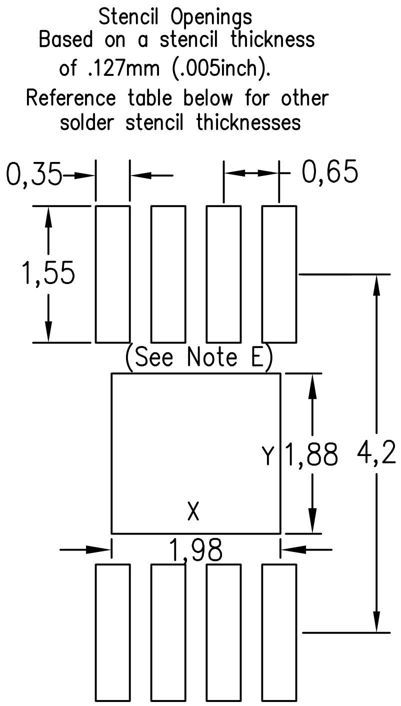
4206323-3/I 12/11

NOTE: All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

DGN (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE





Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	2.2	2.1
0.127mm	1.98	1.88
0.152mm	1.85	1.75
0.178mm	1.75	1.60

4207737–3/F 02/13

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
- F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

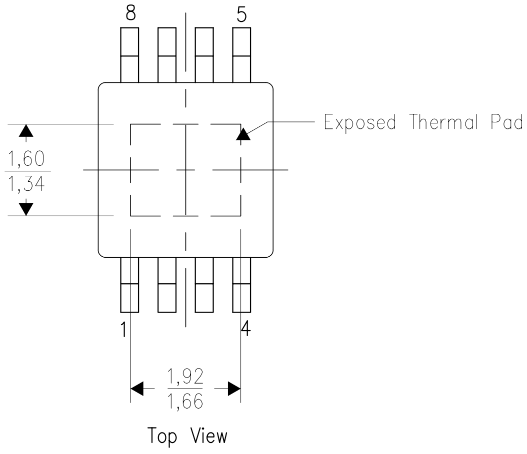
DGN (S-PDSO-G8) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Exposed Thermal Pad Dimensions

4206323-4/I 12/11

NOTE: All linear dimensions are in millimeters

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