

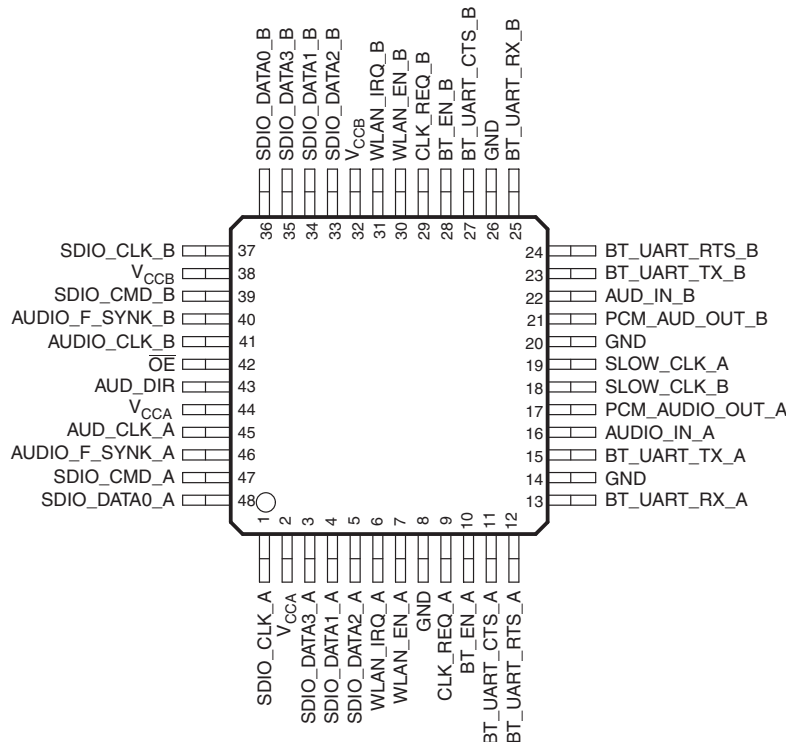
SDIO, UART, AND AUDIO VOLTAGE-TRANSLATION TRANSCEIVER

 Check for Samples: [TWL1200-Q1](#)

FEATURES

- Qualified for Automotive Applications
- AEC-Q100 Test Guidance With the Following Results:
 - Device Temperature Grade 3: –40°C to +85°C Ambient Operating Temperature Range
 - Device HBM ESD Classification Level H1C
 - Device CDM ESD Classification Level C3B
- Level Translator
 - V_{CCA} and V_{CCB} Range of 1.1 V to 3.6 V
- Seamlessly Bridges 1.8-V/2.6-V Digital-Switching Compatibility Gap Between 2.6-V processors and TI's Wi-Link (WL1271 and WL1273)
- Latch-Up Performance Exceeds 100 mA per JESD 78, Class II

**PFB PACKAGE
(TOP VIEW)**



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

DESCRIPTION

The TWL1200-Q1 is a 19-bit voltage translator specifically designed to bridge seamlessly the 1.8-V/2.6-V digital-switching compatibility gap between 2.6-V baseband and the TI Wi-Link-6 (WL1271/3). The device is optimized for SDIO, UART, and audio functions. The TWL1200-Q1 has two supply-voltage pins, V_{CCA} and V_{CCB} , that can be operated over the full range of 1.1 V to 3.6 V. The TWL1200-Q1 enables system designers easily to interface applications processors or digital basebands to peripherals operating at a different I/O voltage levels, such as the TI Wi-Link-6 (WL1271/3) or other SDIO/memory cards.

The TWL1200-Q1 is offered in a thin quad flat pack [TQFP (PFB)] package. Low static power consumption and small package size make the TWL1200-Q1 an ideal choice for mobile-phone applications.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION⁽¹⁾

| T_A | PACKAGE ⁽²⁾ | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---------------|------------------------|---------------|-----------------------|------------------|
| -40°C to 85°C | TQFP – PFB | Tape and reel | TWL1200IPFBRQ1 | TWL1200Q1 |

(1) For the most-current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

TERMINAL FUNCTIONS

| TERMINAL | | TYPE | DESCRIPTION |
|-----------------|---------------|------|---|
| NAME | NO. | | |
| AUD_CLK_A | 45 | I/O | Connected to baseband audio subsystem; drive strength = 4 mA |
| AUDIO_CLK_B | 41 | I/O | Connected to Wi-Link-6 PCM subsystem; drive strength = 4 mA |
| AUD_DIR | 43 | I | Direction control signal for AUDIO_CLK and AUDIO_F-SYNK signals |
| AUDIO_F_SYNK_A | 46 | I/O | Connected to baseband audio subsystem; drive strength = 4 mA |
| AUDIO_F_SYNK_B | 40 | I/O | Connected to Wi-Link-6 PCM subsystem; drive strength = 4 mA |
| AUDIO_IN_A | 16 | I | Connected to baseband audio subsystem |
| AUD_IN_B | 22 | O | Connected to Wi-Link-6 PCM subsystem; drive strength = 4 mA |
| BT_EN_A | 10 | I | Connected to baseband UART subsystem |
| BT_EN_B | 28 | O | Connected to BT UART subsystem of Wi-Link-6; drive strength = 2 mA |
| BT_UART_CTS_A | 11 | I | Connected to baseband UART subsystem |
| BT_UART_CTS_B | 27 | O | Connected to BT UART subsystem of Wi-Link-6; drive strength = 4 mA |
| BT_UART_RTS_A | 12 | O | Connected to baseband UART subsystem; drive strength = 4 mA |
| BT_UART_RTS_B | 24 | I | Connected to BT UART subsystem of Wi-Link-6 |
| BT_UART_RX_A | 13 | I | Connected to baseband UART subsystem |
| BT_UART_RX_B | 25 | O | Connected to BT UART subsystem of Wi-Link-6; drive strength = 8 mA |
| BT_UART_TX_A | 15 | O | Connected to baseband UART subsystem; drive strength = 8 mA |
| BT_UART_TX_B | 23 | I | Connected to BT UART subsystem of Wi-Link-6 |
| CLK_REQ_A | 9 | O | Connected to baseband SDIO controller; drive strength = 4 mA |
| CLK_REQ_B | 29 | I | Connected to SD/SDIO peripheral |
| GND | 8, 14, 20, 26 | | Ground |
| \overline{OE} | 42 | I | Output enable (active low) |
| PCM_AUDIO_OUT_A | 17 | O | Connected to baseband audio subsystem; drive strength = 4 mA |
| PCM_AUD_OUT_B | 21 | I | Connected to Wi-Link-6 PCM subsystem |
| SDIO_CLK_A | 1 | I | Clock signal connected to baseband SDIO controller. Referenced to V_{CCA} |
| SDIO_CLK_B | 37 | O | Clock signal connected to SD/SDIO peripheral. Referenced to V_{CCB} ; drive strength = 8 mA |

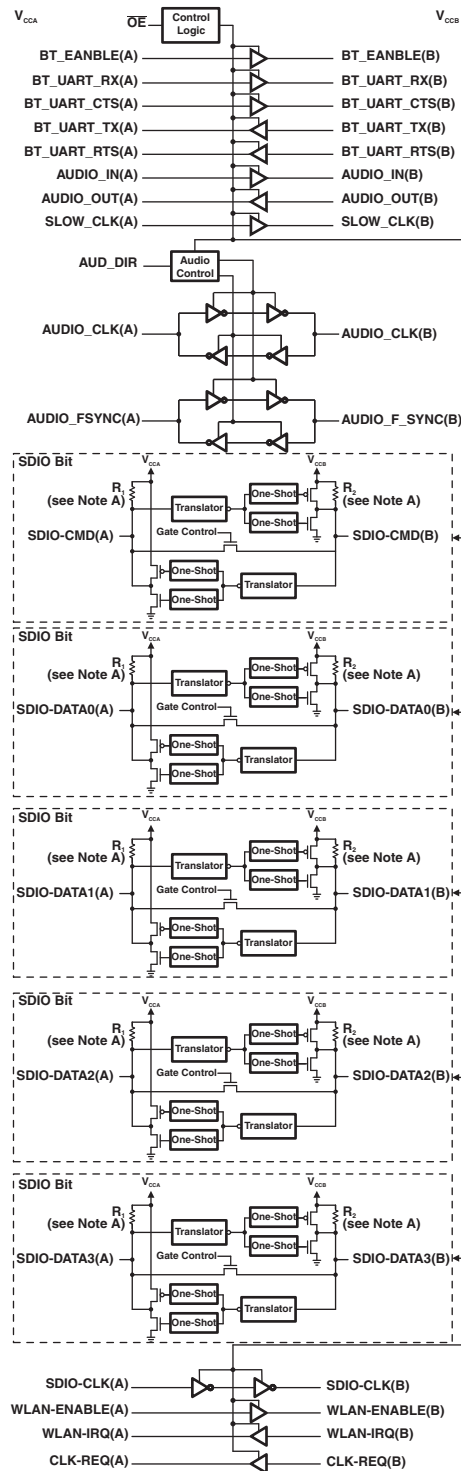
TERMINAL FUNCTIONS (continued)

| TERMINAL | | TYPE | DESCRIPTION |
|------------------|--------|------|---|
| NAME | NO. | | |
| SDIO_CMD_A | 47 | I/O | Command bit connected to baseband SDIO controller. Referenced to V _{CCA} . |
| SDIO_CMD_B | 39 | I/O | Command bit connected to SD/SDIO peripheral. Includes a 15-kΩ pullup resistor to V _{CCB} . |
| SDIO_DATA0_A | 48 | I/O | Data bit 1 connected to baseband SDIO controller |
| SDIO_DATA0_B | 36 | I/O | Data bit 0 connected to SD/SDIO peripheral |
| SDIO_DATA1_A | 4 | I/O | Data bit 1 connected to baseband SDIO controller |
| SDIO_DATA1_B | 34 | I/O | Data bit 1 connected to SD/SDIO peripheral |
| SDIO_DATA2_A | 5 | I/O | Data bit 2 connected to baseband SDIO controller |
| SDIO_DATA2_B | 33 | I/O | Data bit 2 connected to SD/SDIO peripheral |
| SDIO_DATA3_A | 3 | I/O | Data bit 3 connected to baseband SDIO controller |
| SDIO_DATA3_B | 35 | I/O | Data bit 3 connected to SD/SDIO peripheral |
| SLOW_CLK_A | 19 | I | Low frequency 32-kHz clock connected to baseband device |
| SLOW_CLK_B | 18 | O | Low frequency 32-kHz clock connected to Wi-Link-6 device; drive strength = 2 mA |
| V _{CCA} | 2, 44 | Pwr | A-side supply voltage (1.1 V to 3.6 V) |
| V _{CCB} | 32, 38 | Pwr | B-side supply voltage (1.1 V to 3.6 V) |
| WLAN_EN_A | 7 | I | Connected to baseband SDIO controller |
| WLAN_EN_B | 30 | O | Connected to SD/SDIO peripheral; drive strength = 2 mA |
| WLAN_IRQ_A | 6 | O | Connected to baseband SDIO controller; drive strength = 4 mA |
| WLAN_IRQ_B | 31 | I | Connected to SD/SDIO peripheral |

Table 1. FUNCTION TABLE

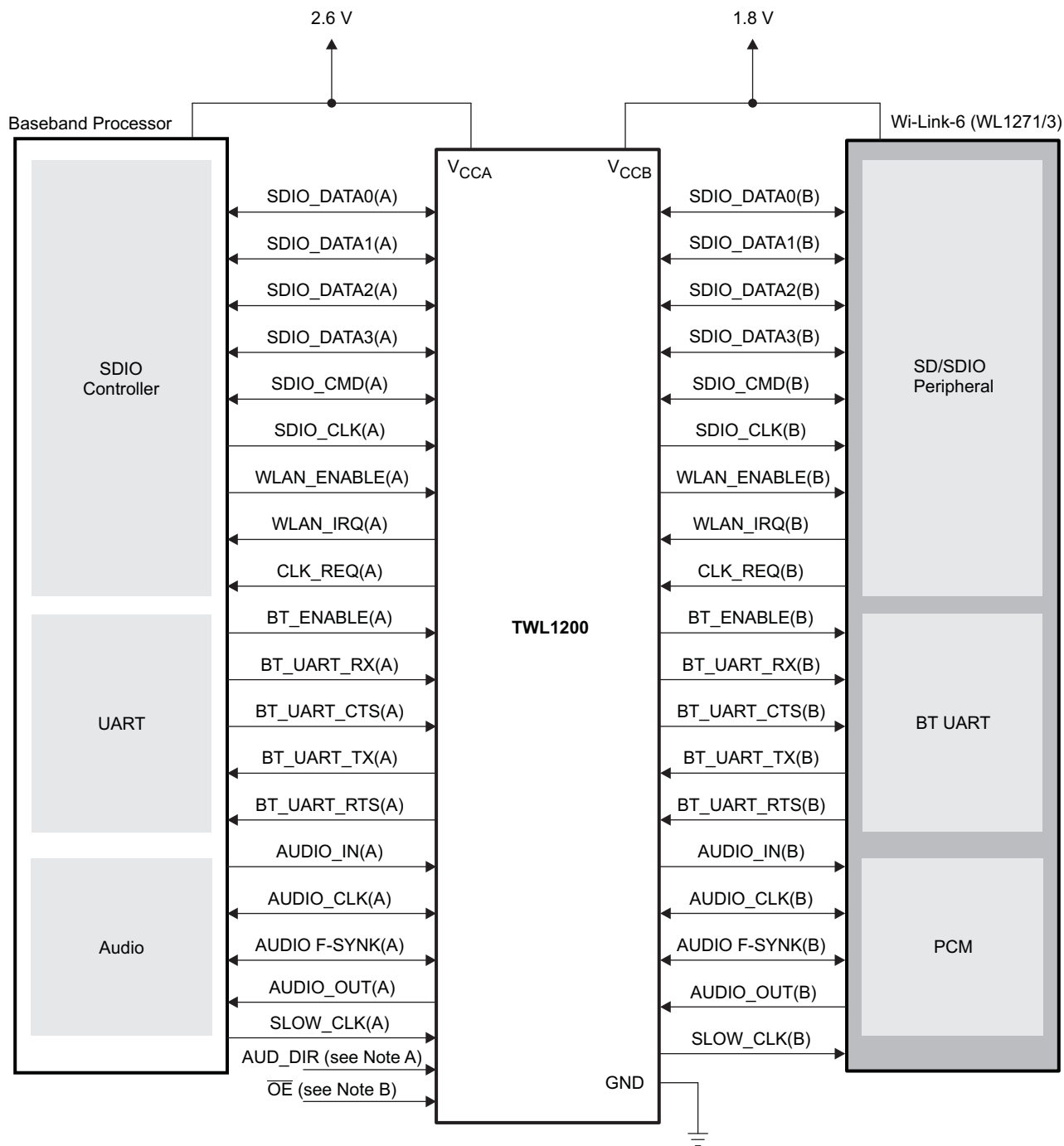
| CONTROL INPUTS | | OPERATION |
|----------------|---------|--|
| OE | AUD_DIR | |
| H | X | All outputs are Hi-Z |
| L | H | AUDIO_CLK_A to AUDIO_CLK_B and AUDIO_F-SYNC_A_ to AUDIO_F-SYNC_B |
| L | L | AUDIO_CLK_B to AUDIO_CLK_A and AUDIO_F-SYNC_B to AUDIO_F-SYNC_A |

LOGIC DIAGRAM



- A. R_1 and R_2 resistor values are determined based upon the logic level applied to the A port or B port as follows:
 R_1 and $R_2 = 25\text{ k}\Omega$ when a logic-level low is applied to the A port or B port.
 R_1 and $R_2 = 4\text{ k}\Omega$ when a logic-level high is applied to the A port or B port.
 R_1 and $R_2 = 70\text{ k}\Omega$ when the port is deselected (or in Hi-Z state).
- B. \overline{OE} controls all output buffers. When $\overline{OE} = \text{high}$, all outputs are Hi-Z.

TYPICAL APPLICATION BLOCK DIAGRAM



- A. AUD_DIR must be biased to determine audio direction (see Function Table for properly establishing the bias).
- B. OE is an active-low pin that must be grounded to 0 V to enable operation of the TWL1200-Q1 device.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT | |
|------------------|---|--------------------|------|------|---|
| V _{CCA} | Supply voltage range | -0.5 | 4.6 | V | |
| V _{CCB} | Supply voltage range | -0.5 | 4.6 | V | |
| V _I | Input voltage range | I/O ports (A port) | -0.5 | 4.6 | V |
| | | I/O ports (B port) | -0.5 | 4.6 | |
| | | Control inputs | -0.5 | 4.6 | |
| V _O | Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾ | A port | -0.5 | 4.6 | V |
| | | B port | -0.5 | 4.6 | |
| V _O | Voltage range applied to any output in the high or low state ⁽²⁾ | A port | -0.5 | 4.6 | V |
| | | B port | -0.5 | 4.6 | |
| I _{IK} | Input clamp current | V _I < 0 | -50 | mA | |
| I _{OK} | Output clamp current | V _O < 0 | -50 | mA | |
| I _O | Continuous output current | | ±50 | mA | |
| | Continuous current through V _{CCA} , V _{CCB} , or GND | | ±100 | mA | |
| T _{stg} | Storage temperature range | -65 | 150 | °C | |
| ESD rating | Human-body model (HBM) AEC-Q100 Classification Level H1C | | 1.5 | kV | |
| | Charged-device model (CDM) AEC-Q100 Classification Level C3B | | 750 | V | |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

THERMAL INFORMATION

| THERMAL METRIC ⁽¹⁾ | | TWL1200-Q1 | |
|-------------------------------|---|------------|------|
| | | PFB | UNIT |
| | | 48 PINS | |
| θ _{JA} | Junction-to-ambient thermal resistance ⁽²⁾ | 70.1 | °C/W |
| θ _{JCtop} | Junction-to-case (top) thermal resistance ⁽³⁾ | 20.8 | °C/W |
| θ _{JB} | Junction-to-board thermal resistance ⁽⁴⁾ | 32.8 | °C/W |
| ψ _{JT} | Junction-to-top characterization parameter ⁽⁵⁾ | 0.6 | °C/W |
| ψ _{JB} | Junction-to-board characterization parameter ⁽⁶⁾ | 32.6 | °C/W |
| θ _{JCbot} | Junction-to-case (bottom) thermal resistance ⁽⁷⁾ | N/A | °C/W |

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).
- (2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
- (3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
- (4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
- (5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
- (6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
- (7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

RECOMMENDED OPERATING CONDITIONS⁽¹⁾

| | | | V_{CCI} | V_{CCO} | MIN | MAX | UNIT |
|---------------------|------------------------------------|-------------------------------|----------------|------------------|-----------------------|-----------------------|------|
| V_{CCA} | Supply voltage | | | | 1.1 | 3.6 | V |
| V_{CCB} | Supply voltage | | | | 1.1 | 3.6 | V |
| V_{IH} | High-level input voltage | Buffer type | 1.1 V to 3.6 V | 1.1 V to 3.6 V | $V_{CCI} \times 0.65$ | 3.6 | V |
| | | \overline{OE} and AUD_DIR | | | $V_{CCA} \times 0.65$ | 3.6 | |
| V_{IH} | High-level input voltage | Switch type | 1.1 V to 3.6 V | 1.1 V to 3.6 V | $V_{CCI} - 0.2$ | V_{CCI} | V |
| V_{IL} | Low-level input voltage | Buffer type and Control Logic | 1.1 V to 3.6 V | 1.1 V to 3.6 V | 0 | $V_{CCI} \times 0.35$ | V |
| | | \overline{OE} and AUD_DIR | | | 0 | $V_{CCA} \times 0.35$ | |
| $V_{IL}^{(2)}$ | Low-level input voltage | Switch type | 1.1 V to 3.6 V | 1.1 V to 3.6 V | 0 | 0.15 | V |
| V_I | Input voltage | | | | 0 | 3.6 | V |
| V_O | Output voltage | Active state | | | 0 | V_{CCO} | V |
| | | High-impedance state | | | 0 | 3.6 | |
| I_{OH} | High-level output current | | | 1.1 V to 1.3 V | | -0.5 | mA |
| | | | | 1.4 V to 1.6 V | | -1 | |
| | | | | 1.65 V to 1.95 V | | -2 | |
| | | | | 2.3 V to 2.7 V | | -4 | |
| | | | | 3 V to 3.6 V | | -8 | |
| I_{OL} | Low-level output current | | | 1.1 V to 1.3 V | | 0.5 | mA |
| | | | | 1.4 V to 1.6 V | | 1 | |
| | | | | 1.65 V to 1.95 V | | 2 | |
| | | | | 2.3 V to 2.7 V | | 4 | |
| | | | | 3 V to 3.6 V | | 8 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | | | | 5 | ns/V |
| T_A | Operating free-air temperature | | | | -40 | 85 | °C |

- (1) All unused data inputs of the device must be held at V_{CCI} or GND to ensure proper device operation. See the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
- (2) Note, the max V_{IL} value is provided to ensure that a valid V_{OL} is maintained. The V_{OL} value is the V_{IL} + the voltage-drop across the pass-gate transistor.

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CCA} | V _{CCB} | MIN | TYP ⁽¹⁾ | MAX | UNIT | |
|------------------|---|---|--|------------------|------------------------|------------------------|------|------|------|
| V _{OH} | A port (Buffer-type output, 8-mA drive) | I _{OH} = -100 µA | 1.1 V to 3.6 V | 1.1 V to 3.6 V | V _{CC0} - 0.2 | | | V | |
| | | I _{OH} = -8 mA | 1.65 V | 1.65 V | 1.2 | | | | |
| | | | 2.5 V | 2.5 V | 1.97 | | | | |
| | A port (Buffer-type output, 4-mA drive) | I _{OH} = -100 µA | 1.1 V to 3.6 V | 1.1 V to 3.6 V | V _{CC0} - 0.2 | | | | |
| | | I _{OH} = -4 mA | 1.65 V | 1.65 V | 1.2 | | | | |
| | | | 2.5 V | 2.5 V | 1.97 | | | | |
| V _{OH} | A port (Switch-type outputs) | I _{OH} = -20 µA | 1.65 V | 1.65 V | 1.5 | | | V | |
| | | | 2.5 V | 2.5 V | 2.3 | | | | |
| V _{OL} | A port (Buffer-type output, 8-mA drive) | I _{OL} = 100 µA | 1.1 V to 3.6 V | 1.1 V to 3.6 V | | | 0.2 | V | |
| | | I _{OL} = 8 mA | 1.65 V | 1.65 V | | | 0.45 | | |
| | | | 2.5 V | 2.5 V | | | 0.55 | | |
| | A port (Buffer-type output, 4-mA drive) | I _{OL} = 100 µA | 1.1 V to 3.6 V | 1.1 V to 3.6 V | | | 0.2 | | |
| | | I _{OL} = 4 mA | 1.65 V | 1.65 V | | | 0.45 | | |
| | | | 2.5 V | 2.5 V | | | 0.55 | | |
| V _{OL} | A port (Switch-type outputs) | I _{OL} = 220 µA, V _{IN} = 0.15 V | 1.65 V | 1.65 V | | | 0.45 | V | |
| | | I _{OL} = 300 µA, V _{IN} = 0.15 V | 2.5 V | 2.5 V | | | 0.55 | | |
| V _{OH} | B port (Buffer-type output, 8-mA drive) | I _{OH} = -100 µA | 1.1 V to 3.6 V | 1.1 V to 3.6 V | V _{CC0} - 0.2 | | | V | |
| | | | I _{OH} = -8 mA | 1.65 V | 1.65 V | 1.2 | | | |
| | | | | 2.5 V | 2.5 V | 1.97 | | | |
| | B port (Buffer-type output, 4-mA drive) | I _{OH} = -100 µA | I _{OH} = -4 mA | 1.1 V to 3.6 V | 1.1 V to 3.6 V | V _{CC0} - 0.2 | | | |
| | | | | 1.65 V | 1.65 V | 1.2 | | | |
| | | | | 2.5 V | 2.5 V | 1.97 | | | |
| | B port (Buffer-type output, 2-mA drive) | I _{OH} = -100 µA | I _{OH} = -2 mA | 1.1 V to 3.6 V | 1.1 V to 3.6 V | V _{CC0} - 0.2 | | | |
| | | | | 1.65 V | 1.65 V | 1.2 | | | |
| | | | | 2.5 V | 2.5 V | 1.97 | | | |
| | B port (Switch-type outputs) | I _{OH} = -20 µA | | 1.65 V | 1.65 V | 1.5 | | | |
| | | | | 2.5 V | 2.5 V | 2.3 | | | |
| | | | | | | | | | |
| V _{OL} | B port (Buffer-type output, 8-mA drive) | I _{OL} = 100 µA | 1.1 V to 3.6 V | 1.1 V to 3.6 V | | | 0.2 | V | |
| | | | I _{OL} = 8 mA | 1.65 V | 1.65 V | | | | 0.45 |
| | | | | 2.5 V | 2.5 V | | | | 0.55 |
| | B port (Buffer-type output, 4-mA drive) | I _{OL} = 100 µA | I _{OL} = 4 mA | 1.1 V to 3.6 V | 1.1 V to 3.6 V | | | | 0.2 |
| | | | | 1.65 V | 1.65 V | | | | 0.45 |
| | | | | 2.5 V | 2.5 V | | | | 0.55 |
| | B port (Buffer-type output, 2-mA drive) | I _{OL} = 100 µA | I _{OL} = 2 mA | 1.1 V to 3.6 V | 1.1 V to 3.6 V | | | | 0.2 |
| | | | | 1.65 V | 1.65 V | | | | 0.45 |
| | | | | 2.5 V | 2.5 V | | | | 0.55 |
| | B port (Switch-type outputs) | I _{OL} = 220 µA, V _{IN} = 0.15 V | I _{OL} = 300 µA, V _{IN} = 0.15 V | 1.65 V | 1.65 V | | | | 0.45 |
| | | | | 2.5 V | 2.5 V | | | | 0.55 |
| | I _I | | V _I = V _{CCA} or GND | 1.1 V to 3.6 V | 1.1 V to 3.6 V | | | | ±1 |
| I _{CCA} | | Switch-type I/O are open and all other inputs are biased at either V _{CC} or GND | 1.1 V to 3.6 V | 1.1 V to 3.6 V | | | 15 | µA | |
| | | | 3.6 V | 0 V | | | 14 | | |
| | | | 0 V | 3.6 V | | | -12 | | |

(1) All typical values are at T_A = 25°C.

ELECTRICAL CHARACTERISTICS (continued)

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CCA} | V _{CCB} | MIN | TYP ⁽¹⁾ | MAX | UNIT |
|-------------------------------------|---------------------------|---|------------------|------------------|-----|--------------------|-----|------|
| I _{CCB} | | Switch-type I/O are open and all other inputs are biased at either V _{CC} or GND | 1.1 V to 3.6 V | 1.1 V to 3.6 V | | | 15 | μA |
| | | | 3.6 V | 0 V | | | -12 | |
| | | | 0 V | 3.6 V | | | 14 | |
| I _{CCA} + I _{CCB} | | V _I = V _{CC1} or GND, I _O = 0 | 1.1 V to 3.6 V | 1.1 V to 3.6 V | | | 30 | μA |
| C _{io} ⁽²⁾ | Auto-Dir (SDIO lines) | V _I = V _{CC1} | | | | | 5.5 | pF |
| | Bi-Dir buffer | V _I = V _{CCX} or GND | | | | | 4.5 | |
| C _i ⁽²⁾ | AUD_DIR / \overline{OE} | V _I = V _{CCA} or GND | | | | | 4 | pF |
| | Buffer | V _I = V _{CCX} or GND | | | | | 4 | |
| C _o ⁽²⁾ | 2-mA buffer | V _I = V _{CCX} or GND | | | | | 5 | pF |
| | 4-mA buffer | V _I = V _{CCX} or GND | | | | | 5 | |
| | 8-mA buffer | V _I = V _{CCX} or GND | | | | | 6 | |

(2) Not production tested

OUTPUT DRIVE STRENGTH

| 2 mA | 4 mA | 8 mA |
|------------|----------------|--------------|
| WLAN_EN_B | AUDIO_OUT_A | SDIO_CLK_B |
| SLOW_CLK_B | WLAN_IRQ_A | BT_UART_TX_A |
| BT_EN_B | CLK_REQ_A | BT_UART_RX_B |
| | AUDIO_IN_B | |
| | AUDIO_CLK_A | |
| | BT_UART_CTS_B | |
| | BT_UART_RTS_A | |
| | AUDIO_F-SYNC_A | |

TIMING REQUIREMENTS⁽¹⁾

$V_{CCA} = 2.5\text{ V} \pm 0.2\text{ V}$

over recommended operating free-air temperature range (unless otherwise noted)

| | | | $V_{CCB} = 1.8\text{ V} \pm 0.15\text{ V}$ | | UNIT |
|----------------------|------------|--------------------|--|-----|---------------|
| | | | MIN | MAX | |
| Data rate | SDIO_CMD | Push-pull driving | 60 | | Mbps |
| | | Open-drain driving | 1 | | |
| | SDIO_CLK | Push-pull driving | 50 | | MHz |
| | SDIO_DATAx | | 60 | | Mbps |
| t_w Pulse duration | SDIO_CMD | Push-pull driving | 17 | | ns |
| | | Open-drain driving | 1 | | μs |
| | SDIO_CLK | Push-pull driving | 10 | | ns |
| | SDIO_DATAx | | 17 | | ns |

(1) Not production tested

TIMING REQUIREMENTS⁽¹⁾

$V_{CCA} = 3.3\text{ V} \pm 0.3\text{ V}$

over recommended operating free-air temperature range (unless otherwise noted)

| | | | $V_{CCB} = 1.8\text{ V} \pm 0.15\text{ V}$ | | UNIT |
|----------------------|------------|--------------------|--|-----|---------------|
| | | | MIN | MAX | |
| Data rate | SDIO_CMD | Push-pull driving | 60 | | Mbps |
| | | Open-drain driving | 1 | | |
| | SDIO_CLK | Push-pull driving | 50 | | MHz |
| | SDIO_DATAx | | 60 | | Mbps |
| t_w Pulse duration | SDIO_CMD | Push-pull driving | 17 | | ns |
| | | Open-drain driving | 1 | | μs |
| | SDIO_CLK | Push-pull driving | 10 | | ns |
| | SDIO_DATAx | | 17 | | ns |

(1) Not production tested

SWITCHING CHARACTERISTICS⁽¹⁾

$V_{CCA} = 2.5 \text{ V} \pm 0.2 \text{ V}$

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | $V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$ | | UNIT |
|---------------|----------------------------|----------------------------|-----------------------------|--|------|---------------|
| | | | | MIN | MAX | |
| t_{pd} | SDIO_CMD_A | SDIO_CMD_B | Push-pull driving | | 7 | ns |
| | | | Open-drain driving (H-to-L) | 1.1 | 7 | |
| | | | Open-drain driving (L-to-H) | 30 | 510 | |
| | SDIO_CMD_B | SDIO_CMD_A | Push-pull driving | | 7 | |
| | | | Open-drain driving (H-to-L) | 1 | 7.5 | |
| | | | Open-drain driving (L-to-H) | 30 | 515 | |
| | SDIO_CLK_A | SDIO_CLK_B | Push-pull driving | 1 | 6.5 | |
| | SDIO_DATAx_A | SDIO_DATAx_B | Push-pull driving | 1 | 7 | |
| | SDIO_DATAx_B | SDIO_DATAx_A | | 1 | 7 | |
| | | Buffered input | 2-mA drive strength output | Push-pull driving | 1 | |
| | Buffered input | 4-mA drive strength output | Push-pull driving | 1 | 7 | |
| | Buffered input | 8-mA drive strength output | Push-pull driving | 1 | 6.5 | |
| t_{en} | OE | 2-mA drive strength output | Push-pull driving | | 16 | ns |
| | | 4-mA drive strength output | Push-pull driving | | 19 | |
| | | 8-mA drive strength output | Push-pull driving | | 18 | |
| | | Switch-type output | Push-pull driving | | 1 | μs |
| t_{dis} | OE | 2-mA drive strength output | Push-pull driving | | 17 | ns |
| | | 4-mA drive strength output | Push-pull driving | | 16.5 | |
| | | 8-mA drive strength output | Push-pull driving | | 16 | |
| | | Switch-type outputs | Push-pull driving | | 1 | μs |
| t_{rA} | SDIO_CMD_A rise time | | Push-pull driving | 1 | 5 | ns |
| | | | Open-drain driving | 15 | 420 | |
| | | SDIO_DATAx_A rise time | | Push-pull driving | 1 | 4.7 |
| t_{rB} | SDIO_CMD_B rise time | | Push-pull driving | 1 | 9.7 | ns |
| | | | Open-drain driving | 15 | 420 | |
| | SDIO_CLK_B rise time | | Push-pull driving | 0.5 | 6 | |
| | | SDIO_DATAx_B rise time | | 1 | 9.7 | |
| t_{fA} | SDIO_CMD_A fall time | | Push-pull driving | 0.7 | 8.3 | ns |
| | | | Open-drain driving | 1.6 | 8.3 | |
| | | SDIO_DATAx_A fall time | | 1 | 8.3 | |
| t_{fB} | SDIO_CMD_B fall time | | Push-pull driving | 1 | 9.9 | ns |
| | | | Open-drain driving | 1.6 | 10.9 | |
| | SDIO_CLK_B fall time | | Push-pull driving | 0.5 | 5.3 | |
| | | SDIO_DATAx_B fall time | | 1 | 9.9 | |
| $t_{sk(O)}$ | SDIO Ch-A to Ch-B skew | | Push-pull driving | | 0.4 | ns |
| | SDIO Ch-B to Ch-A skew | | Push-pull driving | | 0.4 | |
| | SDIO channel-to-clock skew | | Push-pull driving | | 1.3 | |
| Max data rate | SDIO_CMD | | Push-pull driving | | 60 | Mbps |
| | | | Open-drain driving | | 1 | |
| | SDIO_CLK | | | | 50 | MHz |
| SDIO_DATAx | | Push-pull driving | | 60 | Mbps | |

(1) Not production tested

SWITCHING CHARACTERISTICS⁽¹⁾

V_{CCA} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | V _{CCB} = 1.8 V ± 0.15 V | | UNIT |
|--------------------|----------------------------|----------------------------|-----------------------------|-----------------------------------|------|------|
| | | | | MIN | MAX | |
| t _{pd} | SDIO_CMD_A | SDIO_CMD_B | Push-pull driving | | 7 | ns |
| | | | Open-drain driving (H-to-L) | 1.1 | 7 | |
| | | | Open-drain driving (L-to-H) | 30 | 510 | |
| | SDIO_CMD_B | SDIO_CMD_A | Push-pull driving | | 7 | |
| | | | Open-drain driving (H-to-L) | 1 | 7.5 | |
| | | | Open-drain driving (L-to-H) | 30 | 515 | |
| | SDIO_CLK_A | SDIO_CLK_B | Push-pull driving | 1 | 6.5 | |
| | SDIO_DATAx_A | SDIO_DATAx_B | Push-pull driving | 1 | 7 | |
| | SDIO_DATAx_B | SDIO_DATAx_A | | 1 | 7 | |
| | | Buffered input | 2-mA drive strength output | Push-pull driving | 1 | |
| | Buffered input | 4-mA drive strength output | Push-pull driving | 1 | 7 | |
| | Buffered -nput | 8-mA drive strength output | Push-pull driving | 1 | 6.5 | |
| t _{en} | OE | 2-mA drive strength output | Push-pull driving | | 16 | ns |
| | | 4-mA drive strength output | Push-pull driving | | 19 | |
| | | 8-mA drive strength output | Push-pull driving | | 19 | |
| | | Switch-type output | Push-pull driving | | 1 | µs |
| t _{dis} | OE | 2-mA drive strength output | Push-pull driving | | 17 | ns |
| | | 4-mA drive strength output | Push-pull driving | | 16 | |
| | | 8-mA drive strength output | Push-pull driving | | 16 | |
| | | Switch-type output | Push-pull driving | | 1 | µs |
| t _{rA} | SDIO_CMD_A rise time | | Push-pull driving | 1 | 4.25 | ns |
| | | | Open-drain driving | 15 | 420 | |
| | | SDIO_DATAx_A rise time | | Push-pull driving | 1 | 4.25 |
| t _{rB} | SDIO_CMD_B rise time | | Push-pull driving | 1 | 9.5 | ns |
| | | | Open-drain driving | 15 | 420 | |
| | SDIO_CLK_B rise time | | Push-pull driving | 0.5 | 5.9 | |
| | | SDIO_DATAx_B rise time | | Push-pull driving | 1 | 9.6 |
| t _{fA} | SDIO_CMD_A fall time | | Push-pull driving | 0.7 | 8.2 | ns |
| | | | Open-drain driving | 1.6 | 8.2 | |
| | | SDIO_DATAx_A fall time | | Push-pull driving | 1 | 8.2 |
| t _{fB} | SDIO_CMD_B fall time | | Push-pull driving | 1 | 9.2 | ns |
| | | | Open-drain driving | 1.6 | 10.8 | |
| | SDIO_CLK_B fall time | | Push-pull driving | 0.5 | 5.2 | |
| | | SDIO_DATAx_B fall time | | Push-pull driving | 1 | 9.8 |
| t _{sk(O)} | SDIO Ch-A to Ch-B skew | | Push-pull driving | | 0.4 | ns |
| | SDIO Ch-B to Ch-A skew | | Push-pull driving | | 0.4 | |
| | SDIO Channel-to-Clock skew | | Push-pull driving | | 1.3 | |
| Max data rate | SDIO_CMD | | Push-pull driving | | 60 | Mbps |
| | | | Open-drain driving | | 1 | |
| | SDIO_CLK | | | | 50 | MHz |
| | SDIO_DATAx | | Push-pull driving | | 60 | Mbps |

(1) Not production tested

OPERATING CHARACTERISTICS⁽¹⁾
 $T_A = 25^\circ\text{C}$

| PARAMETER | | | TEST CONDITIONS | $V_{CCA} = V_{CCB} = 1.8\text{ V}$ | $V_{CCA} = V_{CCB} = 2.5\text{ V}$ | UNIT |
|---------------|----------|-----------------------------|---|------------------------------------|------------------------------------|------|
| DATAx and CMD | Enabled | C _{pd} input side | $C_L = 0,$ $f = 10\text{ MHz},$ $t_r = t_f = 1\text{ ns}$ | 18.3 | 20.3 | pF |
| | | C _{pd} output side | | 18.25 | 19.52 | |
| | Disabled | C _{pd} input side | | 0.8 | 0.8 | |
| | | C _{pd} output side | | 0.1 | 0.1 | |
| Clock | Enabled | C _{pd} input side | $C_L = 0,$ $f = 10\text{ MHz},$ $t_r = t_f = 1\text{ ns}$ | 0.6 | 0.9 | pF |
| | | C _{pd} output side | | 8.8 | 10.1 | |
| | Disabled | C _{pd} input side | | 0.1 | 0.1 | |
| | | C _{pd} output side | | 0.1 | 0.1 | |
| 2-mA buffer | Enabled | C _{pd} input side | $C_L = 0,$ $f = 10\text{ MHz},$ $t_r = t_f = 1\text{ ns}$ | 0.6 | 1 | pF |
| | | C _{pd} output side | | 7.1 | 7.9 | |
| | Disabled | C _{pd} input side | | 0.1 | 0.1 | |
| | | C _{pd} output side | | 0.1 | 0.1 | |
| 4-mA buffer | Enabled | C _{pd} input side | $C_L = 0,$ $f = 10\text{ MHz},$ $t_r = t_f = 1\text{ ns}$ | 0.6 | 1.0 | pF |
| | | C _{pd} output side | | 7.6 | 8.6 | |
| | Disabled | C _{pd} input side | | 0.1 | 0.1 | |
| | | C _{pd} output side | | 0.1 | 0.1 | |
| 8-mA buffer | Enabled | C _{pd} input side | $C_L = 0,$ $f = 10\text{ MHz},$ $t_r = t_f = 1\text{ ns}$ | 0.6 | 1 | pF |
| | | C _{pd} output side | | 8.8 | 10.1 | |
| | Disabled | C _{pd} input side | | 0.1 | 0.1 | |
| | | C _{pd} output side | | 0.1 | 0.1 | |
| 4-mA I/O | Enabled | C _{pd} input side | $C_L = 0,$ $f = 10\text{ MHz},$ $t_r = t_f = 1\text{ ns}$ | 0.6 | 0.95 | pF |
| | | C _{pd} output side | | 8.2 | 9.1 | |
| | Disabled | C _{pd} input side | | 0.1 | 0.1 | |
| | | C _{pd} output side | | 0.1 | 0.1 | |

(1) Not production tested

TYPICAL CHARACTERISTICS

**LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT**

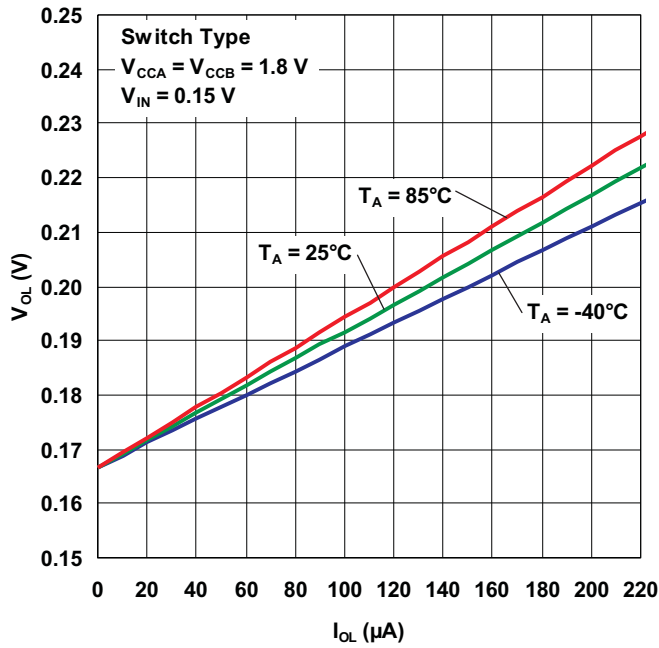


Figure 1.

**LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT**

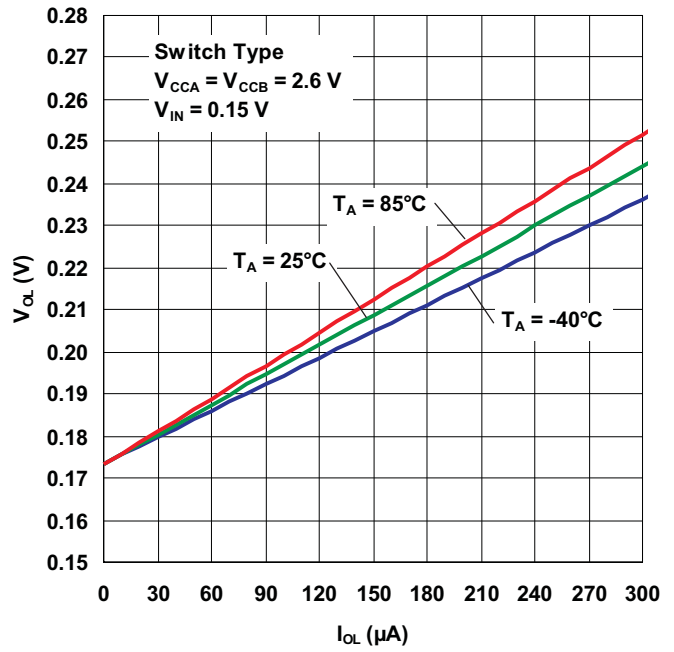


Figure 2.

**LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT**

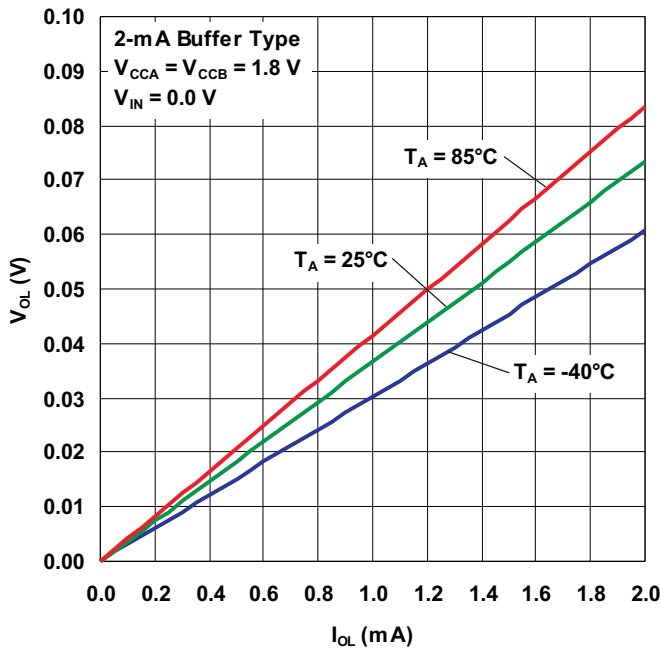


Figure 3.

**LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT**

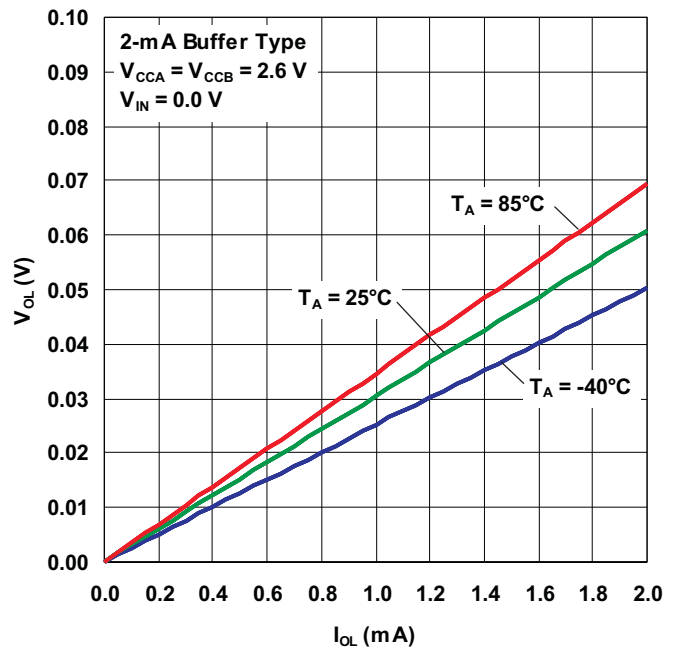


Figure 4.

TYPICAL CHARACTERISTICS (continued)

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

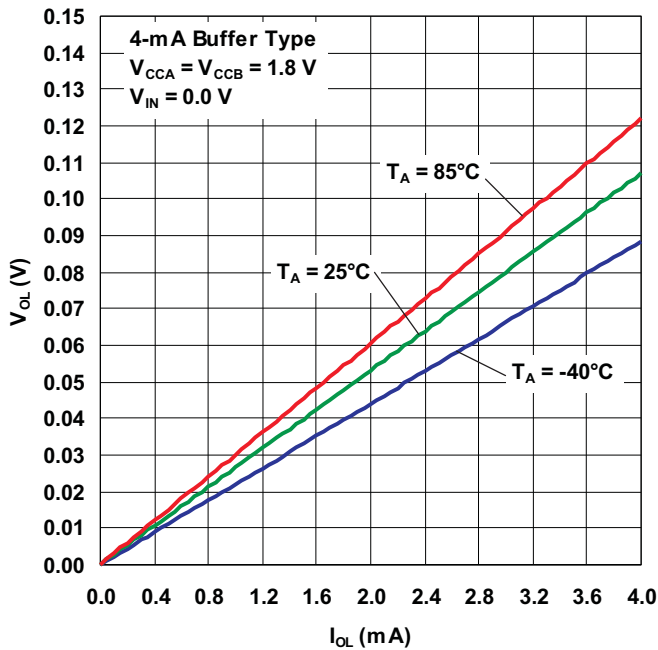


Figure 5.

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

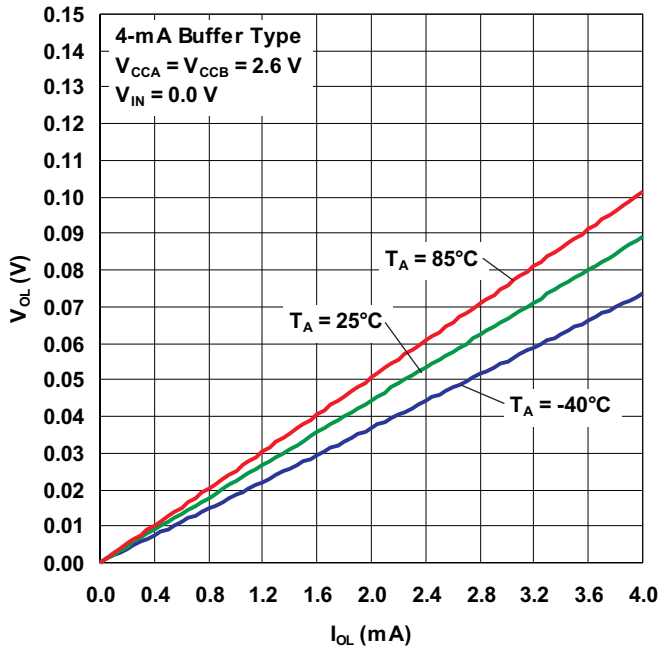


Figure 6.

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

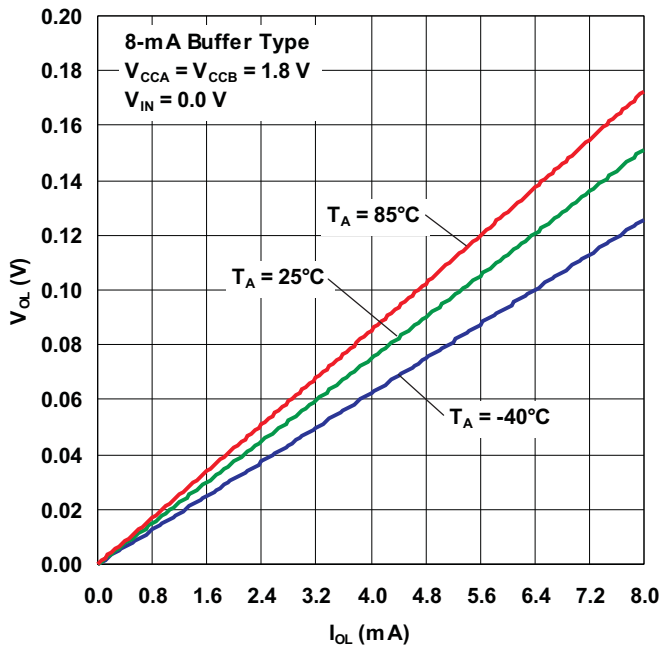


Figure 7.

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

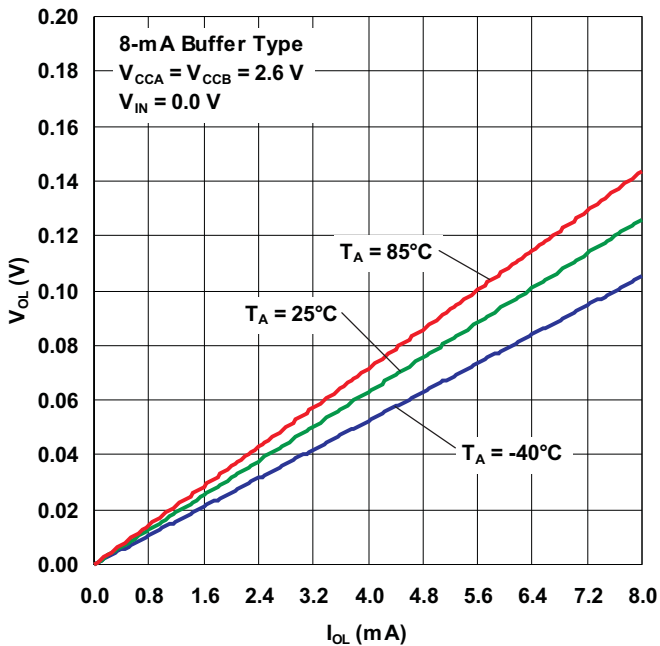


Figure 8.

TYPICAL CHARACTERISTICS (continued)

**HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT**

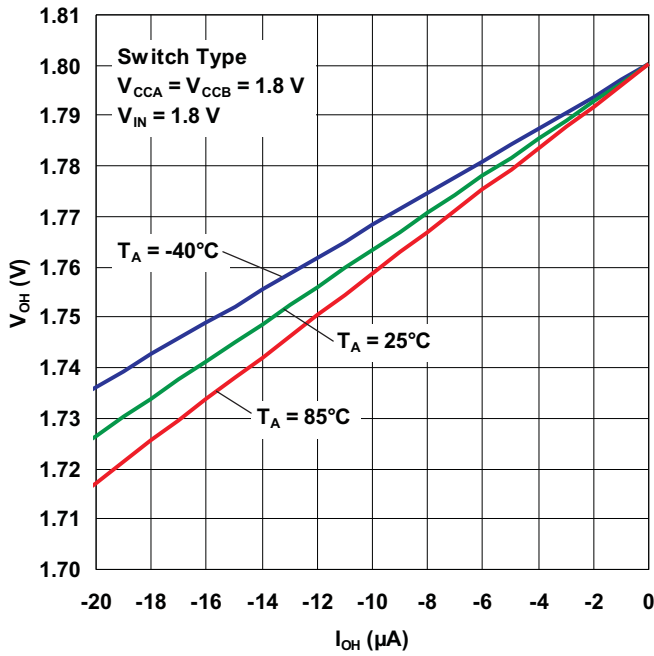


Figure 9.

**HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT**

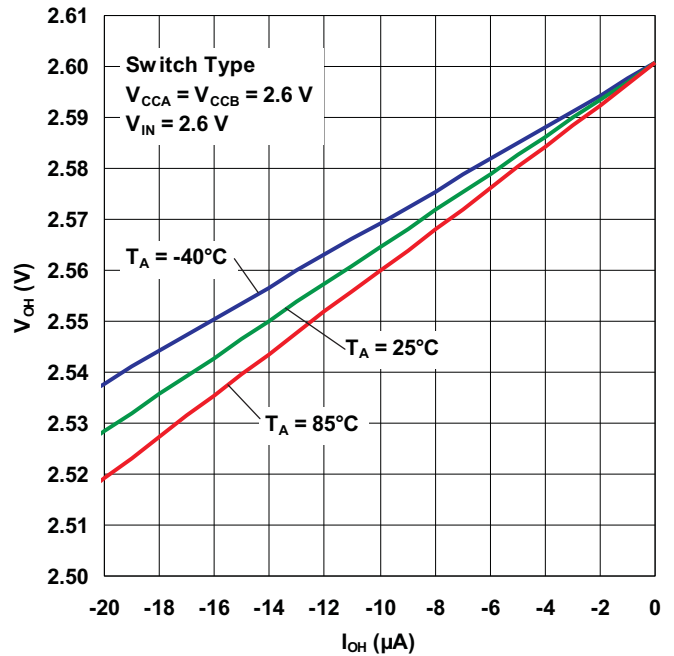


Figure 10.

**HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT**

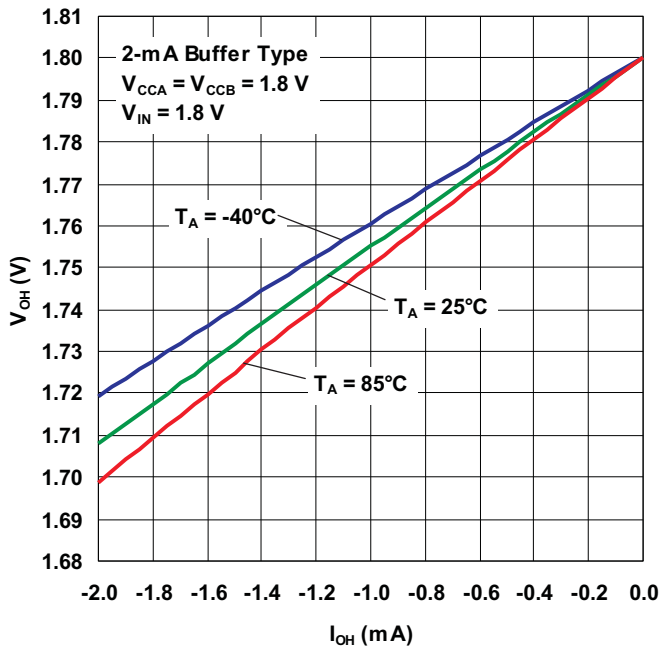


Figure 11.

**HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT**

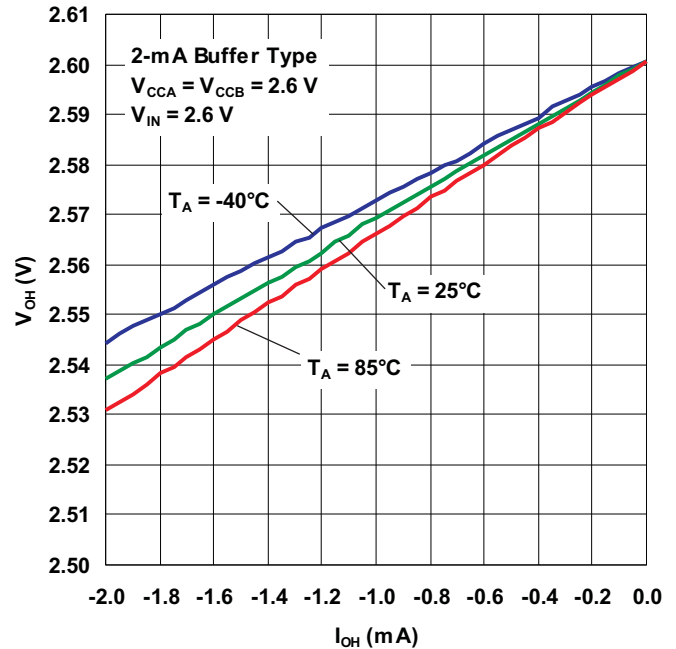


Figure 12.

TYPICAL CHARACTERISTICS (continued)

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

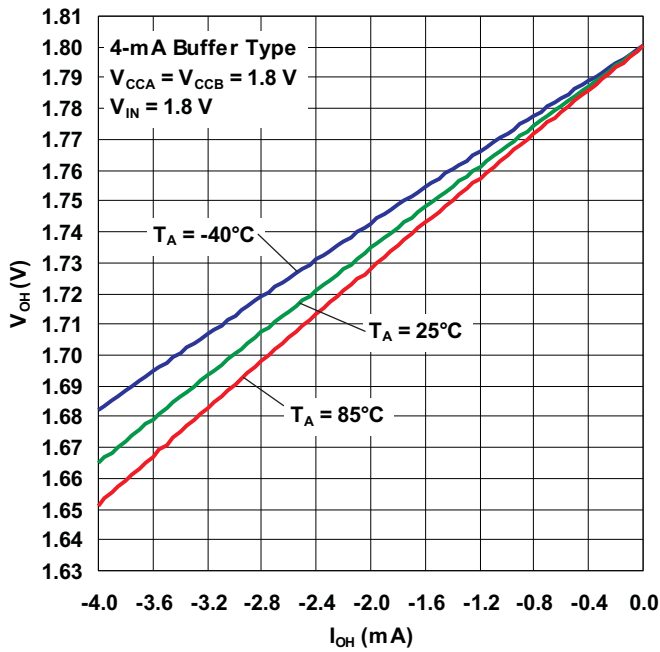


Figure 13.

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

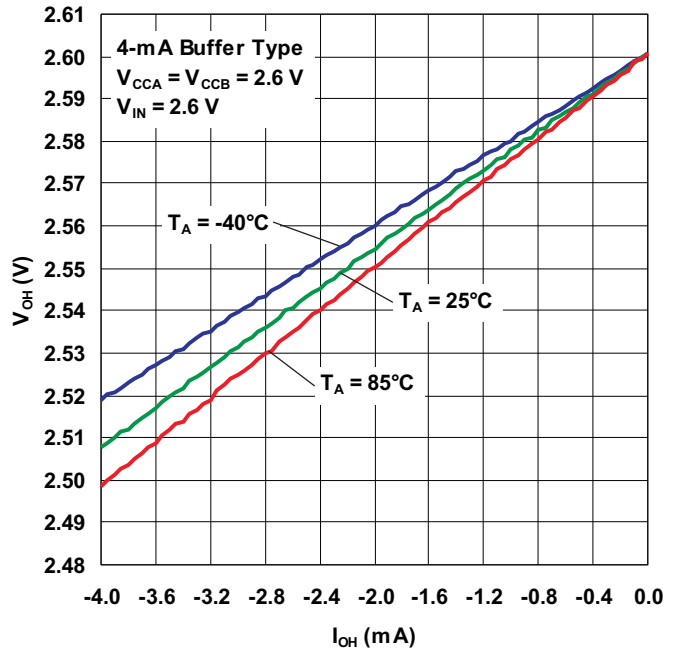


Figure 14.

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

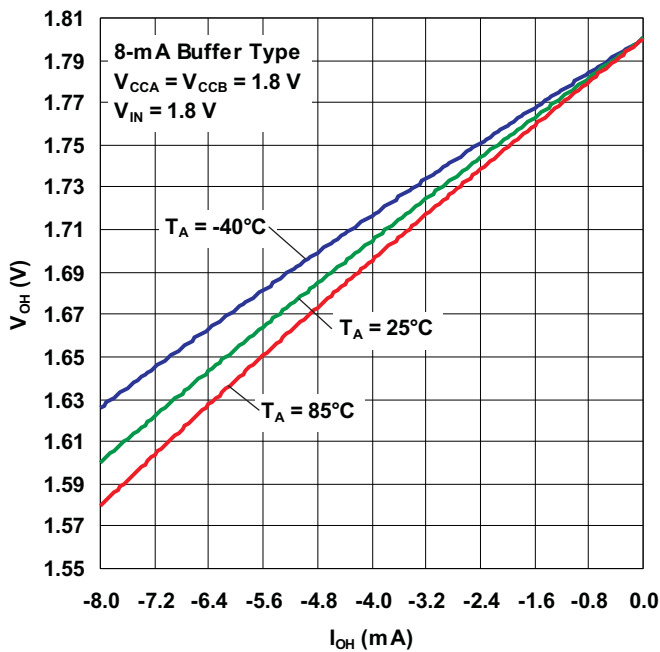


Figure 15.

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

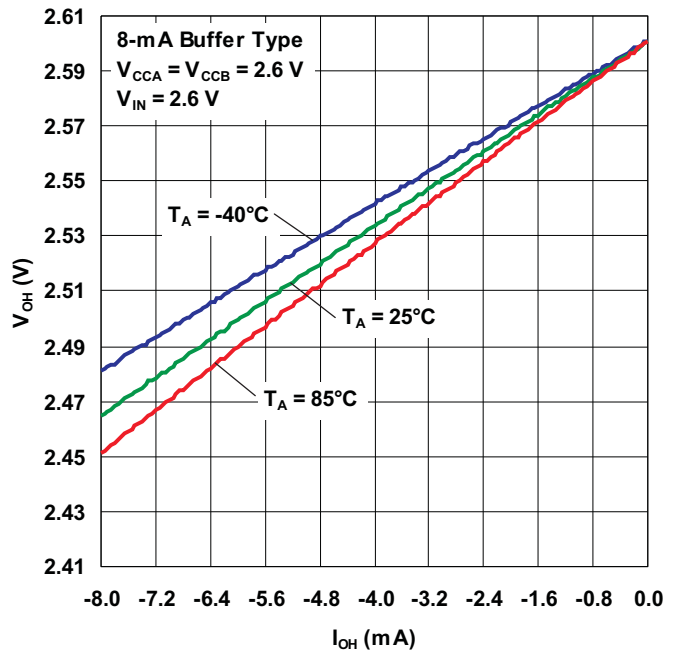


Figure 16.

TYPICAL CHARACTERISTICS (continued)

**PROPAGATION DELAY TIME (HIGH TO LOW)
vs
LOAD CAPACITANCE**

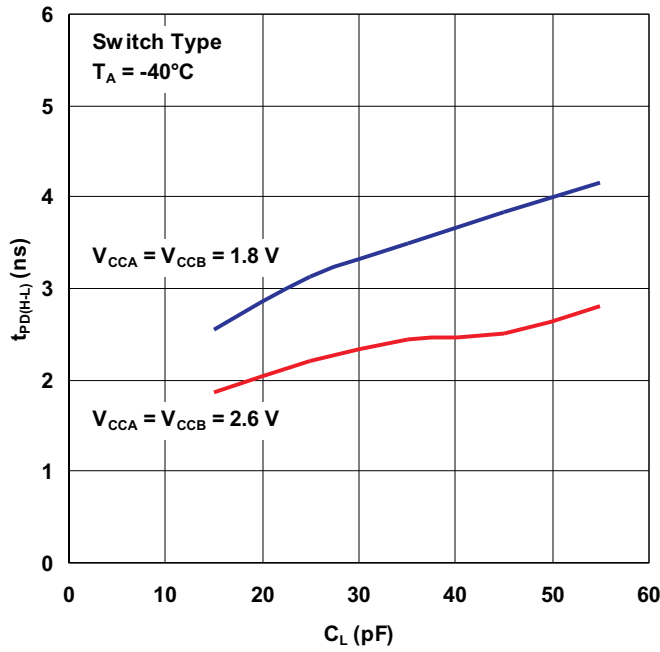


Figure 17.

**PROPAGATION DELAY TIME (LOW TO HIGH)
vs
LOAD CAPACITANCE**

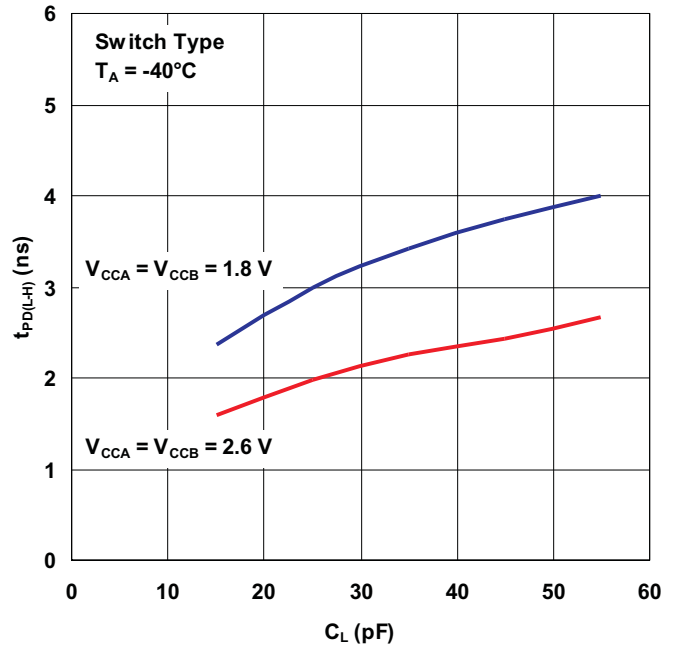


Figure 18.

**PROPAGATION DELAY TIME (HIGH TO LOW)
vs
LOAD CAPACITANCE**

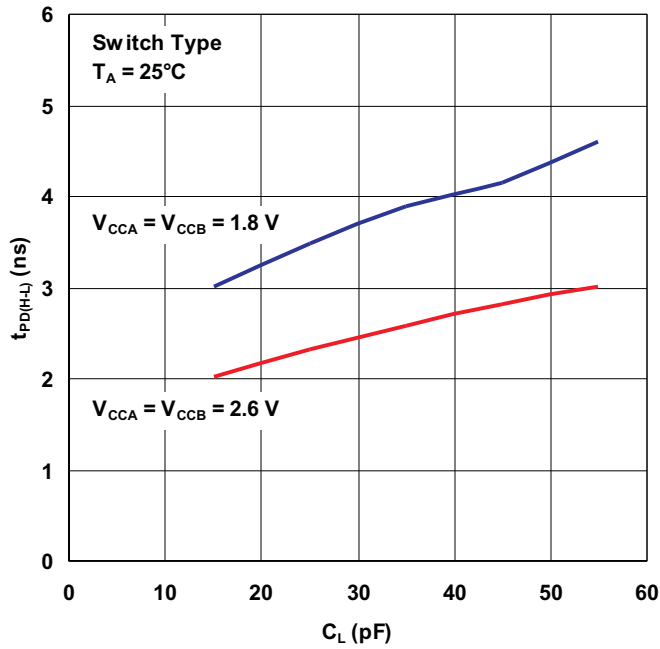


Figure 19.

**PROPAGATION DELAY TIME (LOW TO HIGH)
vs
LOAD CAPACITANCE**

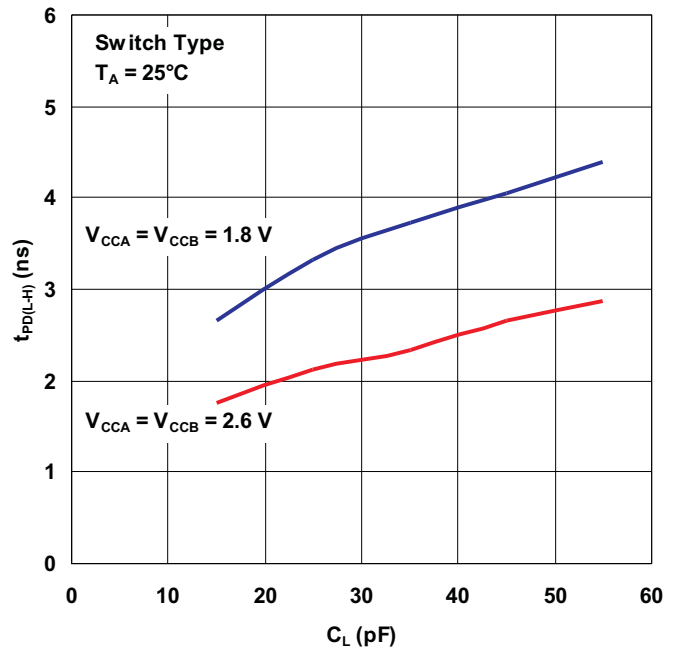


Figure 20.

TYPICAL CHARACTERISTICS (continued)

PROPAGATION DELAY TIME (HIGH TO LOW)
vs
LOAD CAPACITANCE

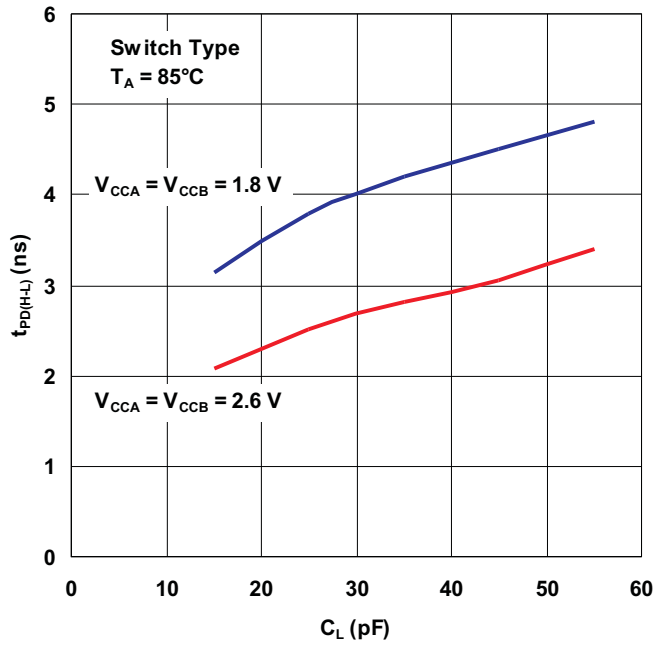


Figure 21.

PROPAGATION DELAY TIME (LOW TO HIGH)
vs
LOAD CAPACITANCE

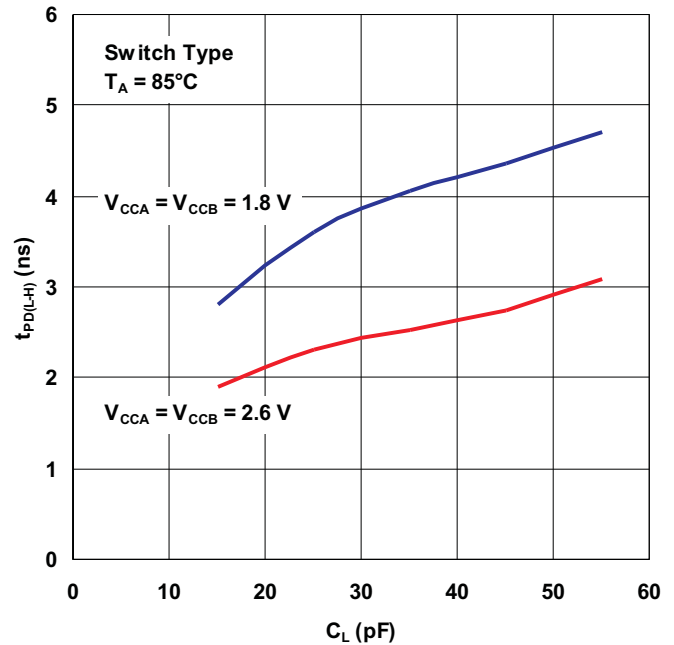


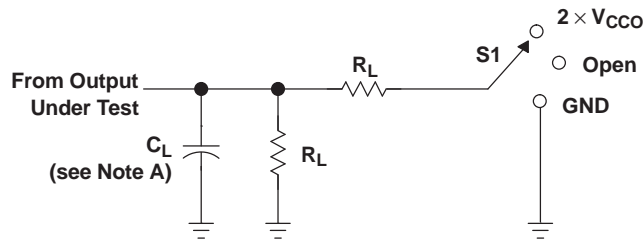
Figure 22.

Typical Application Wiring for TWL1200-Q1 When Connecting to the WL1271

Table 2. WL1271+TWL1200-Q1 Interface

| HOST (MSM) | PIN NAME | BALL NO. | TYPE | | TYPE | BALL NO. | PIN NAME | WL1271 COB |
|------------|-----------------|----------|-------------|------------|---------------|----------|---------------|------------|
| | VCCA | C4 | Power (3 V) | TWL1200-Q1 | Power (1.8 V) | C5 | VCCB | |
| | VCCA | D4 | Power (3 V) | | Power (1.8 V) | D5 | VCCB | |
| | SDIO_DATA0_A | B2 | I/O ↔ | | I/O ↔ | B6 | SDIO_DATA0_B | K4 |
| | SDIO_DATA1_A | C2 | I/O ↔ | | I/O ↔ | C6 | SDIO_DATA1_B | J4 |
| | SDIO_DATA2_A | C1 | I/O ↔ | | I/O ↔ | C7 | SDIO_DATA2_B | J3 |
| | SDIO_DATA3_A | B1 | I/O ↔ | | I/O ↔ | B7 | SDIO_DATA3_B | J5 |
| | SDIO_CMD_A | A2 | I/O ↔ | | I/O ↔ | A6 | SDIO_CMD_B | L3 |
| | SDIO_CLK_A | A1 | I → | | O → | A7 | SDIO_CLK_B | M3 |
| | WLAN_EN_A | D1 | I → | | O → | D6 | WLAN_EN_B | J2 |
| | WLAN_IRQ_A | D2 | O ← | | I ← | D7 | WLAN_IRQ_B | G4 |
| | CLK_REQ_A | E1 | O ← | | I ← | E7 | CLK_REQ_B | F5 |
| | BT_EN_A | E2 | I → | | O → | E6 | BT_EN_B | G5 |
| | BT_UART_RX_A | G1 | I → | | O → | G7 | BT_UART_RX_B | G7 |
| | BT_UART_CTS_A | F1 | I → | | O → | F7 | BT_UART_CTS_B | E11 |
| | BT_UART_TX_A | G2 | O ← | | I ← | G6 | BT_UART_TX_B | G8 |
| | BT_UART_RTS_A | F2 | O ← | | I ← | F6 | BT_UART_RTS_B | G11 |
| | AUDIO_IN_A | F3 | I → | | I/O ↔ | F5 | AUDIO_IN_B | F6 |
| | AUDIO_CLK_A | A3 | I/O ↔ | | I/O ↔ | A5 | AUDIO_CLK_B | F8 |
| | AUDIO_F-SYN_A | B3 | I/O ↔ | | I/O ↔ | B5 | AUDIO_F-SYN_B | H11 |
| | AUDIO_OUT_A | G3 | O ← | | I ← | G5 | AUDIO_OUT_B | F7 |
| | SLOW_CLK_A | G4 | I → | | O → | F4 | SLOW_CLK_B | K9 |
| | AUD_DIR | A4 | I → | | GND | D3 | GND | |
| | \overline{OE} | B4 | Active low | | | E3 | GND | |
| | | | | | | E4 | GND | |
| | | | | | | E5 | GND | |

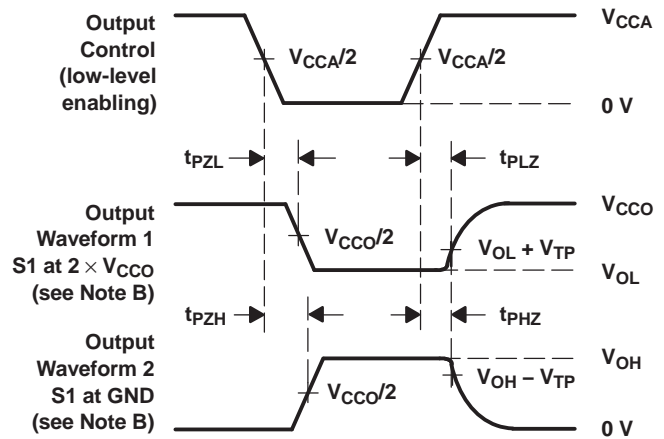
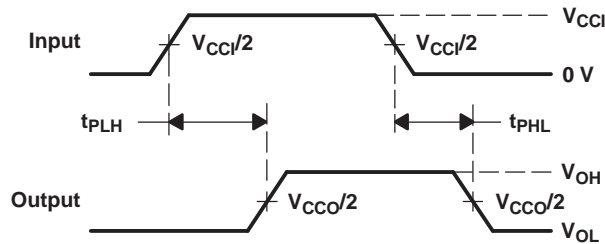
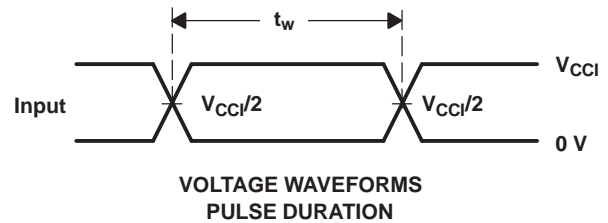
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT FOR BUFFER-TYPE OUTPUTS

| V_{CCO} | C_L | R_L | V_{TP} |
|----------------------------------|-------|--------------|----------|
| $1.8\text{ V} \pm 0.15\text{ V}$ | 15 pF | 2 k Ω | 0.15 V |
| $2.5\text{ V} \pm 0.2\text{ V}$ | 15 pF | 2 k Ω | 0.15 V |
| $3.3\text{ V} \pm 0.3\text{ V}$ | 15 pF | 2 k Ω | 0.3 V |

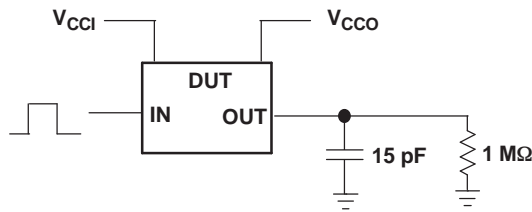
| TEST | S1 |
|-------------------|--------------------|
| t_{pd} | Open |
| t_{PLZ}/t_{PZL} | $2 \times V_{CCO}$ |
| t_{PHZ}/t_{PZH} | GND |



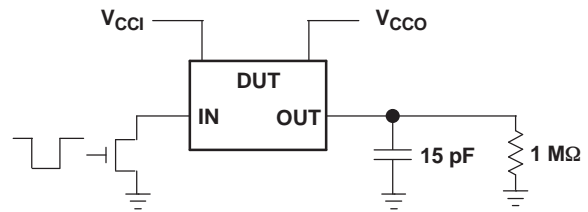
- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $dv/dt \geq 1\text{ V/ns}$.
 - D. The outputs are measured one at a time, with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .
 - H. V_{CCi} is the V_{CC} associated with the input port.
 - I. V_{CCo} is the V_{CC} associated with the output port.

Figure 23. Push-Pull Buffered Direction-Control Load Circuit and Voltage Waveform

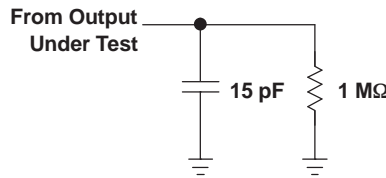
PARAMETER MEASUREMENT INFORMATION (continued)



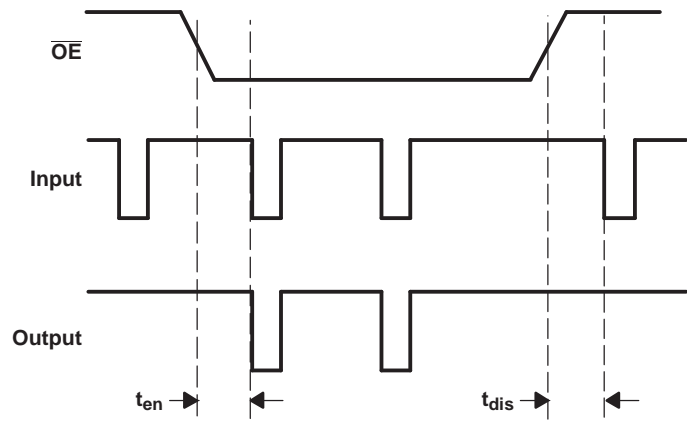
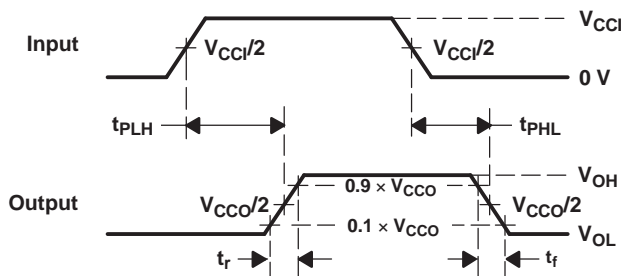
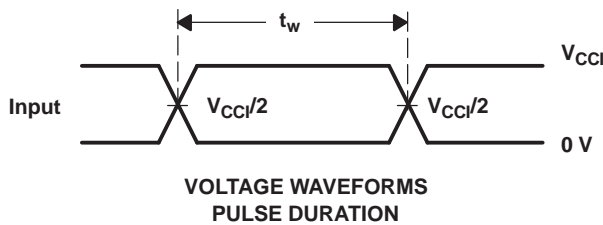
DATA RATE, PULSE DURATION, PROPAGATION DELAY, OUTPUT RISE AND FALL TIME MEASUREMENT USING A PUSH-PULL DRIVER



DATA RATE, PULSE DURATION, PROPAGATION DELAY, OUTPUT RISE AND FALL TIME MEASUREMENT USING AN OPEN-DRAIN DRIVER



LOAD CIRCUIT FOR ENABLE/DISABLE TIME MEASUREMENT – SWITCH-TYPE SDIOs



- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$, $dv/dt \geq 1$ V/ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PLH} and t_{PHL} are the same as t_{pd} .
- H. V_{CCI} is the V_{CC} associated with the input port.
- I. V_{CCO} is the V_{CC} associated with the output port.
- J. All parameters and waveforms are not applicable to all devices.

Figure 24. Auto-Direction-Control Load Circuit and Voltage Waveform

APPLICATION CIRCUIT EXAMPLES

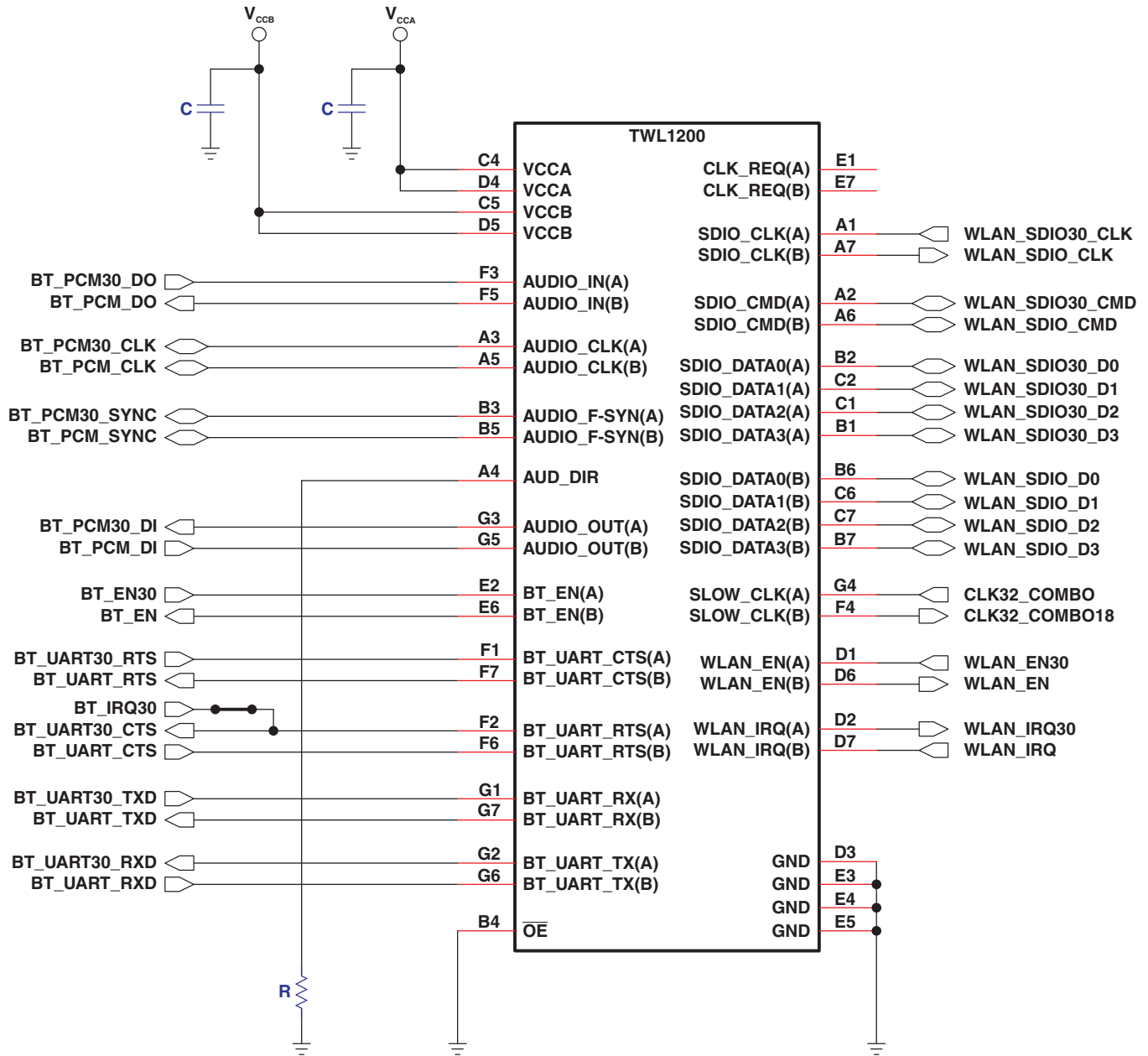


Figure 25. Application Circuit Example, \overline{OE} Connection With Audio_CLK and Audio_F-SYNC Channels Established From B Side to A Side

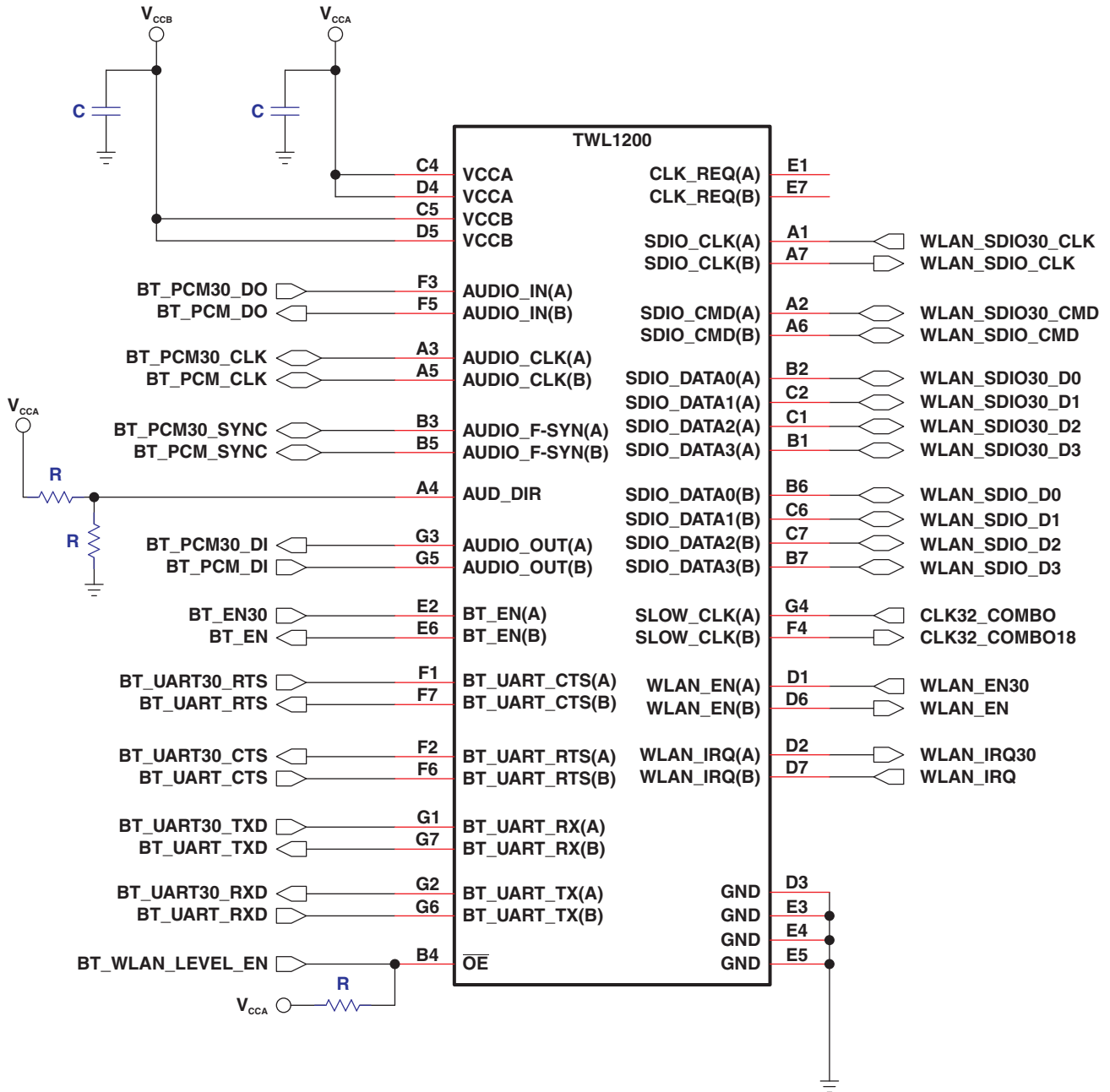


Figure 26. Application Circuit Example, With Voltage Divider for AUD_DIR Connection

PRINCIPLES OF OPERATION

Applications

The TWL1200-Q1 device has been designed to bridge the digital-switching compatibility gap between two voltage nodes to interface successfully the logic threshold levels between a host processor and the Texas Instruments Wi-Link-6 WLAN/BT/FM products. The device is intended to be used in a point-to-point topology when interfacing these devices that may or may not be operating at different interface voltages.

Architecture

The BT/UART and PCM/Audio subsystem interfaces consist of a fully-buffered voltage translator design that has its output transistors to source and sink current optimized for drive strength.

The SDIO lines constitute a semi-buffered auto-direction-sensing based translator architecture (see Figure 27) that does not require a direction-control signal to control the direction of data flow of the A to B ports (or from B to A ports).

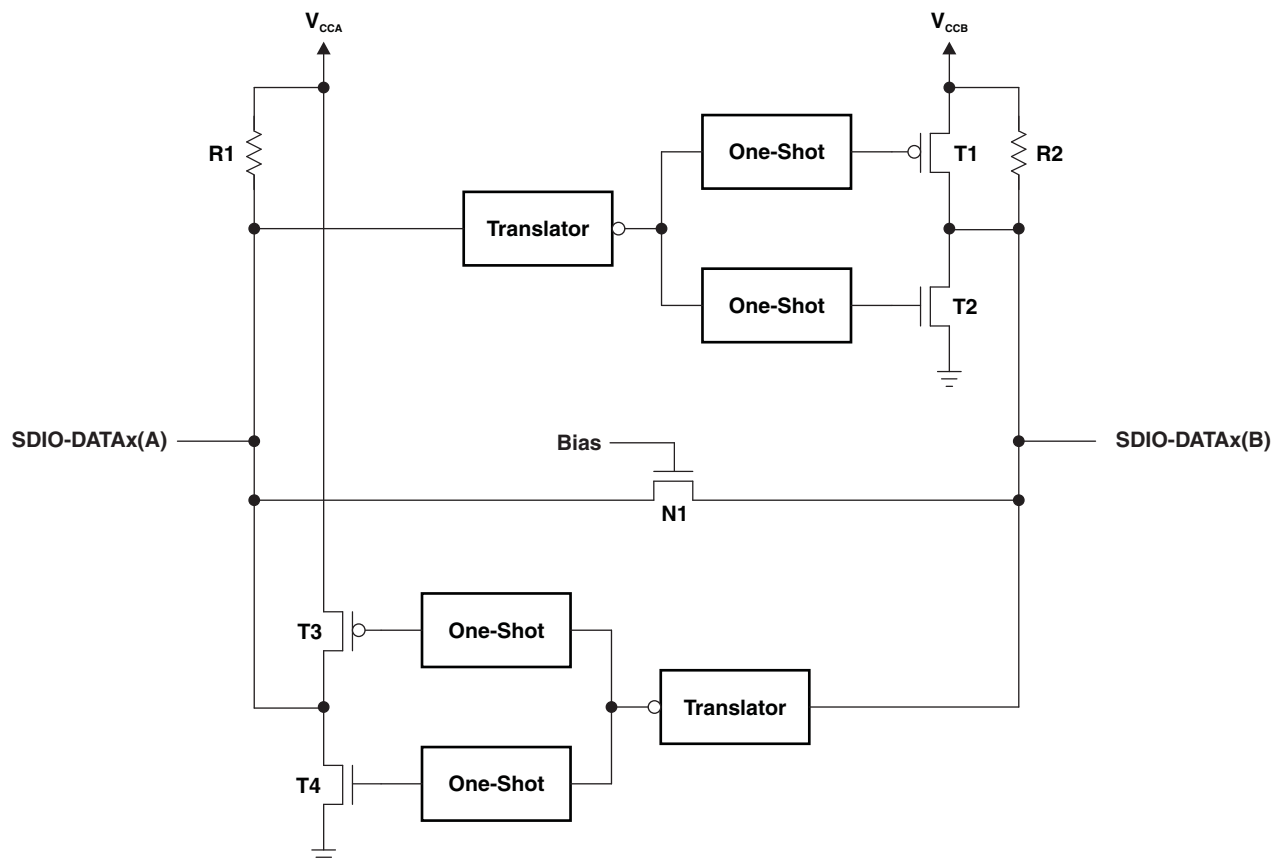


Figure 27. Architecture of an SDIO Switch-Type Cell

Each of these bidirectional SDIO channels independently determines the direction of data flow without a direction-control signal. Each I/O pin can be automatically reconfigured as either an input or an output, which is how this auto-direction feature is realized.

The following two key circuits are employed to facilitate the *switch-type* voltage-translation function:

1. Integrated pullup resistors to provide dc-bias and drive capabilities
2. An N-channel pass-gate transistor topology (with a high R_{ON} of approximately 300 Ω) that ties the A-port to the B-port
3. Output one-shot (O.S.) edge-rate accelerator circuitry to detect and accelerate rising edges on the A or B ports

For bidirectional voltage translation, pullup resistors are included on the device for dc current-sourcing capability. The V_{GATE} gate bias of the N-channel pass transistor is set at a level that optimizes the switch characteristics for maximum data rate as well as minimal static supply leakage. Data can flow in either direction without guidance from a control signal.

The edge-rate acceleration circuitry speeds up the output slew rate by monitoring the input edge for transitions, helping maintain the data rate through the device.

During a low-to-high rising edge of a signal, the O.S. circuits turn on the PMOS transistors (T_1 , T_3) and its associated driver output resistance of the driver is decreased to approximately $50\ \Omega$ to $70\ \Omega$ during this acceleration phase to increase the current drive capability of the driver for approximately 30 ns or 95% of the input edge, whichever occurs first. This edge-rate acceleration provides high ac drive by bypassing the internal pullup resistors during the low-to-high transition to speed up the rising-edge signal.

During a high-to-low signal falling-edge, the O.S. circuits turn on the NMOS transistors (T_2 , T_4) and its associated driver output resistance of the driver is decreased to approximately $50\ \Omega$ to $70\ \Omega$ during this acceleration phase to increase the current drive capability of the driver for approximately 30 ns or 95% of the input edge, whichever occurs first.

To minimize dynamic I_{CC} and the possibility of signal contention, the user should wait for the O.S. circuit to turn off before applying a signal in the opposite direction. The worst-case duration is equal to the minimum pulse-duration number provided in the *Timing Requirements* section of this data sheet.

Once the O.S. is triggered and switched off, both the A and B ports must go to the same state (that is, both High or both Low) for the one-shot to trigger again. In a dc state, the output drivers maintain a Low state through the pass transistor. The output drivers maintain a High through the *smart pullup resistors* that dynamically change value based on whether a Low or a High is being passed through the SDIO lines, as follows:

- R_{PU1} and R_{PU2} values are 25 k Ω when the output is driving a low.
- R_{PU1} and R_{PU2} values are 4 k Ω when the output is driving a high.
- R_{PU1} and R_{PU2} values are 70 k Ω when the device is disabled via the \overline{OE} pin or by pulling the either V_{CCA} or V_{CCB} to 0 V.

The reason for using these *smart pullup resistors* is to allow the TWL1200-Q1 to realize a lower static power consumption (when the I/Os are low), support lower V_{OL} values for the same size pass-gate transistor, and improved simultaneous switching performance.

Input Driver Requirements

The continuous dc-current sinking capability is determined by the external system-level driver interfaced to the SDIO pins. Because the high bandwidth of these bidirectional SDIO circuits necessitates a port quickly changing from an input to an output (and vice-versa), they have a modest dc-current sourcing capability of hundreds of microamps, as determined by the smart pullup resistor values.

The fall time (t_{fA} , t_{fB}) of a signal depends on the edge rate and output impedance of the external device driving the SDIO I/Os, as well as the capacitive loading on these lines.

Similarly, the t_{pd} and maximum data rates also depend on the output impedance of the external driver. The values for t_{fA} , t_{fB} , t_{pd} , and maximum data rates in the data sheet assume that the output impedance of the external driver is less than $50\ \Omega$.

Output Load Considerations

TI recommends careful PCB layout practices with short PCB trace lengths to avoid excessive capacitive loading and to ensure that proper O.S. triggering takes place. PCB signal trace-lengths should be kept short enough such that the round trip delay of any reflection is less than the one-shot duration. This improves signal integrity by ensuring that any reflection sees a low impedance at the driver. The O.S. circuits have been designed to stay on for approximately 30 ns. The maximum capacitance of the lumped load that can be driven also depends directly on the one-shot duration. With very heavy capacitive loads, the one-shot can time-out before the signal is driven fully to the positive rail. The O.S. duration has been set to best optimize trade-offs between dynamic I_{CC} , load driving capability, and maximum bit-rate considerations. Both PCB trace length and connectors add to the capacitance that the TWL1200-Q1 SDIO output sees, so it is recommended that this lumped-load capacitance be considered and kept below 75 pF to avoid O.S. retriggering, bus contention, output signal oscillations, or other adverse system-level affects.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Top-Side Markings (4) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|------------------|----------------------|--------------|--------------------------|-------------------------|
| TWL1200IPFBRQ1 | ACTIVE | TQFP | PFB | 48 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 85 | TWL1200Q1 | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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OTHER QUALIFIED VERSIONS OF TWL1200-Q1 :

- Catalog: [TWL1200](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TWL1200IPFBRQ1 | TQFP | PFB | 48 | 1000 | 330.0 | 16.4 | 9.6 | 9.6 | 1.5 | 12.0 | 16.0 | Q2 |

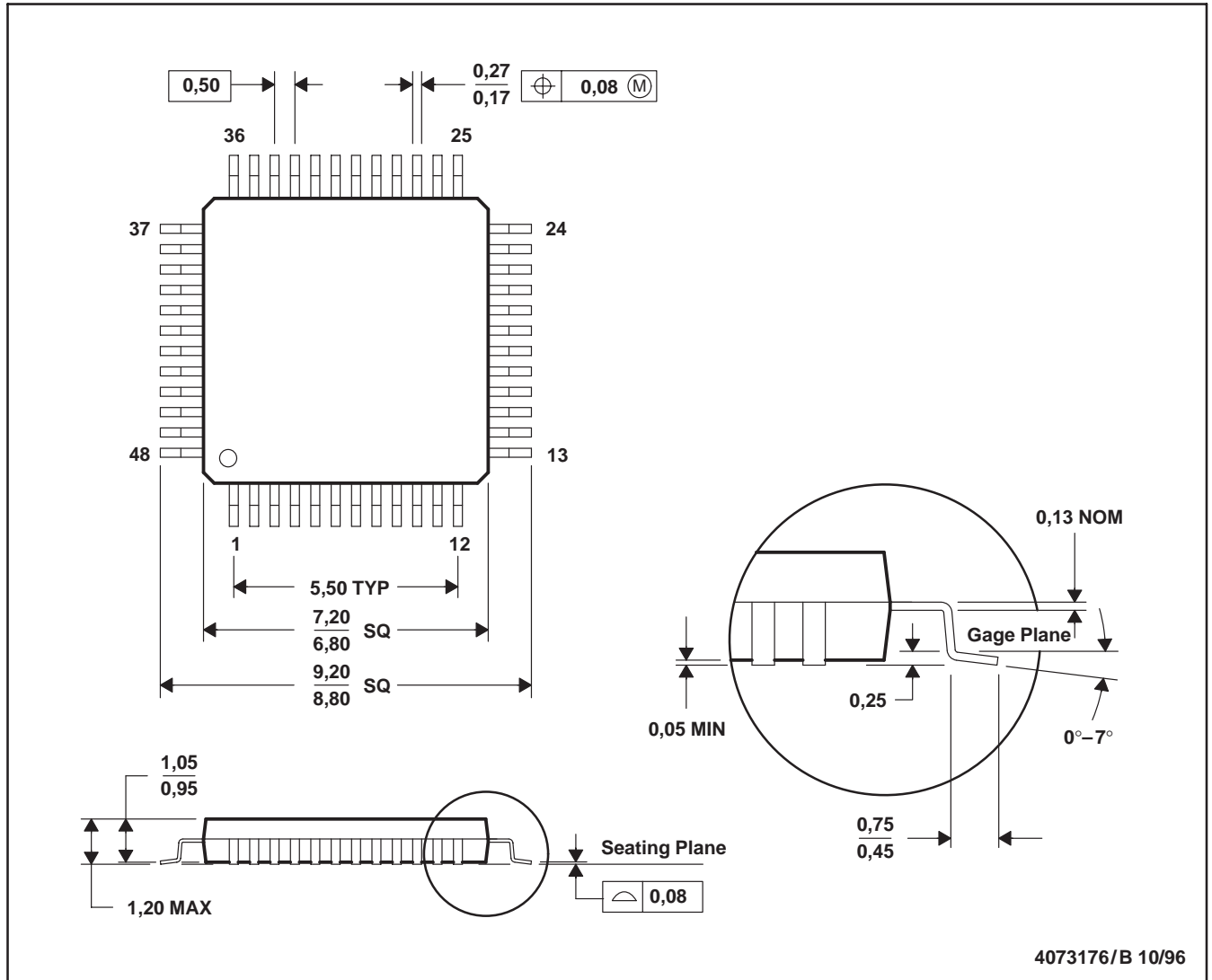
TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TWL1200IPFBRQ1 | TQFP | PFB | 48 | 1000 | 367.0 | 367.0 | 38.0 |

PFB (S-PQFP-G48)

PLASTIC QUAD FLATPACK



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-026

PFB (S-PQFP-G48)



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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