UNITRODE

UCC1837
UCC2837
UCC3837

8-Pin N-FET Linear Regulator Controller

FEATURES

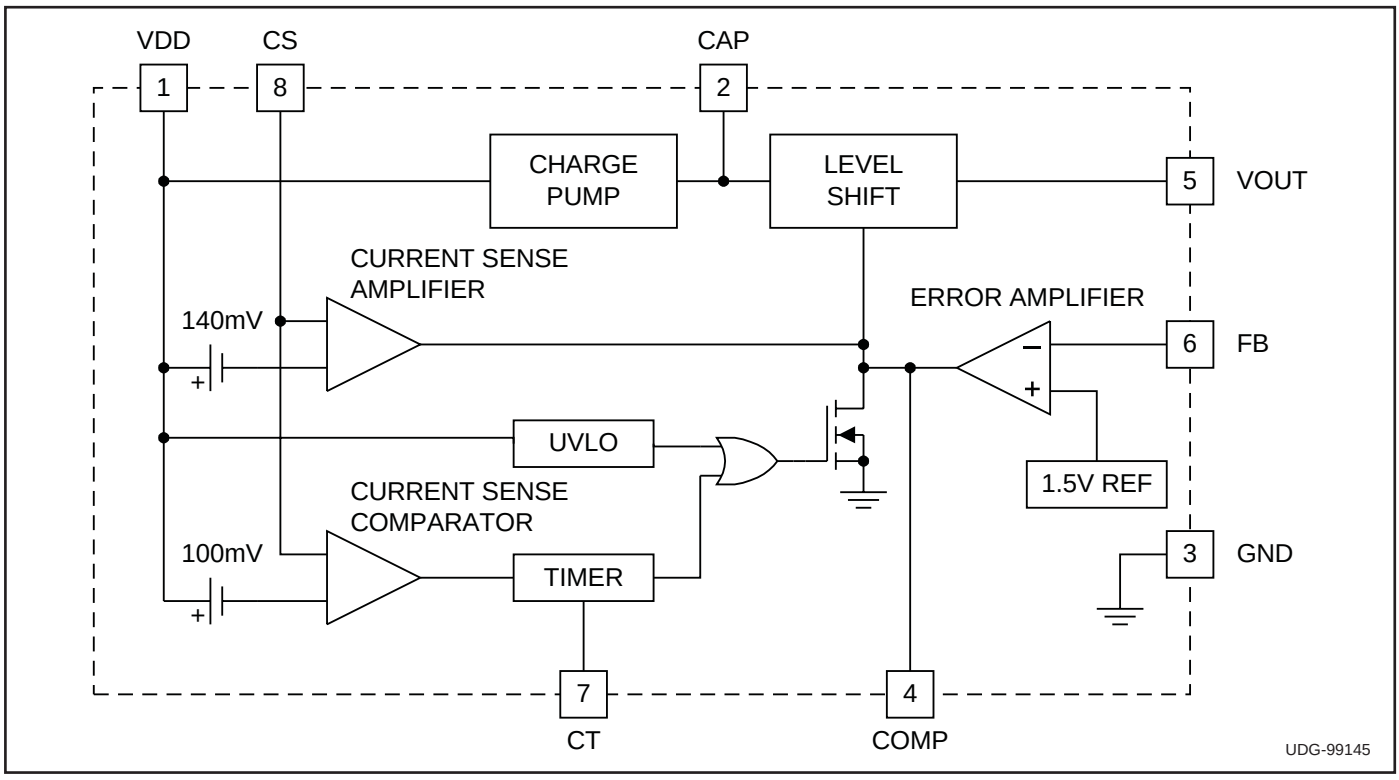
- On Board Charge Pump to Drive External N-MOSFET
- Input Voltage as Low as 3V
- Duty Ratio Mode Over Current Protection
- Extremely Low Dropout Voltage
- Low External Parts Count
- Output Voltages as Low as 1.5V

DESCRIPTION

The UCC3837 Linear Regulator Controller includes all the features required for an extremely low dropout linear regulator that uses an external N-channel MOSFET as the pass transistor. The device can operate from input voltages as low as 3V and can provide high current levels, thus providing an efficient linear solution for custom processor voltages, bus termination voltages, and other logic level voltages below 3V. The on board charge pump creates a gate drive voltage capable of driving an external N-MOSFET which is optimal for low dropout voltage and high efficiency. The wide versatility of this IC allows the user to optimize the setting of both current limit and output voltage for applications beyond or between standard 3-terminal linear regulator ranges.

This 8-pin controller IC features a duty ratio current limiting technique that provides peak transient loading capability while limiting the average power dissipation of the pass transistor during fault conditions. See the Application Section for detailed information.

BLOCK DIAGRAM



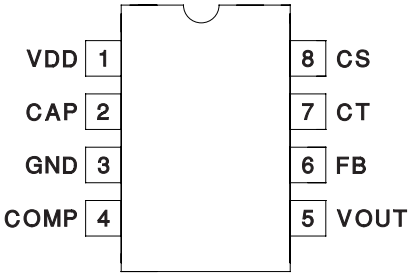
ABSOLUTE MAXIMUM RATINGS

All pins referenced to GND . . . . . –0.3V to +15V
CS, CT, FB . . . . . –0.3V to VDD + 0.3V
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature . . . . . –55°C to +150°C
Lead Temperature (Soldering, 10sec.) . . . . . +300°C

Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAM

DIL-8, SOIC-8 (Top View)
J or N Package, D Package



ELECTRICAL CHARACTERISTICS: Unless otherwise specified, T_A = –55°C to 125°C for the UCC1837, –25°C to 85°C for the UCC2837 and 0°C to 70°C for UCC3837; VDD = 5V, C_T = 10nF, C_{CAP} = 100nF.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Supply					
Supply Current	VDD = 5V		1	1.5	mA
	VDD = 10V		1.2	2	mA
Under Voltage Lockout					
Minimum Voltage to Start		2.00	2.65	3.00	V
Minimum Voltage After Start		1.6	2.2	2.6	V
Hysteresis		0.25	0.45	0.65	V
Reference (Note 1)					
V_{REF}	25°C	1.485	1.5	1.515	V
	0°C to 70°C	1.470	1.5	1.530	V
	–55°C to 125°C	1.455	1.5	1.545	V
Current Sense					
Comparator Offset	0°C to 70°C	90	100	110	mV
Comparator Offset	–55°C to 125°C	85	100	115	mV
Amplifier Offset		120	140	160	mV
Input Bias Current	V_{CS} = 5V		0.5	5	µA
Current Fault Timer					
CT Charge Current	V_{CT} = 1V	16	36	56	µA
CT Discharge Current	V_{CT} = 1V	0.4	1.2	1.9	µA
CT Fault Low Threshold		0.4	0.5	0.6	V
CT Fault Hi Threshold		1.3	1.5	1.7	V
Fault Duty Cycle		2	3.3	5	%
Error Amplifier					
Input Bias Current			0.5	2	µA
Open Loop Gain		60	90		dB
Transconductance	–10µA to 10µA	2	5	8	mMho
Charge Current	V_{COMP} = 6V	20	40	60	µA
Discharge Current	V_{COMP} = 6V	10	25	40	µA

ELECTRICAL CHARACTERISTICS: Unless otherwise specified, T_A = –55°C to 125°C for the UCC1837, –25°C to 85°C for the UCC2837 and 0°C to 70°C for UCC3837; VDD = 5V, C_T = 10nF, C_{CAP} = 100nF.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
FET Driver					
Peak Output Current	V_{CAP} = 10V, VOUT = 1V	0.5	1.5	2.5	mA
Average Output Current	VOUT = 1V	25	100	175	µA
Max Output Voltage	VDD = 4.5V, I_{OUT} = 0µA	8.4	9.7		V
	VDD = 4.5V, I_{OUT} = 10µA, 0°C to 70°C	8	9		V
	VDD = 4.5V, I_{OUT} = 10µA, –55°C to 125°C	7.5	9		V
Charge Pump					
CAP Voltage	VDD = 4.5V, C/S = 0V	11	12.5		V
	VDD = 12V, C/S = 0V		15	16.5	V

Note 1: This is defined as the voltage on FB which results in a DC voltage of 8V on VOUT.

PIN DESCRIPTIONS

CAP: The output of the charge pump circuit. A capacitor is connected between this pin and GND to provide a floating bias voltage for an N-Channel MOSFET gate drive. A minimum of a 0.01µF ceramic capacitor is recommended. CAP can be directly connected to an external regulated source such as +12V, in which case the external voltage will be the source for driving the N-Channel MOSFET.

COMP: The output of the transconductance error amplifier and current sense amplifier. Used for compensating the small signal characteristics of the voltage loop (and current loop when Current Sense Amplifier is active in over curret mode).

CS: The negative current sense input signal. This pin should be connected through a low noise path to the low side of the current sense resistor.

CT: The input to the duty cycle timer circuit. A capacitor is connected from this pin to GND, setting the maximum ON time of the over current protection circuits. See the Application Section for programming instructions.

FB: The inverting terminal of the voltage error amplifier, used to feedback the output voltage for comparison with the internal reference voltage. The nominal DC operating voltage at this pin is 1.5V

GND: Ground reference for the device. For accurate output voltage regulation, GND should be referenced to the output load ground.

VDD: The system input voltage is connected to this point. VDD must be above 3V. VDD also acts as one side of the Current Sense Amplifier and Comparator.

VOUT: This pin directly drives the gate of the external N-MOSFET pass element. The typical output impedance of this pin is 6.5kΩ.

APPLICATION INFORMATION

Topology and General Operation

Unitrode Application Note U-152 is a detailed design of a low dropout linear regulator using an N-channel MOSFET as a pass element, and should be used as a guide for understanding the operation of the circuit shown in Fig. 1.

Charge Pump Operation

The internal charge pump of the UCC3837 is designed to create a voltage equal to 3 times the input VDD voltage at the CAP pin. There is an internal 5V clamp at the input of the charge pump however that insures the voltage at CAP does not exceed the ratings of the IC. This CAP voltage is used to provide gate drive current to the external pass element as well as bias current to internal sections of the UCC3837 itself. The charge pump output has a typical impedance of 80kΩ and therefore the loading of the IC and the external gate drive reduces the voltage from its ideal level. The UCC3837 can operate in several states including having the error amplifier disabled (shut down), in normal linear regulation mode, and in overdrive mode where the linear regulator is responding to a transient load or line condition. The maximum output voltage available at VOUT is shown in Fig. 2 for these various modes of operation.

The charge pump output is designed to supply 10µA of average current to the load which is typically the MOSFET gate capacitance present at the VOUT pin.The capacitor value used at CAP is chosen to provide holdup

APPLICATION INFORMATION

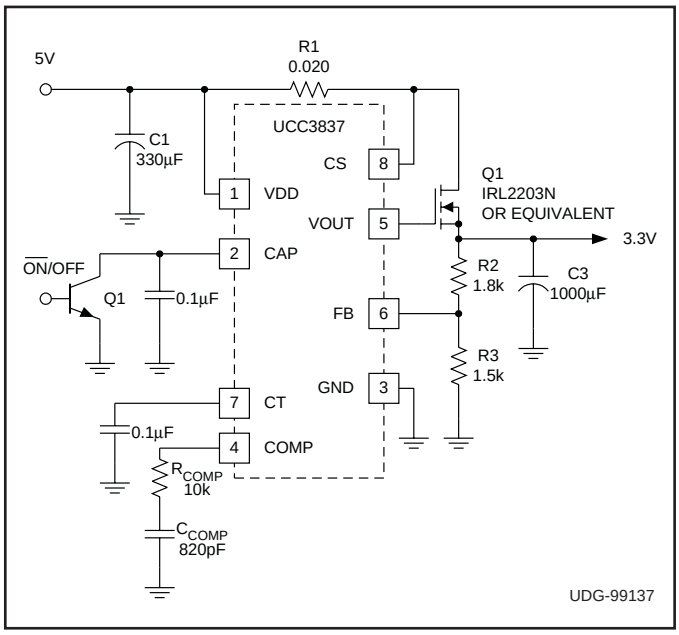


Figure 1. Typical application 5V to 3.3V, 5A

of the CAP voltage should the external load exceed the average current, which occurs during load and line transient conditions. The value of CAP also determines the startup time of the linear regulator. The voltage at CAP charges up with a time constant determined by the charge pump output impedance (typically 80kΩ) and the value of the capacitor on CAP.

An external voltage such as +12V may be tied to the CAP pin directly to insure a higher value of VOUT, which may be useful when a standard level MOSFET is used or when VDD is very low and the resulting VOUT voltage may need to be higher. With an external source applied to CAP, the maximum voltage at VOUT will be approximately 1V below the external source.The external +12V source should be decoupled to GND using a minimum of a 0.01µF capacitor.

Choosing a Pass Element

The UCC3837 is designed for use with an N-channel MOSFET pass element only. The designer may choose a logic level or standard gate level MOSFET depending on the input voltage, the required gate drive, and the available voltage at VOUT as discussed previously. MOSFET selection should be based on required dropout voltage and gate drive characteristics. A lower $R_{DS(on)}$ MOSFET is used when low dropout is required, but this type of MOSFET will have higher gate capacitance which may result in a slower transient response.

A MOSFET used in linear regulation is typically operated at a gate voltage between the threshold voltage and the gate plateau voltage in order to maintain high gain. This

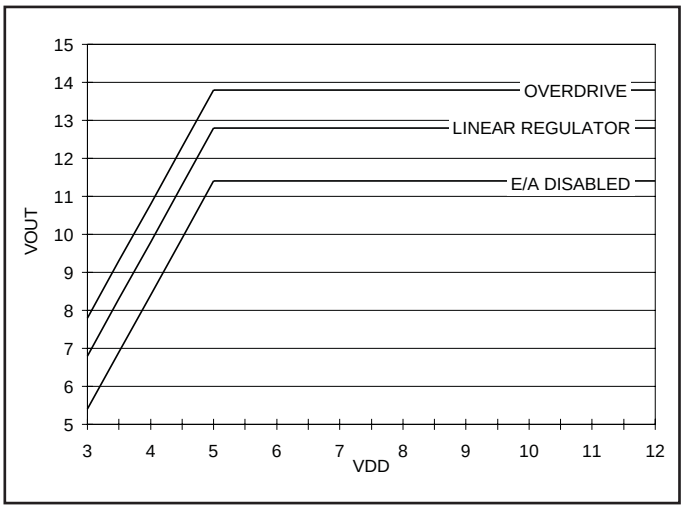


Figure 2. Typical $V_{OUT(max)}$ vs. VDD.

mode of operation is linear, and therefore the channel resistance is higher than the manufacturer's published $R_{DS(on)}$ value. The MOSFET should only be operated in the non-linear (switch) mode under transient conditions, when minimum dropout voltage is required.

Disabling the UCC3837

Grounding the CAP pin will remove the drive voltage and effectively disable the output voltage. The device used to short the output of CAP should have a very low leakage current when in the OPEN state, since even a few microamps will lower the charge pump voltage.

A second method of disabling the UCC3837 is to place a short circuit across C_{COMP}. This will have an advantage of a quicker restart time as the voltage at CAP will not be completely discharged. The charge pump will be loaded down by the typical 40µA charging current of the error amplifier with this configuration, resulting in a lower voltage at CAP.

Compensating the Error Amplifier

Using a MOSFET as an external pass element introduces a pole in the control loop that is a function of the UCC3837 output impedance, R_{OUT}, typically 6.5kΩ, and the MOSFET input gate capacitance. Fig. 3 indicates that in the normal operation of a linear regulator using a MOSFET, the gate capacitance can be predicted directly from the MOSFET characteristic charge curve, using the relationship:

$$C_{IN} = \frac{\Delta Qgth}{\Delta Vgth}$$

This pole can be canceled by programming a zero frequency on the output of the UCC3837 error amplifier equal to the pole frequency. Therefore:

APPLICATION INFORMATION (cont.)

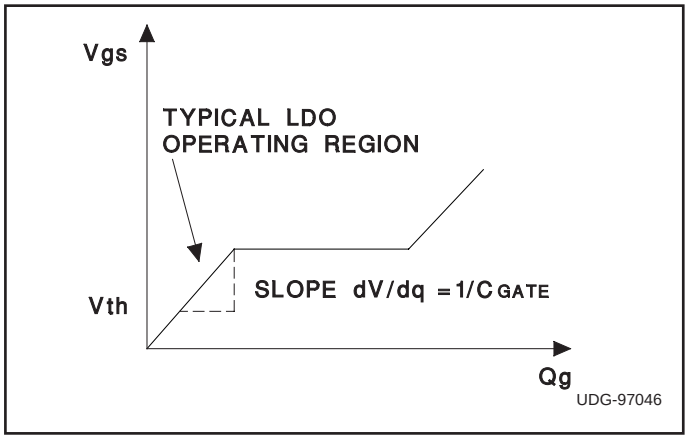


Figure 3. MOSFET turn-on characteristics.

$$F_{POLE} = \frac{1}{2 \bullet \pi \bullet C_{IN} \bullet R_{OUT}}$$

$$F_{ZERO} = F_{POLE} = \frac{1}{2 \bullet \pi \bullet R_{COMP} \bullet C_{COMP}}$$

$$R_{COMP} C_{COMP} = \frac{1}{2 \bullet \pi \bullet F_{POLE}}$$

where C_{IN} is the MOSFET input capacitance and R_{OUT} is the output impedance of VOUT.

The value of C_{COMP} should be large enough that parasitics connected to COMP do not effect the zero frequency. A minimum of 220pF is recommended.

Transient Response

The transient performance of a linear regulator built using the UCC3837 can be predicted by understanding the dynamics of the transient event. Consider a load transient on the application circuit of Fig. 1, where the output current steps from a low value to a high value. Initially, the output voltage will drop as a function of the output capacitors ESR times the load current change. In response to the decrease in feedback voltage at FB, the UCC3837 error amplifier will increase its charge current to a typical value of 40µA. The output of the amplifier will therefore respond by first stepping the voltage proportional to 40µA times R_{COMP}, and then ramping up proportional to 40µA and the value of C_{COMP}. Dynamic response can therefore be improved by increasing R_{COMP} and decreasing C_{COMP} .

The value of VOUT will increase the same amount as the increase in the error amplifier output. The UCC3837 output gate drive current, however, is internally limited to 1.5mA. The response of the voltage at the gate of the external pass element is therefore a function of the 1.5mA drive current and the external gate charge, as obtained from the MOSFET data sheet gate charge curve.

For the application circuit shown in Fig. 1, the voltage at the error amplifier output will increase quickly by 400mV due to the 40µA current through R_{COMP}. The error amplifier will then slew at approximately 50mV per microsecond as the 40µA charges C_{COMP}.

From the IRL2203N data sheet, the typical required gate voltage at room temperature, to deliver 5A is 2.6V. The threshold for the device is approximately 1.5V. From the gate charge curve for the IRL2203N, approximately 7nC charge is required to change the gate voltage from 1.5V to 2.6V. With 1.5mA gate drive current, the required time to charge the gate is therefore 4.7µs.

Overcurrent Protection and Thermal Management:

Overcurrent protection is provided via the UCC3837's internal current amplifier and overcurrent comparator. If at any time the voltage across the current sense resistor crosses the comparator threshold, the UCC3837 begins to modulate the output driver at a 3% duty cycle. During the 3% on time, if the current forces 140mV across the sense amplifier, the UCC3837 will enter a constant output current mode. Fig. 4 illustrates the cyclical retry of the UCC3837 under fault conditions. Note that the initial fault time is longer than subsequent cycles due to the fact that the timing capacitor is completely discharged and must initially charge to the reset threshold of 0.5V.

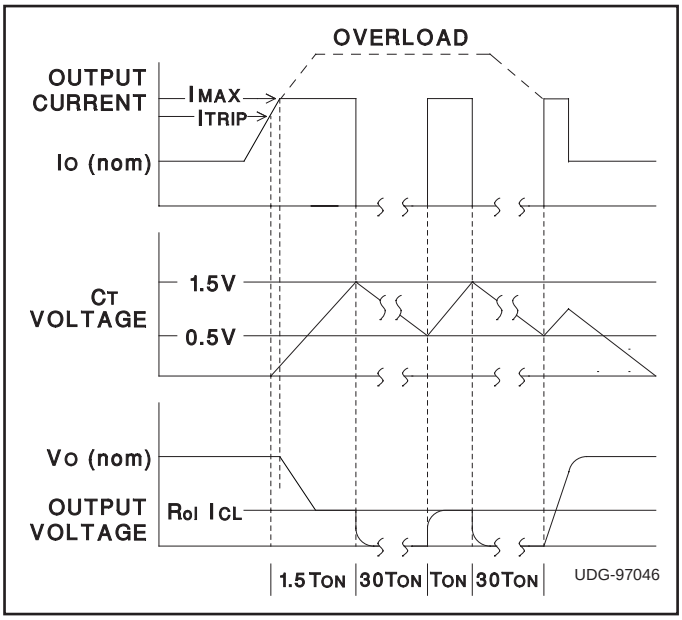


Figure 4. Load current, timing capacitor voltage and output voltage under fault conditions.

Fault time duration is controlled by the value of the timing capacitor, C_T, according to the following equation:

$$t_{FAULT} = C_T \bullet \frac{\Delta V}{I} = C_T \bullet \frac{15 - 0.5}{36 \bullet 10^{-6}} = 27.8 \bullet 10^3 \bullet C_T \quad (1)$$

Fig. 5 provides a plot of fault time vs. timing capacitance. The fault time duration is set based upon the load capacitance, load current, and the maximum output current. The "on" or fault time must be of sufficient duration to charge the load capacitance during a normal startup sequence or when recovering from a fault. If not, the charge accumulated on the output capacitance will be depleted by the load during the "off" time. The cycle will then repeat, preventing the output from turning on.

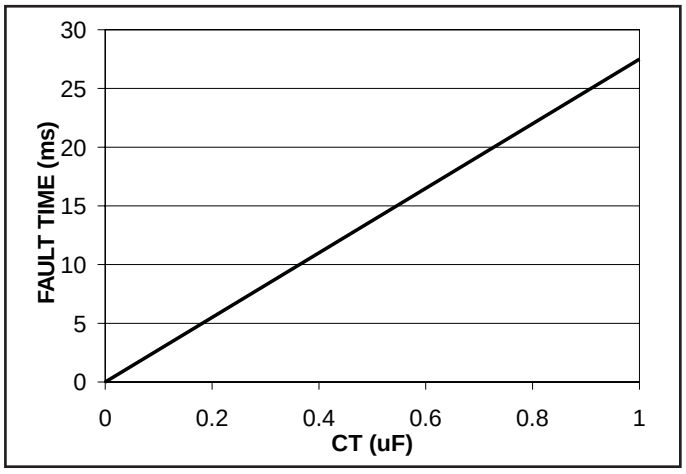


Figure 5. Fault time vs. timing capacitance.

To determine the minimum fault time, assume a maximum load current just less than the trip limit. This leaves the difference between the IMAX and I_{TRIP} values as the current available to charge the output capacitance. The minimum required fault time can then be calculated as follows:

$$t_{FAULT(\min)} = \frac{C_{OUT} \bullet V_{OUT}}{I_{MAX} - I_{TRIP}} \quad (2)$$

The minimum timing capacitor can be calculated by substituting equation (1) for t_{FAULT} in equation (2) and solving for CT.

$$C_{T(\min)} = \frac{C_{OUT} \bullet V_{OUT}}{27.8 \bullet 10^3 \bullet (I_{MAX} - I_{TRIP})} \quad (3)$$

Switchmode protection offers significant heat sinking advantages when compared to conventional, constant current solutions. Since the average power during a fault condition is reduced as a function of the duty cycle, the heat sink need only have adequate thermal mass to absorb the maximum steady state power dissipation and not the full short circuit power. With a 5.25V input and a maximum output current of 5A, the power dissipated in the MOSFET is given by:

$$P = (V_{IN} - V_{SENSE} - V_{OUT}) \bullet I_{OUT} \quad (4)$$

$$P = (5.25 - (5 \bullet 0.02) - 3.3) \bullet 5 = 9.25W$$

Given that the thermal resistivity of the MOSFET is specified as 1°C/W for the TO-220 package style and assuming an ambient temperature of 50°C and a case to heat sink resistivity of θ_{CS} = 0.3°C/W, the heat sink required to maintain a 125°C junction temperature can be calculated as follows:

$$T_J = T_A + P(\theta_{JC} + \theta_{CS} + \theta_{SA}) \quad (5)$$

$$125 = 50 + 9.25 \bullet (1 + 0.3 + \theta_{SA})$$

$$\theta_{SA} \le 6.8 \, ^\circ C/W$$

Based on this analysis, any heatsink with a thermal resistivity of 6.8 °C/W or less should suffice. The current in the circuit of Fig. 1, under short circuit conditions, will be limited to 7A at a 3% duty cycle, resulting in a MOSFET power dissipation of only:

$$P = \left[\left(V_{IN(\max)} - I_{OUT} \bullet (R_{SENSE}) \right) \bullet I_{OUT} \right] \bullet Duty \quad (6)$$

$$P = \left[\left(5.25 - 7 \bullet (0.02) \right) \bullet 7 \right] \bullet 0.03 = 1.07W$$

Without switchmode protection, the short circuit power dissipation would be 35.8W, almost four times the nominal dissipation.

Using Printed Circuit Board Etch as a Sense Resistor

Unitrode Design Note DN-71 discusses the use of printed circuit board copper etch as a low ohm sense resistor. This technique can easily be applied when using the UCC3837. The application circuit shown in Fig. 1 can be used as an example. This linear regulator is designed with a 5A average load current, demanding a 20mΩ sense resistor to result in a 100mV current sense comparator signal for the UCC3837. The maximum ambient temperature of the linear regulator is 70°C.

Using DN-71, a 1 ounce outer layer etch of 0.05 inches wide and 1.57 inches long results in a resistance of 20mΩ at an ambient temperature of 70°C and an operating current of 5A. Because the resistivity of copper is a function of temperature, the current limit at lower temperatures will be higher, as shown in Fig. 6.

APPLICATION INFORMATION

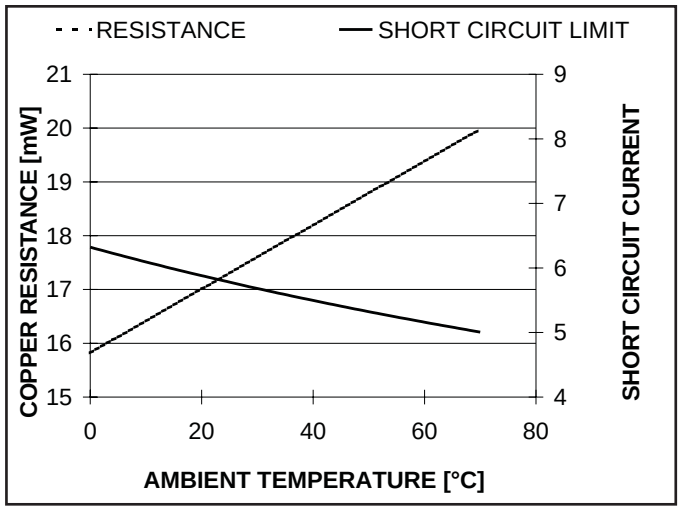


Figure 6. Copper resistance and short circuit limit for example resistor.

Practical Considerations

In order to achieve the expected performance, careful attention must be paid to circuit layout. The printed circuit board should be designed using a single point ground, referenced to the return of the output capacitor. All traces carrying high current should be made as short and wide as possible in order to minimize parasitic resistance and inductance effects.

To illustrate the importance of these concepts, consider the effects of a 1.5" PCB trace located between the output capacitor and the UCC3837 feedback reference. A 0.07" wide trace of 1oz. copper results in an equivalent resistance of 10.4mΩ. At a load current of 3A, 31.2mV is dropped across the trace, contributing almost 1% error to the DC regulation. Likewise, the inductance of the trace is approximately 3.24nH, resulting in a 91mV spike during the 100ns it takes the load current to slew from 200mA to 3A.

The dropout voltage of a linear regulator is often a key design parameter. Calculations of the dropout voltage of a linear regulator based on the UCC3837 Controller should consider all of the following:

- Sense resistor drop, including temperature and tolerance effects,
- Path resistance drops on both the input and output voltages,
- MOSFET resistance as a function of temperature and gate drive, including transient performance,
- Ground path drops.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC2837D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UCC2837	Samples
UCC2837DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UCC2837	Samples
UCC2837DTR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UCC2837	Samples
UCC3837D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	UCC3837	Samples
UCC3837DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	UCC3837	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

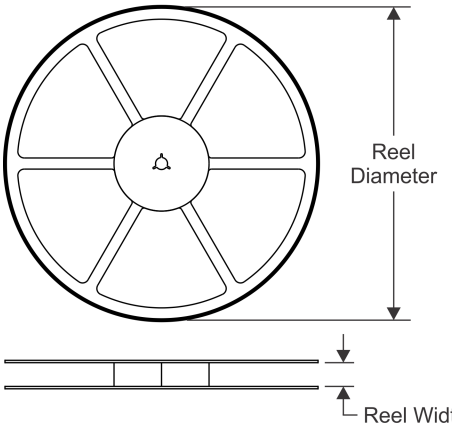
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

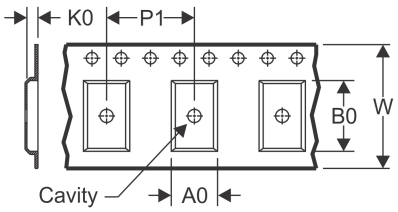
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

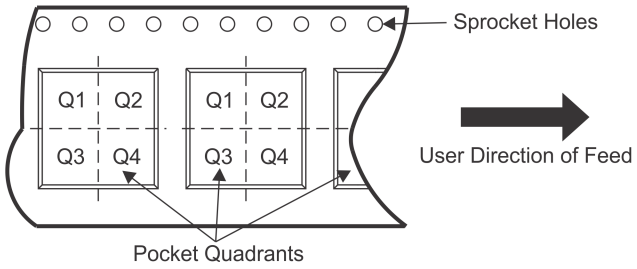


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

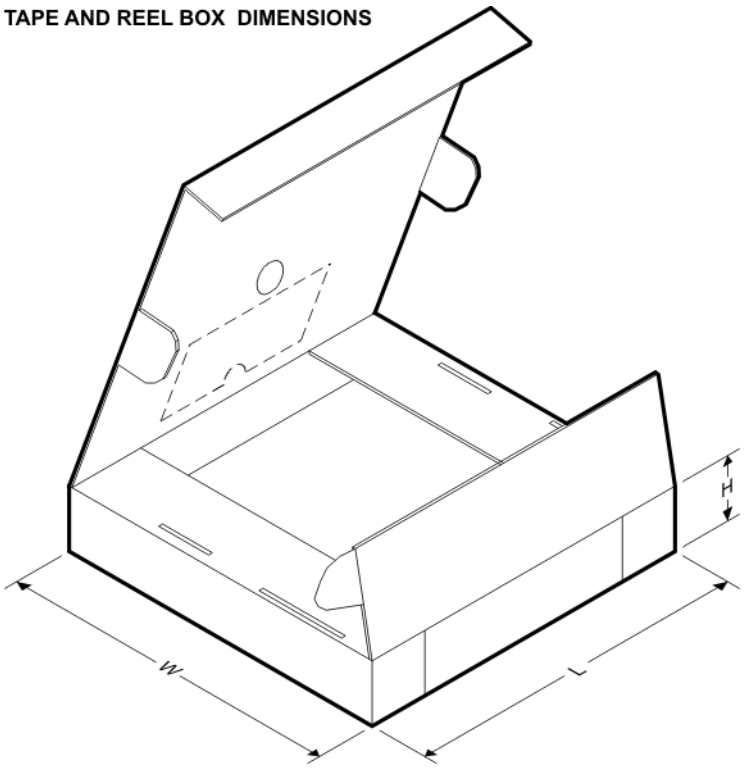
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC2837DTR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

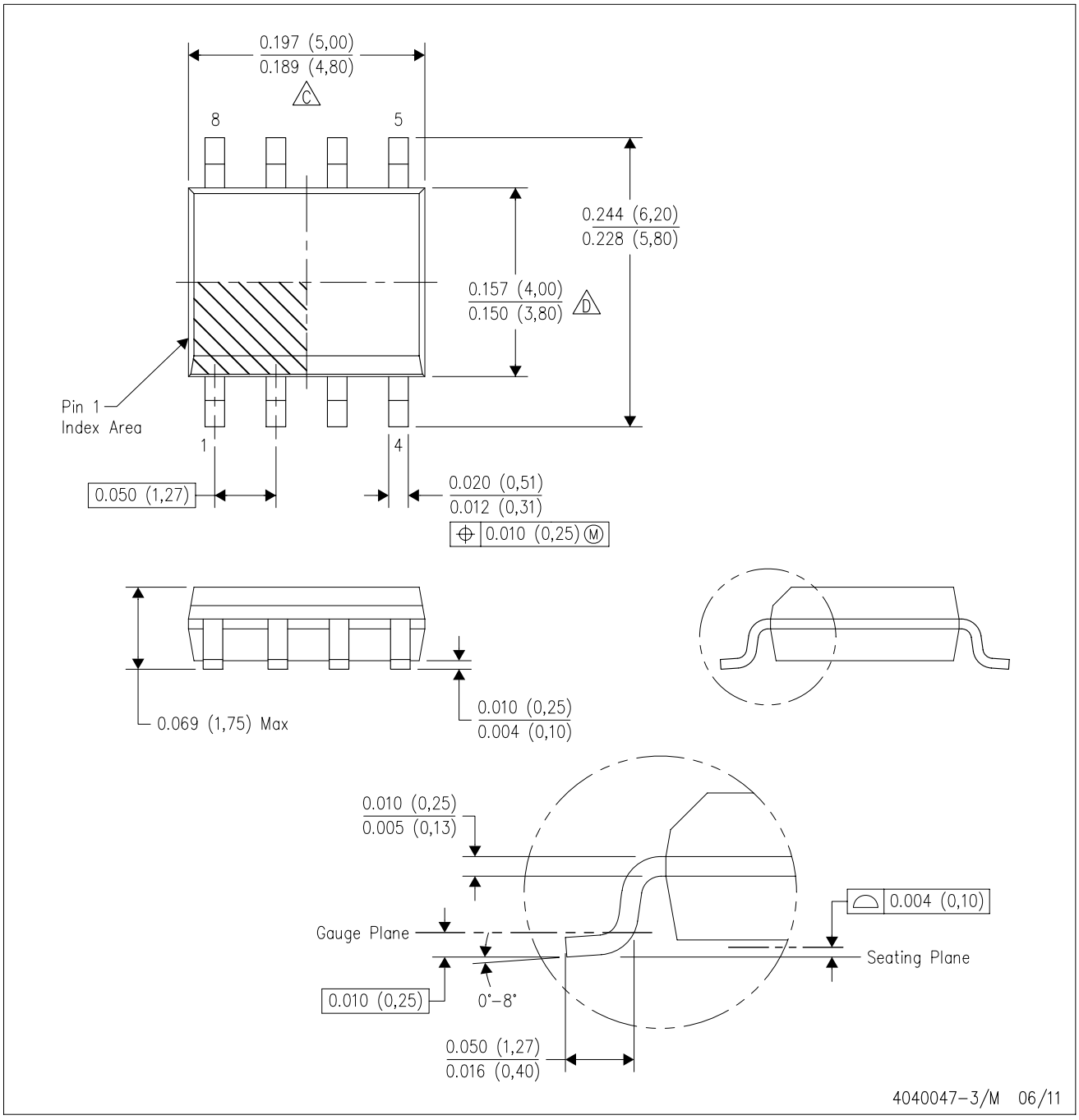
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

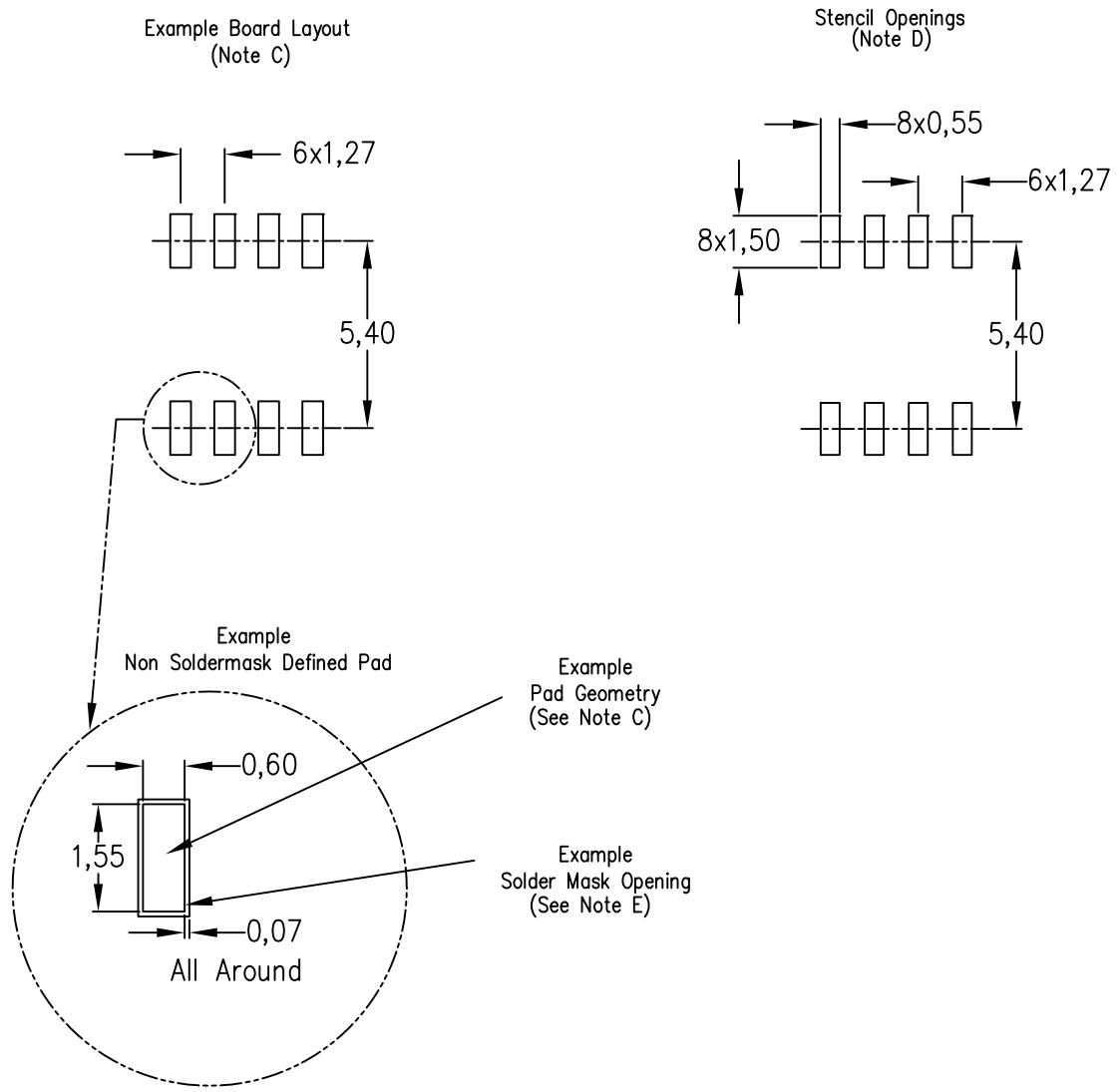
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC2837DTR	SOIC	D	8	2500	367.0	367.0	35.0

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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