TB-7K-325T-IMG
Hardware User Manual

Rev.1.09

Revision History

Version	Date	Description	Publisher
Rev.1.00	2012/05/14	Initial Release	Yoshioka
Rev.1.01	2012/05/18	Add FAN/Heat sink information	Yoshioka
Rev.1.02	2012/05/29	Add related document information	Yoshioka
Rev.1.03	2012/06/06	Modified Figure7-11	Odajima
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Rev.1.05	2013/03/25	Modified Figure7-15 HA13_N	Yoshioka
Rev.1.06	2013/05/16	Modified Table7-6 HA13_P	Amano
Rev.1.07	2013/06/05	Modified Table7-6 Bank No.of LA08,LA12	Amano
Rev.1.08	2014/02/18	Modified Figure7-11, 7.3.2	Amano
Rev.1.09	2014/04/15	Modified Figure7-13、Add EC Declaration of Conformity	Amano

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Introduction

Thank you for purchasing the **TB-7K-325T-IMG** board. Before using the product, be sure to carefully read this user manual and fully understand how to correctly use the product. First read through this manual, then always keep it handy.

SAFETY PRECAUTIONS

Be sure to observe these precautions

Observe the precautions listed below to prevent injuries to you or other personnel or damage to property.

- **Before using the product, read these safety precautions carefully to assure correct use.**
- **These precautions contain serious safety instructions that must be observed.**
- **After reading through this manual, be sure to always keep it handy.**

The following conventions are used to indicate the possibility of injury/damage and classify precautions if the product is handled incorrectly.

Danger	Indicates the high possibility of serious injury or death if the product is handled incorrectly.
Warning	Indicates the possibility of serious injury or death if the product is handled incorrectly.
Caution	Indicates the possibility of injury or physical damage in connection with houses or household goods if the product is handled incorrectly.

The following graphical symbols are used to indicate and classify precautions in this manual.
(Examples)

	Turn off the power switch.
	Do not disassemble the product.
	Do not attempt this.

Warning	
	**In the event of a failure, disconnect the power supply.** If the product is used as is, a fire or electric shock may occur. Disconnect the power supply immediately and contact our sales personnel for repair.
	**If an unpleasant smell or smoking occurs, disconnect the power supply.** If the product is used as is, a fire or electric shock may occur. Disconnect the power supply immediately. After verifying that no smoking is observed, contact our sales personnel for repair.
	**Do not disassemble, repair or modify the product.** Otherwise, a fire or electric shock may occur due to a short circuit or heat generation. For inspection, modification or repair, contact our sales personnel.
	**Do not touch a cooling fan.** As a cooling fan rotates in high speed, do not put your hand close to it. Otherwise, it may cause injury to persons. Never touch a rotating cooling fan.
	**Do not place the product on unstable locations.** Otherwise, it may drop or fall, resulting in injury to persons or failure.
	**If the product is dropped or damaged, do not use it as is.** Otherwise, a fire or electric shock may occur.
	**Do not touch the product with a metallic object.** Otherwise, a fire or electric shock may occur.
	**Do not place the product in dusty or humid locations or where water may splash.** Otherwise, a fire or electric shock may occur.
	**Do not get the product wet or touch it with a wet hand.** Otherwise, the product may break down or it may cause a fire, smoking or electric shock.
	**Do not touch a connector on the product (gold-plated portion).** Otherwise, the surface of a connector may be contaminated with sweat or skin oil, resulting in contact failure of a connector or it may cause a malfunction, fire or electric shock due to static electricity.

Caution	
	Do not use or place the product in the following locations. • Humid and dusty locations • Airless locations such as closet or bookshelf • Locations which receive oily smoke or steam • Locations exposed to direct sunlight • Locations close to heating equipment • Closed inside of a car where the temperature becomes high • Staticky locations • Locations close to water or chemicals Otherwise, a fire, electric shock, accident or deformation may occur due to a short circuit or heat generation.
	Do not place heavy things on the product. Otherwise, the product may be damaged.

■ Disclaimer

This product is an evaluation board for Xilinx Kintex-7 FPGA. Tokyo Electron Device Limited assumes no responsibility for any damages resulting from the use of this product for purposes other than those stated.

Even if the product is used properly, Tokyo Electron Device Limited assumes no responsibility for any damages caused by:

(1) Earthquake, thunder, natural disaster or fire resulting from the use beyond our responsibility, acts by a third party or other accidents, the customer's willful or accidental misuse or use under other abnormal conditions.
(2) Secondary impact arising from use of this product or its unusable state (business interruption or others)
(3) Use of this product against the instructions given in this manual.
(4) Malfunctions due to connection to other devices.

Tokyo Electron Device Limited assumes no responsibility or liability for:

(1) Erasure or corruption of data arising from use of this product.
(2) Any consequences or other abnormalities arising from use of this product, or
(3) Damage of this product not due to our responsibility or failure due to modification

This product has been developed by assuming its use for research, testing or evaluation. It is not authorized for use in any system or application that requires high reliability.

Repair of this product is carried out by replacing it on a chargeable basis, not repairing the faulty devices. However, non-chargeable replacement is offered for initial failure if such notification is received within two weeks after delivery of the product.

The specification of this product is subject to change without prior notice.

The product is subject to discontinuation without prior notice.

1. Related Documents and Accessories

Related documents:

All documents relating to this board can be downloaded from our website. (http://ppg.teldevice.co.jp/eng/index.htm)

Xilinx FPGA document: http://www.xilinx.com/support/documentation/index.htm

DS180: 7 Series FPGAs Overview
UG586: 7 Series FPGAs Memory Interface Solutions User Guide
UG473: 7 Series FPGAs Memory Resources User Guide
UG470: 7 Series FPGAs Configuration User Guide
UG475: 7 Series FPGAs Packaging and Pinout User Guide
UG476: 7 Series FPGAs GTX Transceivers User Guide
UG477: 7 Series FPGAs Integrated Block for PCI Express User Guide
UG480: 7 Series FPGAs XADC User Guide

On board accessories:

- Board Foot
  Rubber foot: 9, Screw M3 x 6: 18, Spacer M3 x 10: 9
- 74.25MHz Oscillator (MXO-50B): Mounted on X2(Socket)

Accessories:

- MMCX Cable Set
  - MMCX - SMA Cable(Samtec: RF174-03SP1-01SP1-0400): 2
  - MMCX - MMCX Cable(Samtec: RF174-03SP1-03SP1-0400): 2
- FMC Spacer Set
  - Spacer M2.6 x 10: 6
  - Screw with washer: 12
- Jumper Socket(Samtec: 2SN-BK-G): 14
- FAN/Heat sink(ALPHA: FS40-15M42): 1
- AC adapter(AIKOH ELECTRONICS CORP: TW-1250P or equivalent): 1

2. Overview

TB-7K-325T-IMG is evaluation platform of Xilinx Kintex-7 FPGA. Mainly, it can used for Video Interface and Video Processing applications. Speed grade -2 FPGA is mounted on this board.

3. Feature

- Xilinx Kintex-7 FPGA: XC7K325T-2FFG900CES (General ES Device)
- DDR3 Memory: EDJ2116DEBG-**-* 2Gbit x 4 or equivalent device
- Configuration PROM: Quad SPI Flash 128Mbit x 1
- FMC option connecters x 4 *Please refer detail pin assign
  - HPC(High Pin Count) x 2
  - LPC(Low Pin Count) x 2
- On Board Clock
  - 74.25MHz OSC(Socket)
  - 135MHz OSC
  - 200MHz OSC
  - PLL
- Interface
  - MMCX for external clocks.
  - UART(RS-232C D-sub 9pin)
  - XADC interface to Pin Header
  - Push Switches, DIP Switches and LEDs
  - JTAG

4. Block Diagram

Following figure shows block diagram of TB-7K-325T-IMG

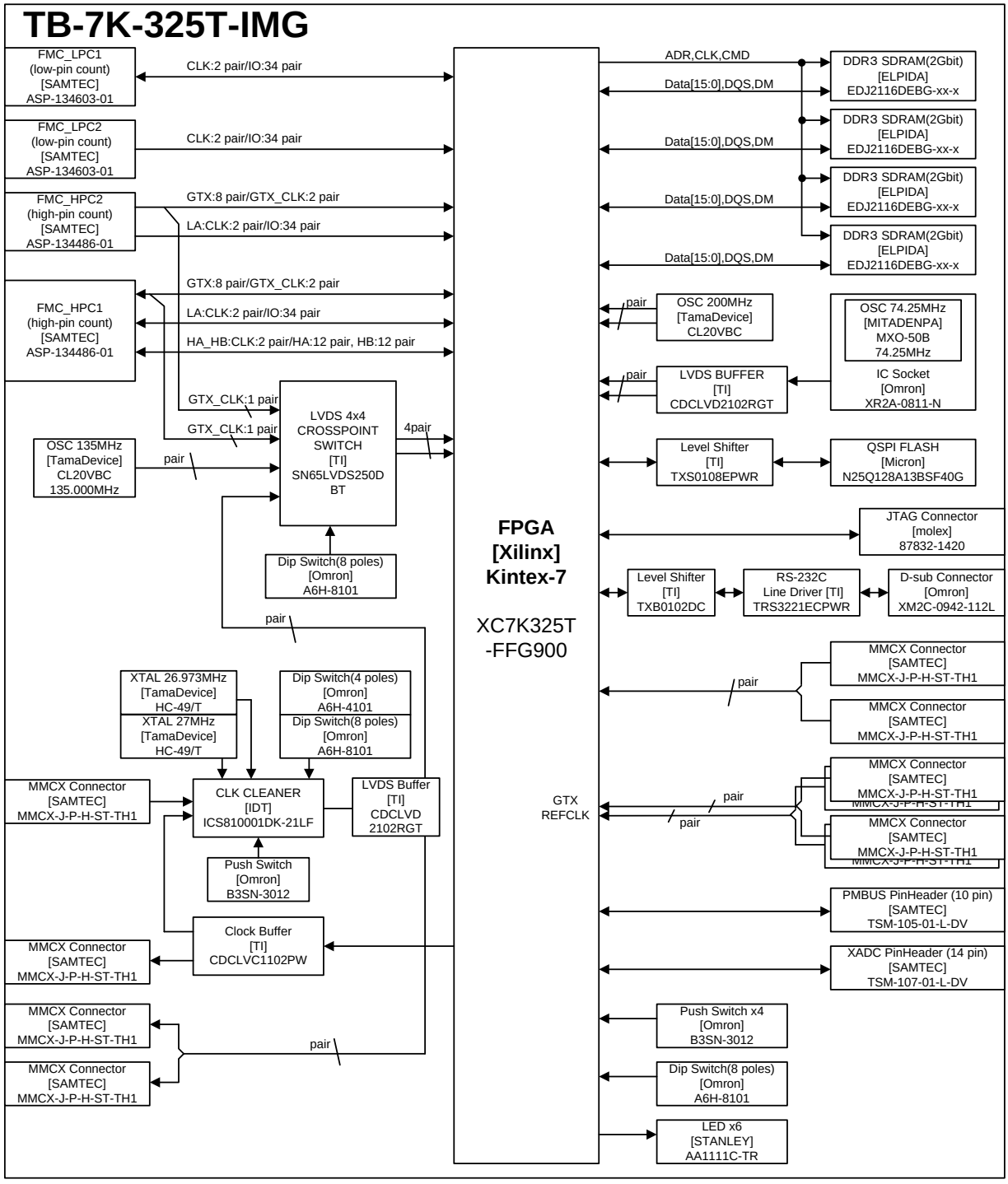

Figure 4-1 Block Diagram

5. External View of the Board

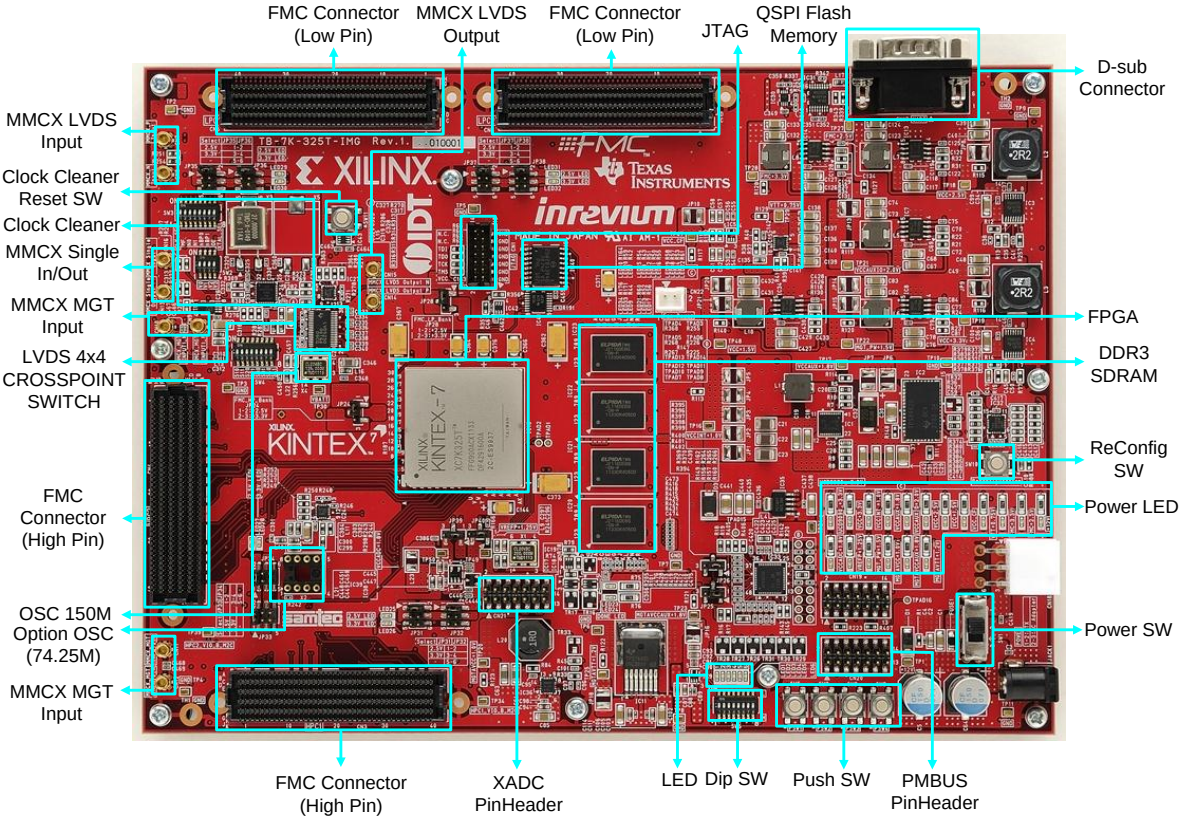

Figure 5-1 Top View of Board

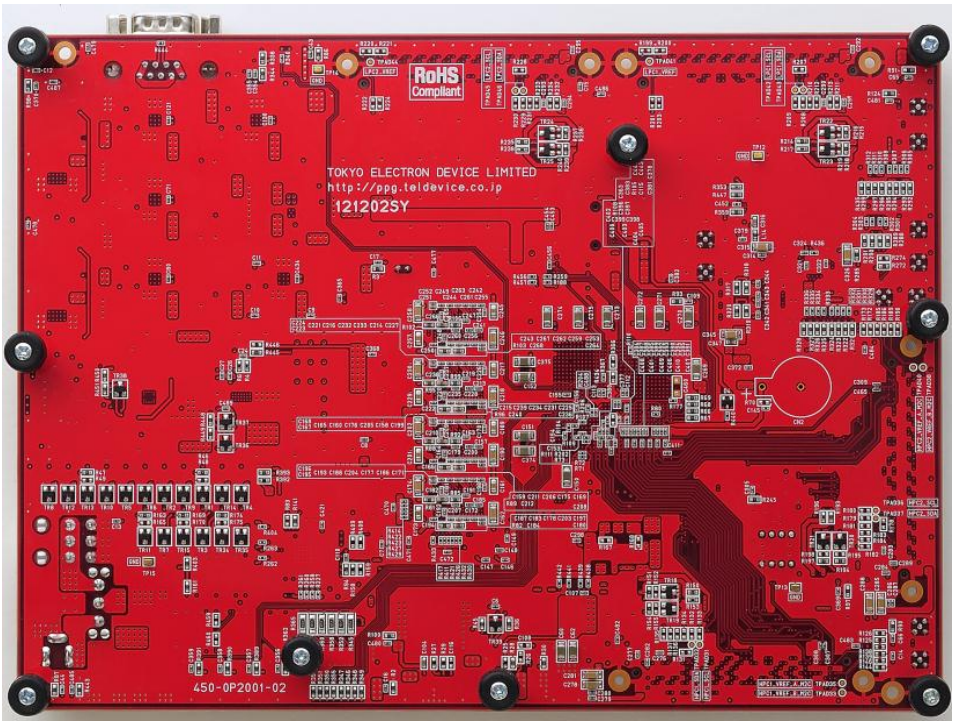

Figure 5-2 Bottom View of Board

6. Board Specifications

Figure 6-1 shows the board specifications.

External Dimensions: 240.0 mm (W) x 175.0 mm (H)
Number of Layers: 12 layers
Board Thickness: 1.6 mm
Material: FR-4

Unit: mm

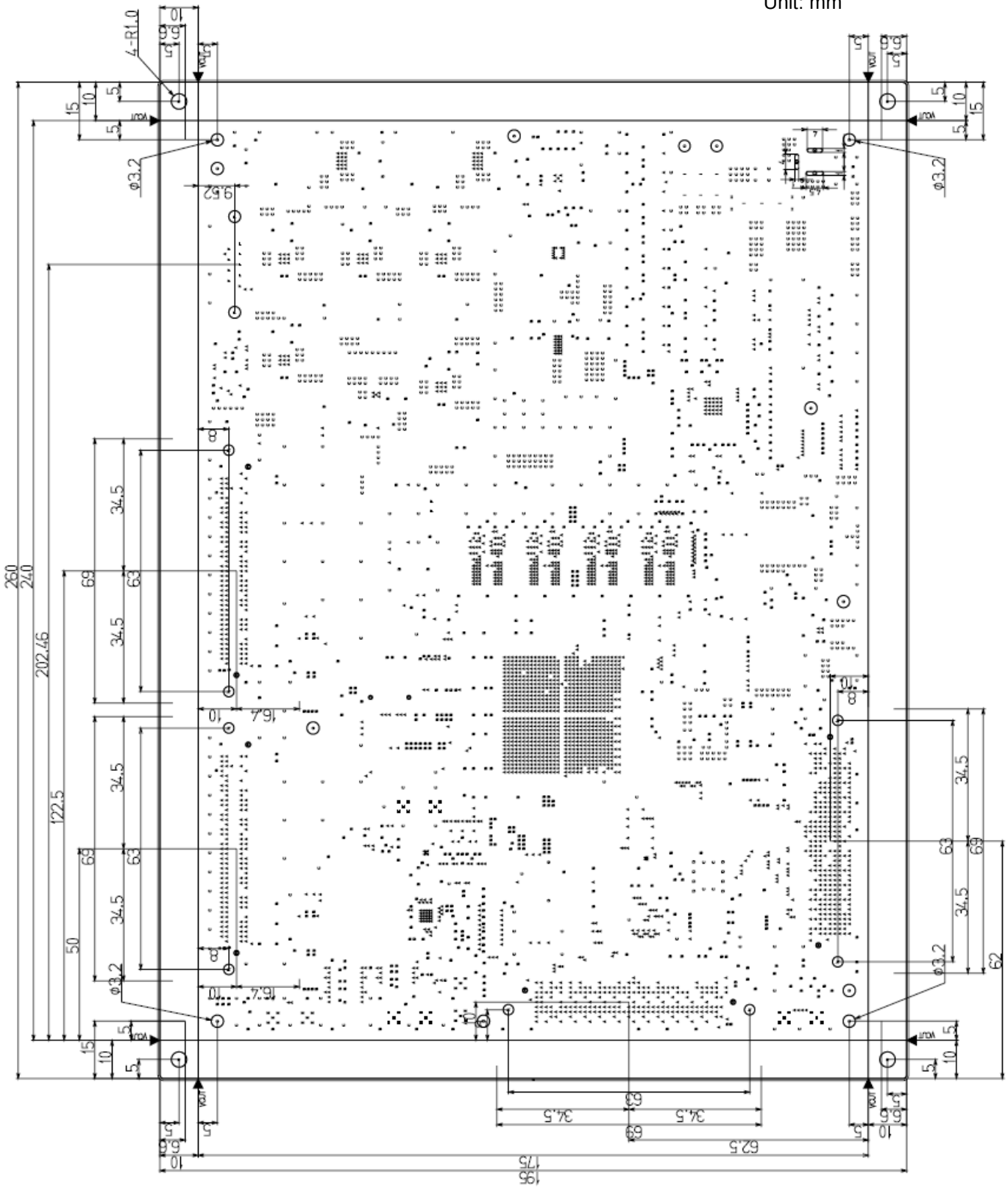

Figure 6-1 Board Dimensions (inclusive of wastable substrate)

7. Description of Components

This section described detail of each component and function.

7.1. Power Supply structure

Figure 7-1 shows a power supply circuit structure. TB-7K-325T-IMG has two power connecters for input 12V power. One is ATX type connector other one is DC JACK type connector. All of required voltages are made by on-board power circuit.

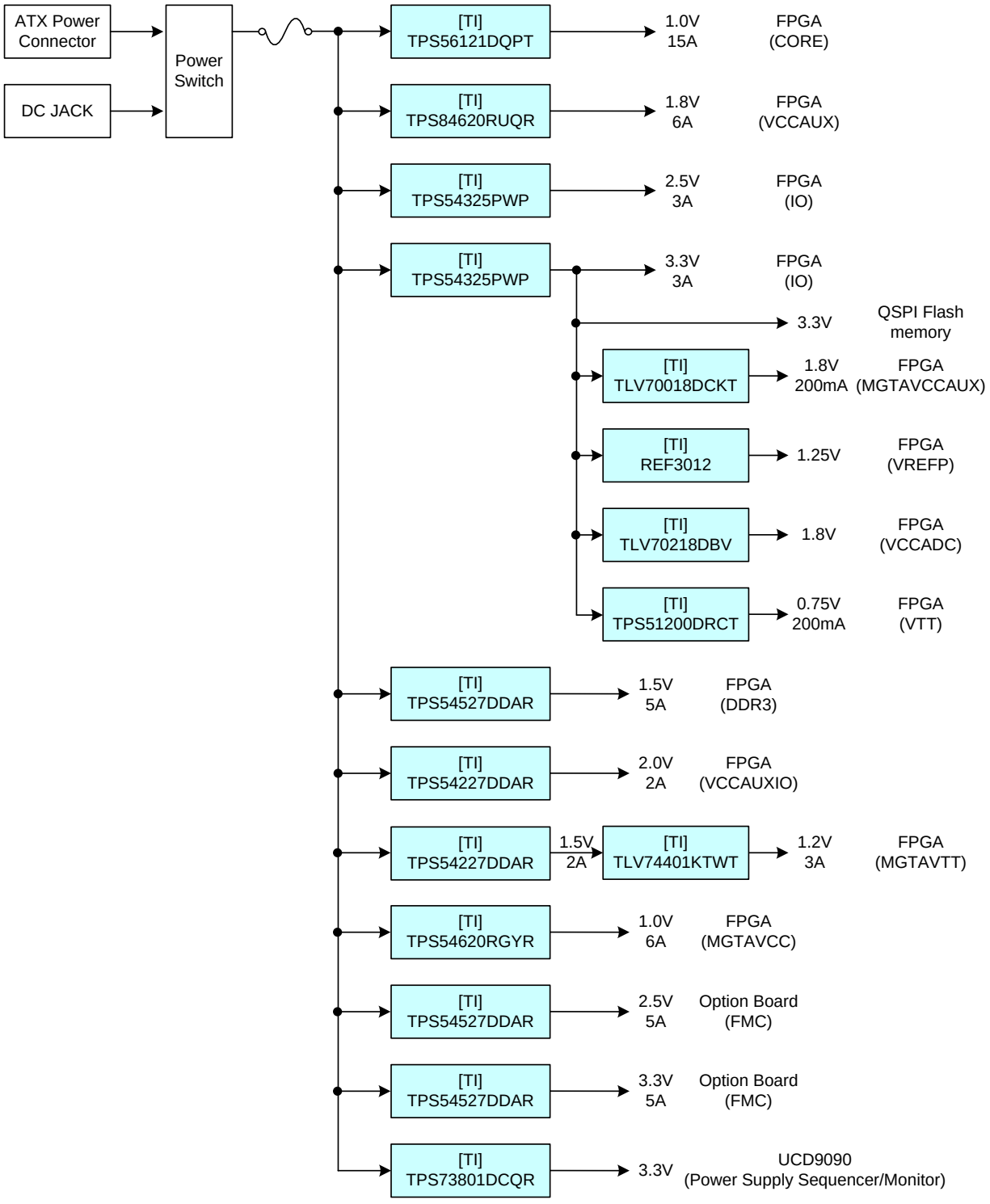

Figure 7-1 Power Supply Circuit Structure

7.1.1. Power Input connectors

TB-7K-325T-IMG has two power connectors, DC Jack or ATX power connector.

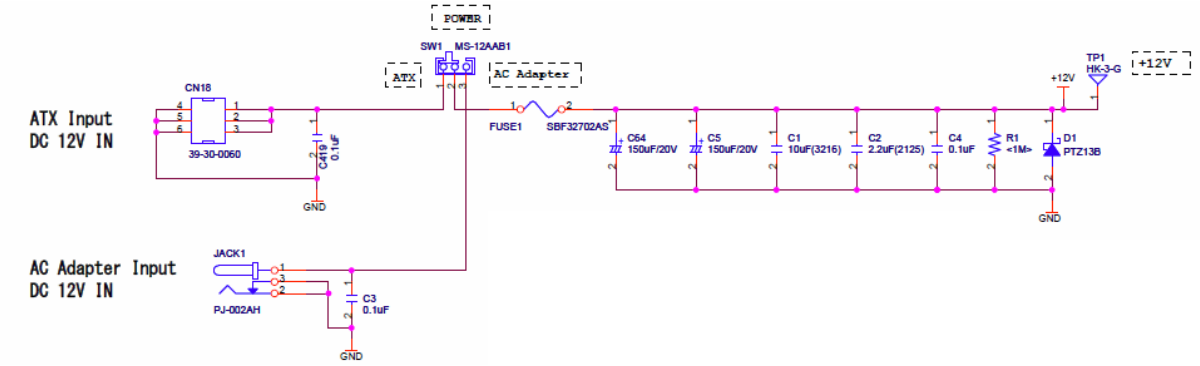

Figure 7-2 Power Input Circuit

7.1.2. Power supply circuit LEDs

All power circuits have an indicating LEDs. If LED is OFF or flashing, Power circuit has a problem.

Table 7-1 Power LED

Voltage	LED #	Power Supply for
VCCINT+1.0V	LED7	FPGA VCCINT
VCCAUXIO+2.0V	LED8	FPGA VCCAUX_IO
MGT_PW+1.5V	LED9	MGT AVTT
UCD9090_+3.3V	LED10	UCD9090RGZT
VCC+1.5V	LED11	FPGA VCCIO
VCC+2.5V	LED12	FPGA VCCIO
MGTAVCCAUX+1.8V	LED13	MGTAVCCAUX
FMC+2.5V	LED14	FMC 2.5V
VCCAUX+1.8V	LED15	FPGA VCCAUX
VCC_CF	LED16	QSPI Flash Memory
MGTAVTT+1.2V	LED17	MGTAVTT
FMC+3.3V	LED18	FMC 3.3V
VTT+0.75V	LED19	FPGA VREF(DDR3)
VCC+3.3V	LED20	FPGA VCCIO
MGTAVCC+1.0V	LED21	MGTAVCC
+12V	LED22	12V Master Power
VREFP+1.25V	LED33	FPGA VREFP
VCCADC+1.8V	LED34	FPGA VCCADC

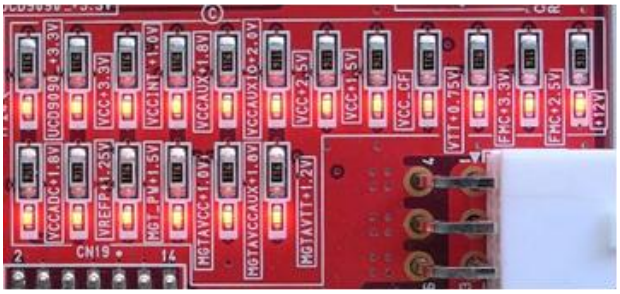

Figure 7-3 Power LED

7.1.3. FPGA Bank Voltage Selection

Various peripheral devices are connected to FPGA as shown in following figure. The FMC connectors allow the developers to select an appropriate FPGA Bank voltage(VCCIO) by setting the on-board jumpers(JP24, JP28) to meet the voltage requirements for the connected interfaces.

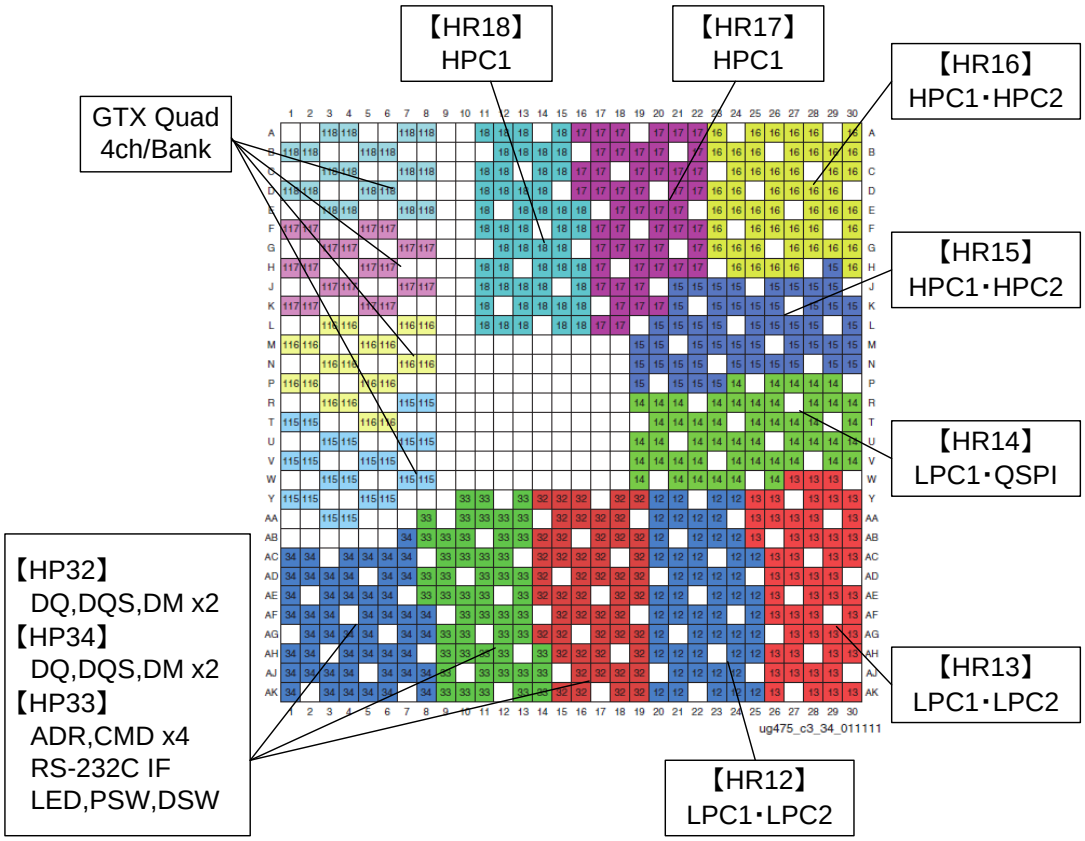

Figure 7-4 Bank Assign Overview

Table 7-2 Bank Voltage Settings

Bank #	Connected Peripherals	Voltage	Setting		
			JP #	2.5V	3.3V
HR12/13/14	FMC_LPC1(CN5) FMC_LPC2(CN6) QSPI	Selectable 3.3V, 2.5V	JP28	1-2 (Default)	2-3
HR15/16/17/18	FMC_HPC1(CN3) FMC_HPC2(CN4)	Selectable 3.3V, 2.5V	JP24	1-2 (Default)	2-3
HP32/33/34	DDR3,DSW,LED,PSW,UART	1.5V	—	—	—

Figure 7-5 IO Bank Voltage Jumpers

7.1.4. Power Supply for XADC

TB-7K-325T-IMG has two voltages for XADC. About XADC, please refer to Kintex-7 datasheet.
VCCADC is power supply of XADC Analog circuit.
VREFP is reference voltage for conversion of deferential signal .

Table 7-3 Setting of XACD Power

XADC Power	JP # and setting		Supplied power
VCCADC	JP39	Short 1-2	VCCAUX+1.8V
		Short 2-3	VCCADC+1.8V
VREFP	JP40	Short 1-2	XADC_AGND
		Short 2-3	VREFP+1.25V

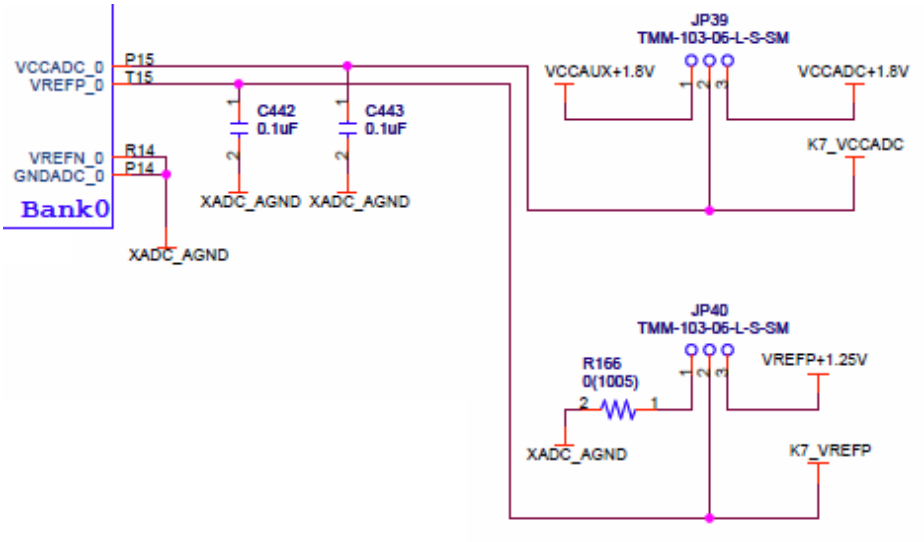

Figure 7-6 XADC Power Select Circuit

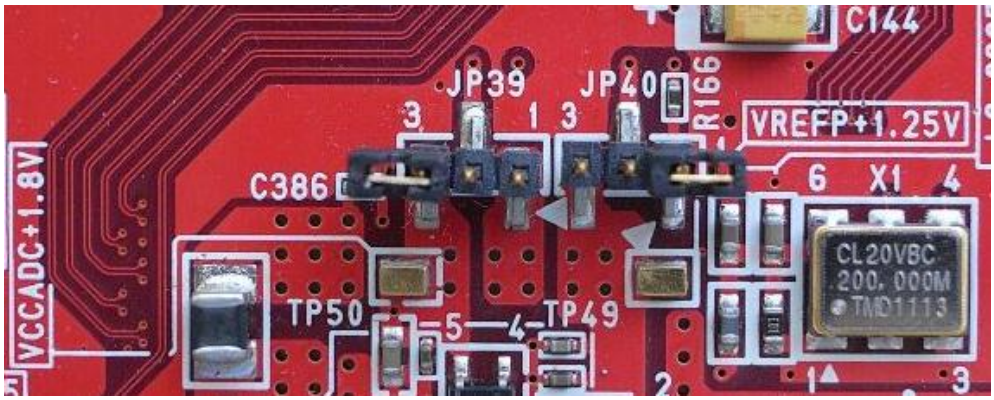

Figure 7-7 XADC Jumper setting

7.1.5. PM Bus interface (CN19)

PM bus interface is TI digital power device control bus interface. This board uses TI UCD9090 for power supply controller and it is programed all settings before shipping. For more details, please refer to UCD9090 and FPGA Power sequence.

7.2. Clock Structure

Figure 7-1 shows clock structure.

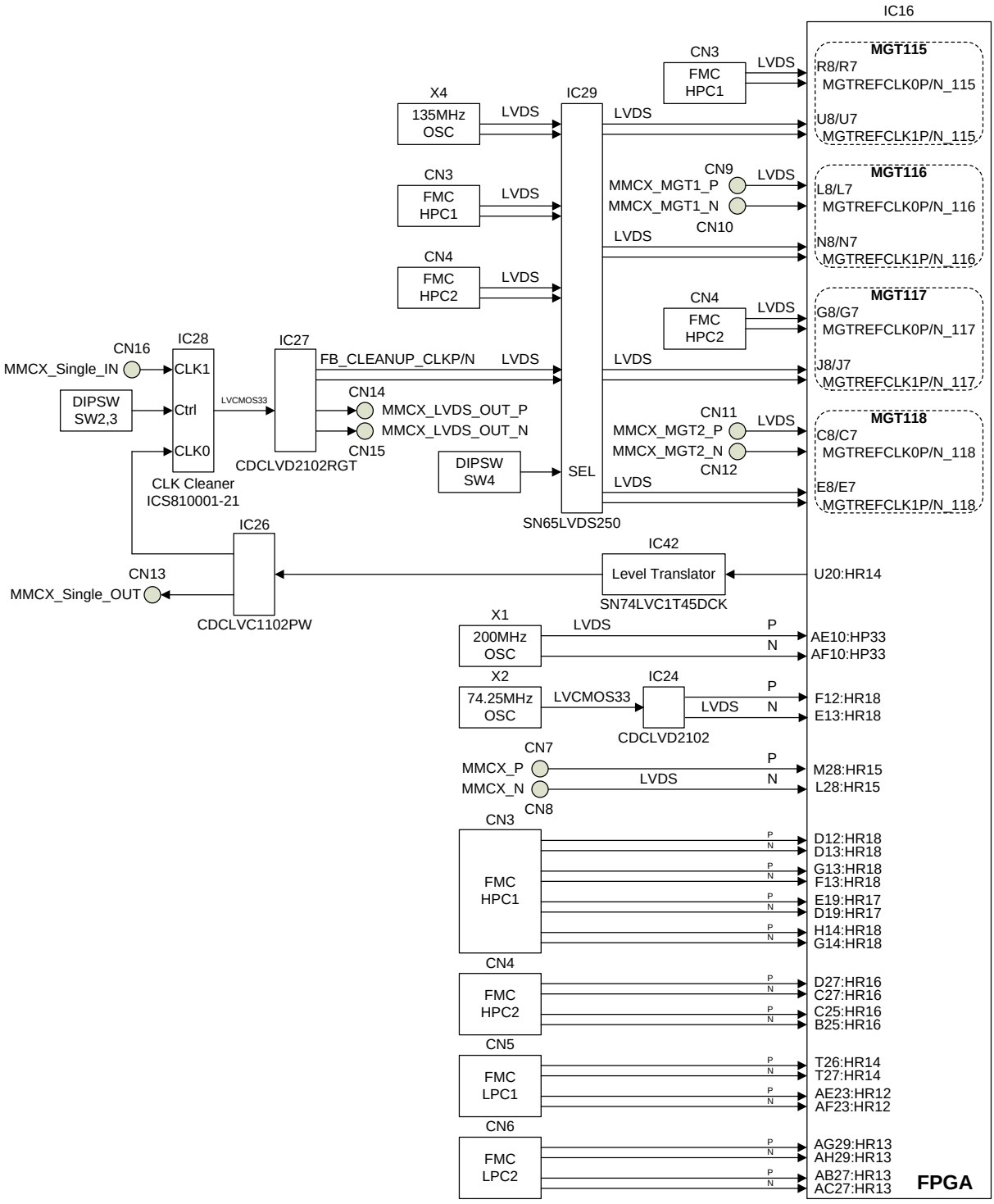

Figure 7-8 Clock Structure

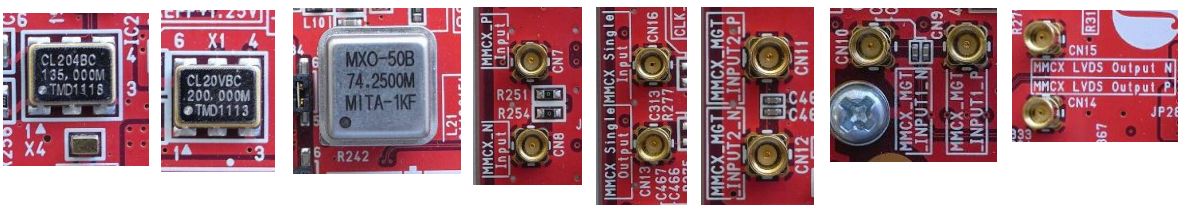

Figure 7-9 On Board Clock Sources and Connectors

Table 7-4 Clock Source Table

Connection	Signal Name	I/F	FPGA PIN	Note
X1(200MHz)	CLK200M_P/N	LVDS	AE10/AF10	For DDR3 (System, iodelayctrl)
X2(74.25MHz)	74.25MHz_P/N	LVDS	F12/E13	Via Single-end to Differential buffer
CN7/8	MMCX_P/N	LVDS	M28/L28	External Clock In
IC27 (FB_CLEANUP_CLKP/N), CN3 (HPC1_GBTCLK1_M2C_P/N), CN4 (HPC2_GBTCLK1_M2C_P/N) or X4(135MHz_P/N)	HPC_CLK_M115_P/N HPC_CLK_M116_P/N HPC_CLK_M117_P/N HPC_CLK_M118_P/N	LVDS	U8/U7 N8/N7 J8/J7 E8/E7	Reference clock of RocketIO
CN3(FMC_HPC1)	HPC1_GBTCLK0_M2C_P/N	LVDS	R8/R7	
CN4(FMC_HPC2)	HPC2_GBTCLK0_M2C_P/N	LVDS	G8/G7	
CN9/10 (MMCX, LVDS input)	MMCX_MGT1_P/N	LVDS	L8/L7	
CN11/12 (MMCX, LVDS input)	MMCX_MGT2_P/N	LVDS	C8/C7	
CN3(FMC_HPC1)	HPC1_CLK0_M2C_P/N	LVDS CMOS	D12/D13	HPC_LA I/F
CN3(FMC_HPC1)	HPC1_CLK1_M2C_P/N	LVDS CMOS	G13/F13	HPC_LA I/F
CN3(FMC_HPC1)	HPC1_CLK2_M2C_P/N	LVDS CMOS	E19/D19	HPC_HA_HB I/F
CN3(FMC_HPC1)	HPC1_CLK3_M2C_P/N	LVDS CMOS	H14/G14	HPC_HA_HB I/F
CN4(FMC_HPC2)	HPC2_CLK0_M2C_P/N	LVDS CMOS	D27/C27	HPC_LA I/F
CN4(FMC_HPC2)	HPC2_CLK1_M2C_P/N	LVDS CMOS	C25/B25	HPC_LA I/F
CN5(FMC_LPC1)	LPC1_CLK0_M2C_P/N	LVDS CMOS	T26/T27	LPC1 I/F
CN5(FMC_LPC1)	LPC1_CLK1_M2C_P/N	LVDS CMOS	AE23/AF23	LPC1 I/F
CN6(FMC_LPC2)	LPC2_CLK0_M2C_P/N	LVDS CMOS	AG29/AH29	LPC2 I/F
CN6(FMC_LPC2)	LPC2_CLK1_M2C_P/N	LVDS CMOS	AB27/AC27	LPC2 I/F

7.3. RocketIO Reference Clock

Following figure shows RocketIO Reference clock structure.

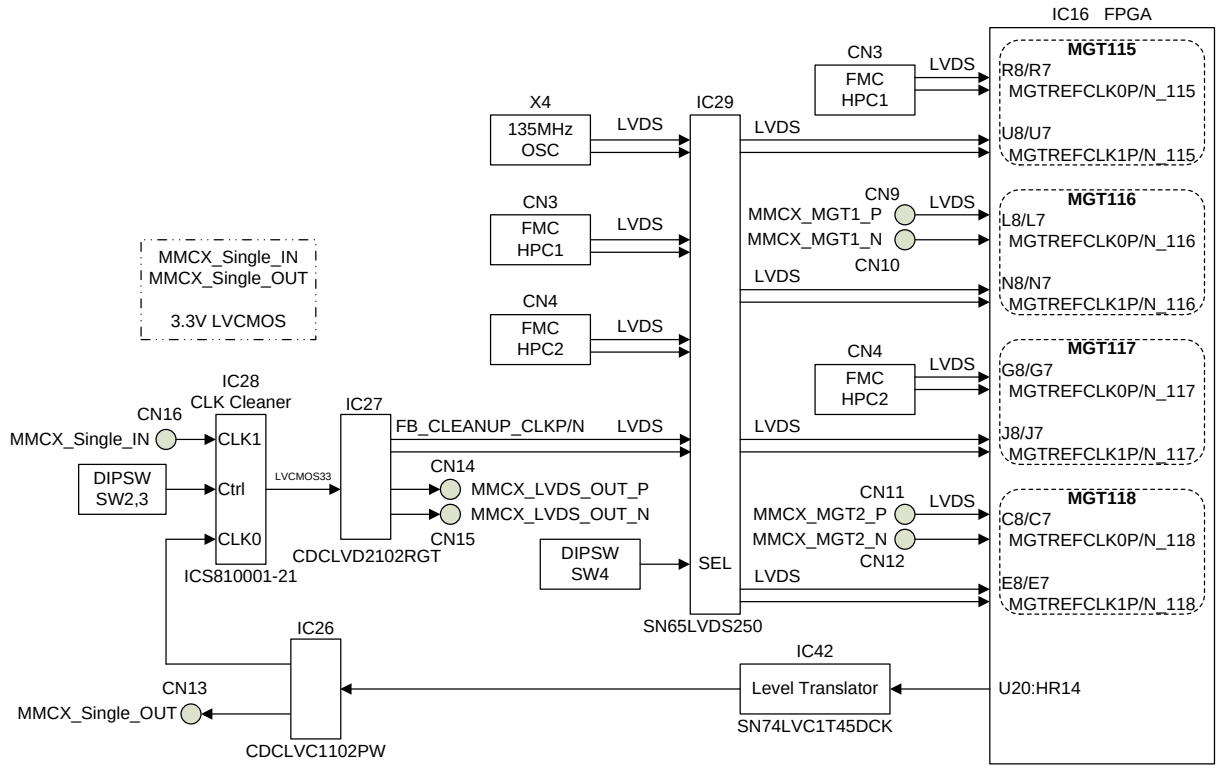

Figure 7-10 RocketIO Reference Clock Structure

7.3.1. FB_CLEANUP_CLP/N Signals

"FB_CLEANUP_CLKP/N" is differential input clock signal for the "SN65LVDS250DBT". This differential signal is converted from single-ended to differential by IC27. The single-ended clock is generated by the IDT video clock generator (ICS810001DK-21LF).

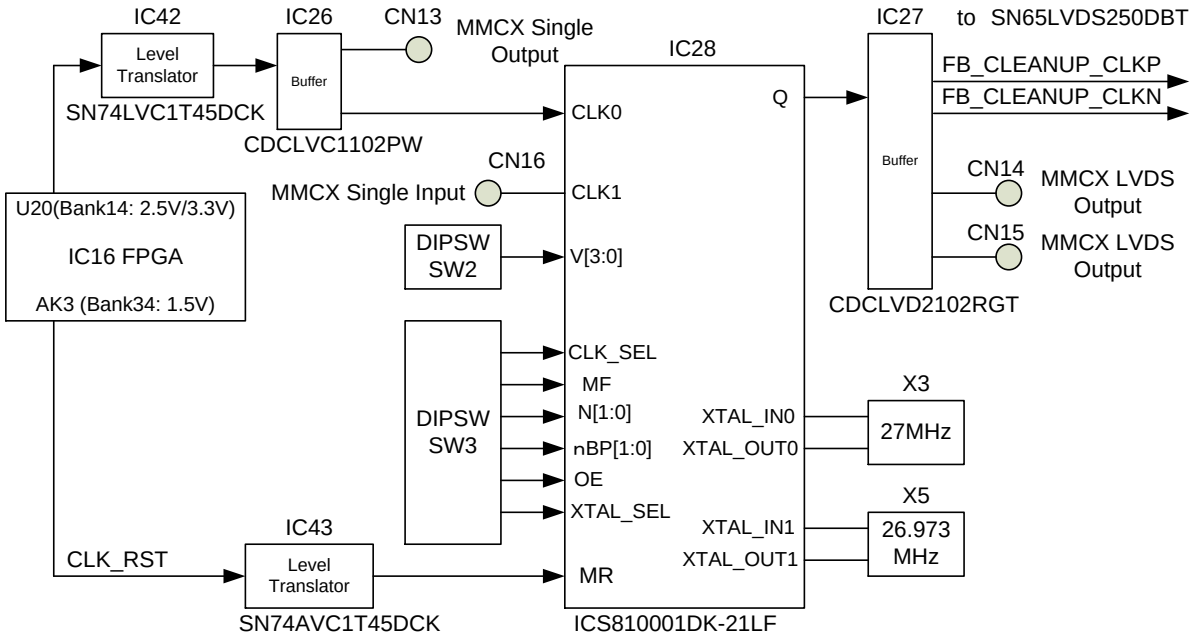

Figure 7-11 FB_CLEANUP_CLKP/N Circuit Block Diagram

7.3.2. Clock Generator (ISC810001DK-21LF)

TB-7K-325T-IMG provides an onboard video clock generation circuit using the IDT ICS810001DK-21LF. For details about setting clock frequencies, refer to the corresponding IDT data sheet.

This device accepts a clock sourced from the FPGA (U20 pin) or from an external MMCX connector (CN16). The clock source selection is made via DIP switch SW2. The user selects the output clock frequency generated by this IDT video clock generator PLL via DIP switch SW3. The XTAL_IN is connected a 27MHz and 26.973MHz oscillator. A reset to this device form FPGA (AK3 pin).

Table 7-5 Clock Generator(ISC810001DK-21F) setting

Signal	SW No.	SW bit	Functions
V[3:0]	SW2	bit[4:1]	Input Clock Settings Ex) bit[4:1] = All Off : V[3:0] = “1001”
CLK_SEL	SW3	bit[1]	Clock Select ON = MMCX OFF = FPGA
MF		bit[2]	PLL coefficient bit[2] = Off > MF = “0” bit[2] = On > MF = “1”
N[1:0]		bit[4:3]	Divide setting “00” = 4 “01” = 8 “10” = 12 “11” = 18
nBP[1:0]		bit[6:5]	Output clock settings Ex) Bit[6:5] = All Off > nBP[1:0] = “11”
OE		bit[7]	Output Clock Enable ON = Enable OFF = Disable
XTAL_SEL		bit[8]	Select X3(27MHz) or X5(26.973MHz) ON = 26.973MHz OFF = 27MHz

nBP[1:0] and OE have reversed ON/OFF setting in comparison with other bits.

It is recommended to set the bit to OFF when using this clock generator.

Output clock formula in nBP[1:0]=11(ON,ON): **Fout = (in_CLK / P) x M x MF / N**

Example: 148.5MHz output

Condition: Input clock: 27MHz (V[3:0]=ALL OFF=(P=1000)=(M=1000))

Setting: MF=OFF (x22), N[1:0]=OFF,OFF (divide-by-4 frequency)

7.3.3. RocketIO Reference Clock Selector

RocketIO reference clocks are selected by LVDS 4x4 cross-point switch IC29 (TI: SN65LVDS250DBT). 4 clock sources are selected by SW4.

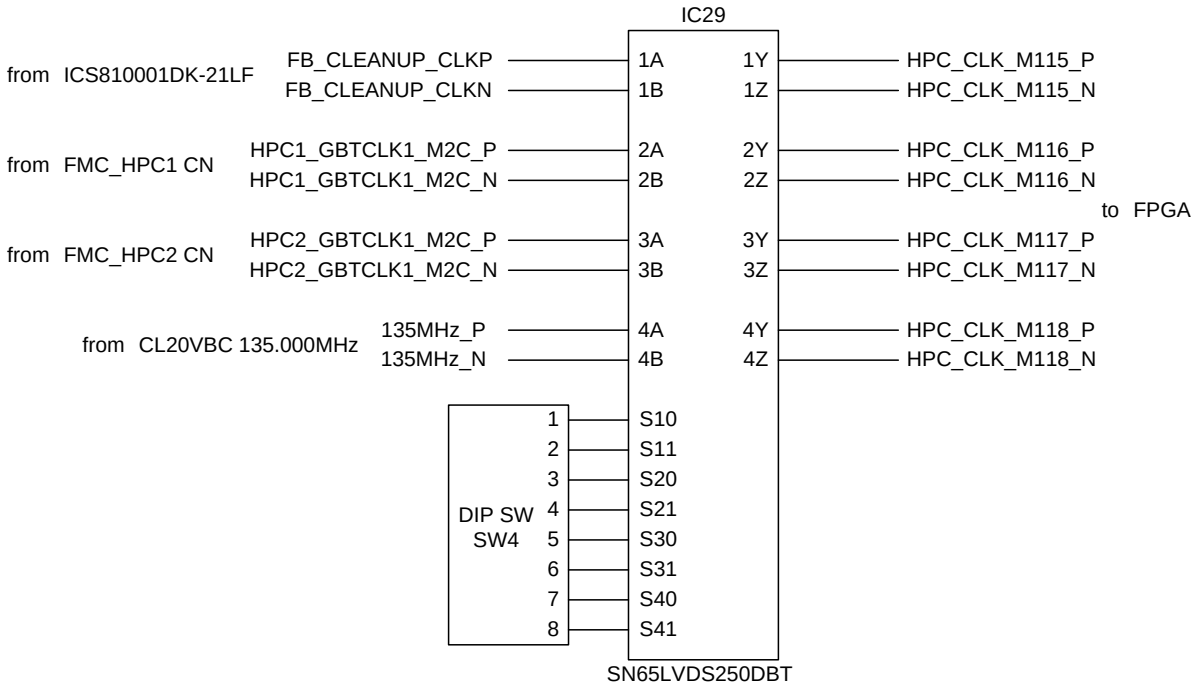

Figure 7-12 RocketIO Reference Clock Selector Block Diagram

Figure 7-13 RocketIO Reference Clock Setting Table

OUTPUT CHANNEL 1			OUTPUT CHANNEL 2			OUTPUT CHANNEL 3			OUTPUT CHANNEL 4		
S10	S11	1Y/1Z	S20	S21	2Y/2Z	S30	S31	3Y/3Z	S40	S41	4Y/4Z
OFF	OFF	1A/1B	OFF	OFF	1A/1B	OFF	OFF	1A/1B	OFF	OFF	1A/1B
OFF	ON	2A/2B	OFF	ON	2A/2B	OFF	ON	2A/2B	OFF	ON	2A/2B
ON	OFF	3A/3B	ON	OFF	3A/3B	ON	OFF	3A/3B	ON	OFF	3A/3B
ON	ON	4A/4B	ON	ON	4A/4B	ON	ON	4A/4B	ON	ON	4A/4B

For example: Selecting FB_CLEANUP_CLKP/N to HPC_CLK_M115/117_P/N and
HPC1_GBTCLK1_M2C_P/N to HPC_CLK_M1116/118_P/N.

SW4	
1 : OFF	2 : OFF
3 : OFF	4 : ON
5 : OFF	6 : OFF
7 : OFF	8 : ON

7.4. FMC connectors

TB-7K-325T-IMG has two HPC(CN3 and CN4) and two LPC(CN5, CN6).

Following figure is FMC standard pin assign.

All pin of each FMC connectors are not connected to FPGA. Please see related documentations and confirm that signals connections before using.

	K	J	H	G	F	E	D	C	B	A
1	VREF_B_M2C	GND	VREF_A_M2C	GND	PG_M2C	GND	PG_C2M	GND	RES1	GND
2	GND	CLK3_M2C_P	PRSNT_M2C_L	CLK1_M2C_P	GND	HA01_P_CC	GND	DP0_C2M_P	GND	DP1_M2C_P
3	GND	CLK3_M2C_N	GND	CLK1_M2C_N	GND	HA01_N_CC	GND	DP0_C2M_N	GND	DP1_M2C_N
4	CLK2_M2C_P	GND	CLK0_M2C_P	GND	HA00_P_CC	GND	GBTCLK0_M2C_P	GND	DP9_M2C_P	GND
5	CLK2_M2C_N	GND	CLK0_M2C_N	GND	HA00_N_CC	GND	GBTCLK0_M2C_N	GND	DP9_M2C_N	GND
6	GND	HA03_P	GND	LA00_P_CC	GND	HA05_P	GND	DP0_M2C_P	GND	DP2_M2C_P
7	HA02_P	HA03_N	LA02_P	LA00_N_CC	HA04_P	HA05_N	GND	DP0_M2C_N	GND	DP2_M2C_N
8	HA02_N	GND	LA02_N	GND	HA04_N	GND	LA01_P_CC	GND	DP8_M2C_P	GND
9	GND	HA07_P	GND	LA03_P	GND	HA09_P	LA01_N_CC	GND	DP8_M2C_N	GND
10	HA06_P	HA07_N	LA04_P	LA03_N	HA08_P	HA09_N	GND	LA06_P	GND	DP3_M2C_P
11	HA06_N	GND	LA04_N	GND	HA08_N	GND	LA05_P	LA06_N	GND	DP3_M2C_N
12	GND	HA11_P	GND	LA08_P	GND	HA13_P	LA05_N	GND	DP7_M2C_P	GND
13	HA10_P	HA11_N	LA07_P	LA08_N	HA12_P	HA13_N	GND	GND	DP7_M2C_N	GND
14	HA10_N	GND	LA07_N	GND	HA12_N	GND	LA09_P	LA10_P	GND	DP4_M2C_P
15	GND	HA14_P	GND	LA12_P	GND	HA16_P	LA09_N	LA10_N	GND	DP4_M2C_N
16	HA17_P_CC	HA14_N	LA11_P	LA12_N	HA15_P	HA16_N	GND	GND	DP6_M2C_P	GND
17	HA17_N_CC	GND	LA11_N	GND	HA15_N	GND	LA13_P	GND	DP6_M2C_N	GND
18	GND	HA18_P	GND	LA16_P	GND	HA20_P	LA13_N	LA14_P	GND	DP5_M2C_P
19	HA21_P	HA18_N	LA15_P	LA16_N	HA19_P	HA20_N	GND	LA14_N	GND	DP5_M2C_N
20	HA21_N	GND	LA15_N	GND	HA19_N	GND	LA17_P_CC	GND	GBTCLK1_M2C_P	GND
21	GND	HA22_P	GND	LA20_P	GND	HB03_P	LA17_N_CC	GND	GBTCLK1_M2C_N	GND
22	HA23_P	HA22_N	LA19_P	LA20_N	HB02_P	HB03_N	GND	LA18_P_CC	GND	DP1_C2M_P
23	HA23_N	GND	LA19_N	GND	HB02_N	GND	LA23_P	LA18_N_CC	GND	DP1_C2M_N
24	GND	HB01_P	GND	LA22_P	GND	HB05_P	LA23_N	GND	DP9_C2M_P	GND
25	HB00_P_CC	HB01_N	LA21_P	LA22_N	HB04_P	HB05_N	GND	GND	DP9_C2M_N	GND
26	HB00_N_CC	GND	LA21_N	GND	HB04_N	GND	LA26_P	LA27_P	GND	DP2_C2M_P
27	GND	HB07_P	GND	LA25_P	GND	HB09_P	LA26_N	LA27_N	GND	DP2_C2M_N
28	HB06_P_CC	HB07_N	LA24_P	LA25_N	HB08_P	HB09_N	GND	GND	DP8_C2M_P	GND
29	HB06_N_CC	GND	LA24_N	GND	HB08_N	GND	TCK	GND	DP8_C2M_N	GND
30	GND	HB11_P	GND	LA29_P	GND	HB13_P	TDI	SCL	GND	DP3_C2M_P
31	HB10_P	HB11_N	LA28_P	LA29_N	HB12_P	HB13_N	TDO	SDA	GND	DP3_C2M_N
32	HB10_N	GND	LA28_N	GND	HB12_N	GND	3P3VAUX	GND	DP7_C2M_P	GND
33	GND	HB15_P	GND	LA31_P	GND	HB19_P	TMS	GND	DP7_C2M_N	GND
34	HB14_P	HB15_N	LA30_P	LA31_N	HB16_P	HB19_N	TRST_L	GA0	GND	DP4_C2M_P
35	HB14_N	GND	LA30_N	GND	HB16_N	GND	GA1	12P0V	GND	DP4_C2M_N
36	GND	HB18_P	GND	LA33_P	GND	HB21_P	3P3V	GND	DP6_C2M_P	GND
37	HB17_P_CC	HB18_N	LA32_P	LA33_N	HB20_P	HB21_N	GND	12P0V	DP6_C2M_N	GND
38	HB17_N_CC	GND	LA32_N	GND	HB20_N	GND	3P3V	GND	GND	DP5_C2M_P
39	GND	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	DP5_C2M_N
40	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	RES0	GND
			LPC Connector	LPC Connector			LPC Connector	LPC Connector		

Figure 7-14 High Pin Count

	K	J	H	G	F	E	D	C	B	A
1	NC	NC	VREF_A_M2C	GND	NC	NC	PG_C2M	GND	NC	NC
2	NC	NC	PRSNT_M2C_L	CLK1_M2C_P	NC	NC	GND	DP0_C2M_P	NC	NC
3	NC	NC	GND	CLK1_M2C_N	NC	NC	GND	DP0_C2M_N	NC	NC
4	NC	NC	CLK0_M2C_P	GND	NC	NC	GBTCLK0_M2C_P	GND	NC	NC
5	NC	NC	CLK0_M2C_N	GND	NC	NC	GBTCLK0_M2C_N	GND	NC	NC
6	NC	NC	GND	LA00_P_CC	NC	NC	GND	DP0_M2C_P	NC	NC
7	NC	NC	LA02_P	LA00_N_CC	NC	NC	GND	DP0_M2C_N	NC	NC
8	NC	NC	LA02_N	GND	NC	NC	LA01_P_CC	GND	NC	NC
9	NC	NC	GND	LA03_P	NC	NC	LA01_N_CC	GND	NC	NC
10	NC	NC	LA04_P	LA03_N	NC	NC	GND	LA06_P	NC	NC
11	NC	NC	LA04_N	GND	NC	NC	LA05_P	LA06_N	NC	NC
12	NC	NC	GND	LA08_P	NC	NC	LA05_N	GND	NC	NC
13	NC	NC	LA07_P	LA08_N	NC	NC	GND	GND	NC	NC
14	NC	NC	LA07_N	GND	NC	NC	LA09_P	LA10_P	NC	NC
15	NC	NC	GND	LA12_P	NC	NC	LA09_N	LA10_N	NC	NC
16	NC	NC	LA11_P	LA12_N	NC	NC	GND	GND	NC	NC
17	NC	NC	LA11_N	GND	NC	NC	LA13_P	GND	NC	NC
18	NC	NC	GND	LA16_P	NC	NC	LA13_N	LA14_P	NC	NC
19	NC	NC	LA15_P	LA16_N	NC	NC	GND	LA14_N	NC	NC
20	NC	NC	LA15_N	GND	NC	NC	LA17_P_CC	GND	NC	NC
21	NC	NC	GND	LA20_P	NC	NC	LA17_N_CC	GND	NC	NC
22	NC	NC	LA19_P	LA20_N	NC	NC	GND	LA18_P_CC	NC	NC
23	NC	NC	LA19_N	GND	NC	NC	LA23_P	LA18_N_CC	NC	NC
24	NC	NC	GND	LA22_P	NC	NC	LA23_N	GND	NC	NC
25	NC	NC	LA21_P	LA22_N	NC	NC	GND	GND	NC	NC
26	NC	NC	LA21_N	GND	NC	NC	LA26_P	LA27_P	NC	NC
27	NC	NC	GND	LA25_P	NC	NC	LA26_N	LA27_N	NC	NC
28	NC	NC	LA24_P	LA25_N	NC	NC	GND	GND	NC	NC
29	NC	NC	LA24_N	GND	NC	NC	TCK	GND	NC	NC
30	NC	NC	GND	LA29_P	NC	NC	TDI	SCL	NC	NC
31	NC	NC	LA28_P	LA29_N	NC	NC	TDO	SDA	NC	NC
32	NC	NC	LA28_N	GND	NC	NC	3P3VAUX	GND	NC	NC
33	NC	NC	GND	LA31_P	NC	NC	TMS	GND	NC	NC
34	NC	NC	LA30_P	LA31_N	NC	NC	TRST_L	GA0	NC	NC
35	NC	NC	LA30_N	GND	NC	NC	GA1	12P0V	NC	NC
36	NC	NC	GND	LA33_P	NC	NC	3P3V	GND	NC	NC
37	NC	NC	LA32_P	LA33_N	NC	NC	GND	12P0V	NC	NC
38	NC	NC	LA32_N	GND	NC	NC	3P3V	GND	NC	NC
39	NC	NC	GND	VADJ	NC	NC	GND	3P3V	NC	NC
40	NC	NC	VADJ	GND	NC	NC	3P3V	GND	NC	NC
			LPC Connector	LPC Connector			LPC Connector	LPC Connector		

Figure 7-15 Low Pin Count

7.4.1. FMC HPC1(CN3)

HPC1 connects a following number of signals to FPGA.

High Speed: 8 ch(TX), 8 ch(TX) and 2 pair clocks

Low Speed: LA 68(signal-end) and 2 pair clocks.
HA 24(single-end) and 2 pair clocks(common of HA/HB)
HB 24(single-end)

Notice: HA05_P/N, HA13_P/N, HB04_P/N and HB05_P/N cannot be differential interface.(only single-end). This limitation is related FPGA IO specification.

Table 7-6 HPC1(CN3) Pin Assign Table

Bank#	Pin#	A		B	Pin#	Bank#
		GND	1	RES1		
MGTXRXP1_115	Y6	DP1_M2C_P	2	GND		
MGTXRXN1_115	Y5	DP1_M2C_N	3	GND		
		GND	4	DP9_M2C_P		
		GND	5	DP9_M2C_N		
MGTXRXP2_115	W4	DP2_M2C_P	6	GND		
MGTXRXN2_115	W3	DP2_M2C_N	7	GND		
		GND	8	DP8_M2C_P		
		GND	9	DP8_M2C_N		
MGTXRXP3_115	V6	DP3_M2C_P	10	GND		
MGTXRXN3_115	V5	DP3_M2C_N	11	GND		
		GND	12	DP7_M2C_P	M6	MGTXRXP3_116
		GND	13	DP7_M2C_N	M5	MGTXRXN3_116
MGTXRXP0_116	T6	DP4_M2C_P	14	GND		
MGTXRXN0_116	T5	DP4_M2C_N	15	GND		
		GND	16	DP6_M2C_P	P6	MGTXRXP2_116
		GND	17	DP6_M2C_N	P5	MGTXRXN2_116
MGTXRXP1_116	R4	DP5_M2C_P	18	GND		
MGTXRXN1_116	R3	DP5_M2C_N	19	GND		
		GND	20	*1 GBTCLK1_M2C_P	*1	*1
		GND	21	*1 GBTCLK1_M2C_N	*1	*1
MGTXTXP1_115	V2	DP1_C2M_P	22	GND		
MGTXTXN1_115	V1	DP1_C2M_N	23	GND		
		GND	24	DP9_C2M_P		
		GND	25	DP9_C2M_N		
MGTXTXP2_115	U4	DP2_C2M_P	26	GND		
MGTXTXN2_115	U3	DP2_C2M_N	27	GND		
		GND	28	DP8_C2M_P		
		GND	29	DP8_C2M_N		
MGTXTXP3_115	T2	DP3_C2M_P	30	GND		
MGTXTXN3_115	T1	DP3_C2M_N	31	GND		
		GND	32	DP7_C2M_P	L4	MGTXTXP3_116
		GND	33	DP7_C2M_N	L3	MGTXTXN3_116
MGTXTXP0_116	P2	DP4_C2M_P	34	GND		
MGTXTXN0_116	P1	DP4_C2M_N	35	GND		
		GND	36	DP6_C2M_P	M2	MGTXTXP2_116
		GND	37	DP6_C2M_N	M1	MGTXTXN2_116
MGTXTXP1_116	N4	DP5_C2M_P	38	GND		
MGTXTXN1_116	N3	DP5_C2M_N	39	GND		
		GND	40	RES0		

Bank#	Pin#	C		D	Pin#	Bank#
		GND	1	*5 PG_C2M		
MGTXTXP0_115	Y2	DP0_C2M_P	2	GND		
MGTXTXN0_115	Y1	DP0_C2M_N	3	GND		
		GND	4	GBTCLK0_M2C_P	R8	MGTREFCLK0P_115
		GND	5	GBTCLK0_M2C_N	R7	MGTREFCLK0N_115
MGTXRXP0_115	AA4	DP0_M2C_P	6	GND		
MGTXRXN0_115	AA3	DP0_M2C_N	7	GND		
		GND	8	LA01_P_CC	H15	18
		GND	9	LA01_N_CC	G15	18
18	F15	LA06_P	10	GND		
18	E16	LA06_N	11	LA05_P	D11	18
		GND	12	LA05_N	C11	18
		GND	13	GND		
17	B18	LA10_P	14	LA09_P	E14	18
17	A18	LA10_N	15	LA09_N	E15	18
		GND	16	GND		
		GND	17	LA13_P	A16	17
17	C17	LA14_P	18	LA13_N	A17	17
17	B17	LA14_N	19	GND		
		GND	20	LA17_P_CC	D17	17
		GND	21	LA17_N_CC	D18	17
17	D16	LA18_P_CC	22	GND		
17	C16	LA18_N_CC	23	LA23_P	G18	17
		GND	24	LA23_N	F18	17
		GND	25	GND		
17	G17	LA27_P	26	LA26_P	J16	18
17	F17	LA27_N	27	LA26_N	H16	18
		GND	28	GND		
		GND	29	TCK		
		*2 SCL	30	*4 TDI		
		*2 SDA	31	*4 TDO		
		GND	32	*6 3P3VAUX		
		GND	33	TMS		
		*3 GA0	34	TRST_L		
		*6 12P0V	35	*3 GA1		
		GND	36	*6 3P3V		
		*6 12P0V	37	GND		
		GND	38	*6 3P3V		
		*6 3P3V	39	GND		
		GND	40	*6 3P3V		

Bank#	Pin#	E		F	Pin#	Bank#
		GND	1	*5 PG M2C		
18	L16	HA01_P_CC	2	GND		
18	K16	HA01_N_CC	3	GND		
		GND	4	HA00_P_CC	F21	17
		GND	5	HA00_N_CC	E21	17
18	G12	HA05_P	6	GND		
18	F16	HA05_N	7	HA04_P	H11	18
		GND	8	HA04_N	H12	18
18	K14	HA09_P	9	GND		
18	J14	HA09_N	10	HA08_P	K13	18
		GND	11	HA08_N	J13	18
17	G19	HA13_P	12	GND		
17	E18	HA13_N	13	HA12_P	L15	18
		GND	14	HA12_N	K15	18
	-	HA16_P	15	GND		
	-	HA16_N	16	HA15_P	-	
		GND	17	HA15_N	-	
	-	HA20_P	18	GND		
	-	HA20_N	19	HA19_P	-	
		GND	20	HA19_N	-	
16	F25	HB03_P	21	GND		
16	E25	HB03_N	22	HB02_P	F26	16
		GND	23	HB02_N	E26	16
16	F23	HB05_P	24	GND		
16	G25	HB05_N	25	HB04_P	M19	15
		GND	26	HB04_N	P19	15
16	H24	HB09_P	27	GND		
16	H25	HB09_N	28	HB08_P	E24	16
		GND	29	HB08_N	D24	16
15	M22	HB13_P	30	GND		
15	M23	HB13_N	31	HB12_P	E23	16
		GND	32	HB12_N	D23	16
	-	HB19_P	33	GND		
	-	HB19_N	34	HB16_P	-	
		GND	35	HB16_N	-	
	-	HB21_P	36	GND		
	-	HB21_N	37	HB20_P	-	
		GND	38	HB20_N	-	
		*6 VADJ	39	GND		
		GND	40	*6 VADJ		

Bank#	Pin#	G		H	Pin#	Bank#
		GND	1	*7 VREF_A_M2C		
18	G13	CLK1_M2C_P	2	*5 PRSNT_M2C_L		
18	F13	CLK1_M2C_N	3	GND		
		GND	4	CLK0_M2C_P	D12	18
		GND	5	CLK0_M2C_N	D13	18
18	F11	LA00_P_CC	6	GND		
18	E11	LA00_N_CC	7	LA02_P	B14	18
		GND	8	LA02_N	A15	18
17	D22	LA03_P	9	GND		
17	C22	LA03_N	10	LA04_P	A11	18
		GND	11	LA04_N	A12	18
17	B22	LA08_P	12	GND		
17	A22	LA08_N	13	LA07_P	C15	18
		GND	14	LA07_N	B15	18
17	D21	LA12_P	15	GND		
17	C21	LA12_N	16	LA11_P	D14	18
		GND	17	LA11_N	C14	18
17	A20	LA16_P	18	GND		
17	A21	LA16_N	19	LA15_P	B13	18
		GND	20	LA15_N	A13	18
17	C20	LA20_P	21	GND		
17	B20	LA20_N	22	LA19_P	J17	17
		GND	23	LA19_N	H17	17
17	C19	LA22_P	24	GND		
17	B19	LA22_N	25	LA21_P	K18	17
		GND	26	LA21_N	J18	17
17	G22	LA25_P	27	GND		
17	F22	LA25_N	28	LA24_P	J19	17
		GND	29	LA24_N	H19	17
17	H21	LA29_P	30	GND		
17	H22	LA29_N	31	LA28_P	F20	17
		GND	32	LA28_N	E20	17
18	C12	LA31_P	33	GND		
18	B12	LA31_N	34	LA30_P	L17	17
		GND	35	LA30_N	L18	17
17	K19	LA33_P	36	GND		
17	K20	LA33_N	37	LA32_P	H20	17
		GND	38	LA32_N	G20	17
		*6 VADJ	39	GND		
		GND	40	*6 VADJ		

Bank#	Pin#	J		K	Pin#	Bank#
		GND	1	*7 VREF_B_M2C		
18	H14	CLK3_M2C_P	2	GND		
18	G14	CLK3_M2C_N	3	GND		
		GND	4	CLK2_M2C_P	E19	17
		GND	5	CLK2_M2C_N	D19	17
	-	HA03_P	6	GND		
	-	HA03_N	7	HA02_P	J11	18
		GND	8	HA02_N	J12	18
	-	HA07_P	9	GND		
	-	HA07_N	10	HA06_P	L12	18
		GND	11	HA06_N	L13	18
	-	HA11_P	12	GND		
	-	HA11_N	13	HA10_P	L11	18
		GND	14	HA10_N	K11	18
	-	HA14_P	15	GND		
	-	HA14_N	16	HA17_P_CC	B23	16
		GND	17	HA17_N_CC	A23	16
	-	HA18_P	18	GND		
	-	HA18_N	19	HA21_P	-	
		GND	20	HA21_N	-	
	-	HA22_P	21	GND		
	-	HA22_N	22	HA23_P	-	
		GND	23	HA23_N	-	
	-	HB01_P	24	GND		
	-	HB01_N	25	HB00_P_CC	G23	16
		GND	26	HB00_N_CC	G24	16
	-	HB07_P	27	GND		
	-	HB07_N	28	HB06_P_CC	B27	16
		GND	29	HB06_N_CC	A27	16
	-	HB11_P	30	GND		
	-	HB11_N	31	HB10_P	A25	16
		GND	32	HB10_N	A26	16
	-	HB15_P	33	GND		
	-	HB15_N	34	HB14_P	C24	16
		GND	35	HB14_N	B24	16
	-	HB18_P	36	GND		
	-	HB18_N	37	HB17_P_CC	-	
		GND	38	HB17_N_CC	-	
		*8 VIO_B_M2C	39	GND		
		GND	40	*8 VIO_B_M2C		

*1: GBTCLK1_M2C_P/N can be assigned to reference clock of 4 MGT tiles by IC29.
For more details, please refer to 7.3. RocketIO Reference Clock.

* 2 SCL, SDA

The board provides test points (with pull-up resistors pad) to enable I2C communications with the FPGA mezzanine card.

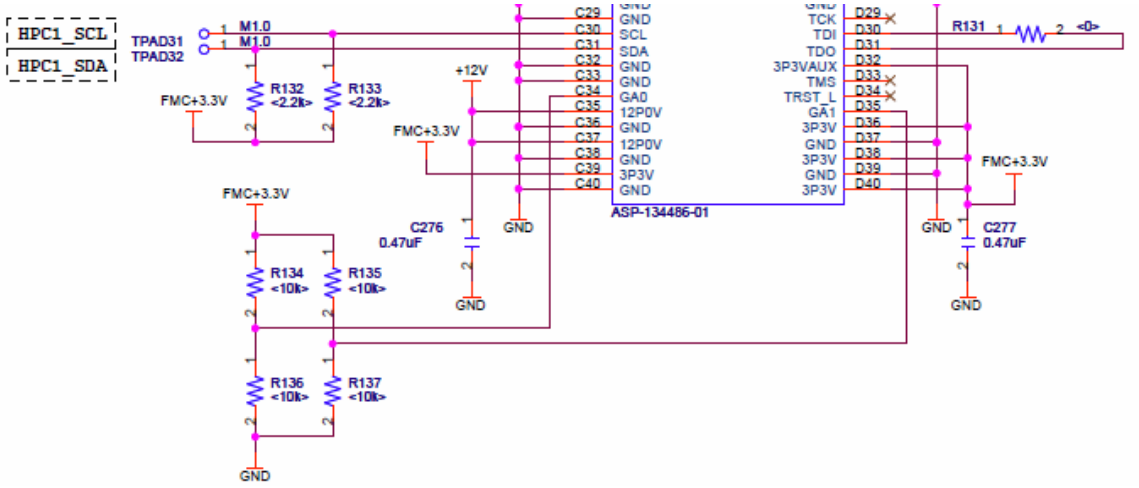

Figure 7-16 HPC1 SDC/SCL, GA1/0, TDI/TDO connection

* 3 GA[1:0]

The board has the above circuit design for notification of an ID to the FPGA mezzanine card. By default, it is set to opne.

* 4 TDI,TDO

The board provides a loopback structure for JTAG communication from the FPGA mezzanine card. By default, this loopback function is not provided because the R131 resistor is not installed.

* 5 PG_C2M, PG_M2C, PRSNT_M2C_L

The board provides a structure to output to the FPGA mezzanine card. It also provides a similar structure for the column of F and H pins of the FMC connector. By default, it is set to open. The PG_M2C, PRSNT_M2C_L also has a similar structure.

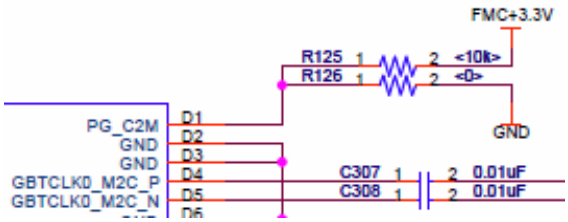

Figure 7-17 HPC1 PG_C2M connection

Table 7-7 HPC1 PG_C2M, PG_M2C, PRSNT_M2C_L Level settings

Pin#	Signal	Setting	
		H (Pull-up)	L (Pull-down)
D1	PG_C2M	R125	R126
F1	PG_M2C	R138	R139
H2	PRSNT_M2C_L	R146	R144

* 6 Power Supply

The board provides a 12V output to the 12P0V pin and a 3.3V output to the 3P3V and 3P3VAUX pins. 3.3V and 2.5V output are also selectable for VADJ pins as shown in the following circuit diagram. The HPC_VADJ voltage supply is set by jumping across the identical pins on jumpers JP31 and JP32. The power status can be monitored by the adjacent LED. By default, JP31 and JP32 are shorted 5-6.

Caution:

Do not jumper more than two portions of JP31 and JP32.

Always jumper the same pins of both JP31 and JP32.

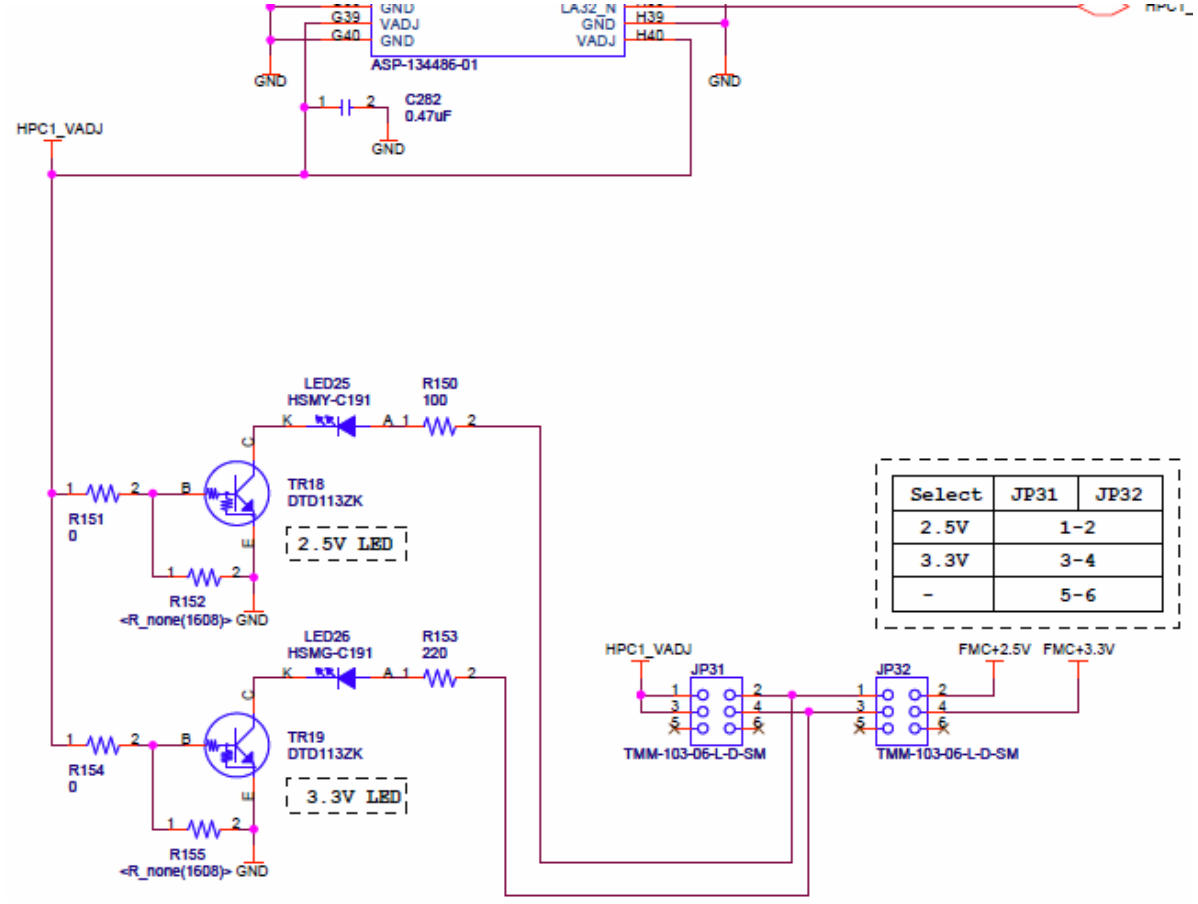

Figure 7-18 HPC1 VADJ Connection

*7 VREF_A_M2C,VREF_B_M2C

The VREF_A_M2C terminal of the H1 pin can be monitored by TPAD35 and the VREF_B_M2C terminal of the K1 pin by TPAD33.

*8 VIO_B_M2C

The VIO_B_M2C terminal of each J39 and K40 pin can be monitored by TP34.

7.4.2. FMC HPC2(CN4)

HPC2 connects a following number of signals to FPGA.
High Speed: 8 ch(TX), 8 ch(TX) and 2 pair clocks
Low Speed: LA 68(signal-end) and 2 pair clocks.

Table 7-8 HPC2(CN4) Pin Assign Table

Bank#	Pin#	A		B	Pin#	Bank#
		GND	1	RES1		
MGTXRXP1_117	H6	DP1_M2C_P	2	GND		
MGTXRXN1_117	H5	DP1_M2C_N	3	GND		
		GND	4	DP9_M2C_P		
		GND	5	DP9_M2C_N		
MGTXRXP2_117	G4	DP2_M2C_P	6	GND		
MGTXRXN2_117	G3	DP2_M2C_N	7	GND		
		GND	8	DP8_M2C_P		
		GND	9	DP8_M2C_N		
MGTXRXP3_117	F6	DP3_M2C_P	10	GND		
MGTXRXN3_117	F5	DP3_M2C_N	11	GND		
		GND	12	DP7_M2C_P	A8	MGTXRXP3_118
		GND	13	DP7_M2C_N	A7	MGTXRXN3_118
MGTXRXP0_118	E4	DP4_M2C_P	14	GND		
MGTXRXN0_118	E3	DP4_M2C_N	15	GND		
		GND	16	DP6_M2C_P	B6	MGTXRXP2_118
		GND	17	DP6_M2C_N	B5	MGTXRXN2_118
MGTXRXP1_118	D6	DP5_M2C_P	18	GND		
MGTXRXN1_118	D5	DP5_M2C_N	19	GND		
		GND	20	*1 GBTCLK1_M2C_P	*1	*1
		GND	21	*1 GBTCLK1_M2C_N	*1	*1
MGTXTXP1_117	J4	DP1_C2M_P	22	GND		
MGTXTXN1_117	J3	DP1_C2M_N	23	GND		
		GND	24	DP9_C2M_P		
		GND	25	DP9_C2M_N		
MGTXTXP2_117	H2	DP2_C2M_P	26	GND		
MGTXTXN2_117	H1	DP2_C2M_N	27	GND		
		GND	28	DP8_C2M_P		
		GND	29	DP8_C2M_N		
MGTXTXP3_117	F2	DP3_C2M_P	30	GND		
MGTXTXN3_117	F1	DP3_C2M_N	31	GND		
		GND	32	DP7_C2M_P	A4	MGTXTXP3_118
		GND	33	DP7_C2M_N	A3	MGTXTXN3_118
MGTXTXP0_118	D2	DP4_C2M_P	34	GND		
MGTXTXN0_118	D1	DP4_C2M_N	35	GND		
		GND	36	DP6_C2M_P	B2	MGTXTXP2_118
		GND	37	DP6_C2M_N	B1	MGTXTXN2_118
MGTXTXP1_118	C4	DP5_C2M_P	38	GND		
MGTXTXN1_118	C3	DP5_C2M_N	39	GND		
		GND	40	RES0		

Bank#	Pin#	C		D	Pin#	Bank#
		GND	1	*5 PG_C2M		
MGTXTXP0_117	K2	DP0_C2M_P	2	GND		
MGTXTXN0_117	K1	DP0_C2M_N	3	GND		
		GND	4	GBTCLK0_M2C_P	G8	MGTREFCLK0P_117
		GND	5	GBTCLK0_M2C_N	G7	MGTREFCLK0N_117
MGTXRXP0_117	K6	DP0_M2C_P	6	GND		
MGTXRXN0_117	K5	DP0_M2C_N	7	GND		
		GND	8	LA01_P_CC	D29	16
		GND	9	LA01_N_CC	C30	16
16	B30	LA06_P	10	GND		
16	A30	LA06_N	11	LA05_P	C29	16
		GND	12	LA05_N	B29	16
		GND	13	GND		
15	N29	LA10_P	14	LA09_P	B28	16
15	N30	LA10_N	15	LA09_N	A28	16
		GND	16	GND		
		GND	17	LA13_P	M29	15
15	L30	LA14_P	18	LA13_N	M30	15
15	K30	LA14_N	19	GND		
		GND	20	LA17_P_CC	K28	15
		GND	21	LA17_N_CC	K29	15
15	L26	LA18_P_CC	22	GND		
15	L27	LA18_N_CC	23	LA23_P	J27	15
		GND	24	LA23_N	J28	15
		GND	25	GND		
15	N27	LA27_P	26	LA26_P	D26	16
15	M27	LA27_N	27	LA26_N	C26	16
		GND	28	GND		
		GND	29	TCK		
		*2 SCL	30	*4 TDI		
		*2 SDA	31	*4 TDO		
		GND	32	*6 3P3VAUX		
		GND	33	TMS		
		*3 GA0	34	TRST_L		
		*6 12P0V	35	*3 GA1		
		GND	36	*6 3P3V		
		*6 12P0V	37	GND		
		GND	38	*6 3P3V		
		*6 3P3V	39	GND		
		GND	40	*6 3P3V		

Bank#	Pin#	E		F	Pin#	Bank#
		GND	1	*5 PG_M2C		
-	-	HA01_P_CC	2	GND		
-	-	HA01_N_CC	3	GND		
		GND	4	HA00_P_CC	-	-
		GND	5	HA00_N_CC	-	-
-	-	HA05_P	6	GND		
-	-	HA05_N	7	HA04_P	-	-
		GND	8	HA04_N	-	-
-	-	HA09_P	9	GND		
-	-	HA09_N	10	HA08_P	-	-
		GND	11	HA08_N	-	-
-	-	HA13_P	12	GND		
-	-	HA13_N	13	HA12_P	-	-
		GND	14	HA12_N	-	-
-	-	HA16_P	15	GND		
-	-	HA16_N	16	HA15_P	-	-
		GND	17	HA15_N	-	-
-	-	HA20_P	18	GND		
-	-	HA20_N	19	HA19_P	-	-
		GND	20	HA19_N	-	-
-	-	HB03_P	21	GND		
-	-	HB03_N	22	HB02_P	-	-
		GND	23	HB02_N	-	-
-	-	HB05_P	24	GND		
-	-	HB05_N	25	HB04_P	-	-
		GND	26	HB04_N	-	-
-	-	HB09_P	27	GND		
-	-	HB09_N	28	HB08_P	-	-
		GND	29	HB08_N	-	-
-	-	HB13_P	30	GND		
-	-	HB13_N	31	HB12_P	-	-
		GND	32	HB12_N	-	-
-	-	HB19_P	33	GND		
-	-	HB19_N	34	HB16_P	-	-
		GND	35	HB16_N	-	-
-	-	HB21_P	36	GND		
-	-	HB21_N	37	HB20_P	-	-
		GND	38	HB20_N	-	-
		*6 VADJ	39	GND		
		GND	40	*6 VADJ		

Bank#	Pin#	G		H	Pin#	Bank#
		GND	1	*7 VREF_A_M2C		
16	C25	CLK1_M2C_P	2	*5 PRSNT_M2C_L		
16	B25	CLK1_M2C_N	3	GND		
		GND	4	CLK0_M2C_P	D27	16
		GND	5	CLK0_M2C_N	C27	16
16	E28	LA00_P_CC	6	GND		
16	D28	LA00_N_CC	7	LA02_P	H30	16
		GND	8	LA02_N	G30	16
15	P23	LA03_P	9	GND		
15	N24	LA03_N	10	LA04_P	G29	16
		GND	11	LA04_N	F30	16
15	N21	LA08_P	12	GND		
15	N22	LA08_N	13	LA07_P	E29	16
		GND	14	LA07_N	E30	16
15	L22	LA12_P	15	GND		
15	L23	LA12_N	16	LA11_P	G28	16
		GND	17	LA11_N	F28	16
15	L21	LA16_P	18	GND		
15	K21	LA16_N	19	LA15_P	G27	16
		GND	20	LA15_N	F27	16
15	J21	LA20_P	21	GND		
15	J22	LA20_N	22	LA19_P	J29	15
		GND	23	LA19_N	H29	15
15	M20	LA22_P	24	GND		
15	L20	LA22_N	25	LA21_P	K26	15
		GND	26	LA21_N	J26	15
15	N19	LA25_P	27	GND		
15	N20	LA25_N	28	LA24_P	J23	15
		GND	29	LA24_N	J24	15
15	P21	LA29_P	30	GND		
15	P22	LA29_N	31	LA28_P	L25	15
		GND	32	LA28_N	K25	15
16	H26	LA31_P	33	GND		
16	H27	LA31_N	34	LA30_P	K23	15
		GND	35	LA30_N	K24	15
15	M24	LA33_P	36	GND		
15	M25	LA33_N	37	LA32_P	N25	15
		GND	38	LA32_N	N26	15
		*6 VADJ	39	GND		
		GND	40	*6 VADJ		

Bank#	Pin#	J		K	Pin#	Bank#
		GND	1	*7 VREF_B_M2C		
-	-	CLK3_M2C_P	2	GND		
-	-	CLK3_M2C_N	3	GND		
		GND	4	CLK2_M2C_P	-	-
		GND	5	CLK2_M2C_N	-	-
-	-	HA03_P	6	GND		
-	-	HA03_N	7	HA02_P	-	-
		GND	8	HA02_N	-	-
-	-	HA07_P	9	GND		
-	-	HA07_N	10	HA06_P	-	-
		GND	11	HA06_N	-	-
-	-	HA11_P	12	GND		
-	-	HA11_N	13	HA10_P	-	-
		GND	14	HA10_N	-	-
-	-	HA14_P	15	GND		
-	-	HA14_N	16	HA17_P_CC	-	-
		GND	17	HA17_N_CC	-	-
-	-	HA18_P	18	GND		
-	-	HA18_N	19	HA21_P	-	-
		GND	20	HA21_N	-	-
-	-	HA22_P	21	GND		
-	-	HA22_N	22	HA23_P	-	-
		GND	23	HA23_N	-	-
-	-	HB01_P	24	GND		
-	-	HB01_N	25	HB00_P_CC	-	-
		GND	26	HB00_N_CC	-	-
-	-	HB07_P	27	GND		
-	-	HB07_N	28	HB06_P_CC	-	-
		GND	29	HB06_N_CC	-	-
-	-	HB11_P	30	GND		
-	-	HB11_N	31	HB10_P	-	-
		GND	32	HB10_N	-	-
-	-	HB15_P	33	GND		
-	-	HB15_N	34	HB14_P	-	-
		GND	35	HB14_N	-	-
-	-	HB18_P	36	GND		
-	-	HB18_N	37	HB17_P_CC	-	-
		GND	38	HB17_N_CC	-	-
		*8 VIO_B_M2C	39	GND		
		GND	40	*8 VIO_B_M2C		

*1: GBTCLK1_M2C_P/N can be assigned to reference clock of 4 MGT tiles by IC29.
For more details, please refer to 7.3. RocketIO Reference Clock.

* 2 SCL, SDA

The board provides test points (with pull-up resistors pad) to enable I2C communications with the FPGA mezzanine card.

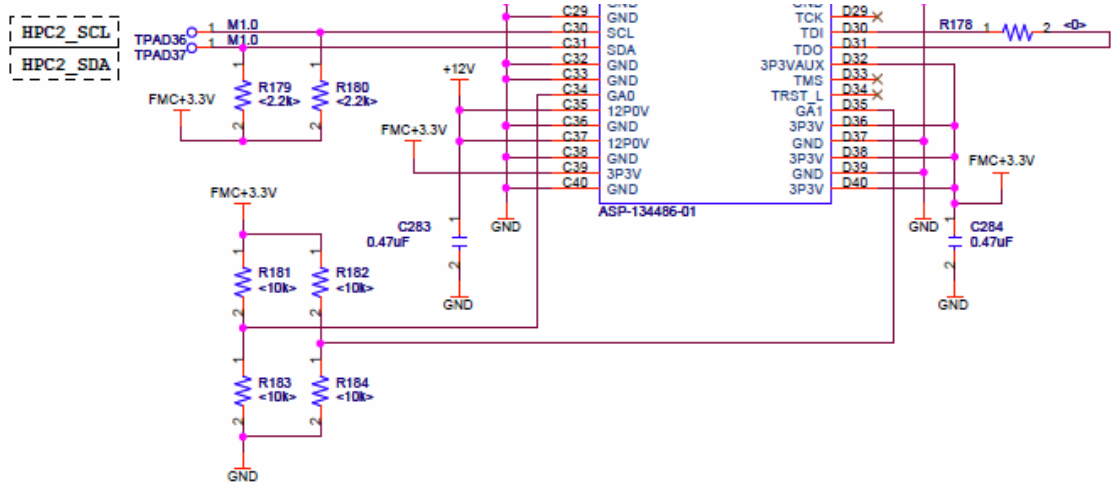

Figure 7-19 HPC2 SDC/SCL, GA1/0, TDI/TDO connection

* 3 GA[1:0]

The board has the above circuit design for notification of an ID to the FPGA mezzanine card. By default, it is set to open.

* 4 TDI,TDO

The board provides a loopback structure for JTAG communication from the FPGA mezzanine card. By default, this loopback function is not provided because the R178 resistor is not installed.

* 5 PG_C2M, PG_M2C, PRSNT_M2C_L

The board provides a structure to output to the FPGA mezzanine card. It also provides a similar structure for the column of F and H pins of the FMC connector. By default, it is set to open. The PG_M2C, PRSNT_M2C_L also has a similar structure.

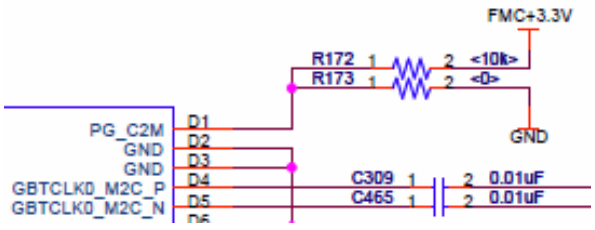

Figure 7-20 HPC2 PG_C2M connection

Table 7-9 HPC2 PG_C2M, PG_M2C, PRSNT_M2C_L Level settings

Pin#	Signal	Setting	
		H (Pull-up)	L (Pull-down)
D1	PG_C2M	R172	R173
F1	PG_M2C	R185	R186
H2	PRSNT_M2C_L	R189	R190

* 6 Power Supply

The board provides a 12V output to the 12P0V pin and a 3.3V output to the 3P3V and 3P3VAUX pins. 3.3V and 2.5V output are also selectable for VADJ pins as shown in the following circuit diagram. The HPC_VADJ voltage supply is set by jumping across the identical pins on jumpers JP33 and JP34. The power status can be monitored by the adjacent LED. By default, JP33 and JP34 are shorted 5-6.

Caution:

Do not jumper more than two portions of JP33 and JP34.

Always jumper the same pins of both JP33 and JP34.

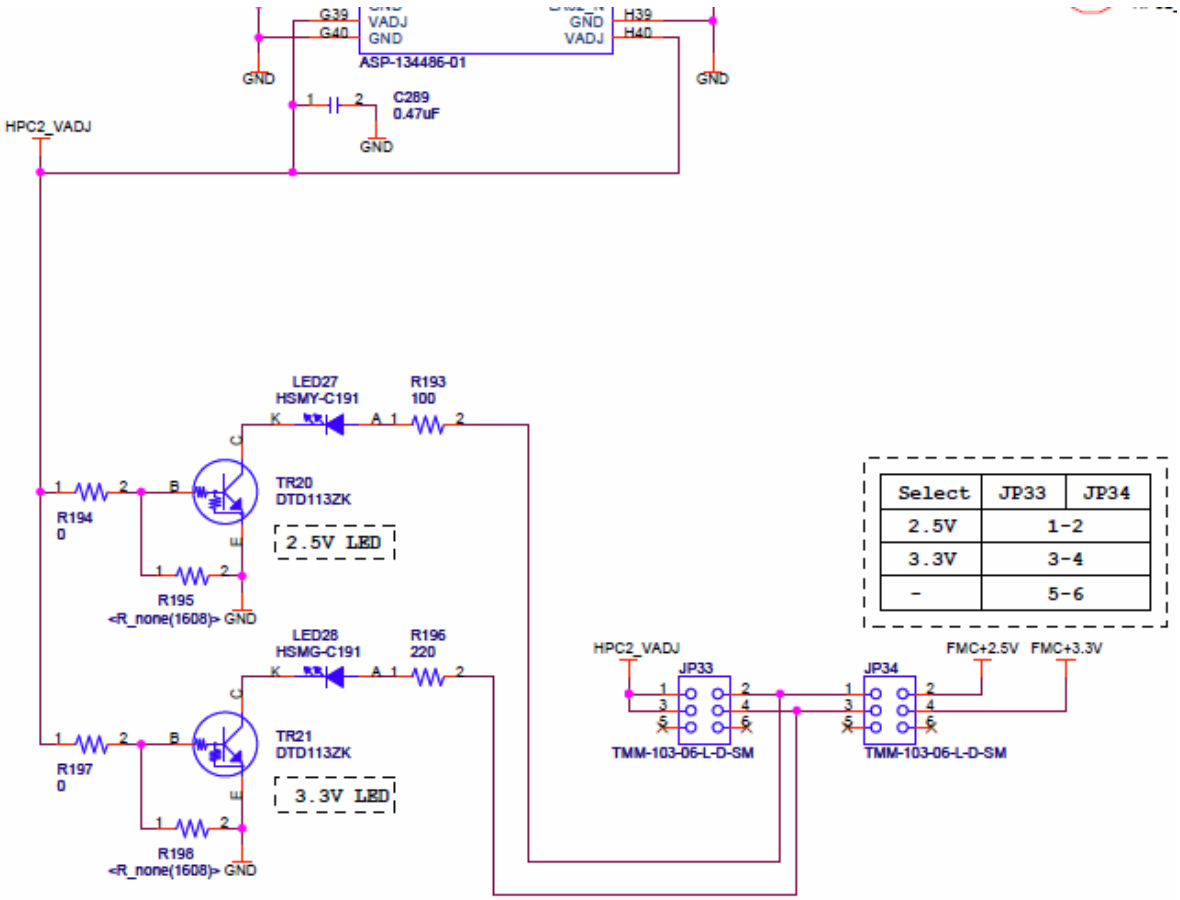

Figure 7-21 HPC2 VADJ Connection

*7 VREF_A_M2C,VREF_B_M2C

The VREF_A_M2C terminal of the H1 pin can be monitored by TPAD40 and the VREF_B_M2C terminal of the K1 pin by TPAD38.

*8 VIO_B_M2C

The VIO_B_M2C terminal of each J39 and K40 pin can be monitored by TP39.

7.4.3. FMC LPC1(CN5)

LPC1 connects a following number of signals to FPGA.

High Speed: no connection.

Low Speed: LA 68(signal-end) and 2 pair clocks.

Notice: LA12_P/N and LA22_P/N cannot be differential interface. This limitation is related FPGA spec.

Table 7-10 LPC1(CN5) Pin Assign Table

Bank#	Pin#	C		D	Pin#	Bank#
		GND	1	*4 PG_C2M		
		DP0_C2M_P	2	GND		
		DP0_C2M_N	3	GND		
		GND	4	GBTCLK0_M2C_P		
		GND	5	GBTCLK0_M2C_N		
		DP0_M2C_P	6	GND		
		DP0_M2C_N	7	GND		
		GND	8	LA01_P_CC	AA22	12
		GND	9	LA01_N_CC	AA23	12
12	Y21	LA06_P	10	GND		
12	AA21	LA06_N	11	LA05_P	AA20	12
		GND	12	LA05_N	AB20	12
		GND	13	GND		
13	AC29	LA10_P	14	LA09_P	AB24	12
13	AC30	LA10_N	15	LA09_N	AC25	12
		GND	16	GND		
		GND	17	LA13_P	AD29	13
13	AE30	LA14_P	18	LA13_N	AE29	13
13	AF30	LA14_N	19	GND		
		GND	20	LA17_P_CC	AD27	13
		GND	21	LA17_N_CC	AD28	13
13	AA27	LA18_P_CC	22	GND		
13	AB28	LA18_N_CC	23	LA23_P	AB29	13
		GND	24	LA23_N	AB30	13
		GND	25	GND		
13	AC26	LA27_P	26	LA26_P	AB22	12
13	AD26	LA27_N	27	LA26_N	AB23	12
		GND	28	GND		
		GND	29	TCK		
		*1 SCL	30	*3 TDI		
		*1 SDA	31	*3 TDO		
		GND	32	*6 3P3VAUX		
		GND	33	TMS		
		*2 GA0	34	TRST_L		
		*6 12P0V	35	*2 GA1		
		GND	36	*6 3P3V		
		*6 12P0V	37	GND		
		GND	38	*6 3P3V		
		*6 3P3V	39	GND		
		GND	40	*6 3P3V		

Bank#	Pin#	G		H	Pin#	Bank#
		GND	1	*5 VREF_A_M2C		
12	AE23	CLK1_M2C_P	2	*4 PRSNT_M2C_L		
12	AF23	CLK1_M2C_N	3	GND		
		GND	4	CLK0_M2C_P	T26	14
		GND	5	CLK0_M2C_N	T27	14
12	Y23	LA00_P_CC	6	GND		
12	Y24	LA00_N_CC	7	LA02_P	V25	14
		GND	8	LA02_N	W26	14
14	V21	LA03_P	9	GND		
14	V22	LA03_N	10	LA04_P	V29	14
		GND	11	LA04_N	V30	14
14	T20	LA08_P	12	GND		
14	T21	LA08_N	13	LA07_P	P29	14
		GND	14	LA07_N	R29	14
14	W19	LA12_P	15	GND		
14	R24	LA12_N	16	LA11_P	V26	14
		GND	17	LA11_N	V27	14
14	V19	LA16_P	18	GND		
14	V20	LA16_N	19	LA15_P	U29	14
		GND	20	LA15_N	U30	14
14	W21	LA20_P	21	GND		
14	W22	LA20_N	22	LA19_P	W23	14
		GND	23	LA19_N	W24	14
14	R23	LA22_P	24	GND		
14	R19	LA22_N	25	LA21_P	U24	14
		GND	26	LA21_N	V24	14
14	R28	LA25_P	27	GND		
14	T28	LA25_N	28	LA24_P	P27	14
		GND	29	LA24_N	P28	14
14	T25	LA29_P	30	GND		
14	U25	LA29_N	31	LA28_P	U27	14
		GND	32	LA28_N	U28	14
14	R30	LA31_P	33	GND		
14	T30	LA31_N	34	LA30_P	P26	14
		GND	35	LA30_N	R26	14
14	U22	LA33_P	36	GND		
14	U23	LA33_N	37	LA32_P	T22	14
		GND	38	LA32_N	T23	14
		*6 VADJ	39	GND		
		GND	40	*6 VADJ		

* 1 SCL, SDA

The board provides test points (with pull-up resistors pad) to enable I2C communications with the FPGA mezzanine card. By default, the pull-up resistors are not mounted.

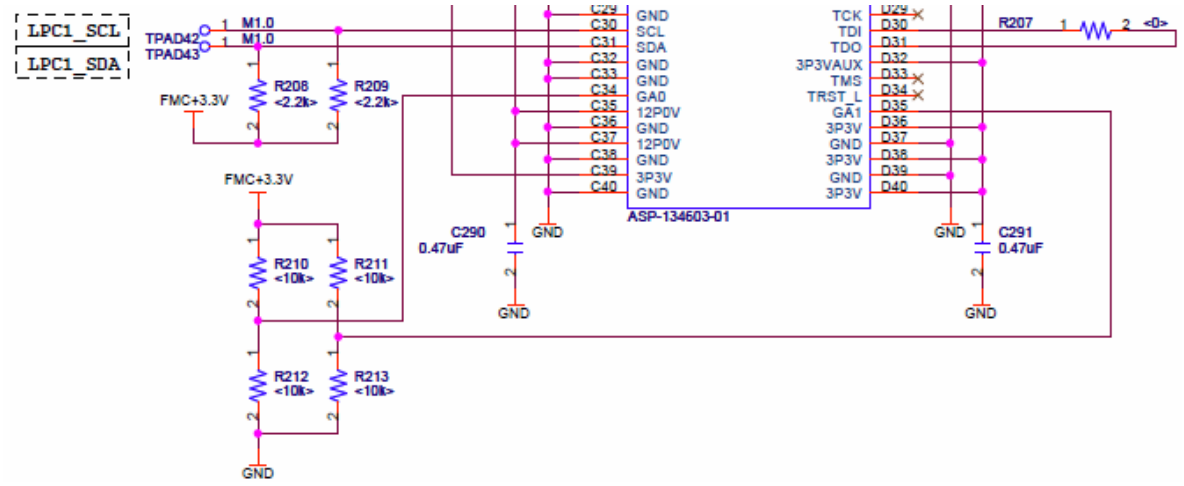

Figure 7-22 LPC1 SDC/SCL, GA1/0, TDI/TDO connection

* 2 GA[1:0]

The board has the above circuit design for notification of an ID to the FPGA mezzanine card. By default, it is set to open.

* 3 TDI,TDO

The board provides a loopback structure for JTAG communication from the FPGA mezzanine card. By default, this loopback function is not provided because the R207 resistor is not installed.

* 4 PG_C2M, PRSNT_M2C_L

The board provides a structure to output to the FPGA mezzanine card. It also provides a similar structure for the column of F and H pins of the FMC connector. By default, it is set to open. The PG_M2C, PRSNT_M2C_L also has a similar structure.

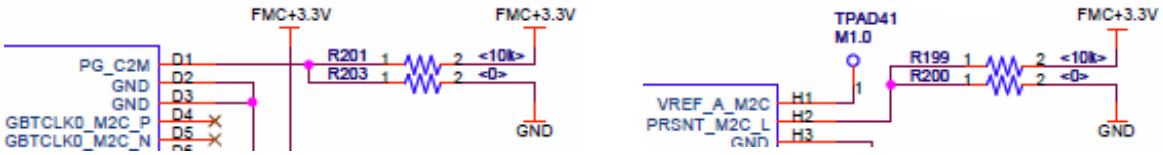

Figure 7-23 LPC1 PG_C2M connection

Table 7-11 LPC1 PG_C2M, PG_M2C, PRSNT_M2C_L Level settings

Pin#	Signal	Setting	
		H (Pull-up)	L (Pull-down)
D1	PG_C2M	R201	R203
H2	PRSNT_M2C_L	R199	R200

* 5 VREF_A_M2C

The board provides a test pad (TPAD41) to monitor the H1 pin (VREF_A_M2C) of the FMC connector.

* 6 Power Supply

The board provides a 12V output to the 12P0V pin and a 3.3V output to the 3P3V and 3P3VAUX pins. 3.3V and 2.5V output are also selectable for VADJ pins as shown in the following circuit diagram. The HPC_VADJ voltage supply is set by jumping across the identical pins on jumpers JP35 and JP36. The power status can be monitored by the adjacent LED. By default, JP35 and JP36 are shorted 5-6.

Caution:

Do not jumper more than two portions of JP35 and JP36.

Always jumper the same pins of both JP35 and JP36.

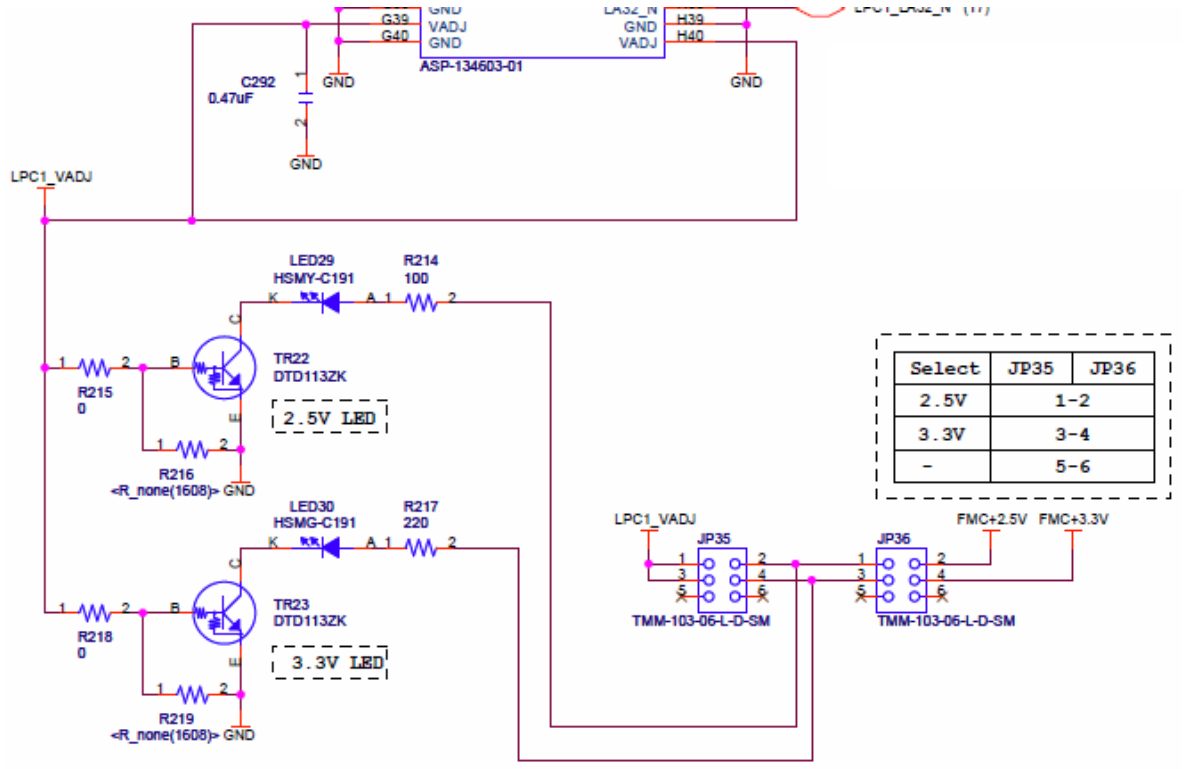

Figure 7-24 LPC1 VADJ Connection

7.4.4. FMC LPC2(CN6)

LPC2 connects a following number of signals to FPGA.

High Speed: no connection.

Low Speed: LA 68(signal-end) and 2 pair clocks.

Notice: LA25_P/N and LA29_P/N cannot be differential interface. This limitation is related FPGA spec.

Table 7-12 LPC2(CN6) Pin Assign Table

Bank#	Pin#	C		D	Pin#	Bank#
		GND	1	*4 PG_C2M		
		DP0_C2M_P	2	GND		
		DP0_C2M_N	3	GND		
		GND	4	GBTCLK0_M2C_P		
		GND	5	GBTCLK0_M2C_N		
		DP0_M2C_P	6	GND		
		DP0_M2C_N	7	GND		
		GND	8	LA01_P_CC	AG30	13
		GND	9	LA01_N_CC	AH30	13
13	AG27	LA06_P	10	GND		
13	AG28	LA06_N	11	LA05_P	AE28	13
		GND	12	LA05_N	AF28	13
		GND	13	GND		
12	AG20	LA10_P	14	LA09_P	AF26	13
12	AH20	LA10_N	15	LA09_N	AF27	13
		GND	16	GND		
		GND	17	LA13_P	AF20	12
12	AG24	LA14_P	18	LA13_N	AF21	12
12	AH24	LA14_N	19	GND		
		GND	20	LA17_P_CC	AD23	12
		GND	21	LA17_N_CC	AE24	12
12	AG25	LA18_P_CC	22	GND		
12	AH25	LA18_N_CC	23	LA23_P	AD21	12
		GND	24	LA23_N	AE21	12
		GND	25	GND		
12	AE25	LA27_P	26	LA26_P	AH26	13
12	AF25	LA27_N	27	LA26_N	AH27	13
		GND	28	GND		
		GND	29	TCK		
		*1 SCL	30	*3 TDI		
		*1 SDA	31	*3 TDO		
		GND	32	*6 3P3VAUX		
		GND	33	TMS		
		*2 GA0	34	TRST_L		
		*6 12P0V	35	*2 GA1		
		GND	36	*6 3P3V		
		*6 12P0V	37	GND		
		GND	38	*6 3P3V		
		*6 3P3V	39	GND		
		GND	40	*6 3P3V		

Bank#	Pin#	G		H	Pin#	Bank#
		GND	1	*5 VREF_A_M2C		
13	AB27	CLK1_M2C_P	2	*4 PRSNT_M2C_L		
13	AC27	CLK1_M2C_N	3	GND		
		GND	4	CLK0_M2C_P	AG29	13
		GND	5	CLK0_M2C_N	AH29	13
13	AJ28	LA00_P_CC	6	GND		
13	AJ29	LA00_N_CC	7	LA02_P	Y28	13
		GND	8	LA02_N	AA28	13
12	AC24	LA03_P	9	GND		
12	AD24	LA03_N	10	LA04_P	W27	13
		GND	11	LA04_N	W28	13
12	AC22	LA08_P	12	GND		
12	AD22	LA08_N	13	LA07_P	Y30	13
		GND	14	LA07_N	AA30	13
12	AC20	LA12_P	15	GND		
12	AC21	LA12_N	16	LA11_P	W29	13
		GND	17	LA11_N	Y29	13
13	AJ26	LA16_P	18	GND		
13	AK26	LA16_N	19	LA15_P	Y26	13
		GND	20	LA15_N	AA26	13
13	AJ27	LA20_P	21	GND		
13	AK28	LA20_N	22	LA19_P	AK20	12
		GND	23	LA19_N	AK21	12
13	AK29	LA22_P	24	GND		
13	AK30	LA22_N	25	LA21_P	AH21	12
		GND	26	LA21_N	AJ21	12
13	Y25	LA25_P	27	GND		
13	AE26	LA25_N	28	LA24_P	AJ22	12
		GND	29	LA24_N	AJ23	12
12	Y20	LA29_P	30	GND		
12	AE20	LA29_N	31	LA28_P	AF22	12
		GND	32	LA28_N	AG23	12
13	AA25	LA31_P	33	GND		
13	AB25	LA31_N	34	LA30_P	AK23	12
		GND	35	LA30_N	AK24	12
12	AJ24	LA33_P	36	GND		
12	AK25	LA33_N	37	LA32_P	AG22	12
		GND	38	LA32_N	AH22	12
		*6 VADJ	39	GND		
		GND	40	*6 VADJ		

* 1 SCL,SDA

The board provides test points (with pull-up resistors pad) to enable I2C communications with the FPGA mezzanine card. By default, the pull-up resistors are not mounted.

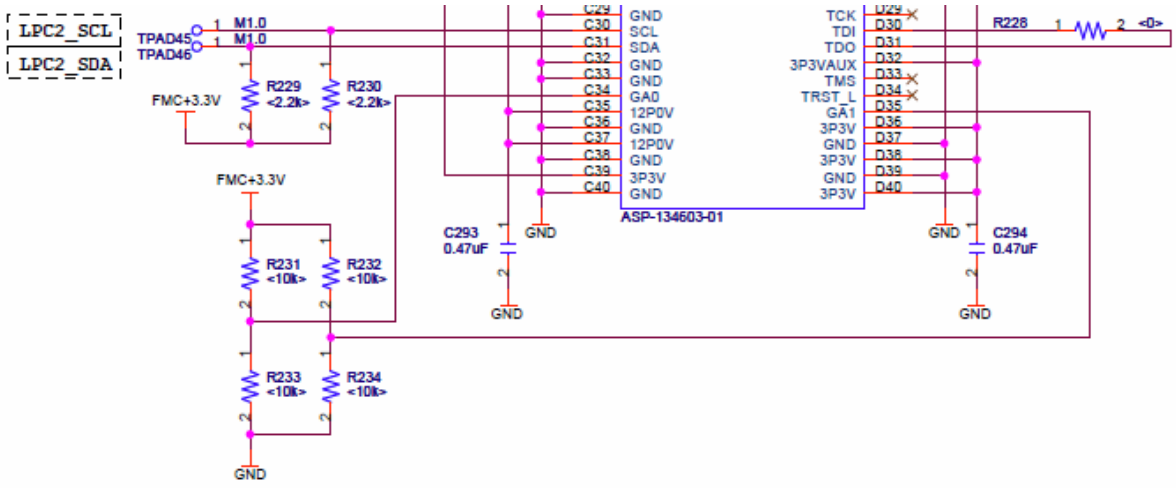

Figure 7-25 LPC2 SDC/SCL, GA1/0, TDI/TDO connection

* 2 GA[1:0]

The board has the above circuit design for notification of an ID to the FPGA mezzanine card. By default, it is OPEN.

* 3 TDI,TDO

The board provides a loopback structure for JTAG communication from the FPGA mezzanine card. By default, this loopback function is not provided because the R228 resistor is not installed.

* 4 PG_C2M, PRSNT_M2C_L

The board provides a structure to output to the FPGA mezzanine card. It also provides a similar structure for the column of F and H pins of the FMC connector. By default, it is set to open. The PG_M2C, PRSNT_M2C_L also has a similar structure.

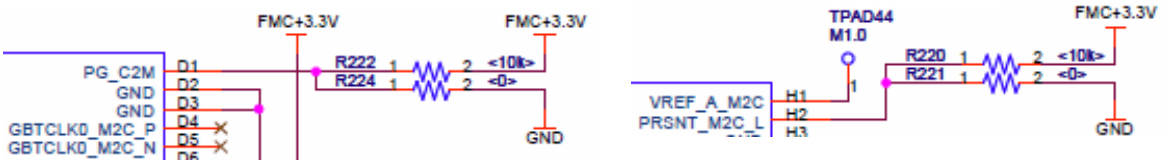

Figure 7-26 LPC2 PG_C2M connection

Table 7-13 LPC2 PG_C2M, PG_M2C, PRSNT_M2C_L Level settings

Pin#	Signal	Setting	
		H (Pull-up)	L (Pull-down)
D1	PG_C2M	R222	R224
H2	PRSNT_M2C_L	R220	R221

* 5 VREF_A_M2C

The board provides a test pad (TPAD44) to monitor the H1 pin (VREF_A_M2C) of the FMC connector.

* 6 Power Supply

The board provides a 12V output to the 12P0V pin and a 3.3V output to the 3P3V and 3P3VAUX pins. 3.3V and 2.5V output are also selectable for VADJ pins as shown in the following circuit diagram. The HPC_VADJ voltage supply is set by jumping across the identical pins on jumpers JP37 and JP38. The power status can be monitored by the adjacent LED. By default, JP37 and JP38 are shorted 5-6.

Caution:

Do not jumper more than two portions of JP37 and JP38.

Always jumper the same pins of both JP37 and JP38.

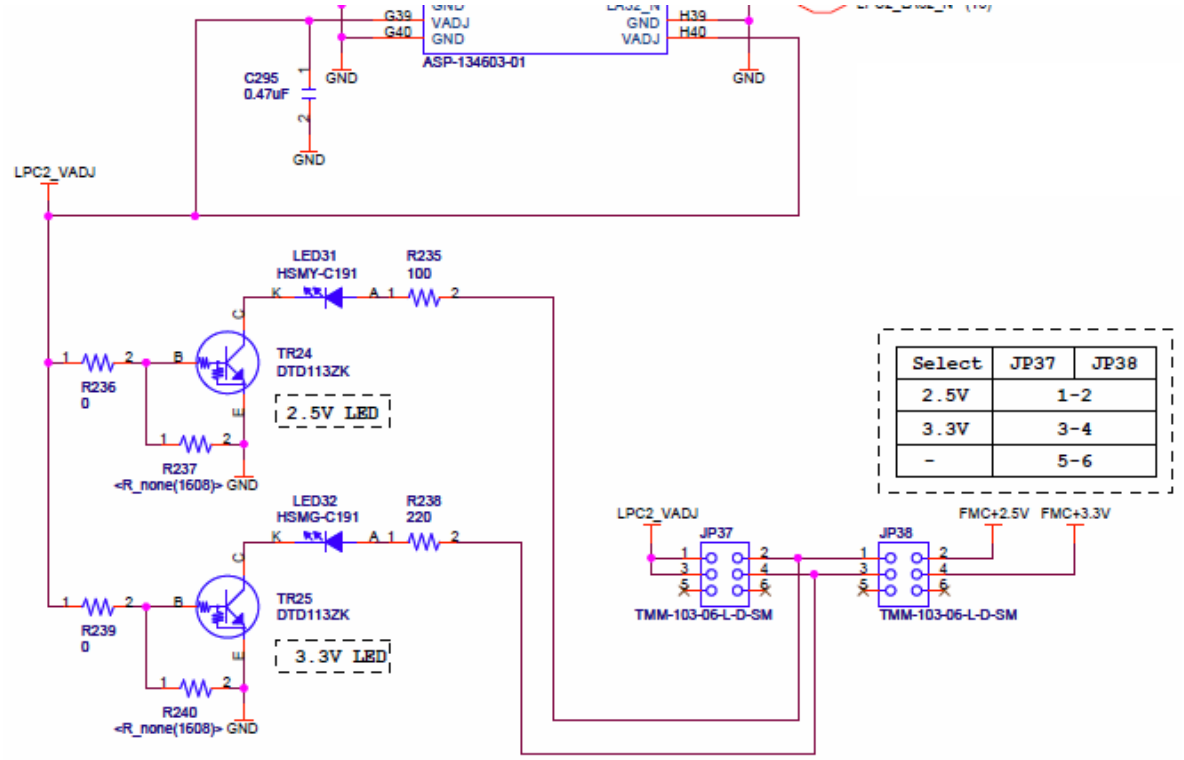

Figure 7-27 LPC2 VADJ Connection

7.5. DDR3 SDRAM

TB-7K-325T-IMG has four DDR3 SDRAMs(EDJ2116DEBG-**-*). Address signals and some control signals are wired in Fly-by Termination scheme which is used for SO-DIMM.

DDR3 SDRAM

Capacity:	2Gbit(16Mword x 16bit x 8 bank)
Address Bus:	14bit(Row Address: 14bit, Column Address: 10bit)
Bank Address:	3bit
Data Bus:	Byte access with data strobe (DQS), Data Mask for each byte.

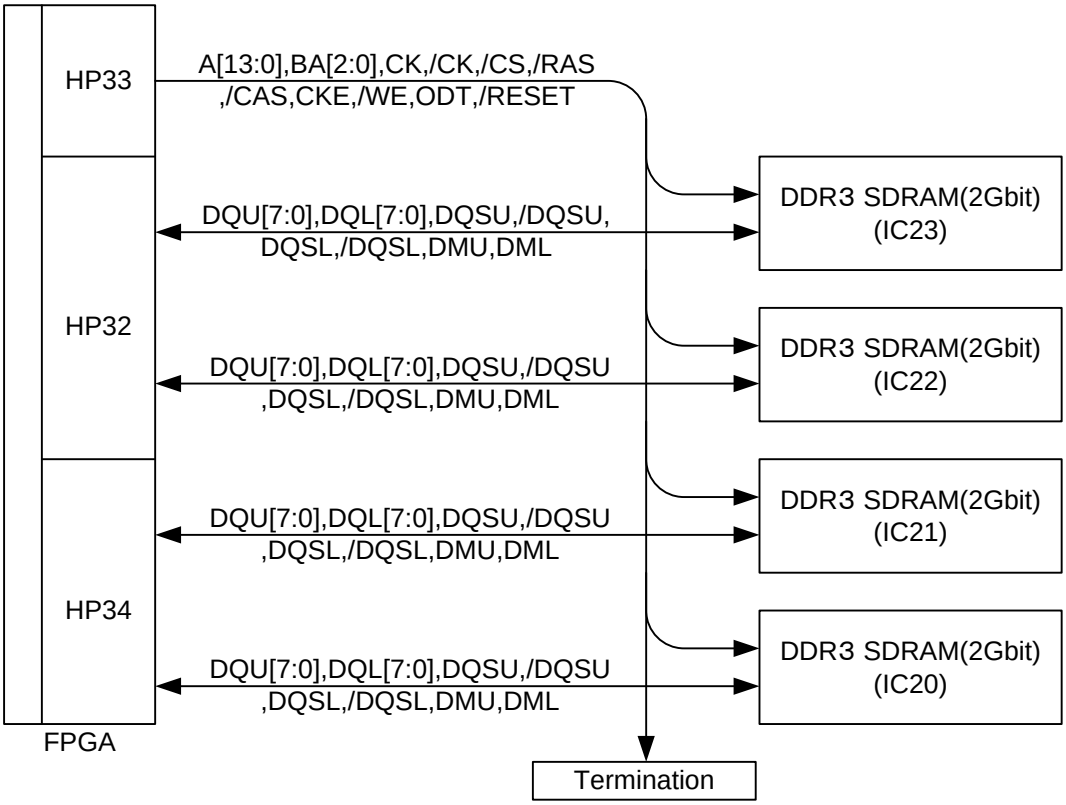

Figure 7-28 DDR3 SDRAM connection

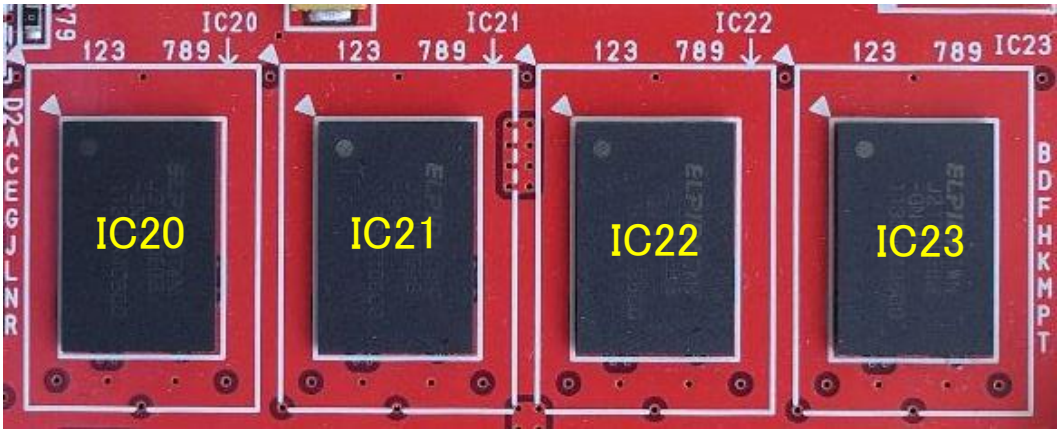

Table 7-14 DDR3 SDRAM on board view

Table 7-15 DDR3 -1 Pin Assign

DDR3	IC20		IC21		IC22		IC23	
Pin Name	Pin#	Bank#	Pin#	Bank#	Pin#	Bank#	Pin#	Bank#
A0	AE8	33	AE8	33	AE8	33	AE8	33
A1	AD8	33	AD8	33	AD8	33	AD8	33
A2	AC10	33	AC10	33	AC10	33	AC10	33
A3	AB10	33	AB10	33	AB10	33	AB10	33
A4	AB13	33	AB13	33	AB13	33	AB13	33
A5	AA13	33	AA13	33	AA13	33	AA13	33
A6	AA10	33	AA10	33	AA10	33	AA10	33
A7	AA11	33	AA11	33	AA11	33	AA11	33
A8	Y10	33	Y10	33	Y10	33	Y10	33
A9	Y11	33	Y11	33	Y11	33	Y11	33
A10	AB8	33	AB8	33	AB8	33	AB8	33
A11	AA8	33	AA8	33	AA8	33	AA8	33
A12	AB12	33	AB12	33	AB12	33	AB12	33
A13	AA12	33	AA12	33	AA12	33	AA12	33
BA0	AD9	33	AD9	33	AD9	33	AD9	33
BA1	AC11	33	AC11	33	AC11	33	AC11	33
BA2	AC12	33	AC12	33	AC12	33	AC12	33
CK	AB9	33	AB9	33	AB9	33	AB9	33
/CK	AC9	33	AC9	33	AC9	33	AC9	33
/RAS	AE9	33	AE9	33	AE9	33	AE9	33
/CAS	AE11	33	AE11	33	AE11	33	AE11	33
CKE	AG10	33	AG10	33	AG10	33	AG10	33
WE	AF11	33	AF11	33	AF11	33	AF11	33
ODT	AH10	33	AH10	33	AH10	33	AH10	33
DQL0	AC5	34	AJ2	34	AG15	32	AE18	32
DQL1	AD3	34	AJ3	34	AJ17	32	AB17	32
DQL2	AC1	34	AK1	34	AK15	32	AD17	32
DQL3	AD6	34	AJ4	34	AH17	32	AC19	32
DQL4	AC4	34	AH2	34	AG14	32	AB18	32
DQL5	AC7	34	AH6	34	AE16	32	AB19	32
DQL6	AC2	34	AJ1	34	AH15	32	AD16	32
DQL7	AE6	34	AH5	34	AF15	32	AA18	32
DQU0	AF2	34	AF7	34	AE19	32	Y15	32
DQU1	AF1	34	AK6	34	AG18	32	AC14	32
DQU2	AF6	34	AJ8	34	AG19	32	AA17	32
DQU3	AE1	34	AK5	34	AF18	32	AA15	32
DQU4	AE5	34	AG7	34	AK19	32	AA16	32
DQU5	AE4	34	AK4	34	AD19	32	AB15	32
DQU6	AF5	34	AK8	34	AH19	32	Y16	32
DQU7	AE3	34	AJ6	34	AF17	32	AD14	32
DQSL	AD2	34	AG2	34	AH16	32	Y19	32
/DQSL	AD1	34	AH1	34	AJ16	32	Y18	32
DQSU	AG4	34	AH7	34	AJ18	32	AC16	32
/DQSU	AG3	34	AJ7	34	AK18	32	AC15	32
DML	AD4	34	AH4	34	AK16	32	AD18	32
DMU	AF3	34	AF8	34	AJ19	32	AE15	32
/RESET	AD11	33	AD11	33	AD11	33	AD11	33

7.6. UART

TB-7K-325T-IMG has a UART interface to communicate with a PC.
Electrical specification is RS-232C(TI: TRS3221E), D-sub 9pin connecter.
RTS and CTS signals are not connected.(No flow control)

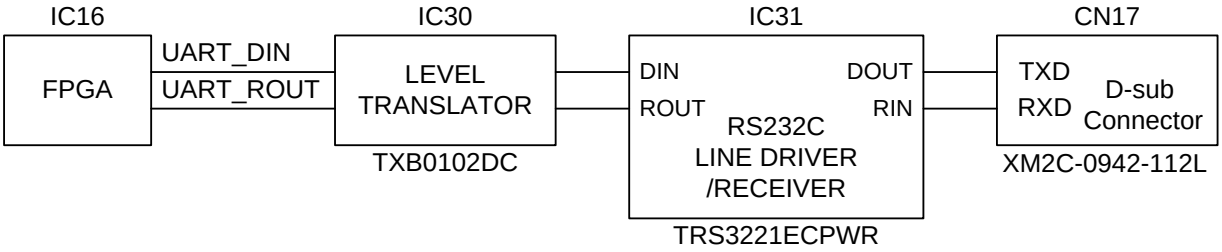

Figure 7-29 UART Bloc Diagram

Figure 7-30 UART Connector

Table 7-16 UART IF Pin Assign

Signal name	UART_DIN	UART_ROUT
FPGA Pin#	AH9	AG9

7.7. LED

TB-7K-325T-IMG has six LEDs for user application. LED is ON when FPGA output “high”.

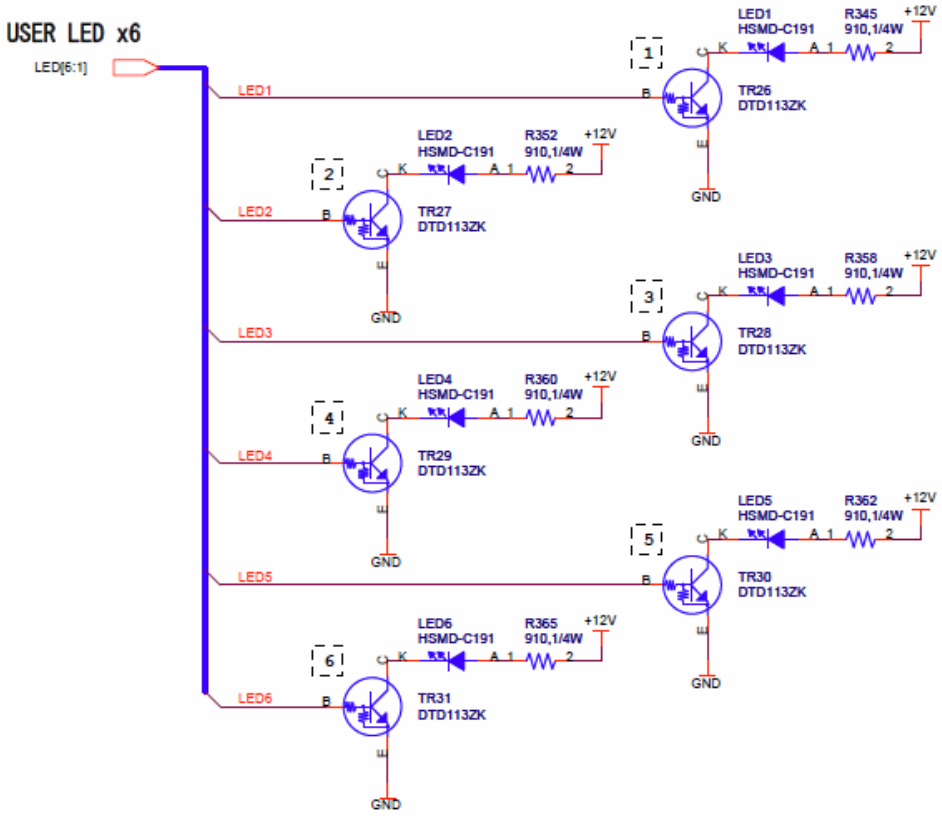

Figure 7-31 LED Circuit

Figure 7-32 LED on board view

Table 7-17 User LED Pin Assign

LED#	LED1	LED2	LED3	LED4	LED5	LED6
FPGA Pin#	AJ11	AH11	AK10	AK11	AK9	AJ9

7.8. DIP SW

TB-7K-325T-IMG has eight poles DIP Switch for user application.

If DIP SW is ON, FPGA receive Low(0) level.

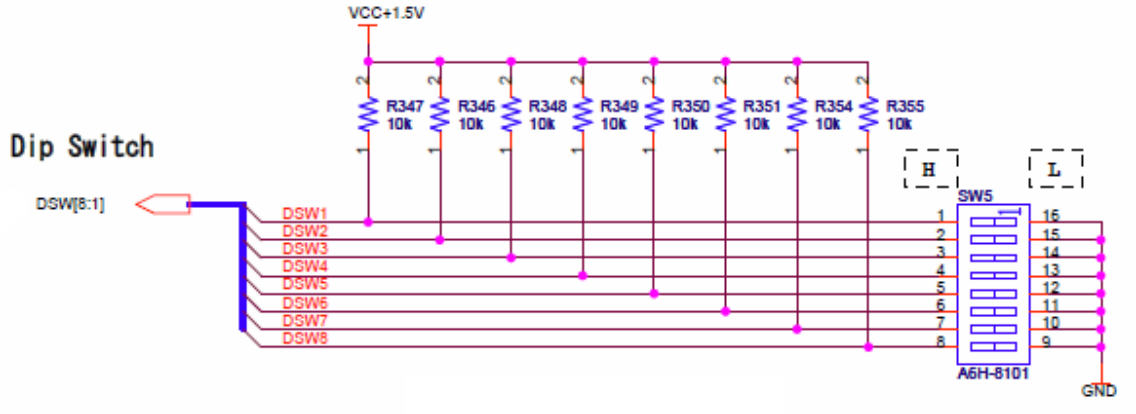

Figure 7-33 DIP SW Circuit

Figure 7-34 DIP SW on board view

Table 7-18 DIP SW Pin Assign

Device		FPGA		
Name	Signal Name	Pin No.	Bank	Level
SW5	DSW1	AH12	33	1.5V
	DSW2	AG13	33	
	DSW3	AG12	33	
	DSW4	AF12	33	
	DSW5	AJ12	33	
	DSW6	AJ13	33	
	DSW7	AJ14	33	
	DSW8	AH14	33	

7.9. Push SW

TB-7K-325T-IMG has four Push Switches for user application. If pushing switch, signal is “Low”.

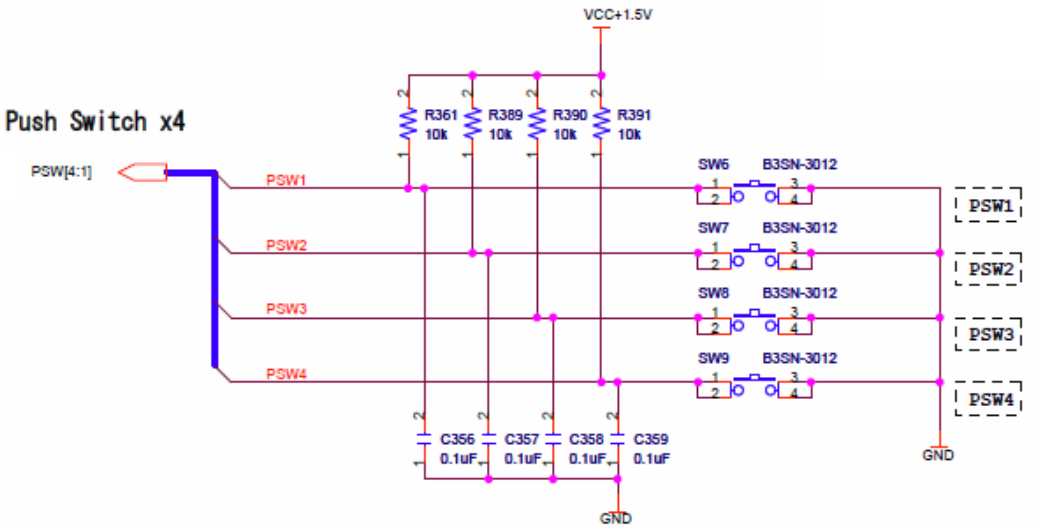

Figure 7-35 Push SW Circuit

Figure 7-36 Push SW on board view

Table 7-19 Push SW Pin Assign

Device		FPGA		
Name	Signal Name	Pin No.	Bank	Level
SW6	PSW1	AK13	33	1.5V
SW7	PSW2	AK14	33	
SW8	PSW3	AF13	33	
SW9	PSW4	AE13	33	

7.10. Pin Header

TB-7K-325T-IMG has a pin header(CN21) for XADC interface. If using VP_0 and VN_0(Differential Analog Input), please remove R438 and R439 resistors. If using DXP_0 and DXN_0(Thermionic Diode), please remove R441 and R442 resistors.

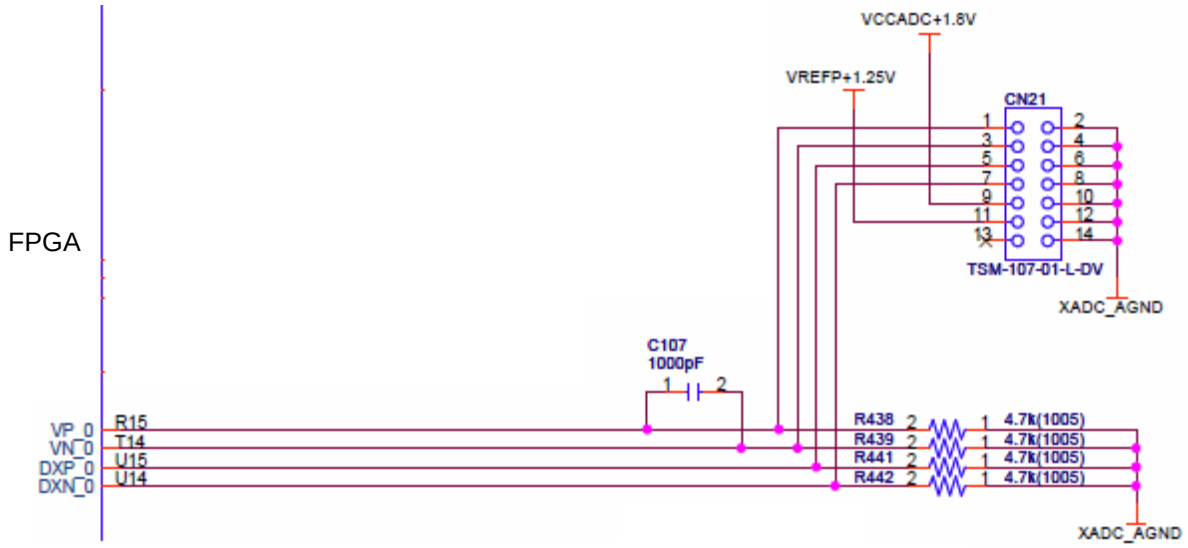

Figure 7-37 XADC Interface Circuit

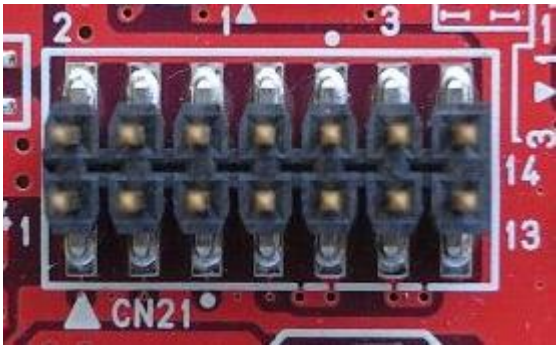

Figure 7-38 XADC Pin header on board view

Figure 7-39 XADC Pin header Pin Assign Table

FPGA		Pin Header			
Bank No.	Pin No.	Signal Name	Pin No.		Signal Name
0	R15	VP	1	2	XADC_AGND
0	T14	VN	3	4	XADC_AGND
0	U15	DXP	5	6	XADC_AGND
0	U14	DXN	7	8	XADC_AGND
-	-	VCCADC+1.8V	9	10	XADC_AGND
-	-	VREFP+1.25V	11	12	XADC_AGND
-	-	-	13	14	XADC_AGND

7.11. Battery

TB-7K-325T-IMG has a battery circuit. Battery and socket are not mounted.
Buttery size is CR1220.

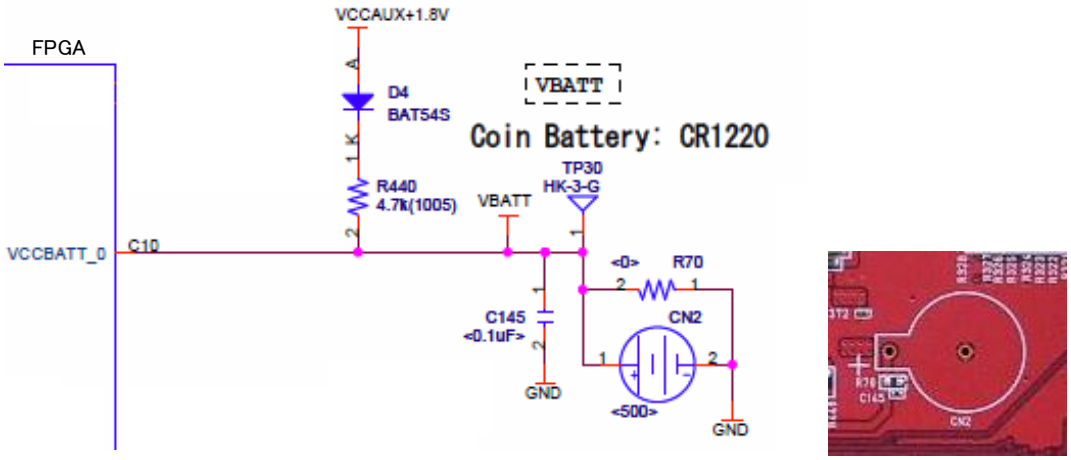

Figure 7-40 Battery circuit and Pad on bottom

7.12. Quad SPI Flash

TB-7K-325T-IMG has a 128Mbit Quad SPI Flash memory for FPGA configuration.
About Configuration, please refer to section 8.

Table 7-20 QSPI Flash memory connection

Signal name	CF_D0	CF_D1	CF_D2	CF_D3	CF_FCS_B
FPGA Pin#	P24	R25	R20	R21	U19

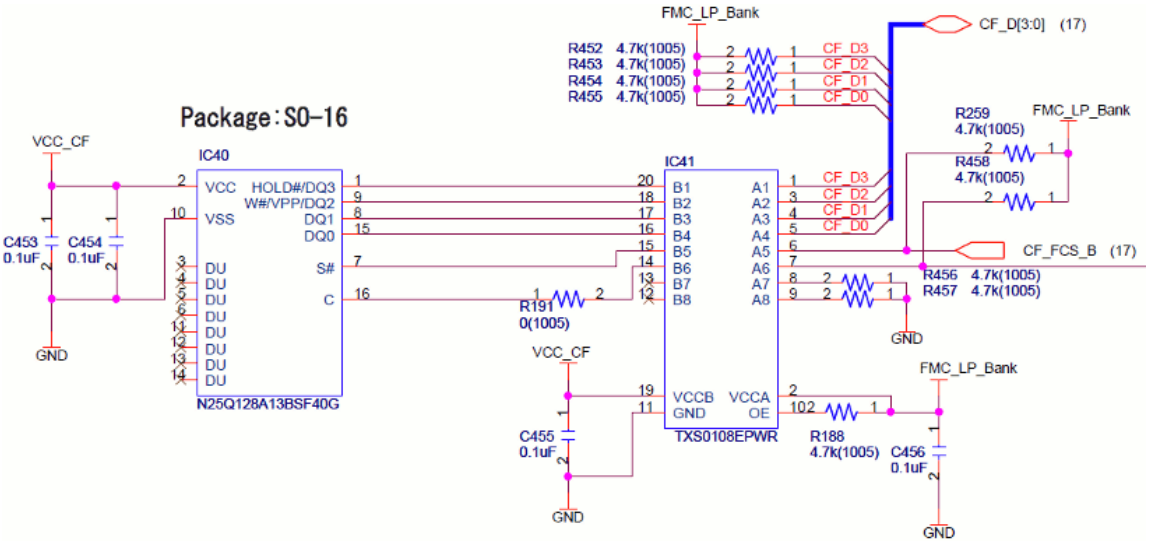

Figure 7-41 QSPI Flash memory circuit

7.13. FPGA JTAG IF

TB-7K-325T-IMG has a JATG interface for programing to FPGA.

Connector pin assign is same as Xilinx official JTAG Cable.

Table 7-21 FPGA JTAG IF Pin Assign

Signal name	TMS	TCK	TDO	TDI
Connector Pin#	4	6	8	10
FPGA Pin#	F10	E10	G10	H10

8. Creating a Configuration File and Operation

This section describe process properties based on ISE13.4.

8.1. Process properties of generate programing file

Right click to “Generate Programing File” on process windows of ISE, select the “Process Properties”.

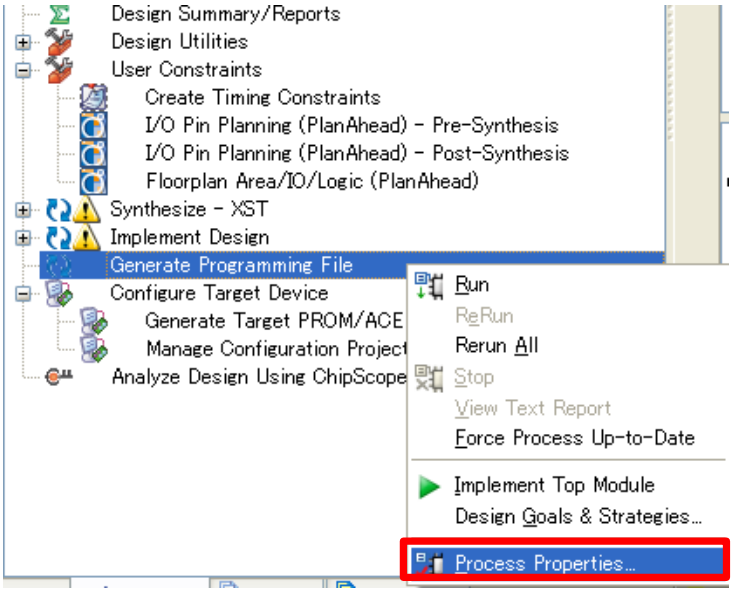

Figure 8-1 Open the process properties window

Select the “Configuration Options” and Set “4” to the “Set SPI Configuration Bus Width”.
Note: property display level should be “Advanced”

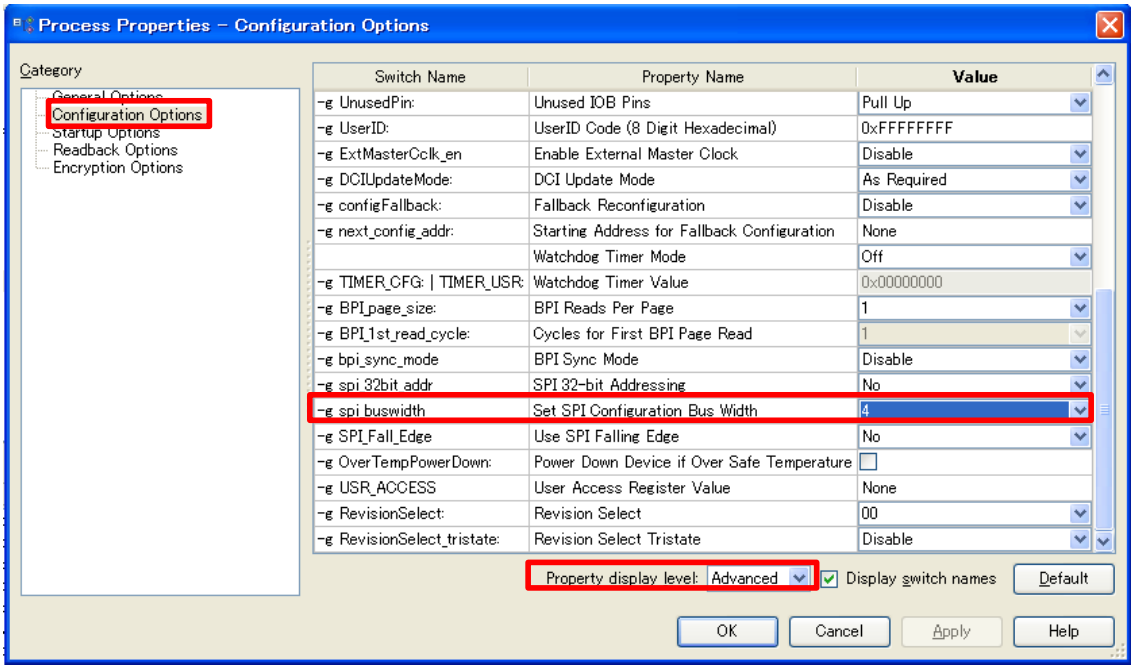

Figure 8-2 Process Properties window

8.2. Configuration Rate

Configuration Rate can be select from the “Process Properties”.

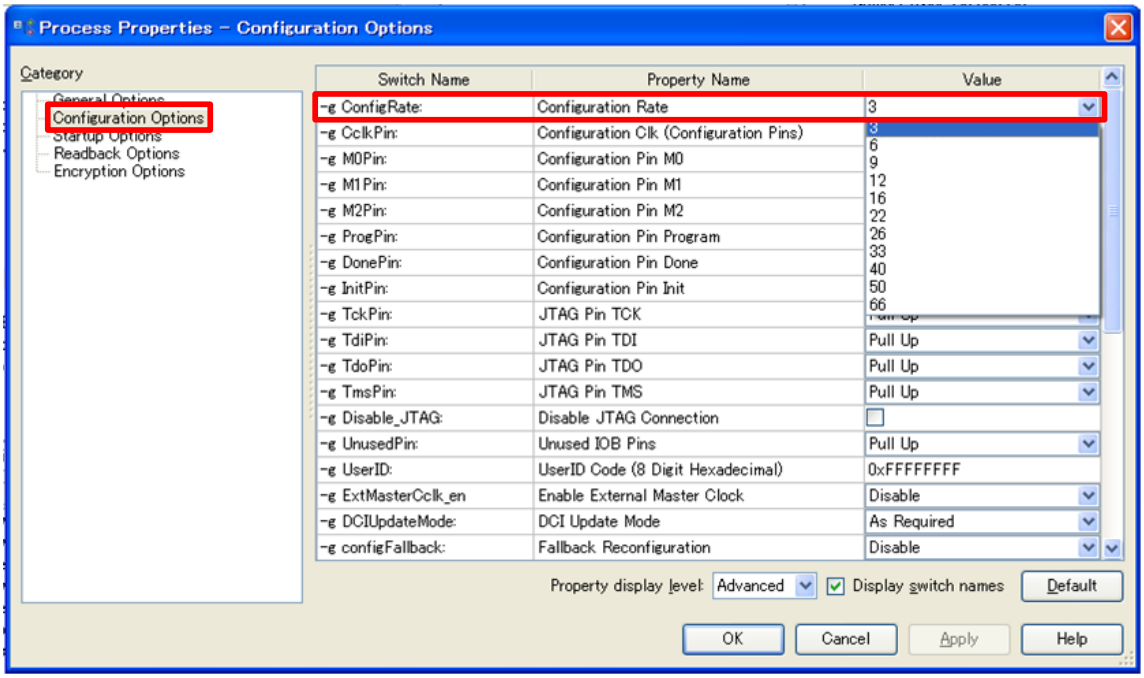

Figure 8-3 Configuration Rate

Configuration Time(only as a guide)

Configuration Rate = 3MHz : Configuration Time = about 10 sec.

Configuration Rate = 16MHz : Configuration Time = about 2 sec.

Configuration Rate = 33MHz : Configuration Time = about 1 sec.

8.3. Setting for unused IOB pins

It should set to “Float” form “Configuration Option”.

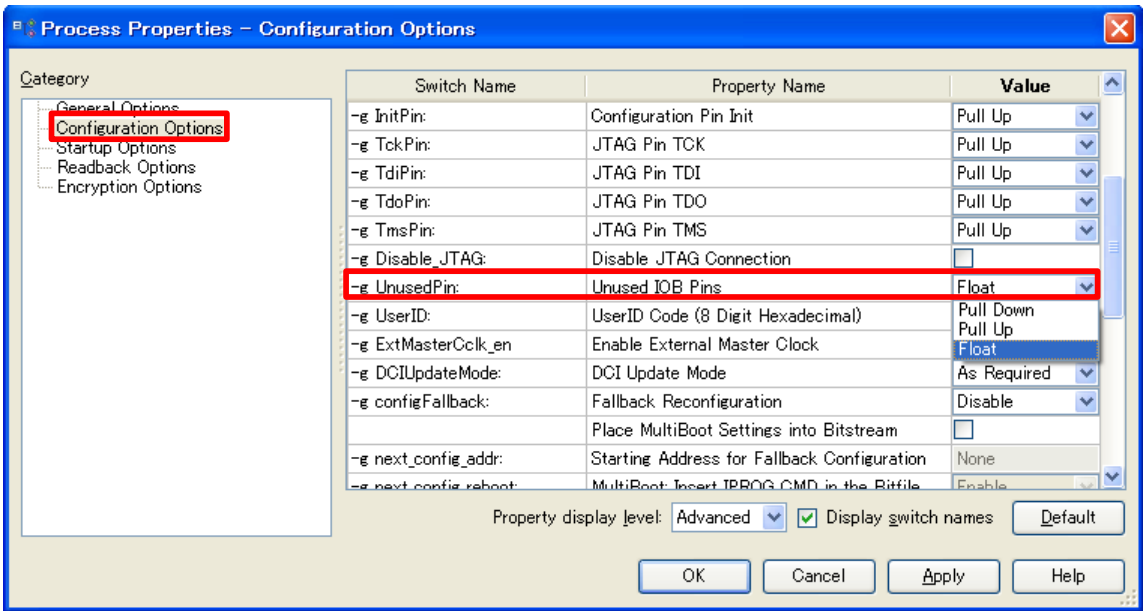

Figure 8-4 Unused IOB pins

8.4. Generate Target PROM File(MCF File)

This section describe operation of “Generate Target PRM File”.

1. Double click to “Generate Target PROM/ACE File”

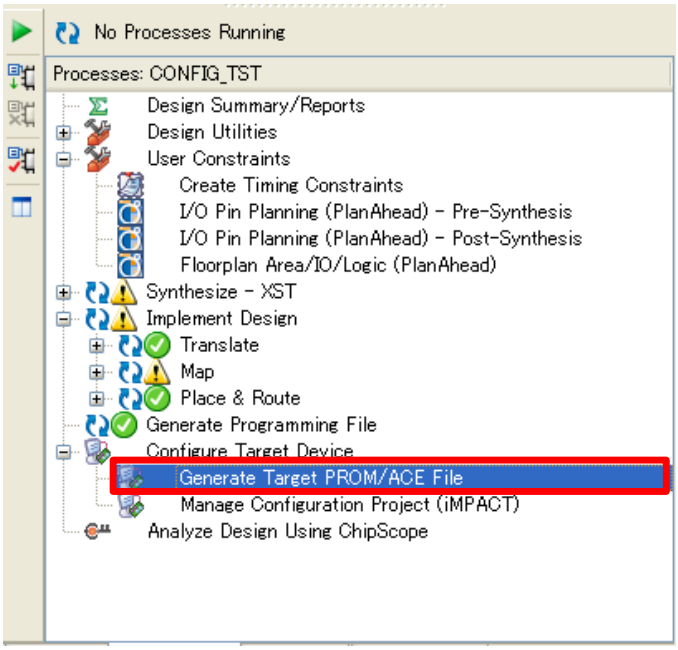

Figure 8-5 Generate Target PROM/ACE File on ISE

2. If pop-up following Warning window, please click “OK”.

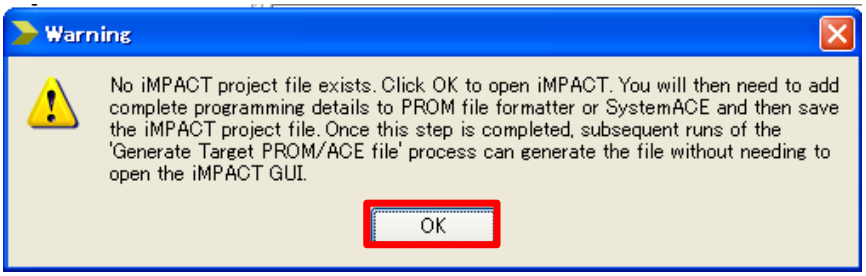

Figure 8-6 Warning window

3. Double click to “Create PROM File” on iMPACT.

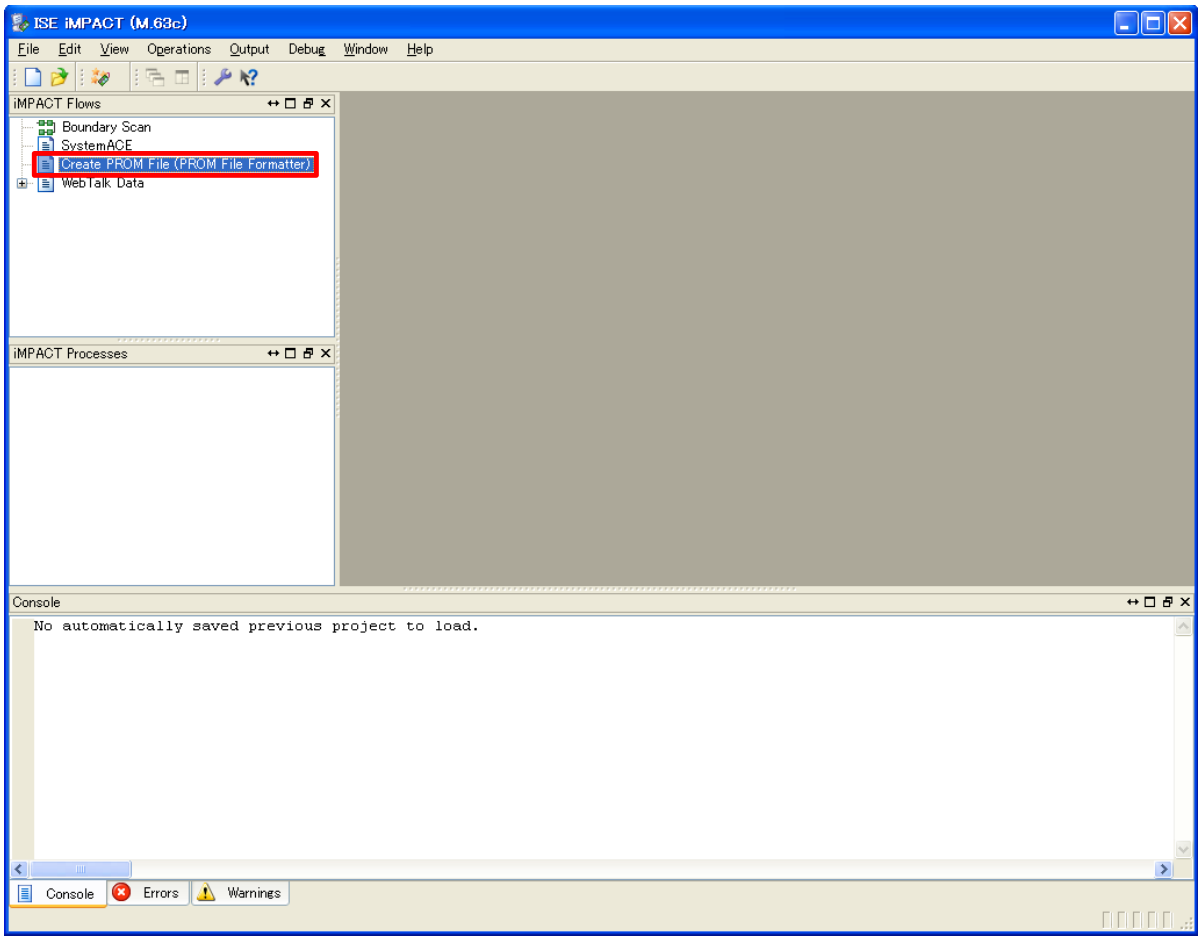

Figure 8-7 iMPCAT - window 1 -

4. Select “SPI Flash - Configure Single FPGA”. Then click the Arrow.

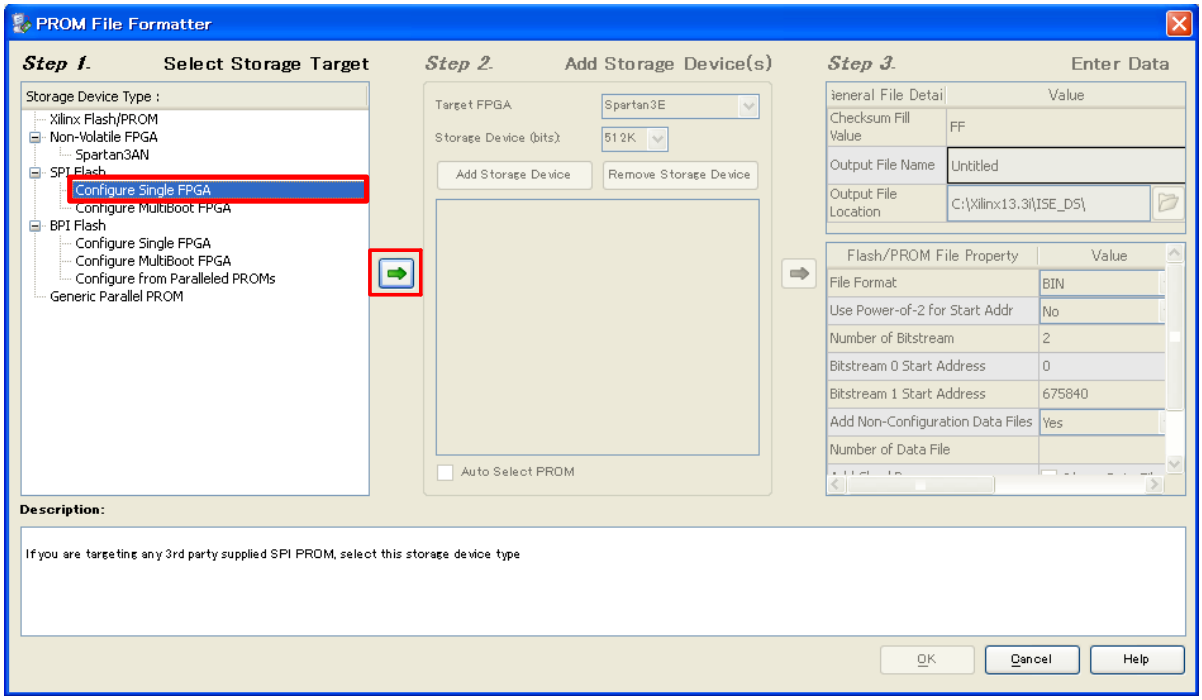

Figure 8-8 iMPACT - windows 2 -

5. Select “128M” at “Storage Device(bits)”. Then click to “Add Storage Device”.

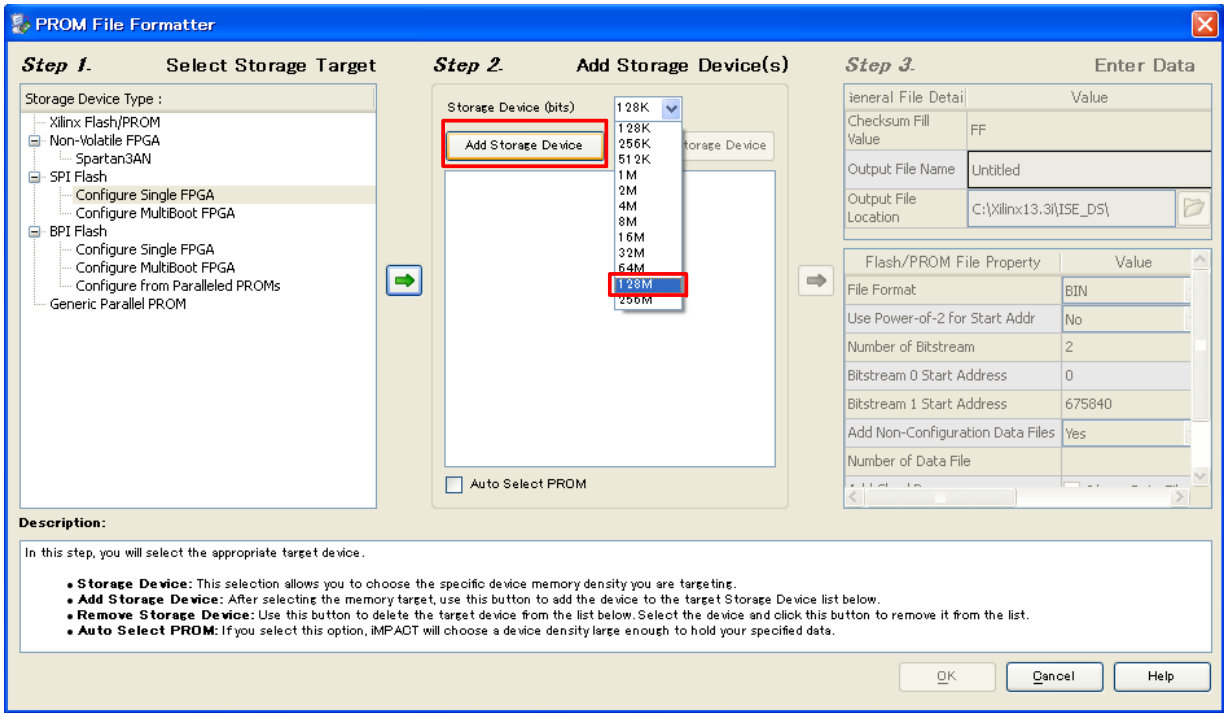

Figure 8-9 iMPACT - window 3 -

6. Click to the Arrow, Select “Output File Name” and “Output File Location” then click “OK”

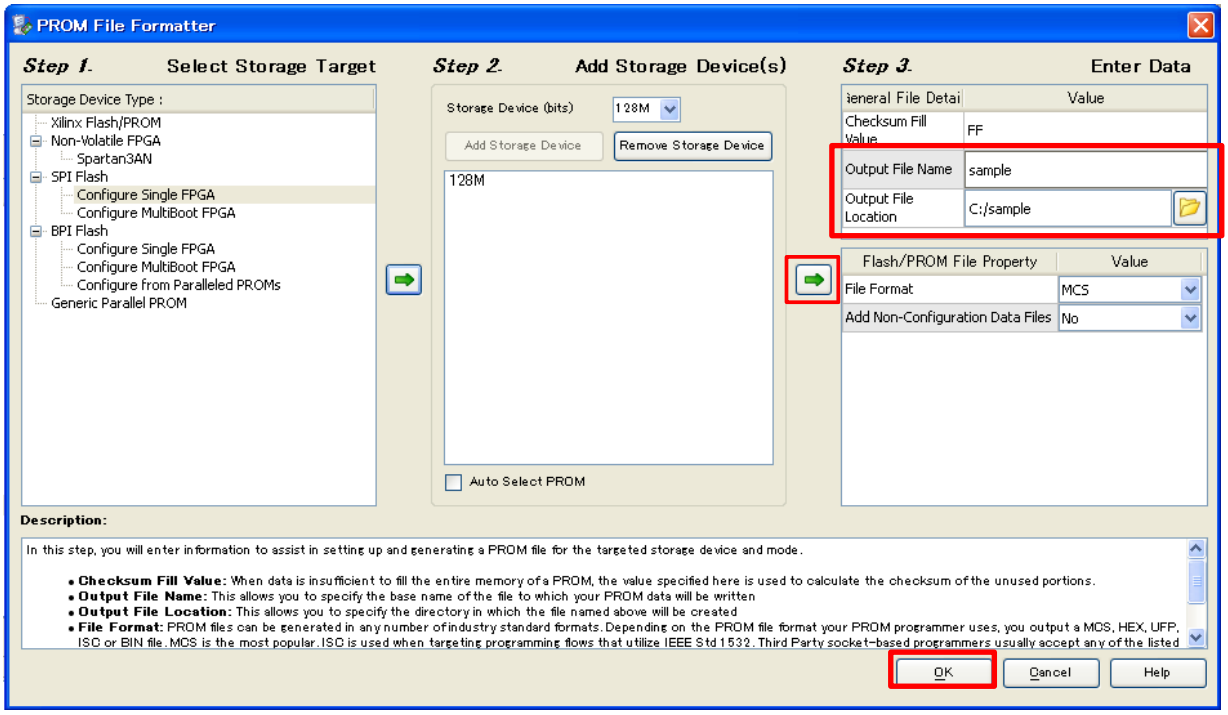

Figure 8-10 iMPACT - window 4 -

7. Click to “OK”

Figure 8-11 iMPACT - window 5 -

8. Select “bit file”

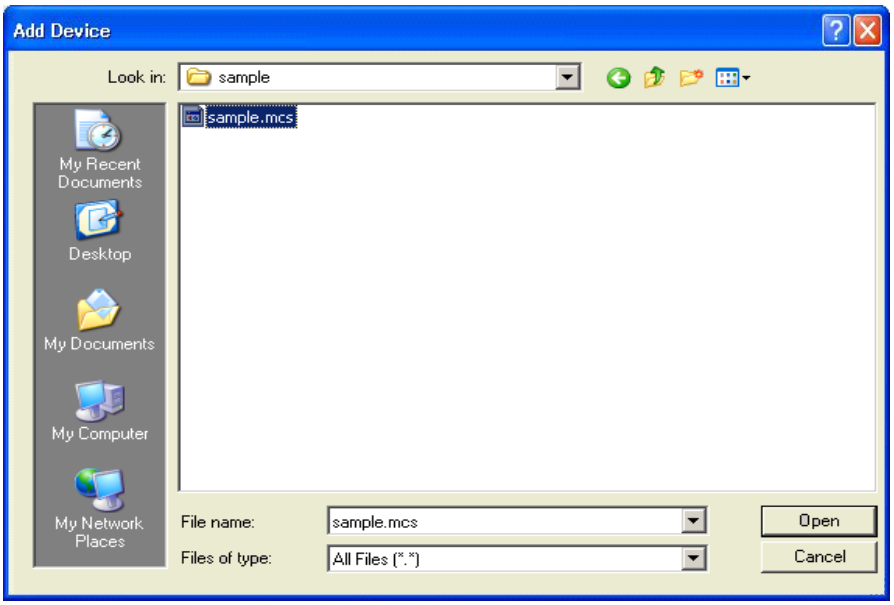

Figure 8-12 iMPACT - window 6 -

9. Click to “No”

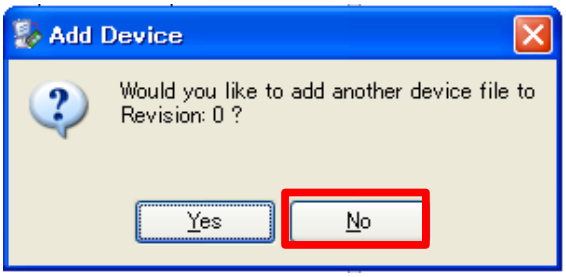

Figure 8-13 iMPACT - window 7 -

10. Click to “OK”

Figure 8-14 iMPACT - window 8 -

11. Double click to “Generate File”

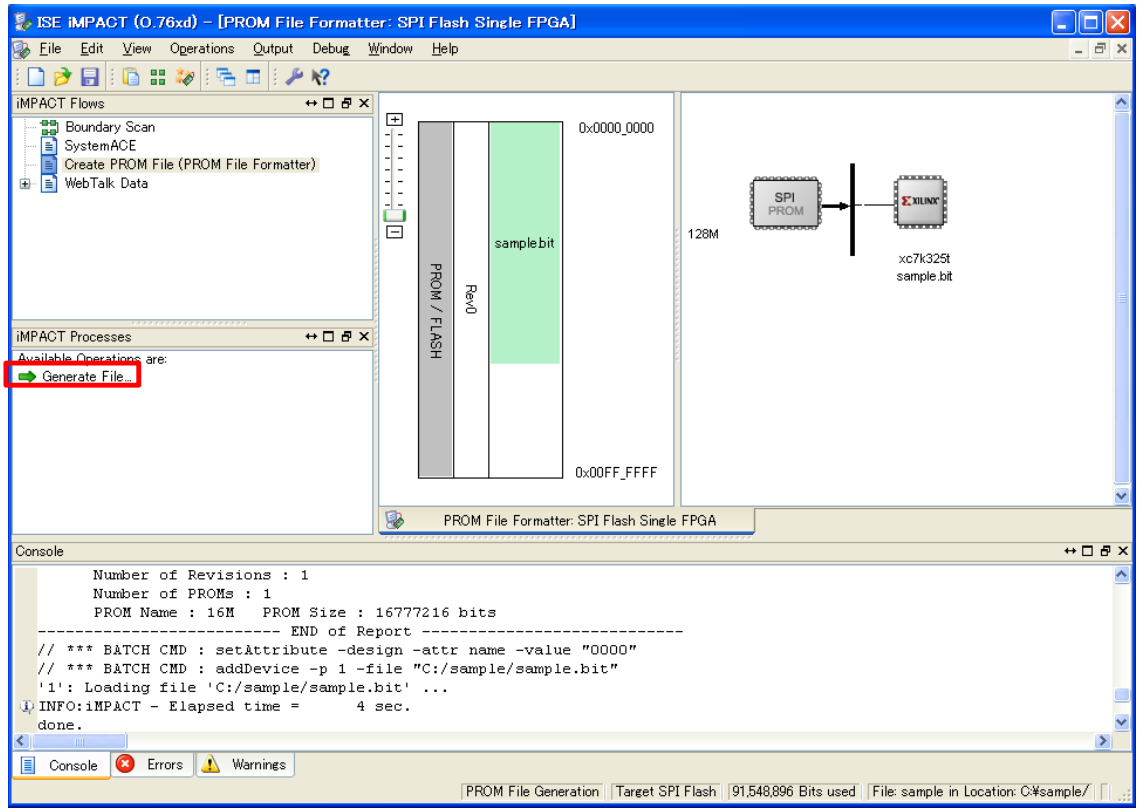

Figure 8-15 iMPACT - window 9 -

12. If iMPACT shoes the “Generate Succeeded”, finished to generate configuration file.

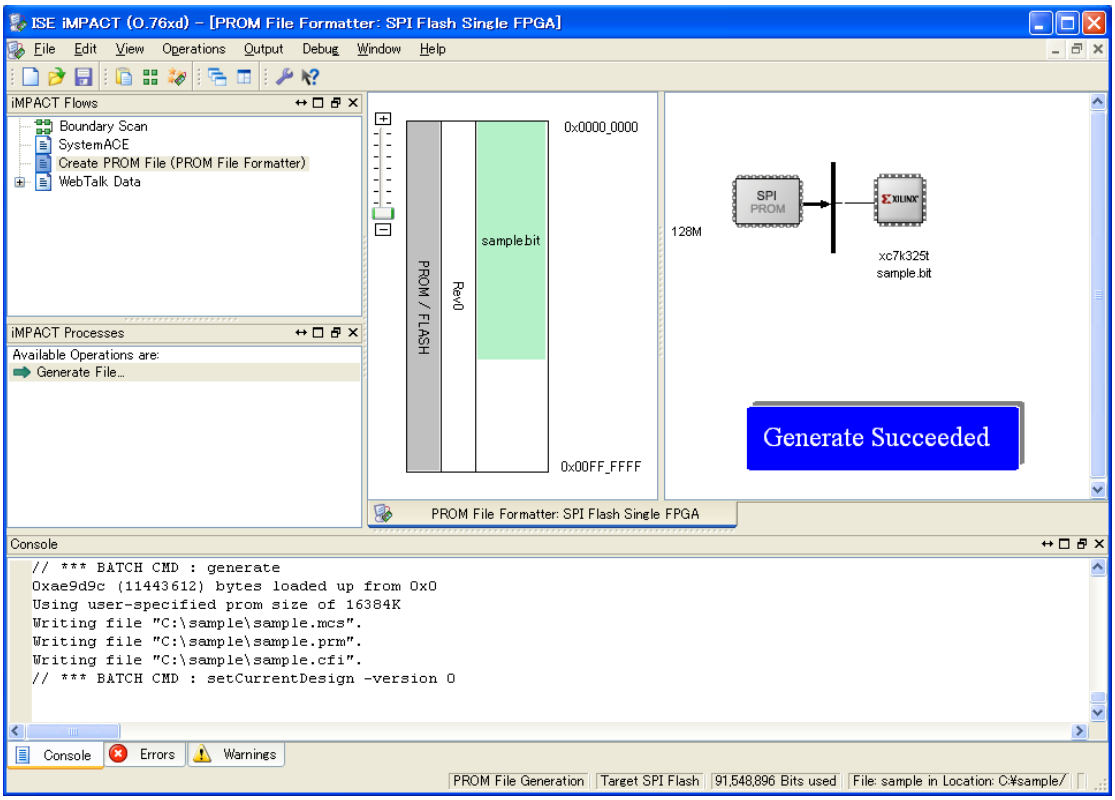

Figure 8-16 iMPACT - window 10 -

8.5. Downloading the configuration file to Flash memory

This section describe the download configuration file to Flash memory.

Connecting Platform USB cable to JTAG connector(CN1) and Power On. Then starting the iMPACT.

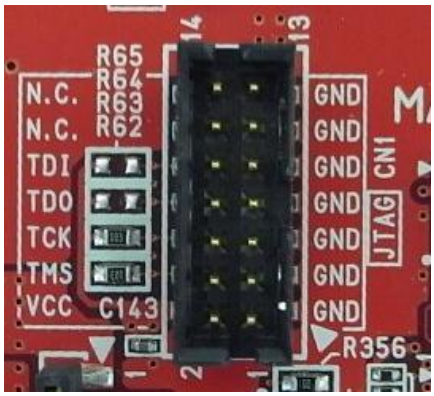

Figure 8-17 JTAG connector (CN1)

1. Double click to “Boundary Scan” then click to “Initialize Chain”.

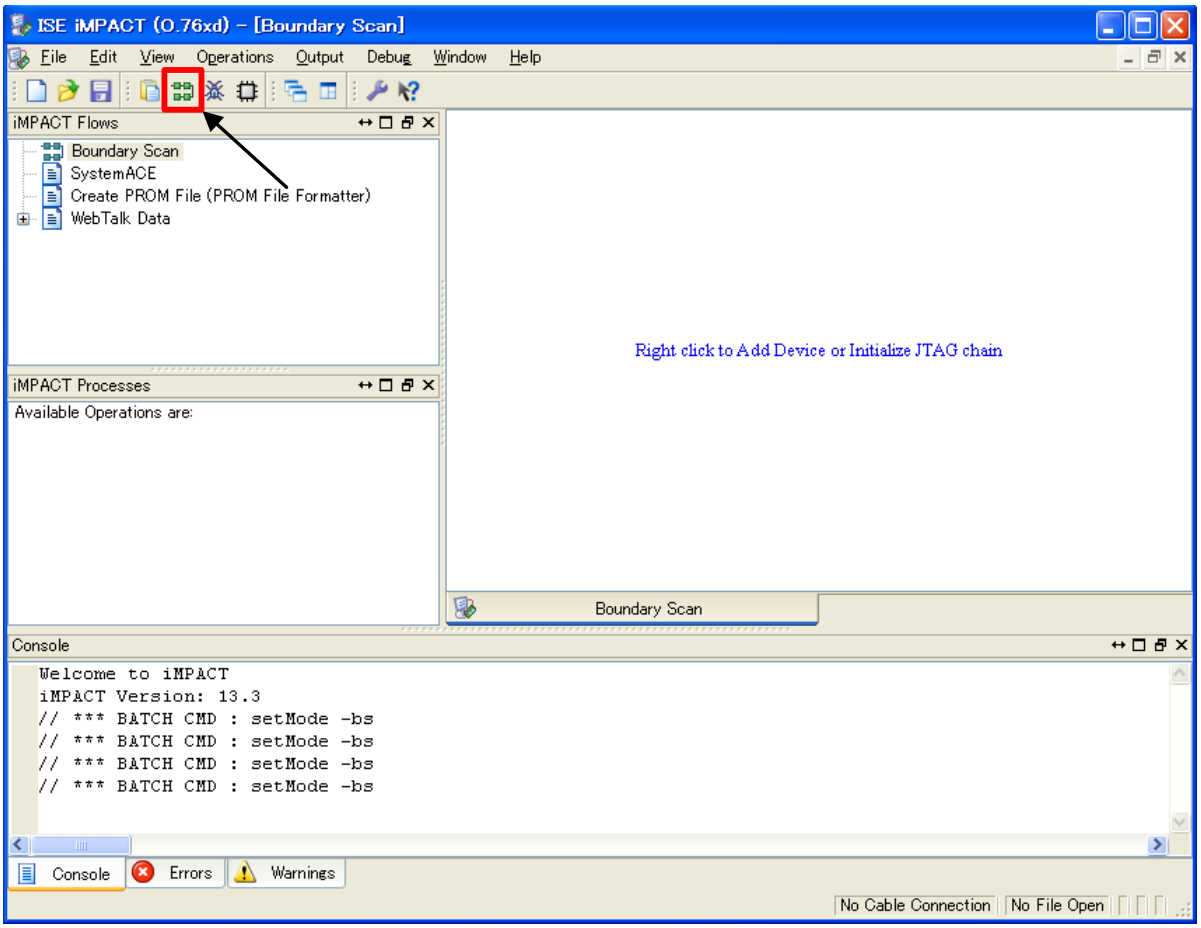

Figure 8-18 Download operation 1

2. Please cancel the file select windows. Then right-click to FPGA and select “Add SPI/BPI Flash”

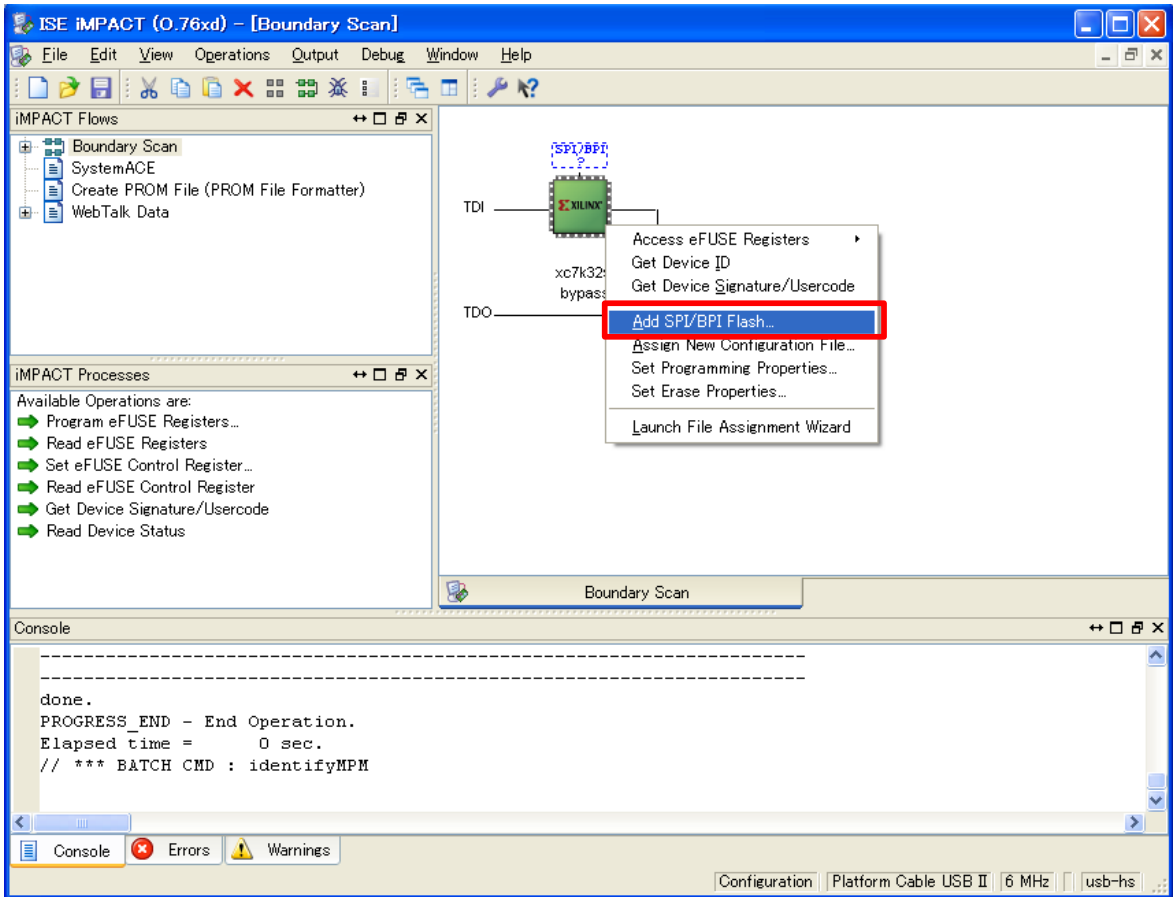

Figure 8-19 Download operation 2

3. Select the configuration file (.MCS)

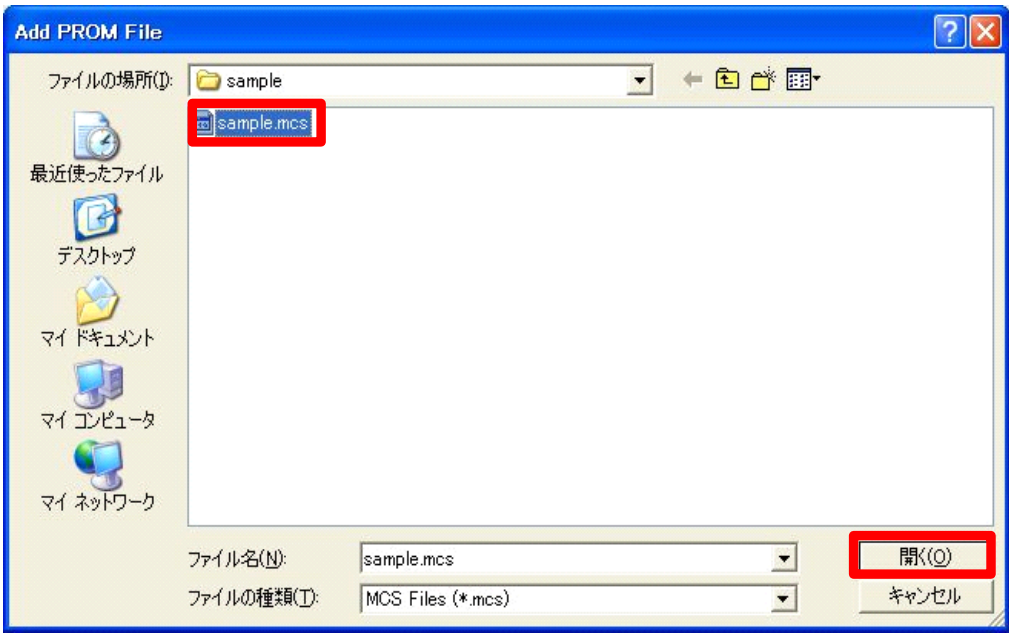

Figure 8-20 Download operation 3

4. Select “N25Q128 1.8/3.3V” and Set Data Width “4” then click to “OK”

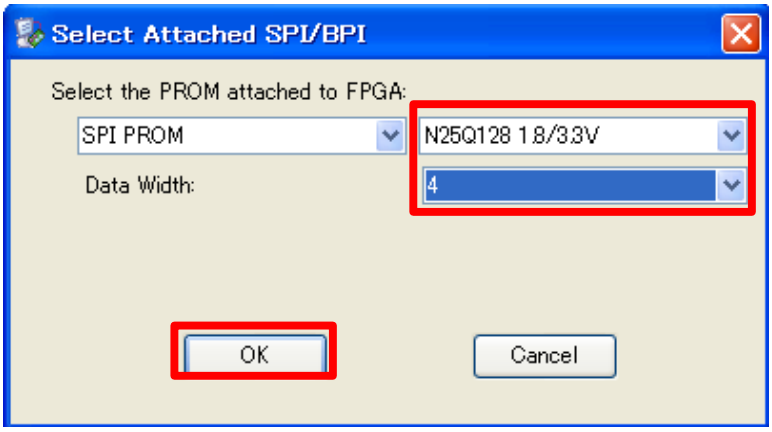

Figure 8-21 Download operation 4

5. Double click to “Program” on iMPACT Processes”

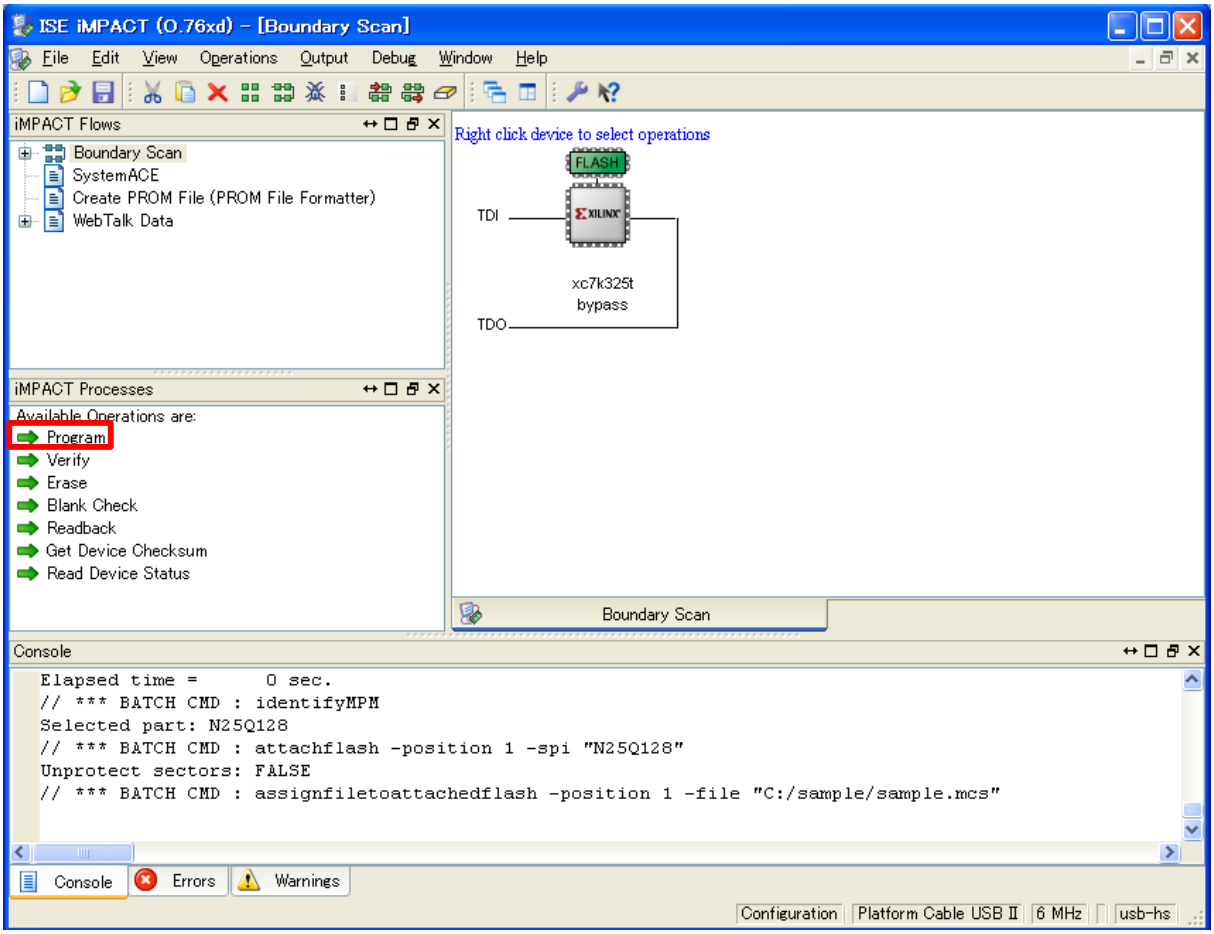

Figure 8-22 Download operation 5

6. Click to “OK”

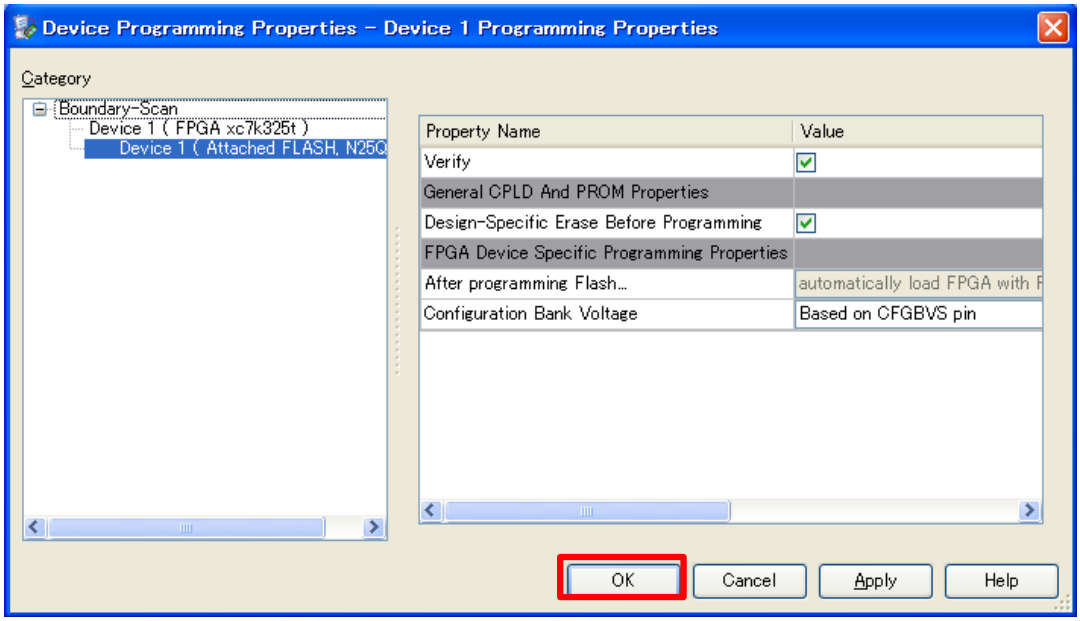

Figure 8-23 Download operation 6

7. iMPACT start to downloading configuration data to Flash Memory

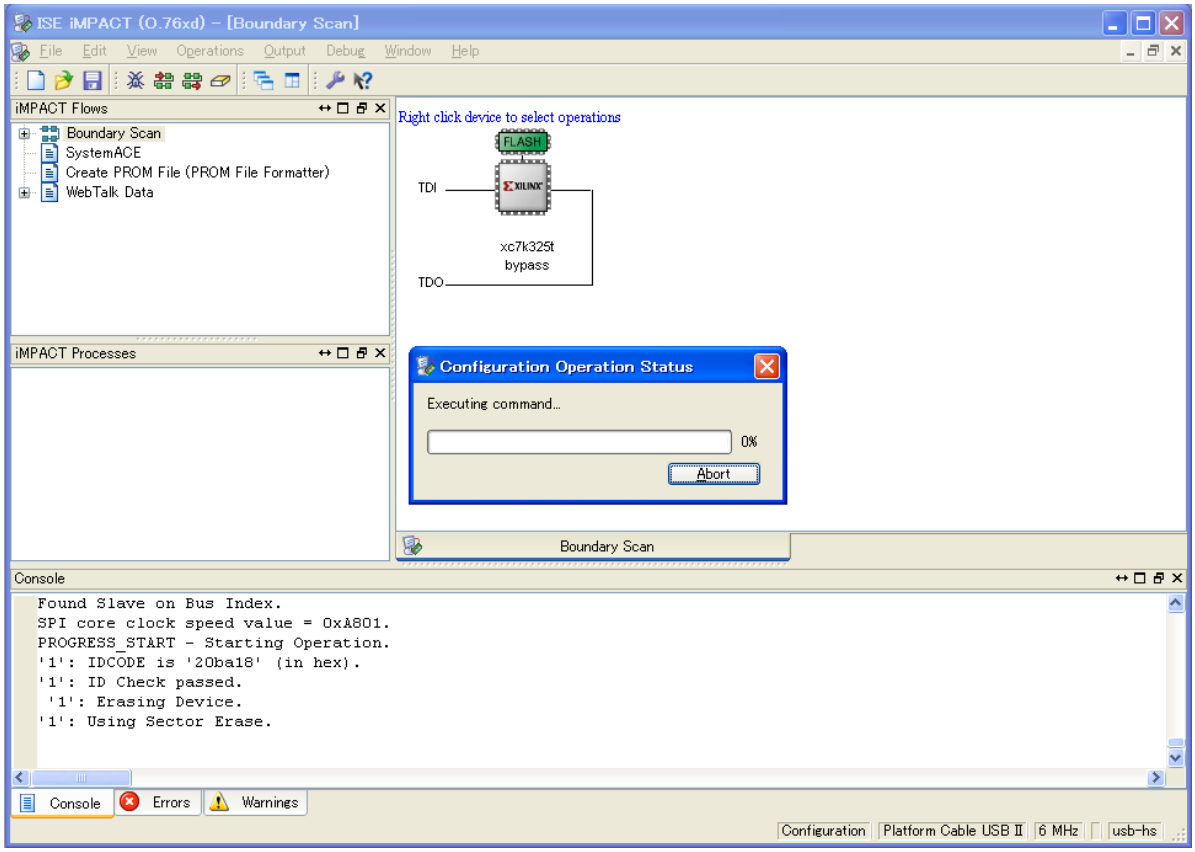

Figure 8-24 Download operation 7

8. If iMPACT shoes the “Program Succeeded”, finished to downloading.

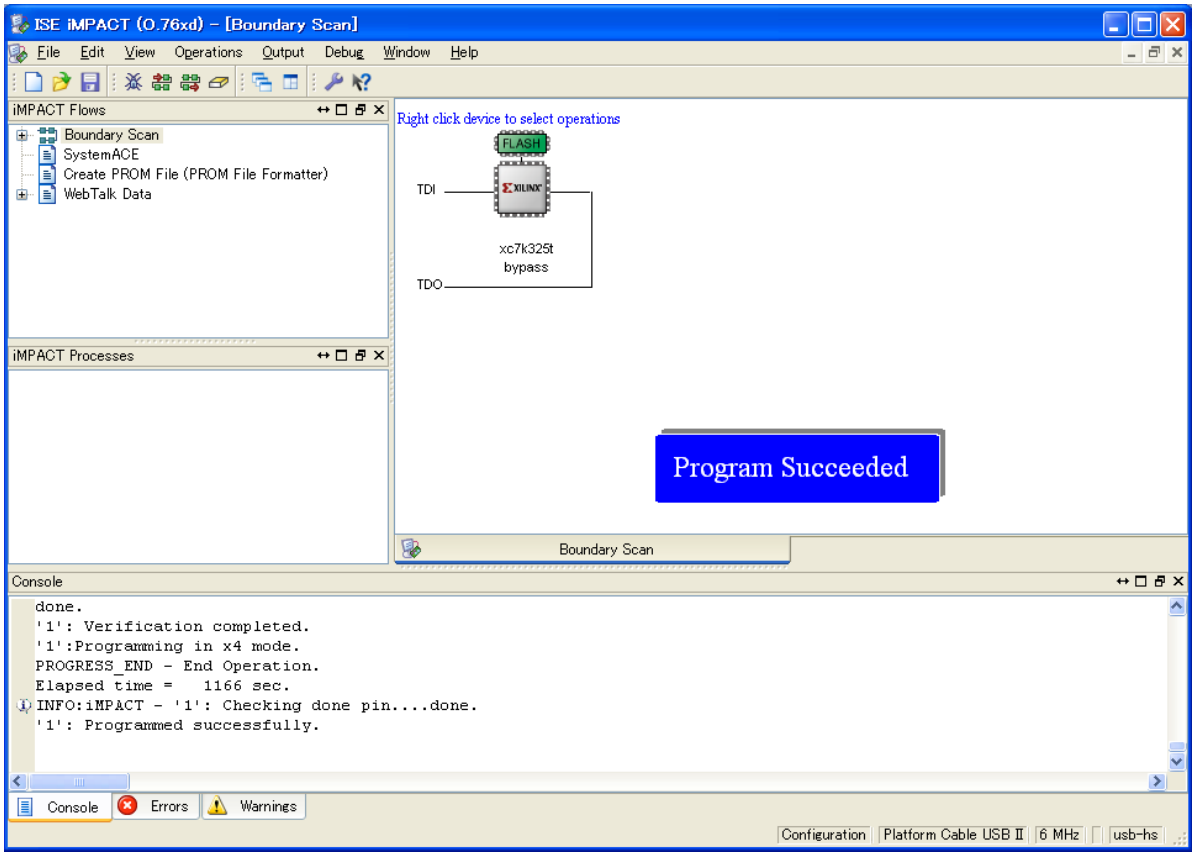

Figure 8-25 Download operation 8

9. FPGA needs to configured by SW10(Reconfiguration SW) or Power Off/On.

Figure 8-26 Reconfiguration Switch

10. FPGA configuration states is indicated by LED23 and LED24
    LED23(Green): Configuration done
    LED24(Red): Configuring or Configuration fail.

Figure 8-27 Configuration Status LED

8.6. Default Settings

Following Figure shows a setting Jumper and DIP switches.

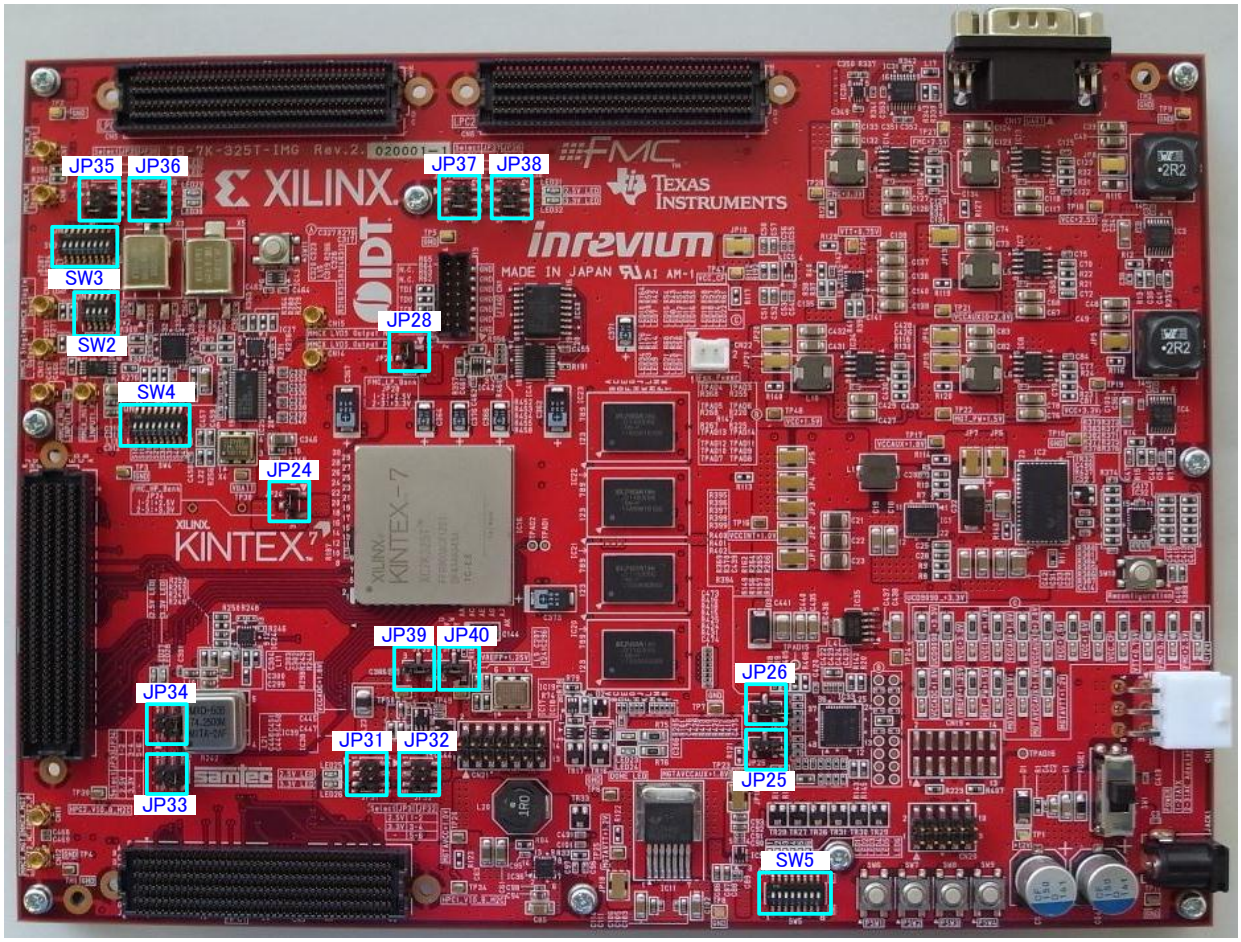

Figure 8-28 Jumper and DIP Switches location

Table 8-1 Default Settings

No.	Silk No.	Initial Setting	Function
1	SW2,3	ALL OFF	Video Clock setting
2	SW4	ALL OFF	Clock select setting
3	SW5	ALL OFF	DIP Switches setting
4	JP24	1-2	FMC_HP_Bank voltage(**2.5V** / 3.3V)
5	JP25	Open	PMBUS_ADDR0(GND_90.9K,1% / GND_41.2K,1% / **No Supply**)
6	JP26	Open	PMBUS_ADDR1(GND_90.9K,1% / GND_41.2K,1% / **No Supply**)
7	JP28	1-2	FMC_LP_Bank voltage (**2.5V** / 3.3V)
8	JP31,32	5-6	FMC_HPC1 VADJ voltage (2.5V / 3.3V / **No Supply**)
9	JP33,34	5-6	FMC_HPC2 VADJ voltage (2.5V / 3.3V / **No Supply**)
10	JP35,36	5-6	FMC_LPC1 VADJ voltage (2.5V / 3.3V / **No Supply**)
11	JP37,38	5-6	FMC_LPC2 VADJ volage (2.5V / 3.3V / **No Supply**)
12	JP39	1-2	VCCADC voltage (**VCCAUX** / VCCADC / No Supply)
13	JP40	1-2	VREFPcoltage (**XADC_AGND** / VREFP / No Supply)

Bold Character are default setting.

EC Declaration of Conformity

Tokyo Electron Device Limited.

We declare, under our solo responsibility, that the product:

Product: Kintex-7 FPGA Evaluation Board
Model: TB-7K-325T-IMG

To which this declaration relates complies with the provisions of following European Directives:

73/23/EEC as amended by 93/68/EEC – Directive on the harmonization of the laws of Member States relating to electrical equipment designed for use within certain voltage limits;
89/336/EEC as amended by 92/31/EEC and 93/68/EEC – Directive on the approximation of the laws of the Member States relating to electromagnetic compatibility.
2004/108/EC as amended by

Allied Harmonized Standards

EN 55022(2010) Class A
EN 61000-3-2(2006) + A2(2009)
EN 61000-3-3(2008)
EN 55024(2010)

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