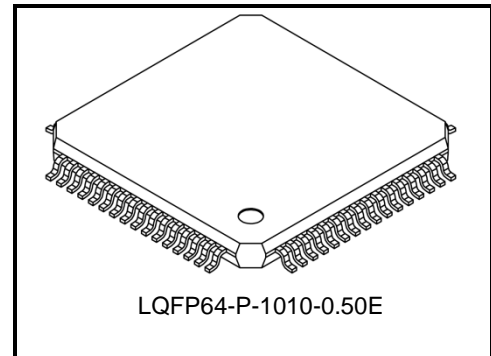


TOSHIBA Bi-CMOS Integrated Circuit Silicon Monolithic

# TB9081FG

Automotive GATE-driver for brushless motor driver

TB9081FG is Pre-driver IC for brushless motor. Fail-safe relay pre-drivers are also built in in addition to 3-phase pre-drivers. The charge pump, the motor current detection circuit, the oscillation, and the SPI-Interface-control circuit are built in. The miscellaneous abnormal detections are carried and the operation after failure detection conditions and failure detections can be set up. About each setup, these can set up through a SPI communication. Also, it have built-in ABIST / LBIST functions for diagnosing the normal operation of the miscellaneous abnormal detection function.



Weight: 0.35g (typ.)

## Features

- 3-phase pre-drivers : PWM control to 20kHz
- Build-in fail-safe relay pre-drivers
- Build-in Charge Pump
- High response Current Detection circuit
- Miscellaneous-abnormal-detection circuits  
(Under voltage (VB, VCC) / Over voltage (VB, VCC) / Over temp. / FET short detection)
- Build-in ABIST/LBIST functions
- Operating voltage range : VB=4.5 to 18V, VCC=3.0 to 5.5V
- Operational temperature range : -40 to 125°C
- Package : LQFP-64pin (0.5mm pitch)

The product(s) is/are compatible with RoHS regulations (EU directive 2011 / 65 / EU) as indicated, if any, on the packaging label ("[[G]]/RoHS COMPATIBLE", "[[G]]/RoHS [[Chemical symbol(s) of controlled substance(s)]]", "RoHS COMPATIBLE" or "RoHS COMPATIBLE, [[Chemical symbol(s) of controlled substance(s)]]>MCV").

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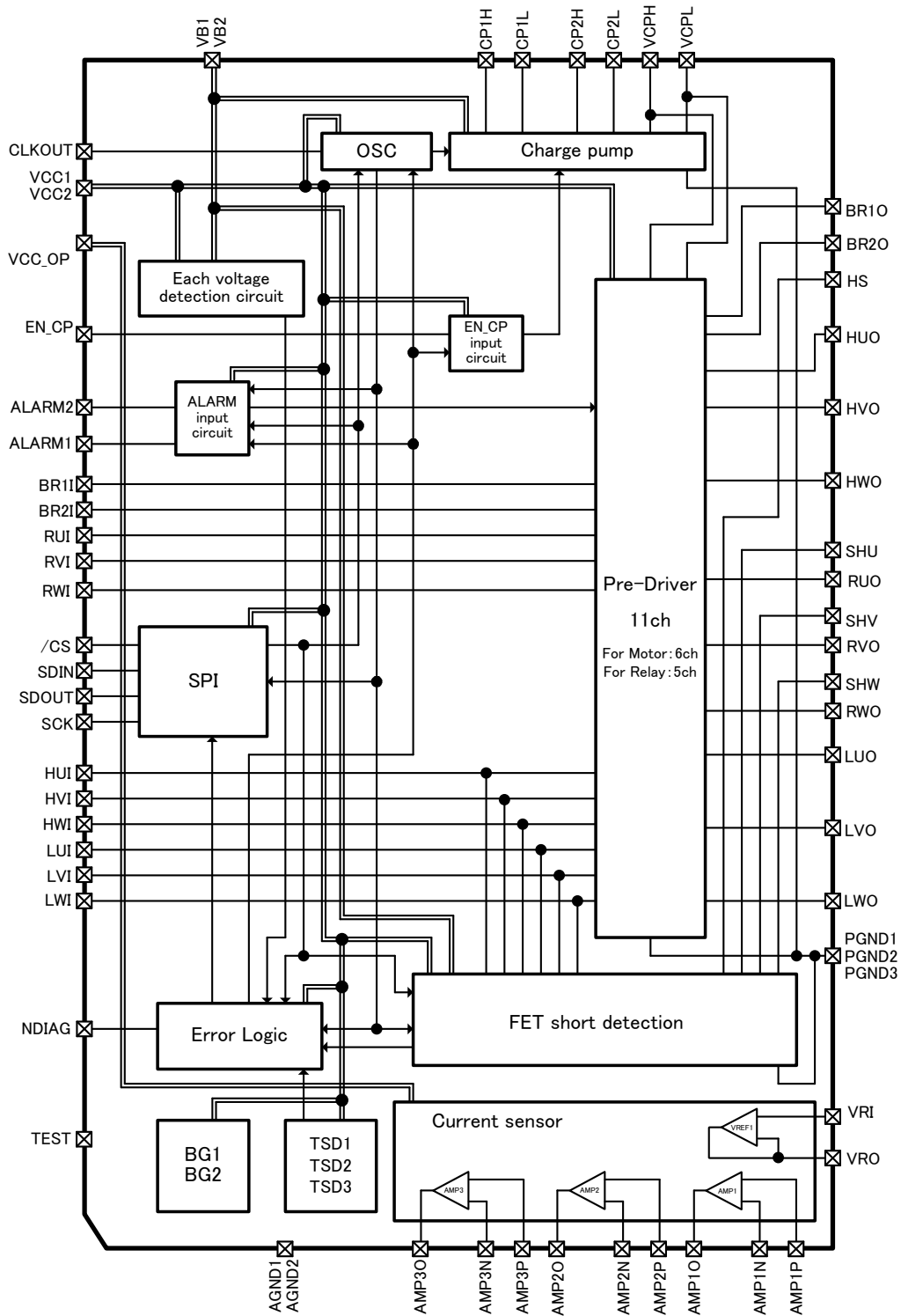
- (1) Charge pump circuit
- (2) Pre-drivers
- (3) Current detector
- (4) An oscillation/frequency divider
- (5) Abnormality detecting circuit
- (6) ALARM input circuit
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- (9) SPI-Interface-control circuit

Reference Circuit Diagram

PACKAGE

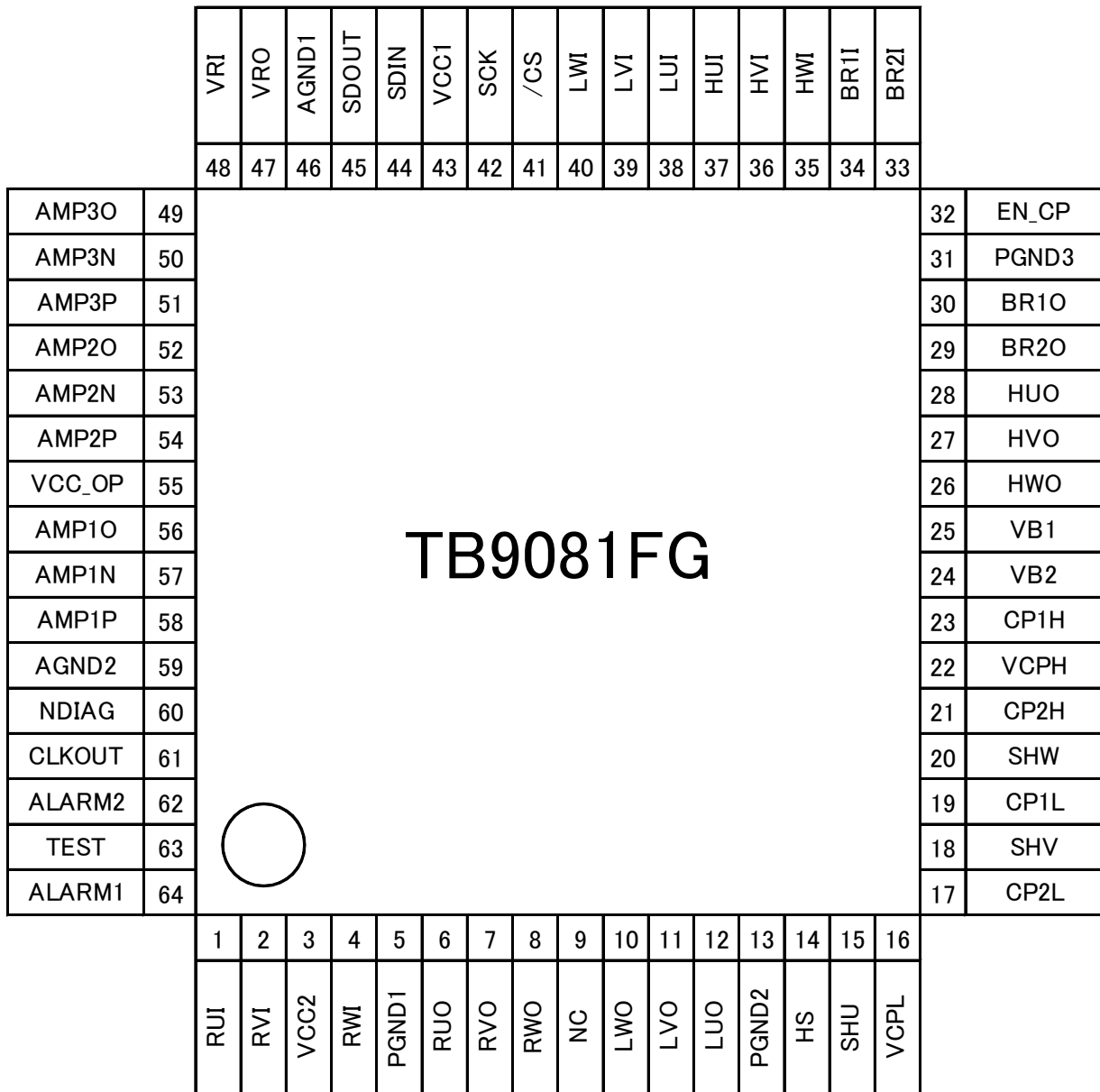
RESTRICTIONS ON PRODUCT USE

Internal Block Diagram



Notes 1: Some of the functional blocks,circuit,or constants in the block diagram may be omitted or simplified for explanatory purpose.

**Package Pin Layout (Top View)**



## Pin Description

Pin No.	Symbol	Input/output	Definition	Pull-Up/Down		Notes
1	RUI	IN	Pre-Driver Input RU (Motor Relay)	Pull-Down	50k $\Omega$	-
2	RVI	IN	Pre-Driver Input RV (Motor Relay)	Pull-Down	50k $\Omega$	-
3	VCC2	Power supply	Power supply 2 (3.3V or 5V)	-	-	-
4	RWI	IN	Pre-Driver Input RW (Motor Relay)	Pull-Down	50k $\Omega$	-
5	PGND1	GND	Power GND1	-	-	-
6	RUO	OUT	Pre-Driver Output RU (Motor Relay)	-	-	push-pull
7	RVO	OUT	Pre-Driver Output RV (Motor Relay)	-	-	push-pull
8	RWO	OUT	Pre-Driver Output RW (Motor Relay)	-	-	push-pull
9	NC	-	-	-	-	-
10	LWO	OUT	Pre-Driver Output LW	-	-	push-pull
11	LVO	OUT	Pre-Driver Output LV	-	-	push-pull
12	LUO	OUT	Pre-Driver Output LU	-	-	push-pull
13	PGND2	GND	Power GND2	-	-	-
14	HS	IN	Pre-Driver High-side Drain Input	-	-	-
15	SHU	IN	Motor Connect PIN U-phase	-	-	-
16	VCPL	Power supply	Charge-pump voltage (for low sides)	-	-	-
17	CP2L	OUT	2nd Charge Pump Drive Output	-	-	push-pull
18	SHV	IN	Motor Connect PIN V-phase	-	-	-
19	CP1L	OUT	1st Charge Pump Drive Output	-	-	push-pull
20	SHW	IN	Motor Connect PIN W-phase	-	-	-
21	CP2H	IN/OUT	2nd Charge Pump Output	-	-	-
22	VCPL	Power supply	Charge-pump voltage (for high sides)	-	-	-
23	CP1H	IN/OUT	1st Charge Pump Output	-	-	-
24	VB2	Power supply	Power Supply2 (Battery 12V)	-	-	-
25	VB1	Power supply	Power Supply1 (Battery 12V)	-	-	-
26	HWO	OUT	Pre-Driver Output HW	-	-	push-pull
27	HVO	OUT	Pre-Driver Output HV	-	-	push-pull
28	HUO	OUT	Pre-Driver Output HU	-	-	push-pull
29	BR2O	OUT	Pre-Driver Output BR2 (Power supply relay)	-	-	push-pull
30	BR1O	OUT	Pre-Driver Output BR1 (Power supply relay)	-	-	push-pull
31	PGND3	GND	Power GND 3	-	-	-
32	EN_CP	IN	Charge-pump enable signal	Pull-Down	50k $\Omega$	-
33	BR2I	IN	Pre-Driver Input BR2 (Power supply relay)	-	-	-
34	BR1I	IN	Pre-Driver Input BR1 (Power supply relay)	-	-	-
35	HWI	IN	Pre-Driver Input HW	Pull-Down	50k $\Omega$	-
36	HVI	IN	Pre-Driver Input HV	Pull-Down	50k $\Omega$	-
37	HUI	IN	Pre-Driver Input HU	Pull-Down	50k $\Omega$	-
38	LUI	IN	Pre-Driver Input LU	Pull-Down	50k $\Omega$	-
39	LVI	IN	Pre-Driver Input LV	Pull-Down	50k $\Omega$	-
40	LWI	IN	Pre-Driver Input LW	Pull-Down	50k $\Omega$	-
41	/CS	IN	SPI chip select	Pull-Up	50k $\Omega$	-
42	SCK	IN	SPI clocked into	Pull-Down	50k $\Omega$	-
43	VCC1	Power supply	Power supply 1 (3.3V or 5V)	-	-	-
44	SDIN	IN	SPI input	Pull-Down	50k $\Omega$	-
45	SDOUT	OUT	SPI Output	-	-	push-pull
46	AGND1	GND	The GND 1 for analog circuits	-	-	-
47	VRO	OUT	Reference voltage amplifier Output	-	-	-
48	VRI	IN	Reference voltage amplifier input	-	-	-
49	AMP3O	OUT	Current-detection amplifier Output 3	-	-	-
50	AMP3N	IN	Current-detection amplifier input 3 (-)	-	-	-
51	AMP3P	IN	Current-detection amplifier input 3 (+)	-	-	-
52	AMP2O	OUT	Current-detection amplifier Output 2	-	-	-
53	AMP2N	IN	Current-detection amplifier input 2 (-)	-	-	-
54	AMP2P	IN	Current-detection amplifier input 2 (+)	-	-	-
55	VCC_OP	Power supply	The power supply for Current-detection amplifier (5V/3.3V)	-	-	-
56	AMP1O	OUT	Current-detection amplifier Output 1	-	-	-
57	AMP1N	IN	Current-detection amplifier input 1 (-)	-	-	-
58	AMP1P	IN	Current-detection amplifier input 1 (+)	-	-	-
59	AGND2	GND	The ground 2 for analog circuits	-	-	-
60	NDIAG	OUT	Error Output Pin	-	-	push-pull
61	CLKOUT	OUT	Clock output	-	-	push-pull
62	ALARM2	IN	Pre-driver enable 2	Pull-Down	50k $\Omega$	-
63	TEST	IN	Test terminal	Pull-Down	50k $\Omega$	-
64	ALARM1	IN	Pre-driver enable 1	Pull-Down	50k $\Omega$	-

Functional descriptions

(1) Charge pump circuit

TB9081FG build in Charge pump for Pre-Drivers and it can control external Nch MOSFETs directly. Two charge pump voltages the object for the high side drive of a motor and the object for the relay drive of a motor, and for the low side drive of a motor is generated.

The charge pump voltage (VCPH) for a high side drive and a relay drive control by an internal circuit, and if VCPH goes up to VB+12V (Typ.), a charge pump will suspend operation. Furthermore, in consideration of an overvoltage state, if VCPH goes up to 37V, a charge pump will stop, and if VCPH is less than 36.5V, a charge pump will resume operation.

The charge pump voltage (VCPL) for a low side drive is generated from VCPH. If VCPL goes up to (16V), a clamp will start and it will not become the voltage more than clamp voltage.

It is possible to build the switching circuit (CP\_SW) in the VB side of a charge pump circuit, to make a transistor turn off by CP\_SW, and to stop the supply to VCPH from VB. VCC voltage turns off the transistor of CP\_SW on condition of the conditions as for which below VCC voltage detection voltage becomes, or EN\_CP="L". For details, please refer to a (7) EN\_CP circuit.

Moreover, it is possible to operate or stop a charge pump by terminal EN\_CP. The charge pump operates at the time of EN\_CP="H", and it stops at the time of EN\_CP="L" and also suspends the supply to VCPH from VB .

A VCPH Output voltage is set to 0V at the time of the charge-pump stop by EN\_CP="L".

When the charge pump is stopped by the control in the IC, VCPH output voltage will become the "VB-3VF".

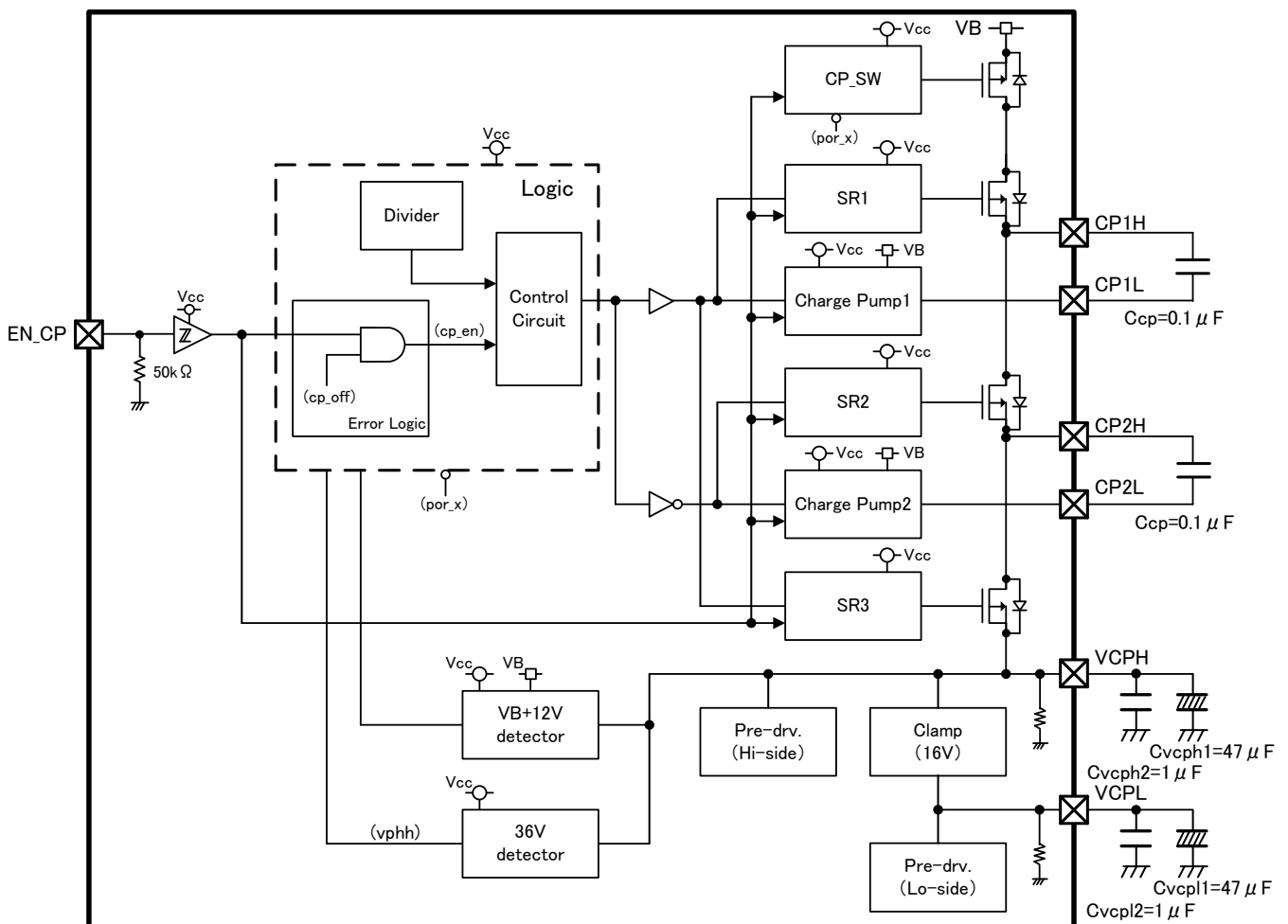


Fig.1- a Charge-pump-circuit Block Diagram

(2) Pre drivers

TB9081FG has the pre-driver circuit it is for the motor relay drive , for the power relay drive , for the low-side drive of the motor and for the high-side drive of the motor. Each pre-driver circuit has a respective input and output terminals are controlled by a signal inputted to the input terminals.

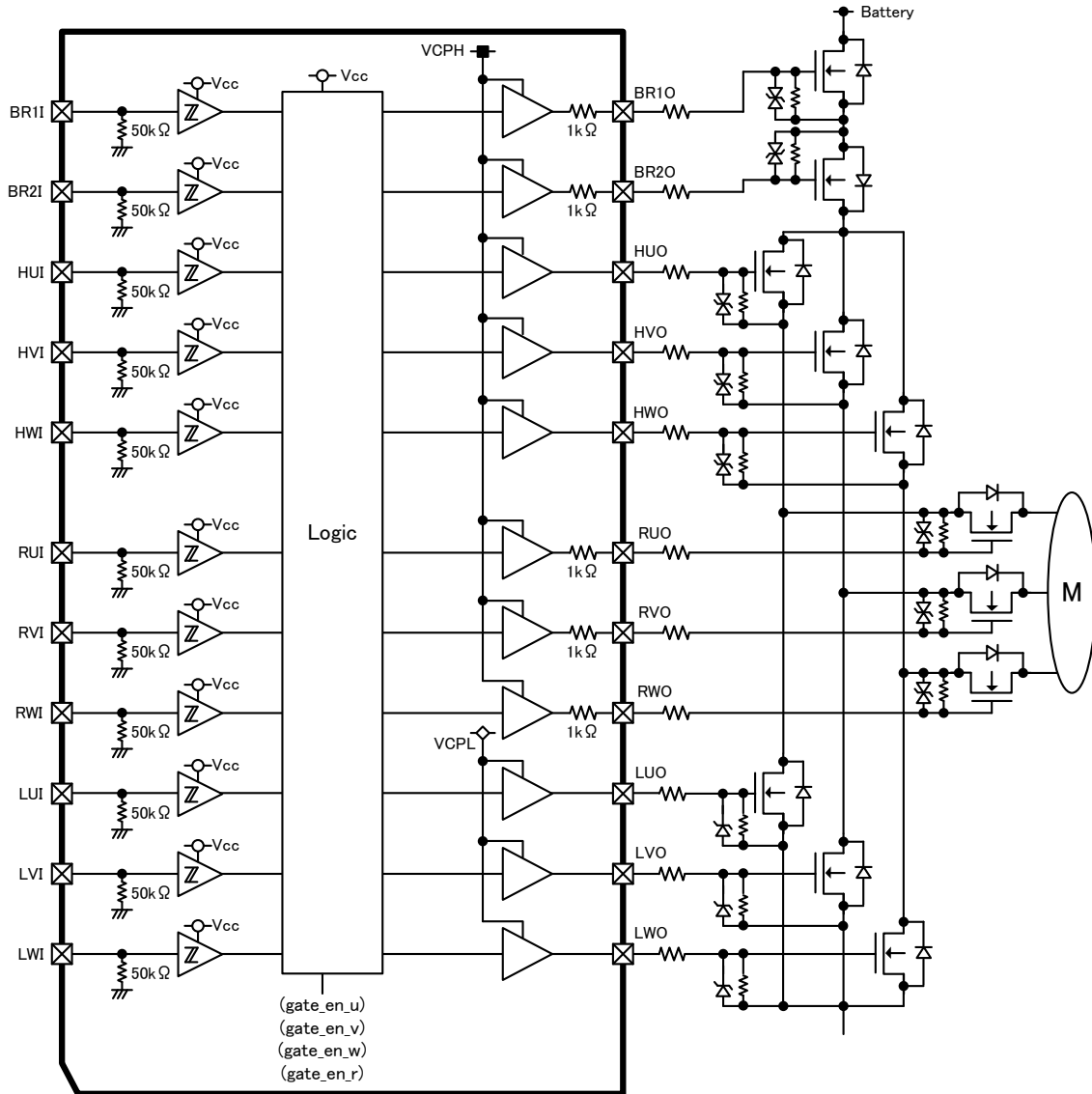


Fig.2- a Pre-drivers Block Diagram

<A power supply relay drive circuit, a motor relay drive circuit>

A power supply relay drive circuit is a circuit which controls FET for a relay on the battery power-supply side.

A motor relay drive circuit is a circuit which controls FET for a relay on the motor side.

A truth table is shown in table 2-a and 2-b. Refer to the (6) ALARM input circuit for the details of the internal signal (gate\_en\_r) in a truth table.

Moreover, resistance 1kΩ is built in the output of a power supply relay drive and a motor relay drive.

Furthermore, the diode for prevention of backflow at the time of reverse connection is built in the output of a power supply relay drive circuit.

- Table 2- a Input/output truth table 1 (power supply relay drive circuit)

- Power supply relay drive circuit 1

Input	Internal signal	Output	Notes
BR1I	(gate_en_r)	BR1O	
L	H	L	-
H	H	H	-
*	L	L	-

\*:Don't care

- Power supply relay drive circuit 2

Input	Internal signal	Output	Notes
BR2I	(gate_en_r)	BR2O	
L	H	L	-
H	H	H	-
*	L	L	-

\*:Don't care

- Table 2- b Input/output truth Table 2 (motor relay drive circuit)

- Motor relay drive circuit 1 (U phase)

Input	Internal signal	Output	Notes
RU1	(gate_en_r)	RU0	
L	H	L	-
H	H	H	-
*	L	L	-

\*:Don't care

- Motor relay drive circuit 2 (V phase)

Input	Internal signal	Output	Notes
RVI	(gate_en_r)	RVO	
L	H	L	-
H	H	H	-
*	L	L	-

\*:Don't care

- Motor relay drive circuit 3 (W phase)

Input	Internal signal	Output	Notes
RWI	(gate_en_r)	RWO	
L	H	L	-
H	H	H	-
*	L	L	-

\*:Don't care



<A high side drive circuit, a low side drive circuit>

A high side drive circuit is a circuit which drives FET of the high side of a motor. A low side drive circuit is a circuit which drives FET of the low side of a motor. A high side drive circuit and a low side drive circuit built in each 3ch.

An input signal (HUI/HVI/HWI, LUI/LVI/LWI) is changed by a control block, and output (HUO/HVO/HWO, LUO/LVO/LWO) is outputted. A truth table is shown in table 2-c. Refer to the (6) ALARM input circuit for the details of the internal signal (gate\_en\_u, gate\_en\_v, gate\_en\_w) in a truth table.

When HUI/LUI, HVI/LVI, and HWI/LWI are H/H, an output will be L/L (prohibition input). The operation at the time of prohibition input detection can be set up through a SPI communication.

Moreover, the current at the time of Turn on/Turn off of a high side drive circuit and a low side drive circuit is the current limit after 5  $\mu$ s (min). This current-limiting time can be set up a 3 value or no limit time through a SPI communication.

- Table 2- c Input/output truth table 3 (a high side drive circuit, a low side drive circuit)

- FET drive circuit 1 (U phase)

Input		Internal signal (gate_en_u)	Output		Notes
HUI	LUI		HUO	LUO	
L	L	H	L	L	-
L	H	H	L	H	-
H	L	H	H	L	-
H	H	H	<u>L</u>	<u>L</u>	Short circuit mode
*	*	L	L	L	-

\*:Don't care

- FET drive circuit 2 (V phase)

Input		Internal signal (gate_en_v)	Output		Notes
HVI	LVI		HVO	LVO	
L	L	H	L	L	-
L	H	H	L	H	-
H	L	H	H	L	-
H	H	H	<u>L</u>	<u>L</u>	Short circuit mode
*	*	L	L	L	-

\*:Don't care

- FET drive circuit 3 (W phase)

Input		Internal signal (gate_en_w)	Output		Notes
HWI	LWI		HWO	LWO	
L	L	H	L	L	-
L	H	H	L	H	-
H	L	H	H	L	-
H	H	H	<u>L</u>	<u>L</u>	Short circuit mode
*	*	L	L	L	-

\*:Don't care

(3) Current detector

TB9081FG are built three amplifiers for motor-current detection and one amplifier for reference voltage generation (Fig3- a).

The amplifiers for motor-current detection can amplify the difference voltage which produces according to the current which flows through the shunt resistance connected to the motor actuator.

The amplifier for reference voltage generation is used as buffer amplifier for reference voltage generation.

As an external configuration of the current detection, it is available in either 1 shunt configuration or 3 shunt configuration.

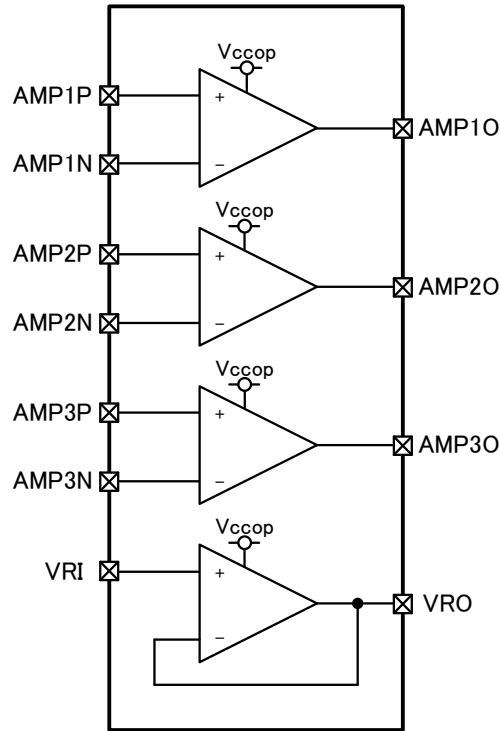


Fig.3- a Motor-current detection circuit block figure

(4) Oscillator /Divider

The oscillator has composition with built-in CR, and an Oscillation frequency is  $F_c=4\text{MHz}$  (typ.). An oscillator will start operation, if  $V_{cc}$  rises, and a divider starts operation after internal signal ( $por\_x$ ) release. 4 MHz ( $clk4m$ ) is used as the system clock of a logic circuit, and an operation clock of the digital filter of the short detector of external FET.

Clock 1MHz ( $clk1m$ ), it is used as an operation clock of the digital filter of an ALARM detector.

Clock 500kHz ( $clk500k$ ), it is used as an operation clock of a charge pump.

Clock 15.625kHz ( $clk16k$ ), it is used as an operation clock of ABIST.

CLKOUT output (terminal) will output a clock set by the SPI ( $clk4m$ ,  $clk500k$ ,  $clk16k$ ).

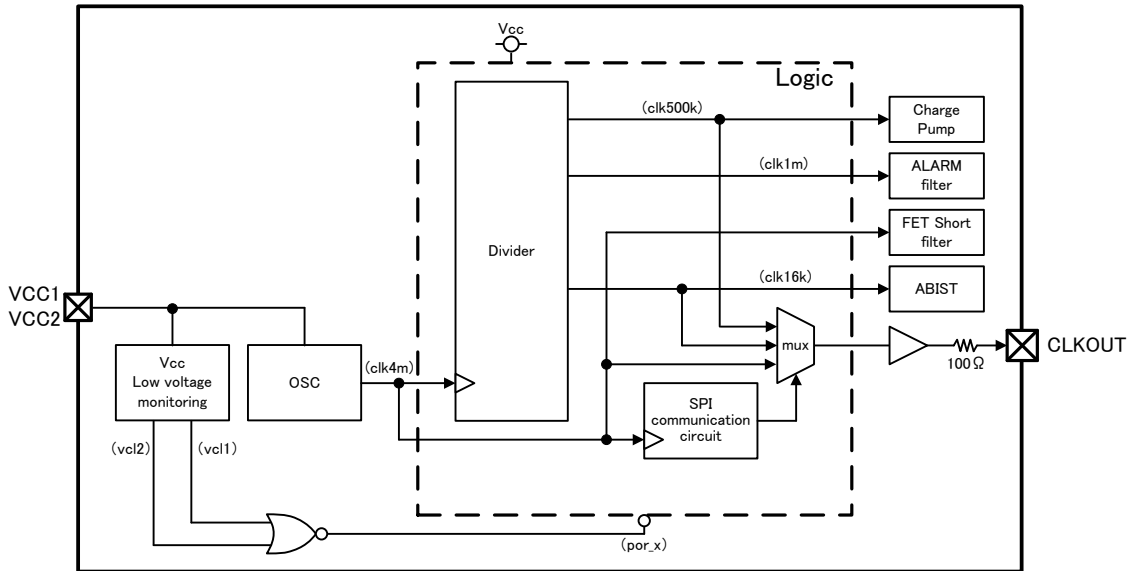


Fig.4- a An oscillator, divider Block Diagrams

(5) Miscellaneous abnormal detection circuit

TB9081FG is built in miscellaneous abnormal detection circuit, such as low voltage detection(VB1, VB2, VCC1, VCC2), high voltage detection(VB1, VB2, VCC1, VCC2), over temperature detection, external FET short detection and frequency abnormal detection.

(6) ALARM input circuit

As an input terminal of an ALARM signal, TB9081FG have two terminals of ALARM1 and ALARM2.

An ALARM signal controls Enable/Disable of the Pre-drivers (a FET drive circuit, a motor relay drive circuit, a power supply relay drive circuit).

In the case of ALARM1="L" or ALARM2="L", the Pre-drivers will be Disable. In the case of ALARM1="H" and ALARM2="H", Enable/Disable is decided by the input and internal signal of each Pre-drivers.

Also, the input side of the ALARM1 and ALARM2 terminal has a built-in digital filter (DF) for noise removal. Digital filter time can be set through the SPI communication.

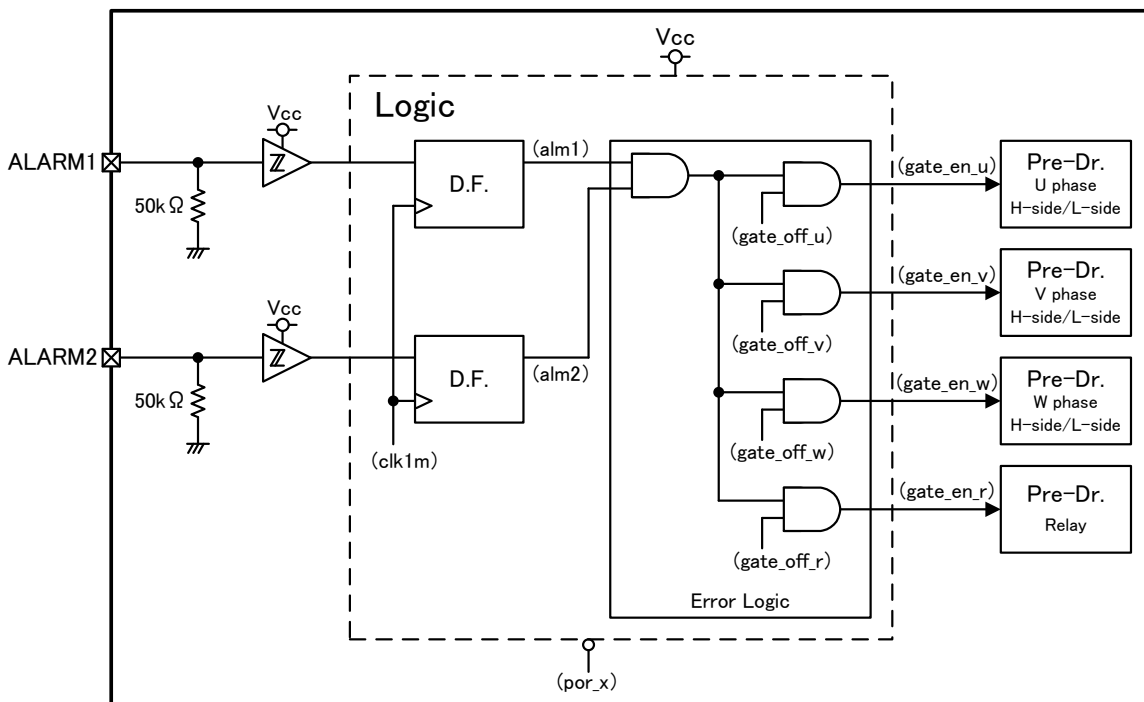


Fig.6-a FET drive circuit control block diagram

Table 6-a FET drive circuit control truth Table

Input Signal		Internal Input Signal					Internal control signal				FET drive circuit
ALARM1	ALARM2	(por_x)	(gate_off_u)	(gate_off_v)	(gate_off_w)	(gate_off_r)	(gate_en_u)	(gate_en_v)	(gate_en_w)	(gate_en_r)	
L	*	*	*	*	*	*	L	L	L	L	Disable
*	L	*	*	*	*	*	L	L	L	L	Disable
*	*	L	*	*	*	*	L	L	L	L	Disable
H	H	H	L	-	-	-	L	-	-	-	U phase Disable
H	H	H	H	-	-	-	H	-	-	-	U phase Enable
H	H	H	-	L	-	-	-	L	-	-	V phase Disable
H	H	H	-	H	-	-	-	H	-	-	V phase Enable
H	H	H	-	-	L	-	-	-	L	-	W phase Disable
H	H	H	-	-	H	-	-	-	H	-	W phase Enable
H	H	H	-	-	-	L	-	-	-	L	Relay Disable
H	H	H	-	-	-	H	-	-	-	H	Relay Enable

(Note 1) "\*":Don't care

(Note 2) Although "-":gate\_off\_\* and gate\_en\_\* have logic dependence in phase, the logic dependence to other phase is nothing.

(7) EN\_CP input circuit

EN\_CP signal controls Enable/Disable of a charge pump circuit.

In the case of input signal EN\_CP= "L", the charge pump circuit will be Disable. In the case of EN\_CP="H", Enable/Disable of the charge pump circuit is decided by an internal signal.

Also, the charge pump SW circuit (CP\_SW) will be Disable in case of input signal EN\_CP = "L" or the internal signal (por\_x) = "L". In the case of EN\_CP = (por\_x) = "H", it will be Enable.

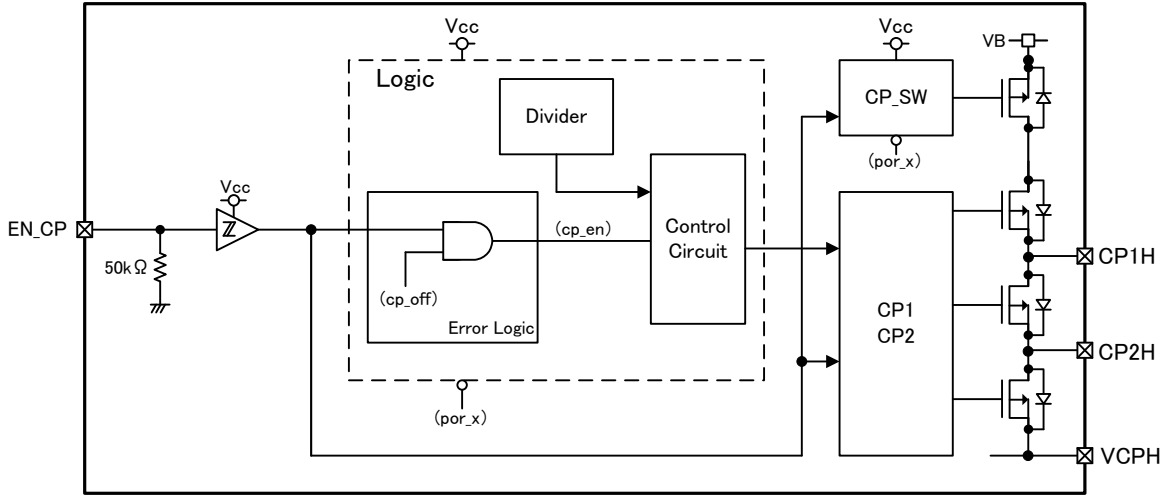


Fig.7-a EN\_CP input circuit Block Diagrams

table 7-a Charge-pump-circuit control truth table

Input Signal	Internal Input Signal		Internal control signal	Charge pump circuit	Charge pump SW circuit
	(por_x)	(cp_off)	(cp_en)		
L	*	*	L	Disable	Disable
H	L	*	L	Disable	Disable
H	H	L	L	Disable	Enable
H	H	H	H	Enable	Enable

(Note) "\*":Don't care

**(8) ABIST function**

At the time of IC starting, it is diagnosed whether miscellaneous abnormal detection is functioning normally.

At the time of IC starting, a divider starts operation after VCC low voltage release, and it starts diagnosis of ABIST after LBIST completion. Diagnosis of ABIST is performed even when a judgment of LBIST is NG.

A diagnostic part is as follows.

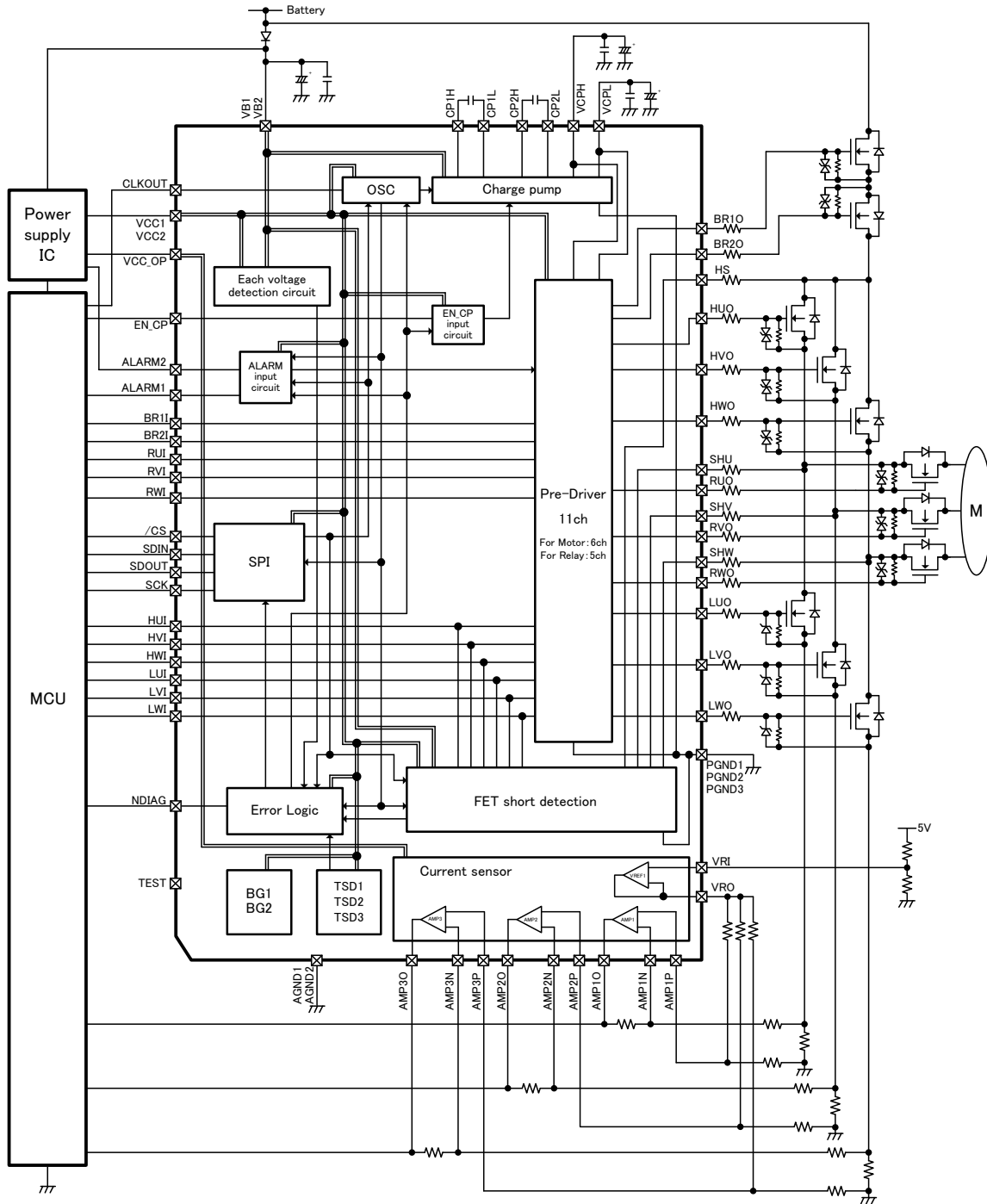
VB1/VB2 high voltage detection, VCC high voltage detection, VCPH clamp voltage detection, over temperature detection, frequency abnormal detection (low frequency side)

**(9) SPI communication circuit**

The SPI communication circuit consists of an SPI core circuit and a register read circuit block.

Only when /CS is L, communication with a microcomputer is attained. A microcomputer writes data in SDIN at the rising edge of a clock, and IC reads data at the following falling edges. Moreover, IC writes data in SDOOUT at the rising edge of a clock, and a microcomputer reads data at the following falling edges. SDIN receives the data bit from a microcomputer in order from MSB to LSB. SDOOUT transmits a data bit to a microcomputer in order from MSB to LSB. An output is push-pull composition and will be a Hi-Z at the time of /CS="H". Moreover, inside IC, the /CS terminal have pull-up by resistance, and the SDIN and SCK terminal have pull-down by resistance.

Reference Circuit Diagram



<Notes>

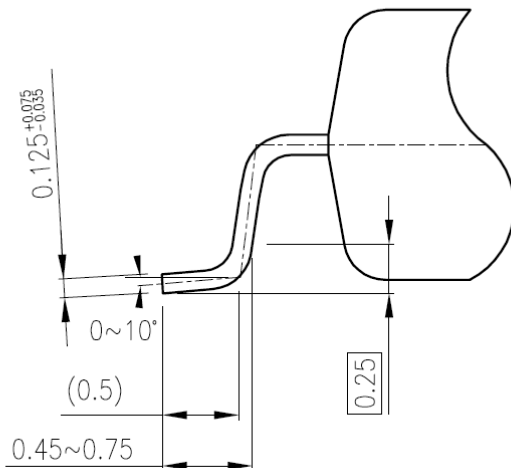
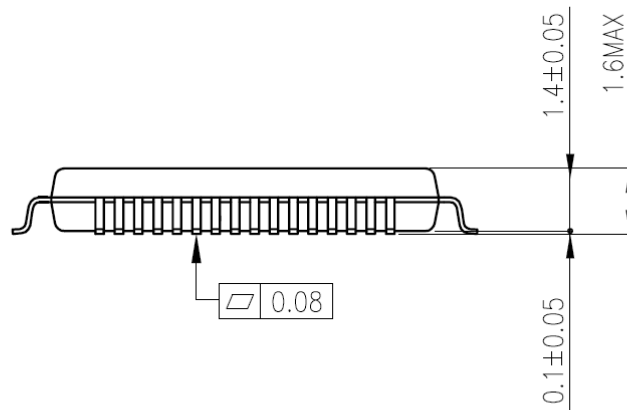
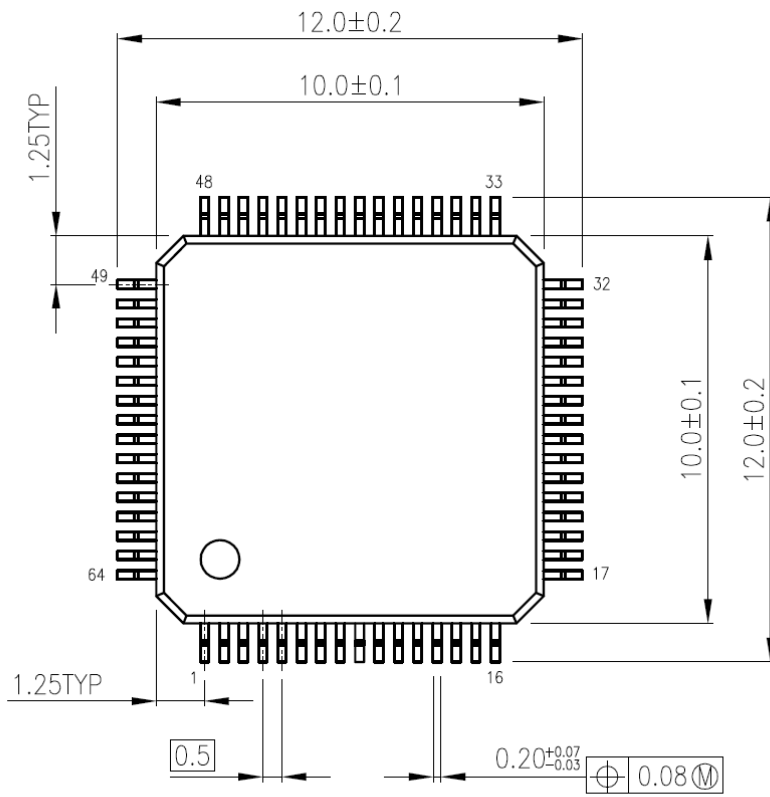
- \* The circuit constant of these is an Application Circuit Examples, and is not guaranteed. On the conditions which assumed the application environment on units boards, please determine an external circuit after fully carrying out evaluation and a check.
- \* The smoothing capacitor which carries out external to a power supply pin (VB1/VB2, VCC1/VCC2, VCC\_OP), Please arrange near the origin of IC as much as possible.
- \* Please give me the power supply of the resistance partial pressure connected to a VRI terminal as VCC\_OP and the power supply.
- \* Please also consider notes of each block in the case of a unit design.
- \* Please do not carry out incorrect wearing. There is a possibility of causing destruction of IC and damage to apparatus.



**PACKAGE**

LQFP64-P-1010-0.50E

Unit: mm



Weight: 0.35g (typ.)

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