TEXAS INSTRUMENTS

**TLV809**

SLVSA03D – JUNE 2010 – REVISED MARCH 2016

# TLV809
# 3-Pin Supply Voltage Supervisor

## 1 Features

- Precision Supply Voltage Monitor:
  2.5 V, 3 V, 3.3 V, 5 V
- Power-On Reset Generator with a
  Fixed Delay Time of 200 ms
- Supply Current: 9 µA (Typical)
- Temperature Range: –40°C to +85°C
- 3-Pin SOT-23 Package
- Pin-for-Pin Compatible with the MAX809

## 2 Applications

- DSPs, Microcontrollers, and Microprocessors
- Wireless Communication Systems
- Portable and Battery-Powered Equipment
- Programmable Controls
- Intelligent Instruments
- Industrial Equipment
- Notebook and Desktop Computers
- Automotive Systems

## 3 Description

The TLV809 family of supervisory circuits provides circuit initialization and timing supervision, primarily for digital signal processors (DSPs) and processor-based systems.

During power-on, $\overline{\text{RESET}}$ is asserted when the supply voltage ($V_{DD}$) becomes greater than 1.1 V. Thereafter, the supervisory circuit monitors $V_{DD}$ and keeps $\overline{\text{RESET}}$ active as long as $V_{DD}$ remains below the threshold voltage, $V_{IT}$. An internal timer delays the return of the output to the inactive state (high) to ensure proper system reset. The delay time ($t_{d(typ)}$ = 200 ms) starts after $V_{DD}$ rises above the threshold voltage, $V_{IT}$. When the supply voltage drops below the $V_{IT}$ threshold voltage, the output becomes active (low) again. No external components are required. All devices in this family have a fixed sense-threshold voltage ($V_{IT}$) set by an internal voltage divider.

The TLV803 has an active-low, push-pull RESET output. See the TLV803 for an open-drain RESET output and the TLV810 for a push-pull, active-high RESET output.

This product family is designed for supply voltages of 2.5 V, 3 V, 3.3 V, and 5 V. The circuits are available in a 3-pin SOT-23 package. The TLV809 devices are characterized for operation over a temperature range of –40°C to +85°C.
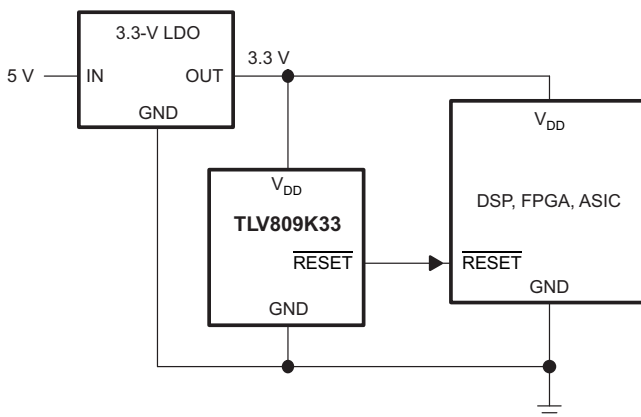
### Device Information[1]

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| TLV809 | SOT-23 (3), DBV | 2.90 mm × 1.60 mm |
| | SOT-23 (3), DBZ | 2.92 mm × 1.30 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

**Typical Application**

## Table of Contents

## 4  Revision History

**Changes from Revision C (February 2012) to Revision D**                                                                   **Page**

**Changes from Revision B (September 2010) to Revision C**                                                                   **Page**

**Changes from Revision A (July 2010) to Revision B**                                                                       **Page**

## 5   Voltage Options

| PRODUCT | THRESHOLD VOLTAGE |
|---|---|
| TLV809J25 | 2.25 V |
| TLV809L30 | 2.64 V |
| TLV809K33 | 2.93 V |
| TLV809I50 | 4.55 V |

## 6   Pin Configuration and Functions

**DBV, DBZ Packages**
**3-Pin SOT-23**
**Top View**

```
GND ──┤ 1      │
                │
              3 ├── V_DD
                │
RESET ─┤ 2      │
```
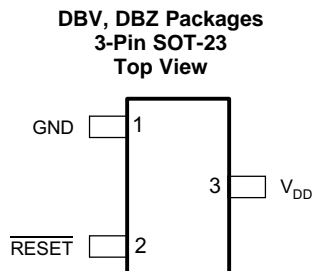
**Pin Functions**

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| **NO.** | **NAME** | | |
| 1 | GND | — | Ground pin. This pin must be connected to ground with a low-impedance connection. |
| 2 | $\overline{RESET}$ | O | $\overline{RESET}$ pin. $\overline{RESET}$ is an active low signal, asserting when $V_{DD}$ is below the threshold voltage. When $V_{DD}$ rises above $V_{IT}$, there is a delay time ($t_d$) until $\overline{RESET}$ deasserts. $\overline{RESET}$ is a push-pull output stage. |
| 3 | $V_{DD}$ | I | Supply voltage pin. A 0.1-µF ceramic capacitor from this pin to ground is recommended to improve stability of the threshold voltage. |

## 7   Specifications

### 7.1   Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{DD}$ | Supply voltage[2] | | 7 | V |
| | All other pins[2] | −0.3 | 7 | |
| $I_{OL}$ | Maximum low output current | | 5 | mA |
| $I_{OH}$ | Maximum high output current | | −5 | mA |
| $I_{IK}$ | Input clamp current ($V_I < 0$ or $V_I > V_{DD}$) | | ±20 | mA |
| $I_{OK}$ | Output clamp current ($V_O < 0$ or $V_O > V_{DD}$) | | ±20 | mA |
| $T_A$ | Operating free-air temperature | −40 | 85 | °C |
| $T_{stg}$ | Storage temperature | −65 | 150 | °C |

(1)   Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2)   All voltage values are with respect to GND. For reliable operation, do not operate the device at 7 V for more than t = 1000h continuously.

## 7.2 ESD Ratings

|  |  |  | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1] | ±2000 | V |
|  |  | Charged-device model (CDM), per JEDEC specification JESD22-C101[2] | ±500 |  |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 7.3 Recommended Operating Conditions

at specified temperature range (unless otherwise noted)

|  |  | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | 2 |  | 6 | V |
| $C_{IN}$ | $V_{DD}$ bypass capacitor |  | 0.1 |  | µF |
| $T_A$ | Operating free-air temperature range | −40 |  | 85 | °C |

## 7.4 Thermal Information

|  | THERMAL METRIC[1] | TLV809 | | UNIT |
|---|---|---|---|---|
|  |  | DBV (SOT-23) | DBZ (SOT-23) |  |
|  |  | 3 PINS | 3 PINS |  |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 242.1 | 286.9 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 213.0 | 105.6 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 123.4 | 124.4 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 45.7 | 25.8 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 130.9 | 107.9 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | — | — | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

## 7.5 Electrical Characteristics

at $T_A$ = −40°C to +85°C (unless otherwise noted); typical values are at $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | High-level output voltage | $V_{DD}$ = 2.5 V to 6 V, $I_{OH}$ = −500 µA | | $V_{DD}$ − 0.2 | | | V |
| | | $V_{DD}$ = 3.3 V, $I_{OH}$ = −2 mA | | $V_{DD}$ − 0.4 | | | |
| | | $V_{DD}$ = 6 V, $I_{OH}$ = −4 mA | | $V_{DD}$ − 0.4 | | | |
| $V_{OL}$ | Low-level output voltage | $V_{DD}$ = 2 V to 6 V, $I_{OH}$ = 500 µA | | | | 0.2 | V |
| | | $V_{DD}$ = 3.3 V, $I_{OH}$ = 2 mA | | | | 0.4 | |
| | | $V_{DD}$ = 6 V, $I_{OH}$ = 4 mA | | | | 0.4 | |
| | Power-up reset voltage[1] | $V_{DD} \geq$ 1.1 V, $I_{OL}$ = 50 µA | | | | 0.2 | V |
| $V_{IT−}$ | Negative-going input threshold voltage[2] | TLV809J25 | $T_A$ = −40°C to +85°C | 2.20 | 2.25 | 2.30 | V |
| | | TLV809L30 | | 2.58 | 2.64 | 2.70 | |
| | | TLV809K33 | | 2.87 | 2.93 | 2.99 | |
| | | TLV809I50 | | 4.45 | 4.55 | 4.65 | |
| $V_{hys}$ | Hysteresis | TLV809J25 | | | 30 | | mV |
| | | TLV809L30 | | | 35 | | |
| | | TLV809K33 | | | 40 | | |
| | | TLV809I50 | | | 60 | | |
| $I_{DD}$ | Supply current | $V_{DD}$ = 2 V, RESET is unconnected | | | 9 | 12 | µA |
| | | $V_{DD}$ = 6 V, RESET is unconnected | | | 20 | 25 | |
| $C_I$ | Input capacitance | $V_I$ = 0 V to $V_{DD}$ | | | 5 | | pF |

(1) The lowest supply voltage at which $\overline{RESET}$ becomes active. $t_{r, VDD} \geq$ 15 ms/V.
(2) To ensure best stability of the threshold voltage, place a bypass capacitor ( 0.1-µF ceramic) near the supply pins.

## 7.6 Timing Requirements

at $T_A$ = 25°C, $R_L$ = 1 MΩ, and $C_L$ = 50 pF

|  |  |  | **MIN** | **NOM** | **MAX** | **UNIT** |
|---|---|---|---|---|---|---|
| $t_w$ | Pulse duration at $V_{DD}$ | $V_{DD} = V_{IT-} + 0.2$ V, $V_{DD} = V_{IT-} - 0.2$ V | 3 |  |  | µs |

## 7.7 Switching Characteristics

at $T_A$ = 25°C, $R_L$ = 1 MΩ, and $C_L$ = 50 pF

| **PARAMETER** |  |  | **TEST CONDITIONS** | **MIN** | **TYP** | **MAX** | **UNIT** |
|---|---|---|---|---|---|---|---|
| $t_d$ | Delay time |  | $V_{DD} \geq V_{IT-} + 0.2$ V; see Figure 1 | 120 | 200 | 280 | ms |
| $t_{PHL}$ | Propagation (delay) time, high-to-low-level output | $V_{DD}$ to $\overline{\text{RESET}}$ delay | $V_{IL} = V_{IT-} - 0.2$ V, $V_{IH} = V_{IT-} + 0.2$ V |  | 1 |  | µs |
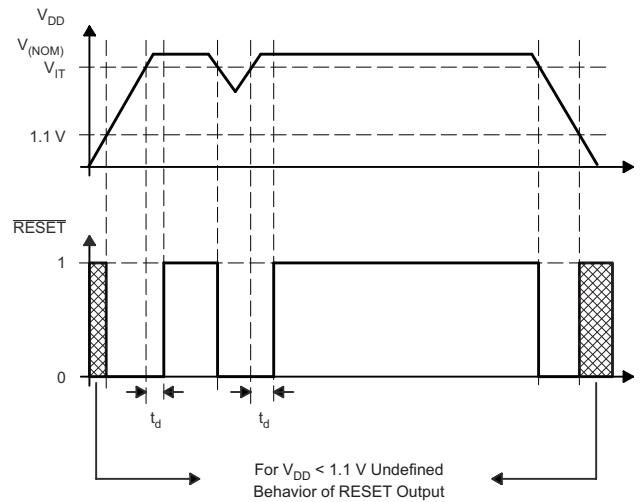


**Figure 1. Timing Diagram**

## 7.8 Typical Characteristics
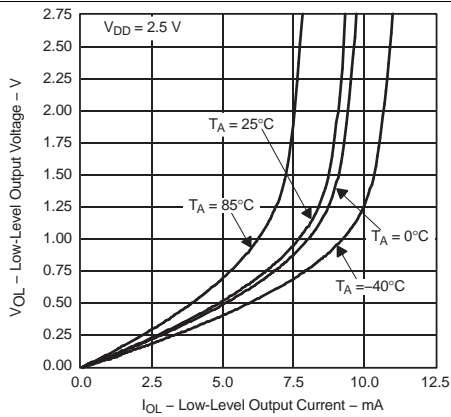


**Figure 2. Low-Level Output Voltage vs
Low-Level Output Current**
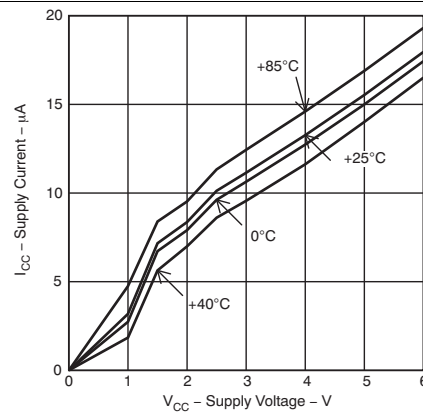


**Figure 3. Supply Current vs Supply Voltage**
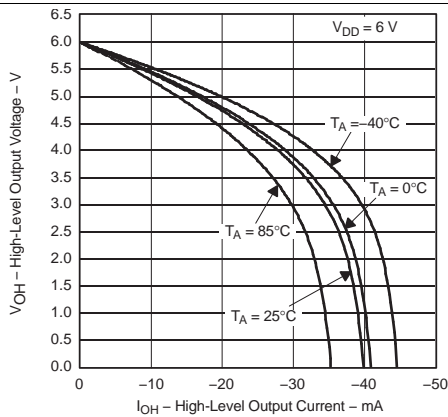


**Figure 4. High-Level Output Voltage vs
High-Level Output Current**
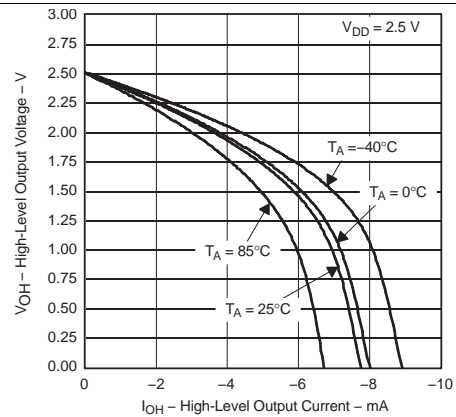


**Figure 5. High-Level Output Voltage vs
High-Level Output Current**
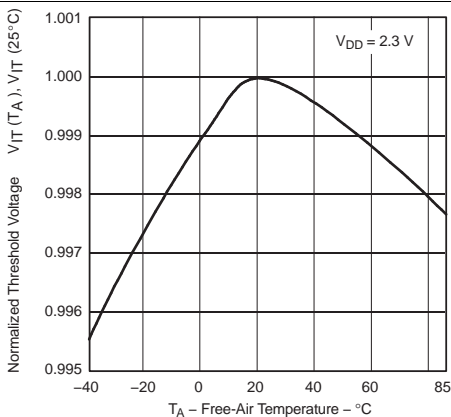


**Figure 6. Normalized Input Threshold Voltage vs
Free-Air Temperature at V$_{DD}$**
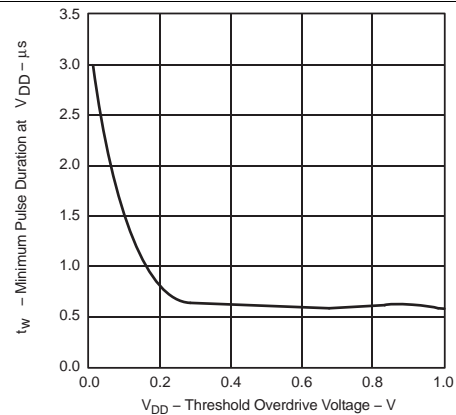


**Figure 7. Minimum Pulse Duration at V$_{DD}$ vs
V$_{DD}$ Threshold Overdrive Voltage**

# 8 Detailed Description

## 8.1 Overview

The TLV809 is a 3-pin voltage detector with fixed detection thresholds, an active-low push-pull $\overline{\text{RESET}}$ output, and an internal timer to delay the $\overline{\text{RESET}}$ signal when $V_{DD}$ rises above the threshold voltage.

## 8.2 Functional Block Diagram
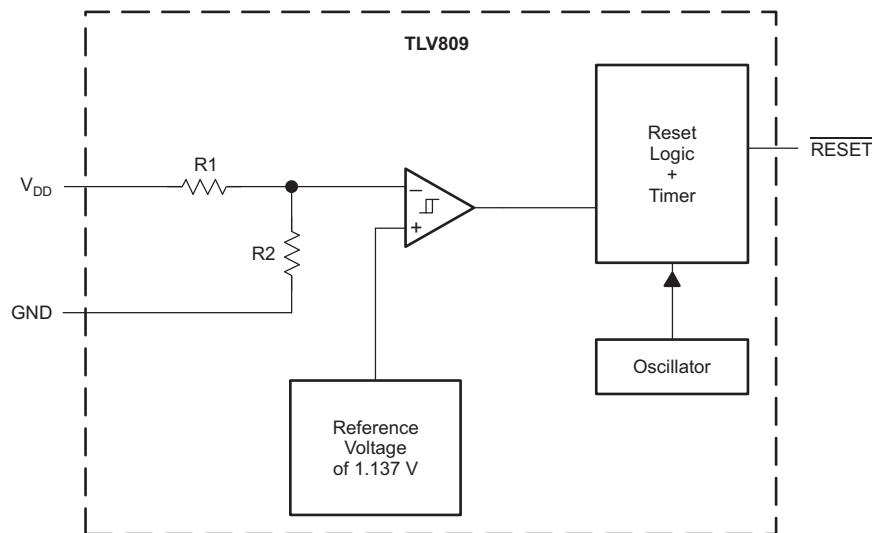


## 8.3 Feature Description

### 8.3.1 Supply Voltage Monitoring

The device actively monitors its supply voltage to ensure that the power supply is above a certain voltage threshold.

The device offers various fixed threshold options that are approximately 10% below several standard supply voltages (2.5 V, 3.0 V, 3.3 V, 5.0 V).

### 8.3.2 $\overline{\text{RESET}}$ Output

The device has a $\overline{\text{RESET}}$ output to indicate the status of the input power supply.

$\overline{\text{RESET}}$ is an active low signal, asserting when $V_{DD}$ is below the threshold voltage. When $V_{DD}$ rises above $V_{IT}$, there is a delay time ($t_d$) until $\overline{\text{RESET}}$ deasserts.

$\overline{\text{RESET}}$ is a push-pull output stage.

## 8.4 Device Functional Modes

When the input supply voltage is in its recommended operating range (2 V to 6 V), the device is in a normal operational mode. In normal operational mode the device monitors $V_{DD}$ for undervoltage detection.

When the input supply is below its recommended operating range, the device is in shutdown mode and therefore tries to assert $\overline{\text{RESET}}$.

# 9 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 9.1 Application Information

### 9.1.1 $V_{DD}$ Transient Rejection

The device has built-in rejection of fast transients on the $V_{DD}$ pin. The rejection of transients depends on both the duration and the amplitude of the transient. The amplitude of the transient is measured from the bottom of the transient to the negative threshold voltage of the device, as shown in Figure 8.
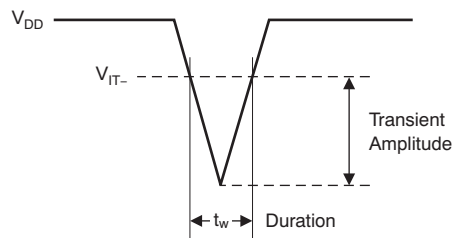


**Figure 8. Voltage Transient Measurement**

The device does not respond to transients that are fast duration and low amplitude or long duration and small amplitude. Figure 7 illustrates the relationship between the transient amplitude and duration needed to trigger a reset. Any combination of duration and amplitude above the curve generates a reset signal.

### 9.1.2 Reset During Power-Up and Power-Down

The device output is valid when $V_{DD}$ is greater than 1.1 V. When $V_{DD}$ is less than 1.1 V, the output transistor turns off and becomes high impedance. The voltage on the $\overline{\text{RESET}}$ pin rises to the voltage level connected to the pullup resistor. Figure 9 shows a typical waveform for power-up.
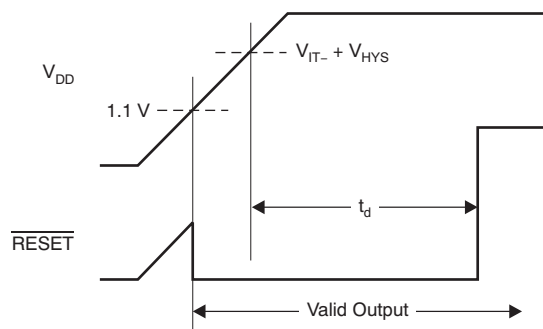


**Figure 9. Power-Up Response**

Product Folder Links: *TLV809*

## 9.2 Typical Application
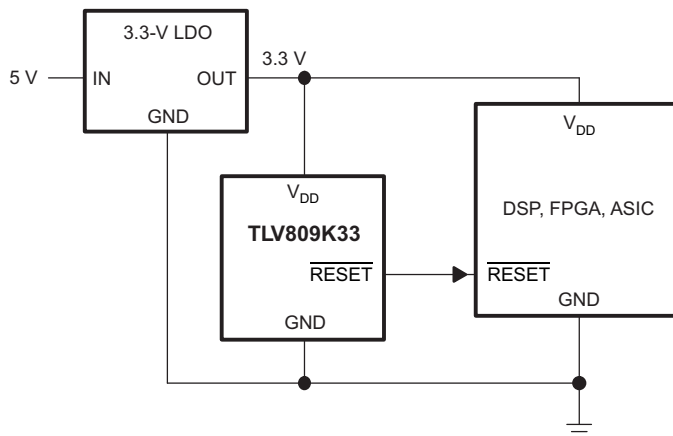


**Figure 10. Monitoring a 3.3-V Supply**

### 9.2.1 Design Requirements

The device must ensure that the supply voltage does not drop more than 15% below 3.3 V. If the supply voltage falls below 3.3 V – 15%, then the load must be disabled.

### 9.2.2 Detailed Design Procedure

The TLV809K33 is selected to ensure that $V_{DD}$ is greater than 2.87 V when the load is enabled.

### 9.2.3 Application Curve
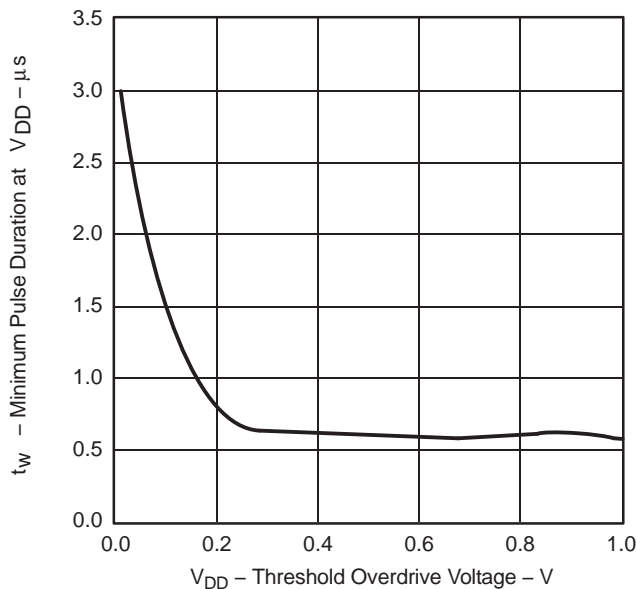


**Figure 11. Minimum Pulse Duration at $V_{DD}$ vs $V_{DD}$ Threshold Overdrive Voltage**

## 10 Power Supply Recommendations

Power the device with a low-impedance supply. A 0.1-µF bypass capacitor from $V_{DD}$ to ground is recommended.

## 11 Layout

### 11.1 Layout Guidelines

Place the device near the load for the input power supply, with a low-impedance connection to the power supply pins of the load to sense the supply voltage.

### 11.2 Layout Example
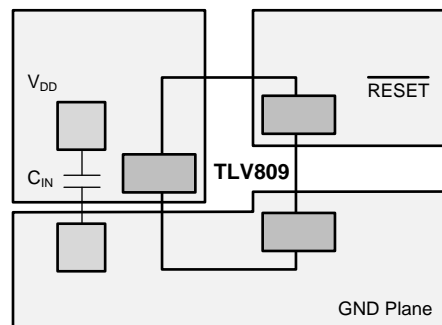


**Figure 12. Example Layout**

Product Folder Links: *TLV809*

## 12 Device and Documentation Support

### 12.1 Documentation Support

#### 12.1.1 Related Documentation

TLV803 Data Sheet, SBVS157

TLV810 Data Sheet, SBVS158

### 12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 12.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

### 12.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 12.5 Glossary

SLYZ022 — *TI Glossary*.
This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TLV809I50DBVR | ACTIVE | SOT-23 | DBV | 3 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | VTBI | Samples |
| TLV809I50DBVT | ACTIVE | SOT-23 | DBV | 3 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | VTBI | Samples |
| TLV809I50DBZR | ACTIVE | SOT-23 | DBZ | 3 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | BCMV | Samples |
| TLV809I50DBZT | ACTIVE | SOT-23 | DBZ | 3 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | BCMV | Samples |
| TLV809J25DBVR | ACTIVE | SOT-23 | DBV | 3 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | VTCI | Samples |
| TLV809J25DBVT | ACTIVE | SOT-23 | DBV | 3 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | VTCI | Samples |
| TLV809J25DBZR | ACTIVE | SOT-23 | DBZ | 3 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | BCMT | Samples |
| TLV809J25DBZT | ACTIVE | SOT-23 | DBZ | 3 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | BCMT | Samples |
| TLV809K33DBVR | ACTIVE | SOT-23 | DBV | 3 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | VTRI | Samples |
| TLV809K33DBVT | ACTIVE | SOT-23 | DBV | 3 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | VTRI | Samples |
| TLV809K33DBZR | ACTIVE | SOT-23 | DBZ | 3 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | BCMX | Samples |
| TLV809K33DBZT | ACTIVE | SOT-23 | DBZ | 3 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | BCMX | Samples |
| TLV809L30DBVR | ACTIVE | SOT-23 | DBV | 3 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | VTXI | Samples |
| TLV809L30DBVT | ACTIVE | SOT-23 | DBV | 3 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | VTXI | Samples |
| TLV809L30DBZR | ACTIVE | SOT-23 | DBZ | 3 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | BCMZ | Samples |
| TLV809L30DBZT | ACTIVE | SOT-23 | DBZ | 3 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | BCMZ | Samples |

**(1)** The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

# PACKAGE MATERIALS INFORMATION

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

**TAPE DIMENSIONS**



| A0 | Dimension designed to accommodate the component width |
|---|---|
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TLV809I50DBVR | SOT-23 | DBV | 3 | 3000 | 180.0 | 9.0 | 3.3 | 3.2 | 1.47 | 4.0 | 8.0 | Q3 |
| TLV809I50DBVT | SOT-23 | DBV | 3 | 250 | 180.0 | 9.0 | 3.3 | 3.2 | 1.47 | 4.0 | 8.0 | Q3 |
| TLV809I50DBZR | SOT-23 | DBZ | 3 | 3000 | 179.0 | 8.4 | 3.15 | 2.95 | 1.22 | 4.0 | 8.0 | Q3 |
| TLV809I50DBZT | SOT-23 | DBZ | 3 | 250 | 179.0 | 8.4 | 3.15 | 2.95 | 1.22 | 4.0 | 8.0 | Q3 |
| TLV809J25DBVR | SOT-23 | DBV | 3 | 3000 | 180.0 | 9.0 | 3.3 | 3.2 | 1.47 | 4.0 | 8.0 | Q3 |
| TLV809J25DBVT | SOT-23 | DBV | 3 | 250 | 180.0 | 9.0 | 3.3 | 3.2 | 1.47 | 4.0 | 8.0 | Q3 |
| TLV809J25DBZR | SOT-23 | DBZ | 3 | 3000 | 179.0 | 8.4 | 3.15 | 2.95 | 1.22 | 4.0 | 8.0 | Q3 |
| TLV809J25DBZT | SOT-23 | DBZ | 3 | 250 | 179.0 | 8.4 | 3.15 | 2.95 | 1.22 | 4.0 | 8.0 | Q3 |
| TLV809K33DBVR | SOT-23 | DBV | 3 | 3000 | 178.0 | 9.0 | 3.3 | 3.2 | 1.47 | 4.0 | 8.0 | Q3 |
| TLV809K33DBVT | SOT-23 | DBV | 3 | 250 | 178.0 | 8.4 | 3.3 | 3.2 | 1.47 | 4.0 | 8.0 | Q3 |
| TLV809K33DBZR | SOT-23 | DBZ | 3 | 3000 | 179.0 | 8.4 | 3.15 | 2.95 | 1.22 | 4.0 | 8.0 | Q3 |
| TLV809K33DBZT | SOT-23 | DBZ | 3 | 250 | 179.0 | 8.4 | 3.15 | 2.95 | 1.22 | 4.0 | 8.0 | Q3 |
| TLV809L30DBVR | SOT-23 | DBV | 3 | 3000 | 180.0 | 9.0 | 3.3 | 3.2 | 1.47 | 4.0 | 8.0 | Q3 |
| TLV809L30DBVT | SOT-23 | DBV | 3 | 250 | 180.0 | 9.0 | 3.3 | 3.2 | 1.47 | 4.0 | 8.0 | Q3 |
| TLV809L30DBZR | SOT-23 | DBZ | 3 | 3000 | 179.0 | 8.4 | 3.15 | 2.95 | 1.22 | 4.0 | 8.0 | Q3 |
| TLV809L30DBZT | SOT-23 | DBZ | 3 | 250 | 179.0 | 8.4 | 3.15 | 2.95 | 1.22 | 4.0 | 8.0 | Q3 |

**TAPE AND REEL BOX DIMENSIONS**



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TLV809I50DBVR | SOT-23 | DBV | 3 | 3000 | 182.0 | 182.0 | 20.0 |
| TLV809I50DBVT | SOT-23 | DBV | 3 | 250 | 182.0 | 182.0 | 20.0 |
| TLV809I50DBZR | SOT-23 | DBZ | 3 | 3000 | 203.0 | 203.0 | 35.0 |
| TLV809I50DBZT | SOT-23 | DBZ | 3 | 250 | 203.0 | 203.0 | 35.0 |
| TLV809J25DBVR | SOT-23 | DBV | 3 | 3000 | 182.0 | 182.0 | 20.0 |
| TLV809J25DBVT | SOT-23 | DBV | 3 | 250 | 182.0 | 182.0 | 20.0 |
| TLV809J25DBZR | SOT-23 | DBZ | 3 | 3000 | 203.0 | 203.0 | 35.0 |
| TLV809J25DBZT | SOT-23 | DBZ | 3 | 250 | 203.0 | 203.0 | 35.0 |
| TLV809K33DBVR | SOT-23 | DBV | 3 | 3000 | 180.0 | 180.0 | 18.0 |
| TLV809K33DBVT | SOT-23 | DBV | 3 | 250 | 180.0 | 180.0 | 18.0 |
| TLV809K33DBZR | SOT-23 | DBZ | 3 | 3000 | 203.0 | 203.0 | 35.0 |
| TLV809K33DBZT | SOT-23 | DBZ | 3 | 250 | 203.0 | 203.0 | 35.0 |
| TLV809L30DBVR | SOT-23 | DBV | 3 | 3000 | 182.0 | 182.0 | 20.0 |
| TLV809L30DBVT | SOT-23 | DBV | 3 | 250 | 182.0 | 182.0 | 20.0 |
| TLV809L30DBZR | SOT-23 | DBZ | 3 | 3000 | 203.0 | 203.0 | 35.0 |
| TLV809L30DBZT | SOT-23 | DBZ | 3 | 250 | 203.0 | 203.0 | 35.0 |

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4203227/C

TEXAS
INSTRUMENTS

PIN 1
INDEX AREA

2.64
2.10

1.4
1.2

B

A

0.95

1.9

3X 0.5
0.3

3.04
2.80

⊕ 0.2 Ⓜ C A B

1

3

2

C

1.12 MAX

⌒ 0.1 C

(0.95)

0.10
0.01 TYP

0.25

GAGE PLANE

0.20
0.08 TYP

0°-8° TYP

0.6
0.2 TYP

SEATING PLANE
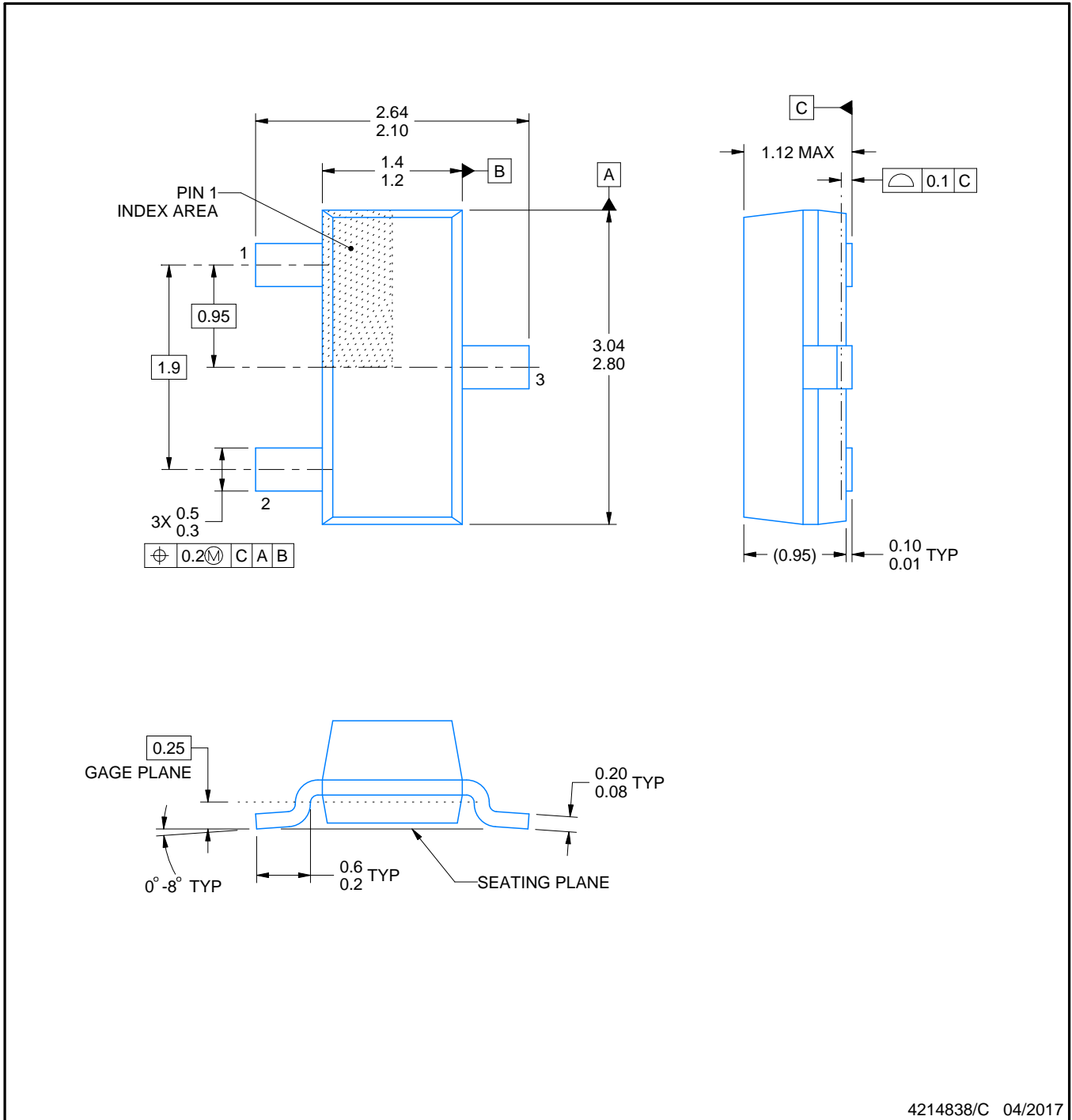
4214838/C 04/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing
   per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration TO-236, except minimum foot length.

3X (1.3)

1

3X (0.6)

PKG ₵

SYMM ₵

3

2X (0.95)

2

(R0.05) TYP

(2.1)
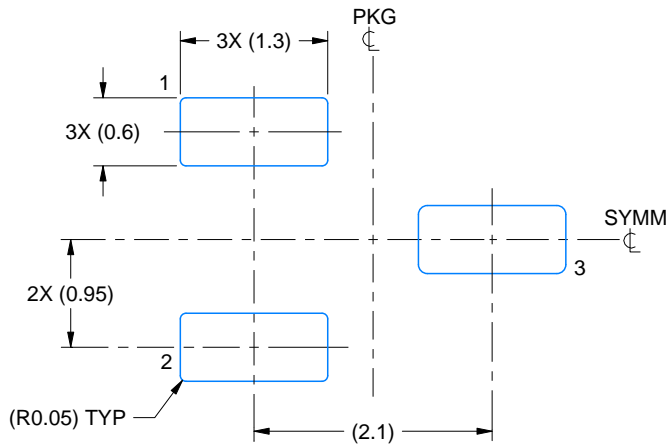
**LAND PATTERN EXAMPLE**
SCALE:15X

SOLDER MASK
OPENING

METAL

0.07 MAX
ALL AROUND

NON SOLDER MASK
DEFINED
(PREFERRED)

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

0.07 MIN
ALL AROUND

SOLDER MASK
DEFINED
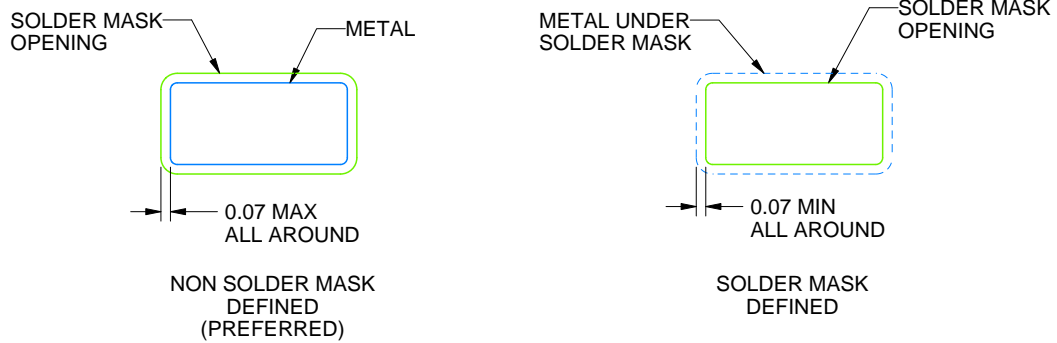
**SOLDER MASK DETAILS**

4214838/C   04/2017

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

PKG

3X (1.3)

1

3X (0.6)

SYMM

3

2X(0.95)

2

(R0.05) TYP

(2.1)

SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

4214838/C 04/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

DBV (R−PDSO−G3)                    PLASTIC SMALL−OUTLINE PACKAGE
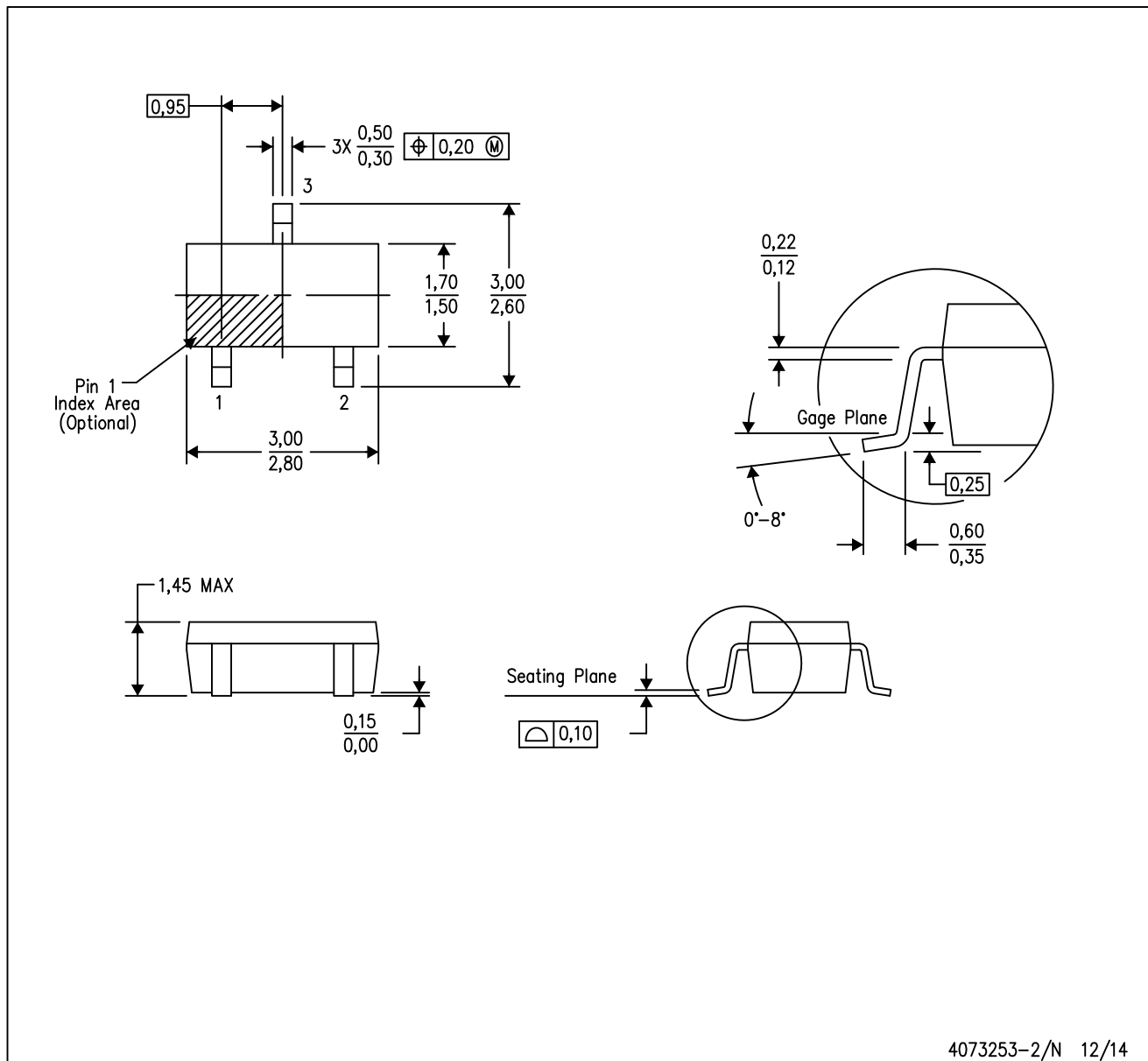


0,95

3X $\frac{0,50}{0,30}$  ⊕ 0,20 Ⓜ

3

$\frac{1,70}{1,50}$   $\frac{3,00}{2,60}$

Pin 1
Index Area
(Optional)

1        2

$\frac{3,00}{2,80}$

$\frac{0,22}{0,12}$

Gage Plane

0°−8°

0,25

$\frac{0,60}{0,35}$

1,45 MAX

$\frac{0,15}{0,00}$

Seating Plane

◠ 0,10

4073253−2/N  12/14

NOTES:  A.  All linear dimensions are in millimeters.
        B.  This drawing is subject to change without notice.
        C.  Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.

DBV (R—PDSO—G3)            PLASTIC SMALL OUTLINE

Example Board Layout

Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).

2,7

1,9

1,00

0,55

2,7

0,95

0,6

Solder Mask Opening

1,05

Pad Geometry

0,07
All Around

4209593—2/C 08/11

NOTES:    A.   All linear dimensions are in millimeters.
            B.   This drawing is subject to change without notice.
            C.   Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
            D.   Publication IPC—7351 is recommended for alternate designs.
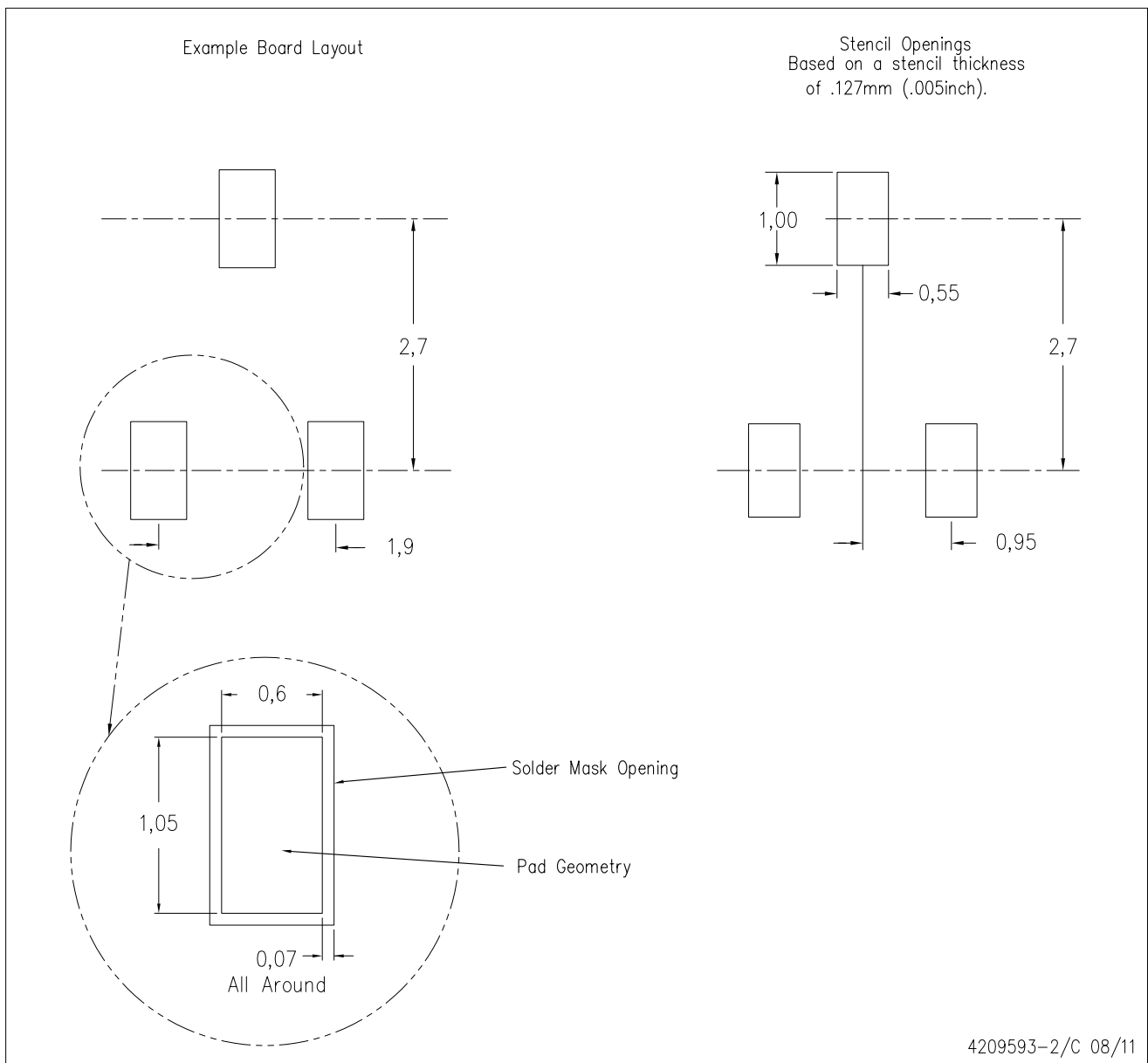            E.   Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC—7525 for other stencil recommendations.

**TEXAS INSTRUMENTS**
www.ti.com

# IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (http://www.ti.com/sc/docs/stdterms.htm) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.