Kintex-7 FPGA KC705 Evaluation Kit

Getting Started Guide

Vivado Design Suite 2014.2

UG883 (v5.0) August 22, 2014

XILINX®

Disclaimer

The information disclosed to you hereunder (the “Materials”) is provided solely for the selection and use of Xilinx products. To the maximum extent permitted by applicable law: (1) Materials are made available "AS IS" and with all faults, Xilinx hereby DISCLAIMS ALL WARRANTIES AND CONDITIONS, EXPRESS, IMPLIED, OR STATUTORY, INCLUDING BUT NOT LIMITED TO WARRANTIES OF MERCHANTABILITY, NON-INFRINGEMENT, OR FITNESS FOR ANY PARTICULAR PURPOSE; and (2) Xilinx shall not be liable (whether in contract or tort, including negligence, or under any other theory of liability) for any loss or damage of any kind or nature related to, arising under, or in connection with, the Materials (including your use of the Materials), including for any direct, indirect, special, incidental, or consequential loss or damage (including loss of data, profits, goodwill, or any type of loss or damage suffered as a result of any action brought by a third party) even if such damage or loss was reasonably foreseeable or Xilinx had been advised of the possibility of the same. Xilinx assumes no obligation to correct any errors contained in the Materials or to notify you of updates to the Materials or to product specifications. You may not reproduce, modify, distribute, or publicly display the Materials without prior written consent. Certain products are subject to the terms and conditions of Xilinx’s limited warranty, please refer to Xilinx’s Terms of Sale which can be viewed at www.xilinx.com/legal.htm#tos; IP cores may be subject to warranty and support terms contained in a license issued to you by Xilinx. Xilinx products are not designed or intended to be fail-safe or for use in any application requiring fail-safe performance; you assume sole risk and liability for use of Xilinx products in such critical applications, please refer to Xilinx’s Terms of Sale which can be viewed at www.xilinx.com/legal.htm#tos.

Automotive Applications Disclaimer

XILINX PRODUCTS ARE NOT DESIGNED OR INTENDED TO BE FAIL-SAFE, OR FOR USE IN ANY APPLICATION REQUIRING FAIL-SAFE PERFORMANCE, SUCH AS APPLICATIONS RELATED TO: (I) THE DEPLOYMENT OF AIRBAGS, (II) CONTROL OF A VEHICLE, UNLESS THERE IS A FAIL-SAFE OR REDUNDANCY FEATURE (WHICH DOES NOT INCLUDE USE OF SOFTWARE IN THE XILINX DEVICE TO IMPLEMENT THE REDUNDANCY) AND A WARNING SIGNAL UPON FAILURE TO THE OPERATOR, OR (III) USES THAT COULD LEAD TO DEATH OR PERSONAL INJURY. CUSTOMER ASSUMES THE SOLE RISK AND LIABILITY OF ANY USE OF XILINX PRODUCTS IN SUCH APPLICATIONS.

Fedora Information

Xilinx obtained the Fedora Linux software from Fedora (http://fedoraproject.org/), and you may too. Xilinx made no changes to the software obtained from Fedora. If you desire to use Fedora Linux software in your product, Xilinx encourages you to obtain Fedora Linux software directly from Fedora (http://fedoraproject.org/), even though we are providing to you a copy of the corresponding source code as provided to us by Fedora. Portions of the Fedora software may be covered by the GNU General Public license as well as many other applicable open source licenses. Please review the source code in detail for further information. To the maximum extent permitted by applicable law and if not prohibited by any such third-party licenses, (1) XILINX DISCLAIMS ANY AND ALL EXPRESS OR IMPLIED WARRANTIES, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE; AND (2) IN NO EVENT SHALL XILINX BE LIABLE FOR ANY DIRECT, INDIRECT, INCIDENTAL, SPECIAL, EXEMPLARY, OR CONSEQUENTIAL DAMAGES (INCLUDING, BUT NOT LIMITED TO, PROCUREMENT OF SUBSTITUTE GOODS OR SERVICES; LOSS OF USE,DATA, OR PROFITS; OR BUSINESS INTERRUPTION) HOWEVER CAUSED AND ON ANY THEORY OF LIABILITY, WHETHER IN CONTRACT, STRICT LIABILITY, OR TORT (INCLUDING NEGLIGENCE OR OTHERWISE) ARISING IN ANY WAY OUT OF THE USE OF THIS SOFTWARE, EVEN IF ADVISED OF THE POSSIBILITY OF SUCH DAMAGE.

Fedora software and technical information is subject to the U.S. Export Administration Regulations and other U.S. and foreign law, and may not be exported or re-exported to certain countries (currently Cuba, Iran, Iraq, North Korea, Sudan, and Syria) or to persons or entities prohibited from receiving U.S. exports (including those (a) on the Bureau of Industry and Security Denied Parties List or Entity List, (b) on the Office of Foreign Assets Control list of Specially Designated Nationals and Blocked Persons, and (c) involved with missile technology or nuclear, chemical or biological weapons). You may not download Fedora software or technical information if you are located in one of these countries, or otherwise affected by these restrictions. You may not provide Fedora software or technical information to individuals or entities located in one of these countries or otherwise affected by these restrictions. You are also responsible for compliance with foreign law requirements applicable to the import and use of Fedora software and technical information.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
01/13/2012	1.0	Initial Xilinx release.
01/25/2012	1.1	Changed document title. Added BIST section. Changed Platform Flash to BPI Linear Flash. Added a note after Figure 30. Updated photos in Figure 2, Figure 3, and Figure 31.
02/27/2012	1.1.1	Added a note to Hardware Test Setup Requirements.
07/10/2012	1.2	Added XPN number to title page. Updated Introduction and Hardware Test Setup Requirements. Added Kit Contents, AMS Bring-up with the AMS101 Evaluation Card, and AMS Bring-up with the AMS101 Evaluation Card. Added Appendix B, Warranty. Removed "Modifying the Kintex-7 FPGA Base TRD" section.
12/20/12	2.0	The document was updated for Vivado® Design Suite 2012.4. Agile Mixed Signal is now Analog Mixed Signal. The USB stick is removed from the kit and instead, design files are accessible from the Docs & Designs tab at www.xilinx.com/kc705. Removing the USB stick affected many sections including these: • Kit Contents, page 8 • Hardware Test Setup Requirements, page 9 • AMS Bring-up with the AMS101 Evaluation Card, page 15 • Step 4 in Install the Linux Driver, page 26. The first bullet under Introduction, page 7 removed "transceivers by using the LogiCORE™ IP Integrated Bit Error Ratio (IBERT) core". Under KC705 Evaluation Board Setup, page 10, "cord and brick" changed to "12V power adapter." Removed the *Transceiver Bring-up Using Integrated Bit Error Ratio Test* section on page 14. Requirements to Get Started, page 14 installation method **a** and step 3 changed. The use of the ChipScope™ tool is eliminated. Step 2 of Evaluating AMS, page 17 changed. Below Figure 9, this sentence was deleted: AMS Evaluator source code is not provided. CD-ROM was replaced with DVD-ROM. Appendix A, Additional Resources was reorganized.
04/16/2013	3.0	Added third, fourth, and fifth bullets in AMS Bring-up with the AMS101 Evaluation Card, page 15. Updated step 2 and step 3 in Requirements to Get Started, page 14. Updated step 2 in Evaluating AMS, page 17. Added eighth bullet in Hardware Test Setup Requirements, page 21.
07/02/2013	4.0	Updated Figure 7. Added Table 2. Replaced Requirements to Get Started with Getting Started, page 16. Updated links in References, page 37
05/28/2014	4.0.1	Changed the print number on the title page.
08/22/2014	5.0	Updated for Vivado Design Suite 2014.2. Updated documentation in Kit Contents, page 8 and References, page 37. Changed part XC7K325T-2FFG900CES to XC7K325T-2FFG900C under Hardware Test Board Setup Requirements, page 10. Replaced *ChipScope* with *Vivado Hardware Manager* in Evaluating AMS, page 17.

Table of Contents

XILINX®

Getting Started with the Kintex-7 FPGA KC705 Evaluation Kit

Introduction

The Kintex®-7 FPGA KC705 evaluation kit provides a comprehensive, high-performance development and demonstration platform using the Kintex-7 FPGA family for high-bandwidth and high-performance applications in multiple market segments. The kit enables designing with DDR3, I/O expansion through FMC, and common serial standards, such as PCI Express®, XAUI, and proprietary serial standards through the SMA interface. See the *KC705 Evaluation Board for the Kintex-7 FPGA User Guide* (UG810) [Ref 1] and the KC705 support website.

The built-in self-test (BIST) and Kintex-7 FPGA Base Targeted Reference Design (TRD) are developed on this kit.

This Getting Started Guide is divided into two sections:

- Basic Hardware Bring-up: Enables hands-on operation of all the features in the BIST as well as evaluation of Analog Mixed Signal (AMS) using the AMS101 evaluation card.
- Advanced Operation: Enables hands-on operation with the base TRD, which features PCIe, DDR3 memory, and AXI—all supported through a custom evaluation graphical user interface (GUI).

Kit Contents

The Kintex-7 FPGA KC705 evaluation kit includes:

- KC705 EK-K7-KC705-G base board, including the XC7K325T-2FFG900C FPGA.
- AMS101 evaluation card, enabling evaluation of the AMS technology built into all 7 series FPGAs.
- Software and licenses:
  - Vivado® Design Suite Installation DVD.
  - Printed entitlement voucher: Provides entitlement of the Vivado Design Suite Logic Edition device-locked to the XC7K325T-2FFG900 FPGA. Follow the printed instructions on the voucher to redeem your software entitlement.
  - Fedora 16 Live DVD to support the Base Targeted Reference Design.
- Designs:
  - Targeted Reference Design: Robust sub-system including PCIe Gen2 x4, Northwest Logic DMA, multi-port virtual FIFO, AXI, and DDR3 memory controller.
  - Additional Reference Designs: Numerous additional reference designs available online and linked from the KC705 product page www.xilinx.com/kc705.
- Documentation:
  - *Kintex-7 FPGA KC705 Evaluation Kit Getting Started Guide* (UG883). This guide is included in the box.
  - Board design files including schematics, Gerber files, and BOM (online on product page)

  These additional documents support this kit:

  - *KC705 Evaluation Board for the Kintex-7 FPGA User Guide* (UG810) [Ref 1]
  - *Kintex-7 FPGA KC705 Base Targeted Reference Design User Guide* (UG882) [Ref 2]
- Cables and power supply:
  - Universal 12V power adapter and cords
  - Two USB cables (1x USB Type-A/Mini-B and 1x USB Type-A/Micro-B) for download and debug
  - Ethernet crossover cable
- HDMI cable

Basic Hardware Bring-up Using the BIST

The built-in self-test (BIST) tests many of the features offered by the Kintex-7 FPGA KC705 evaluation kit. The test is stored in the nonvolatile BPI Linear Flash memory, and configures the FPGA when the mode and upper flash address pins on the board are set for Master BPI.

Figure 1 provides an overview of the board features used by the BIST.

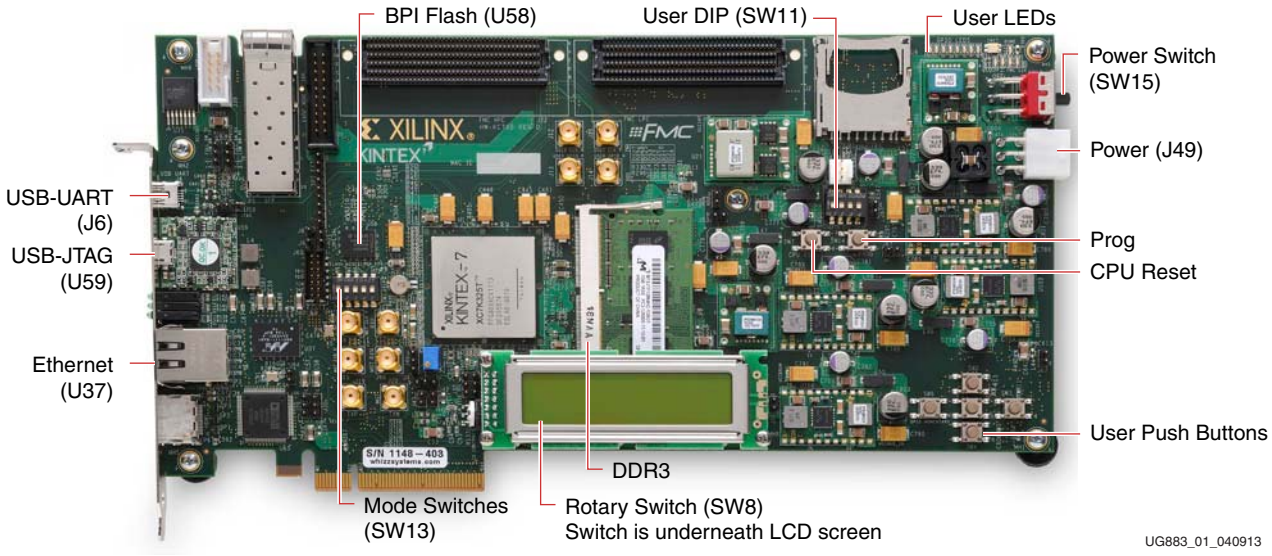


Figure 1: **KC705 Board Features Used by the BIST**

Note: For a diagram of all the features on the KC705, see *KC705 Evaluation Board for the Kintex-7 FPGA User Guide* (UG810) [Ref 1].

Hardware Test Setup Requirements

The prerequisites for testing the design in hardware are:

- KC705 Evaluation board with the Kintex-7 FPGA XC7K325T-2FFG900C device
- USB-to-Mini-B cable (for UART)
- AC power adapter (12 VDC)
- Terminal program [Ref 3]

  Note: The Tera Term Pro program is used for illustrative purposes. Other programs can be used.
- USB-UART drivers from Silicon Labs [Ref 4]

Hardware Test Board Setup Requirements

This section details the hardware setup and use of the terminal program for running the BIST application. It contains step-by-step instructions for board bring-up.

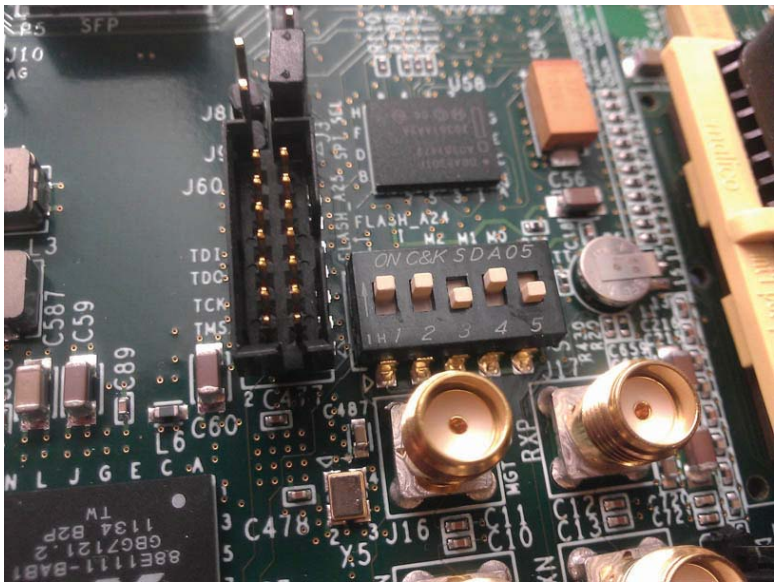
KC705 Evaluation Board Setup

1. Set the jumpers and switches on the KC705 board as follows:
   - The mode switches (SW13) are set for Master BPI mode 010.
   - The upper flash address switches (SW13) are set to 11.
2. Verify the switch and jumper settings are set as shown in Table 1 and Figure 2.

Note: For this application, the board should be set up as a stand-alone system, with power coming from the 12V power adapter included with the KC705 evaluation kit.

Table 1: **Switch & Jumper Settings**

Switch	Setting	
SW15	**Board Power Slide-switch**	
	..	Off
SW11	**User GPIO DIP Switch**	
	4	Off
	3	Off
	2	Off
	1	Off
SW13	**Configuration Mode Switch**	
	5	Off
	4	On
	3	Off
	2	On
	1	On



UG883_02_040913

Figure 2: **BIST Switch and Jumper Settings**

Hardware Bring-Up

This section details the steps for hardware bring-up:

1. With the board switched off, plug a USB-to-Mini-B cable into the UART port of the KC705 board and your PC (see Figure 3).

UG883_03_011912

Figure 3: **KC705 with the UART and Power Cable Attached**

2. Install the power cable.
3. Switch the KC705 board power to ON.

Install the UART Driver

1. Run the downloaded executable UART-USB driver file listed in Hardware Test Setup Requirements, page 9. This enables UART-USB communications with a host PC (see Figure 4).

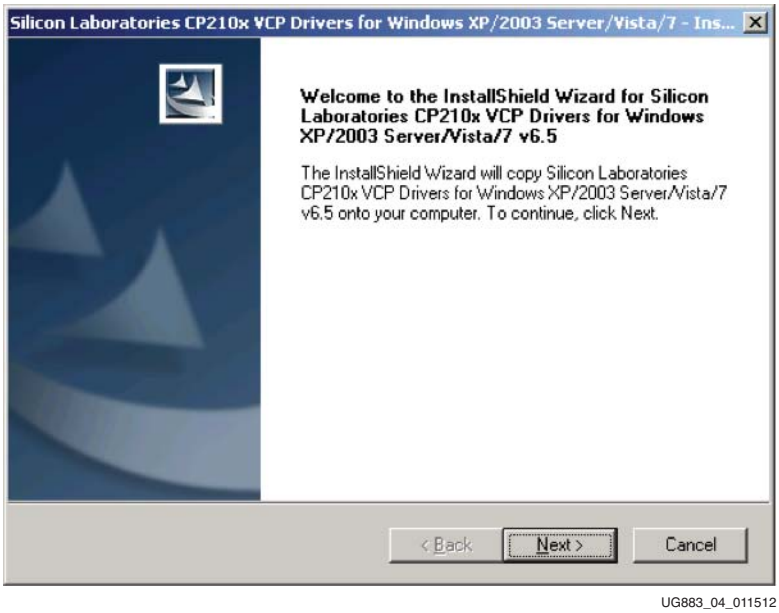


Figure 4: **UART Cable Driver Installation**

2. Set the USB-UART connection to a known port in the Device Manager as follows:
   - Right-click **`My Computer`** and select **`Properties`**.
   - Select the **`Hardware`** tab, then click the **`Device Manager`** button.
   - Find and right-click the Silicon Labs device in the list. Then select **`Properties`**.
   - Click the **`Port Settings`** tab and the **`Advanced...`** button.
   - Select an open COM port between COM1 and COM4.

Figure 5 shows the steps needed to set the USB-UART port.

Note: Steps and diagrams refer to use with a Windows host PC with the Windows XP or Windows 7 operating system.

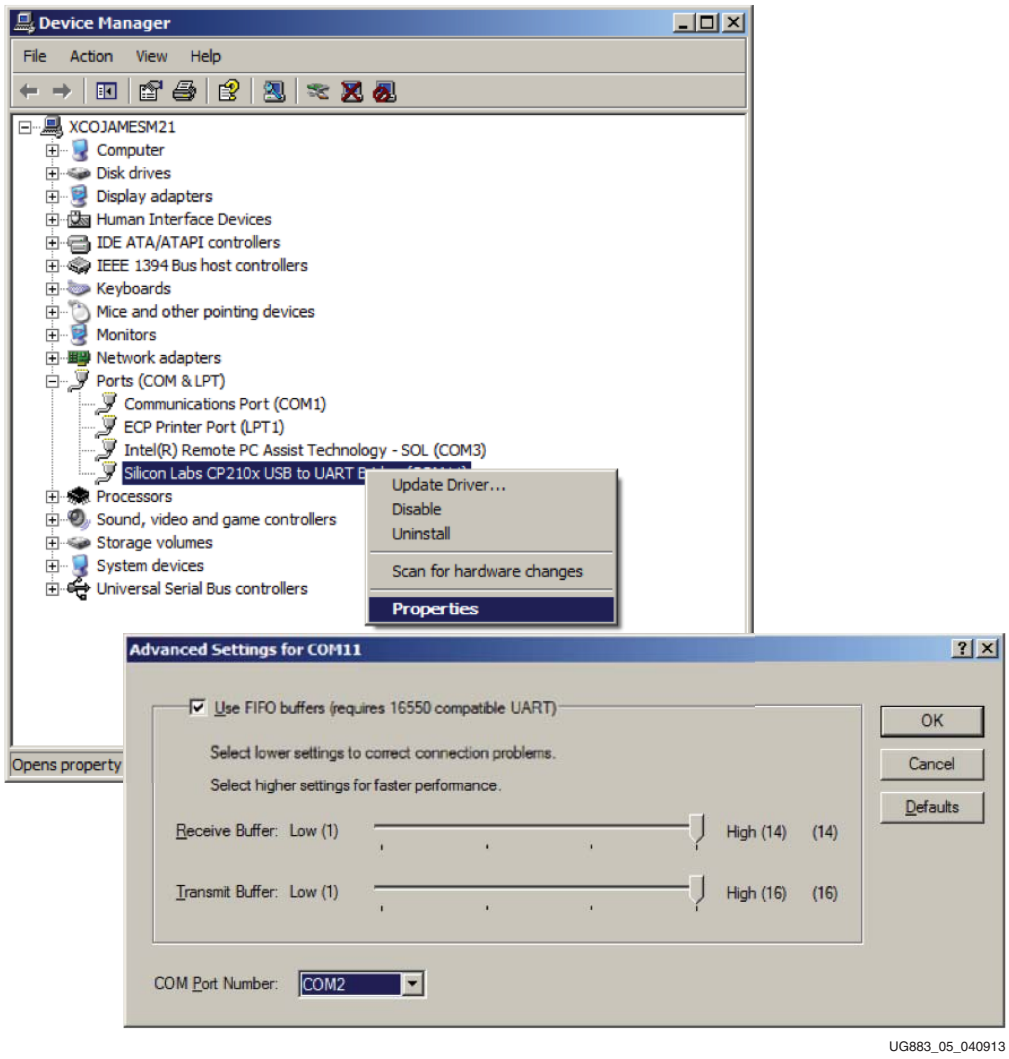


Figure 5: **Port Selection on the Device Manager Screen**

Run the BIST Application

1. Start the installed terminal program.
2. Press PROG (SW14) on the KC705 board, and view the BIST output on the terminal window (see Figure 6).

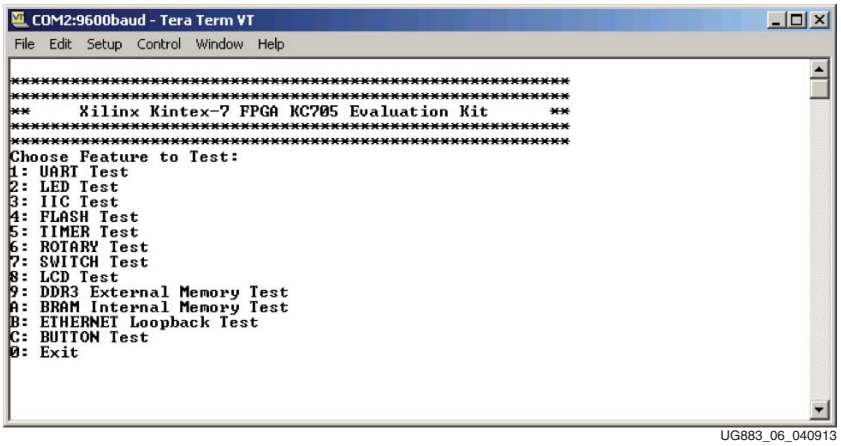


Figure 6: **BIST Main Menu**

3. Select the relevant tests to run, and observe the results.

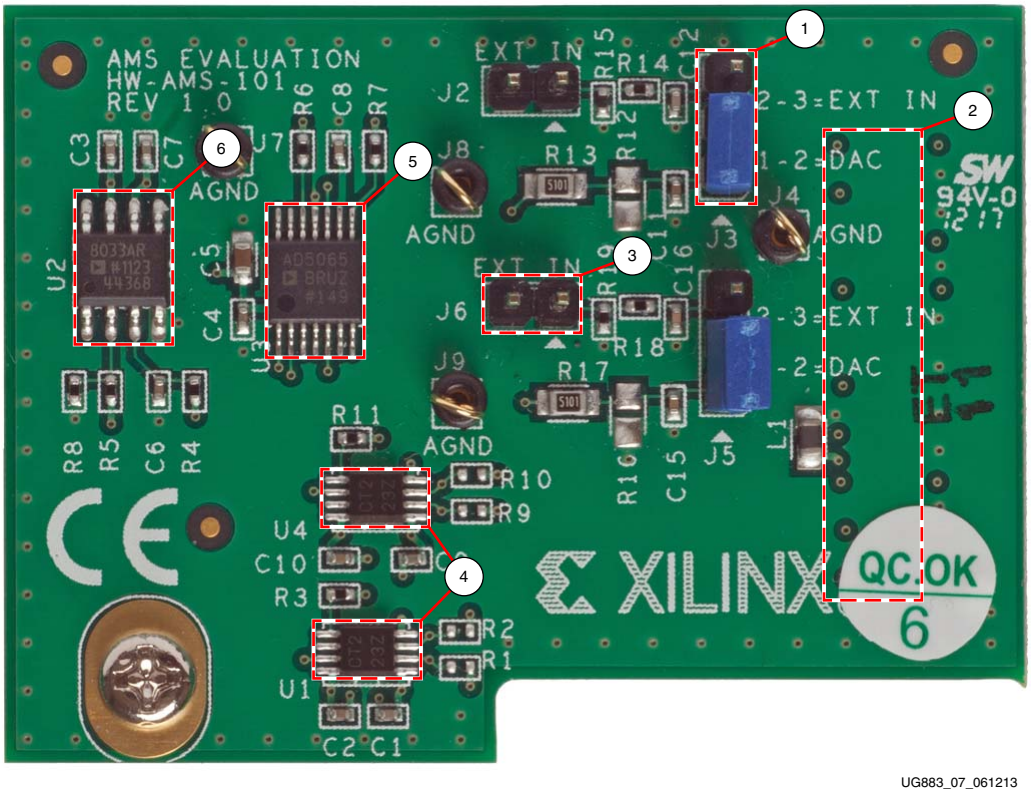
For more information on the BIST software and additional tutorials, including how to restore the default content of the onboard nonvolatile storage, see the KC705 support website.

AMS Bring-up with the AMS101 Evaluation Card

The Xilinx® 7 series FPGAs each feature a 1 MSPS, 12-bit, analog-to-digital converter built into the FPGA for everything from simple analog monitoring to more signal processing intensive tasks like linearization, calibration, oversampling and filtering. The Kintex-7 FPGA KC705 evaluation kit includes the hardware and software to evaluate this feature and determine its usefulness in the user's end system.

For evaluation of Xilinx Analog Mixed Signal (AMS) capability, the following items from your kit are needed:

- Access to XADC header in your FPGA base board
- AMS101 evaluation card (Figure 7)
- FPGA design and software files downloaded from the KC705 support website
- USB/UART drivers from Silicon Labs
- AMS Evaluator tool



UG883_07_061213

Figure 7: **AMS101 Evaluation Card**

Table 2: **AMS101 Evaluation Card Features**

Callout	Component Description
1	Jumpers to select DAC or external signal source.
2	20-pin connector to the XADC header on the KC705 board.
3	Pins for external analog input signals.
4	Digital I/O level translators.

Table 2: **AMS101 Evaluation Card Features *(Cont'd)***

Callout	Component Description
5	16-bit DAC to set analog test voltage.
6	Reference buffer for DAC.

Getting Started

1. Verify the USB/UART Silicon Labs drivers are installed as described in Install the UART Driver, page 12.
2. The AMS101 evaluation card requires a Windows host PC to install the National Instruments LabVIEW run-time engine. Install the AMS101 evaluation installer:
   a. Open the **Docs & Designs** tab at: www.xilinx.com/kc705.
   b. In the example designs, install the AMS101 evaluation tool by unzipping the KC705 AMS evaluation installer files from 7 Series FPGA and Zynq®-7000 AP SoC AMS Evaluator Installer from AMS Targeted Reference Design
   c. After opening the zip folder, click the `setup.exe` file to begin the installation.
   d. When loading the National Instruments LabView run-time engine, click **OK** to accept the license agreement. Running the setup program loads the AMS101 Evaluator GUI with the red Xilinx logo on the desktop.
3. After the AMS Evaluator has successfully installed, restart the host PC.
4. To access the bitstream (`xadc_eval_design.bit`), download and unzip the KC705 AMS design files from secure.xilinx.com/webreg/clickthrough.do?cid=324996&license=RefDesLicense&filename=ams101-kc705-trd-rdf0280.zip&languageID=1

   These files are located in the example designs on the **Docs & Designs** tab at www.xilinx.com/kc705.

Evaluating AMS

1. Connect and power the hardware:
   a. Plug the AMS101 evaluation card into the XADC header on your FPGA base board.

      Note: Ensure the notch on the XADC header lines up correctly with the AMS101 evaluation card (see Figure 8).

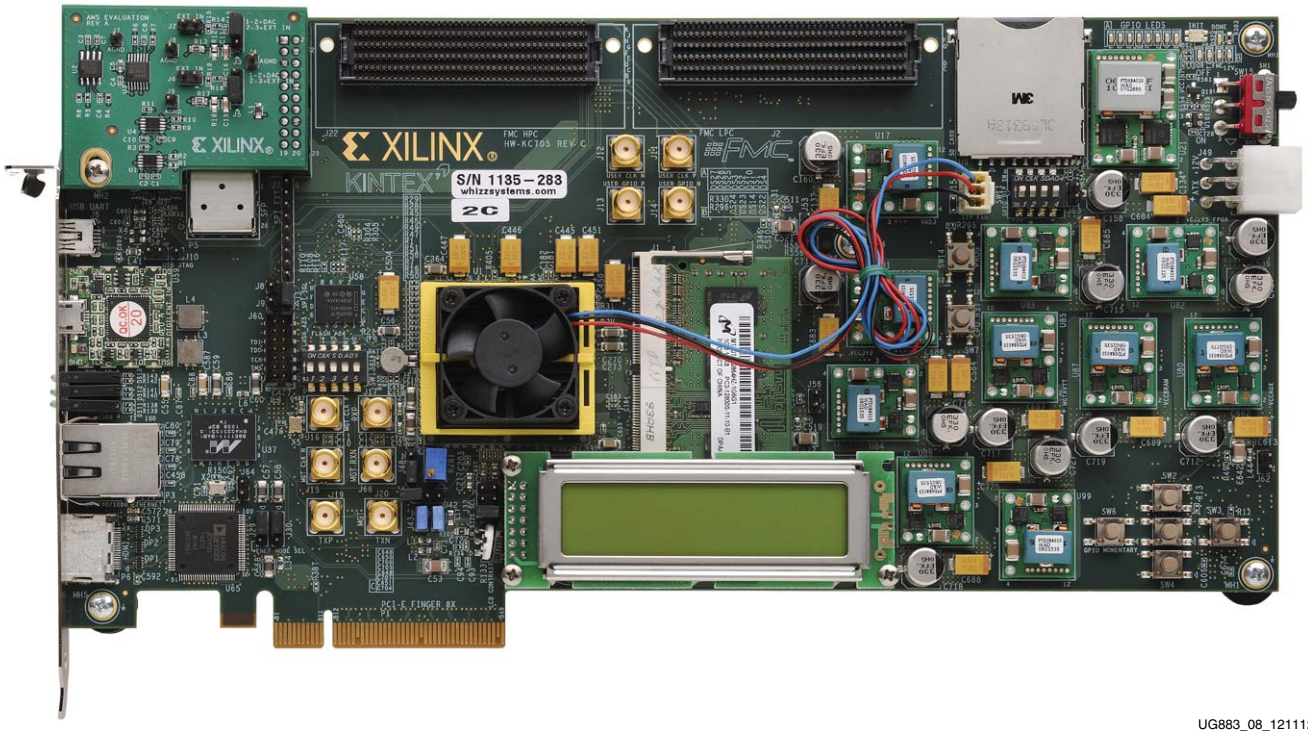


Figure 8: **KC705 Base Board with AMS101 Evaluation Card Plugged into XADC Header**

   b. Power up the FPGA base board
2. Download the design to the FPGA. Use Vivado Hardware Manager for downloading the bitstream to the FPGA.

   Refer to the *Vivado Design Suite User Guide: Programming and Debugging* (UG908) [Ref 5] to obtain information on downloading the design to the FPGA.

   a. Open the `xadc_eval_design.bit` file from the AMS Targeted Reference Design files.
3. Run the AMS101 Evaluator LabVIEW GUI executable from your desktop. After loading the AMS Evaluator installer files, a red X with the AMS Evaluator program should reside on your desktop.

Note: The AMS bitstream can also be loaded with Vivado Hardware Manager.

The AMS101 Evaluator GUI is shown in Figure 9.

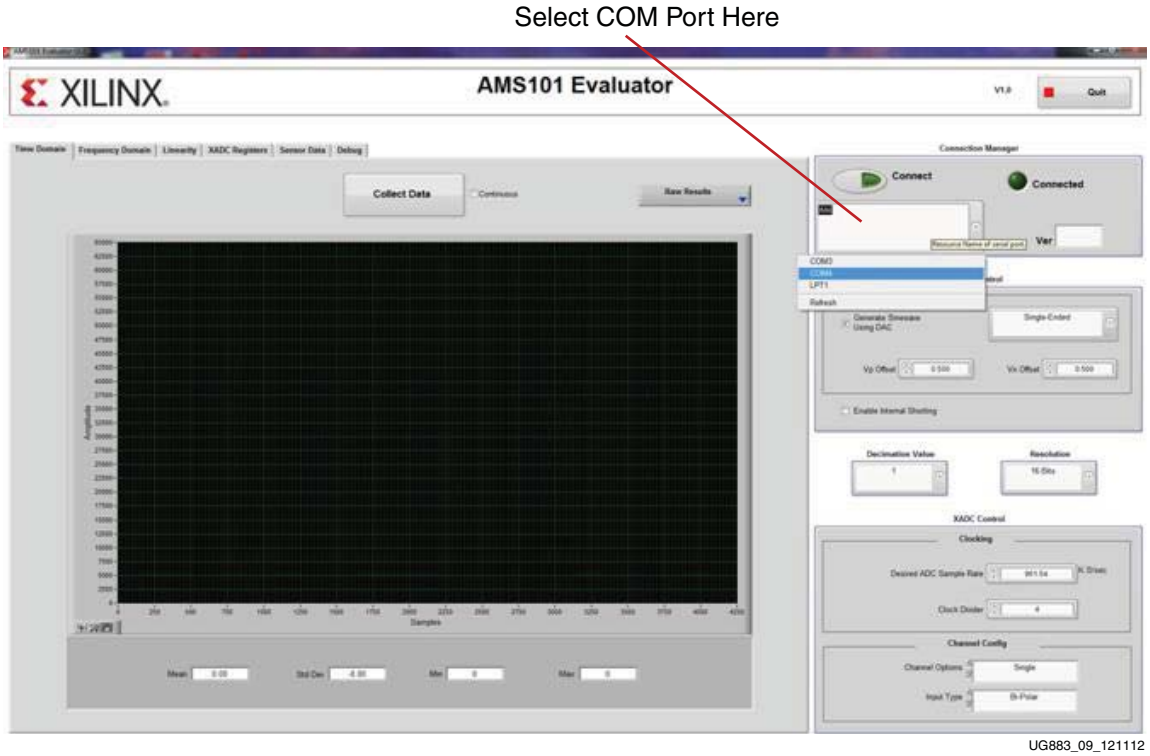


Figure 9: **AMS101 Evaluator GUI**

The AMS Evaluator Tool allows designers to quickly evaluate the analog signals in the time domain, frequency domain, display linearity, verify the XADC register settings, and measure the internal temperature sensor and supply voltages.

For a more extensive explanation of the AMS101 evaluation card and the applicable files, refer to *AMS101 Evaluation Card User Guide* (UG886) [Ref 6].

Advanced Bring-up Using the Base Targeted Reference Design

The primary components of the Kintex-7 FPGA Base TRD are:

- Integrated Endpoint block for PCI Express (PCIe). See *7 Series FPGAs Integrated Block for PCI Express Product Guide* (PG054) [Ref 7]
- Northwest Logic Packet DMA [Ref 8]
- Multiport Virtual FIFO

The TRD system can sustain up to 10 Gb/s throughput end to end.

Figure 10 provides an overview of the TRD.

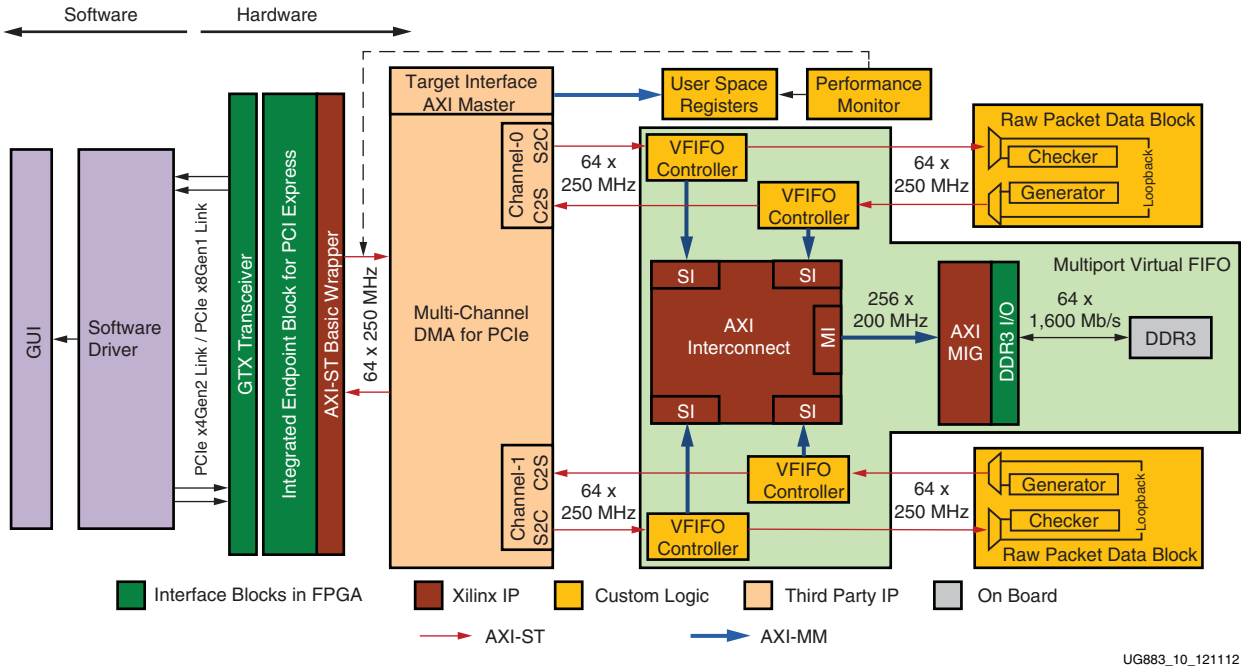


Figure 10: **Kintex-7 FPGA Base TRD Block Diagram**

Note: In Figure 10 the arrows indicate AXI interface directions (from master to slave). They do not indicate data flow directions.

Components

The Kintex-7 FPGA Base TRD features these components:

- Kintex-7 FPGA integrated Endpoint block for PCI Express:
  - Configured with 4 lanes at a 5 Gb/s link rate (Gen2) or 8 lanes at a 2.5 Gb/s link rate (Gen1) for PCI Express v2.0
  - Provides a user interface compliant with AXI4-Stream interface protocol
  - Performance monitor tracks the integrated block's AXI4-Stream interface for PCIe transactions
- Bus Mastering Scatter-Gather Packet DMA from Northwest Logic, a multichannel DMA:
  - Supports full-duplex operation with independent transmit and receive paths
  - Provides an AXI4-Stream interface on the back end
  - Monitors the performance of data transfers in receive and transmit directions
  - Provides an AXI4 memory-mapped target interface to access user-defined registers

  Note: The Northwest Logic Packet DMA shipped with the Base TRD is an evaluation version and expires after 12 hours of run time. To get the full version, contact Northwest Logic [Ref 8].
- Multiport Virtual FIFO:
  - DDR3 SDRAM SODIMM (64-bit @ 1600 Mb/s; 800 MHz) is used for buffering packets. The memory controller delivered through the memory interface generator (MIG) tool interfaces to the DDR3 memory.
  - AXI Interconnect IP along with the memory controller supports multiple ports on the memory.
  - The Packetized Virtual FIFO controller controls addressing of the DDR3 memory for each port, allowing DDR3 to be used as Virtual Packet FIFO.
- Software driver for a 32-bit Linux platform:
  - Configures the hardware design parameters
  - Generates and consumes traffic
  - Provides a GUI to report status and performance statistics

The Kintex-7 FPGA integrated Endpoint block for PCI Express and the Packet DMA are responsible for data transfers from host system to Endpoint card (S2C) and Endpoint card to host system (C2S). Data to and from the host is stored in a Virtual FIFO built around the DDR3 memory. This Multiport Virtual FIFO abstraction layer around the DDR3 memory allows the user to move traffic efficiently without the need to manage addressing and arbitration on the memory interface. It also provides more depth than storage implemented using Block RAMs.

The integrated Endpoint block for PCI Express, Packet DMA, and Multiport Virtual FIFO form the base system. The base system can bridge the host to any user application running on the other end. The raw data packet module is a dummy application that generates and consumes packets. It can be replaced by any user specific protocol like Aurora or XAUI.

The software driver runs on the host system. It generates raw data traffic for transmit operations in the S2C direction. It also consumes the data looped back or generated at the application end in the C2S direction.

Hardware Test Setup Requirements

These are the prerequisites for testing the design in hardware:

- KC705 Evaluation board with the Kintex-7 FPGA XC7K325T-2FFG900C device
- Design files provided as a zipped collection under the Docs & Designs tab at www.xilinx.com/kc705 include:
  - Design source files
  - Device driver files
  - Board design files
- Vivado Design Suite
- Use Vivado Hardware Manager
- Micro USB cable
- 4-pin to 6-pin PCIe adapter cable
- Fedora 16 Live DVD [Ref 9]
- PC with PCIe v2.0 slot. For a complete list of machines tested, and all known issues, refer to the Kintex-7 FPGA Base Targeted Reference Design Release Notes and Known Issues Master Answer Record AR 45679.This PC could also have Fedora Core 16 Linux OS installed on it.

TRD Demonstration Setup

This section describes hardware setup and use of the application GUI to help the user get started quickly with the design in hardware. It provides a step-by-step explanation of hardware bring-up, and describes using the application GUI.

When following the demonstration setup steps for the Kintex-7 FPGA Base TRD, if the behavior is not as described, refer to the known issues at www.xilinx.com/support/answers/45679.htm.

Board Setup

This section describes how to set up the KC705 Evaluation board required to demonstrate the TRD.

1. Set the KC705 Jumpers and Switches: Verify that the KC705 Evaluation board jumpers and switches are set as shown in Table 3 and Figure 11.

Table 3: **Switch and Jumper Settings**

Jumper	Function		Setting
J32	PCIe configuration width — 4 lane design		Jump 3-4
Switch	**Function or Type**		**Setting**
SW15	Board power slide-switch		Off
SW11	User GPIO DIP switch		
	4		Off
	3		Off
	2		Off
	1		Off
S13	DIP switch SW13 positions 1 and 2 control the setting of address bits of the flash. DIP switch SW13 positions 3, 4, and 5 control which configuration mode.		
	5 (M0)	M2 =0 M1=1 M0=0 – Master BPI M2 =0 M1=0 M0=1 – Master SPI M2 =1 M1=0 M0=1 – JTAG	Off
	4 (M1)		On
	3 (M2)		Off
	2		Off
	1		Off

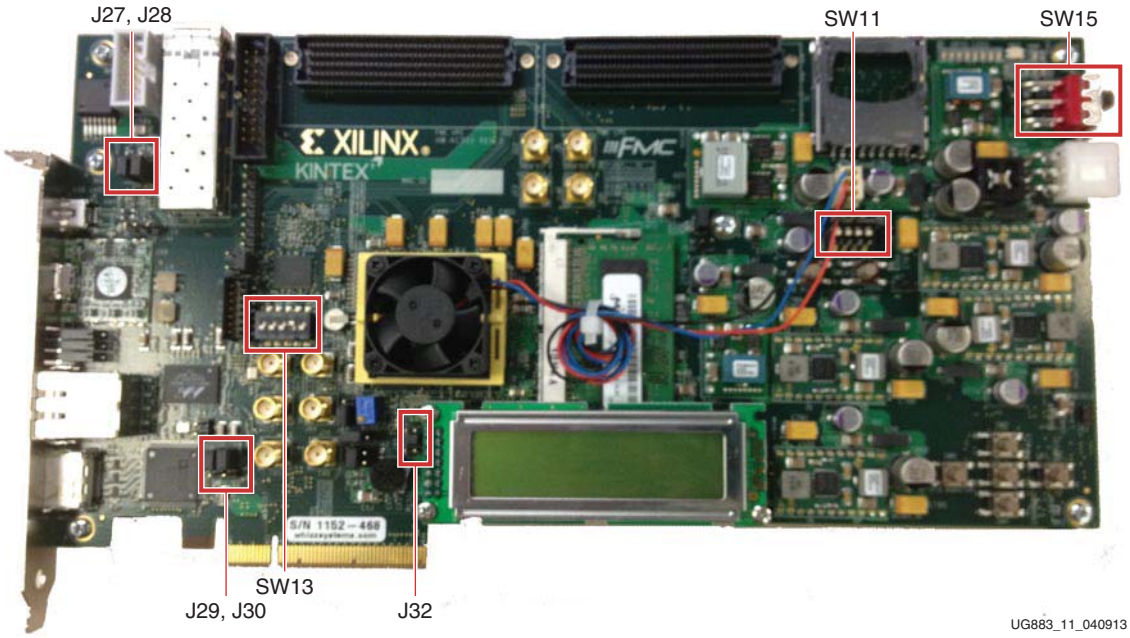


Figure 11: **Switch and Jumper Settings**

Hardware Bring-Up

This section presents steps for hardware bring-up.

1. With the host system switched off, insert the KC705 board in the PCIe slot through the PCI Express x8 or x16 edge connector (Figure 12).

   The TRD programmed on the KC705 board has a 4-lane PCIe v2.0 configuration, running at a 5 Gb/s link rate per lane. The PCI Express specification allows for a smaller lane width Endpoint to be installed into a larger lane width PCIe connector.

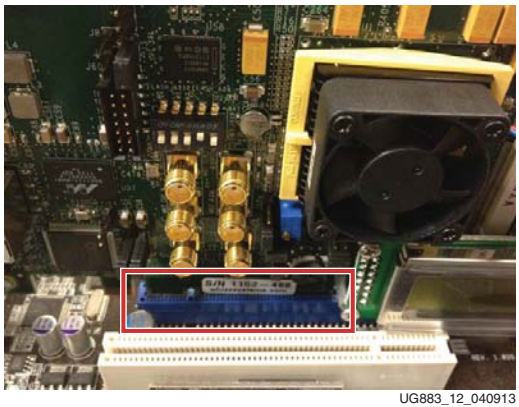


Figure 12: **KC705 Board Plugged into a PCIe x16 Slot**

2. Figure 13 shows the 12V power connection. Connect the 12V ATX power supply's available 4-pin connector to the board (J49) via a 4-pin to 6-pin PCIe adapter cable. Toggle the Power switch SW15 to the ON position.

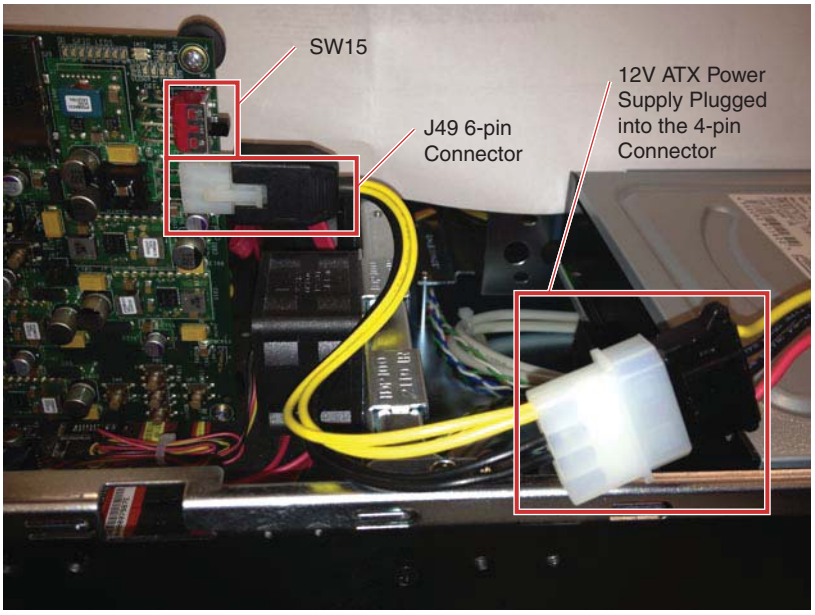


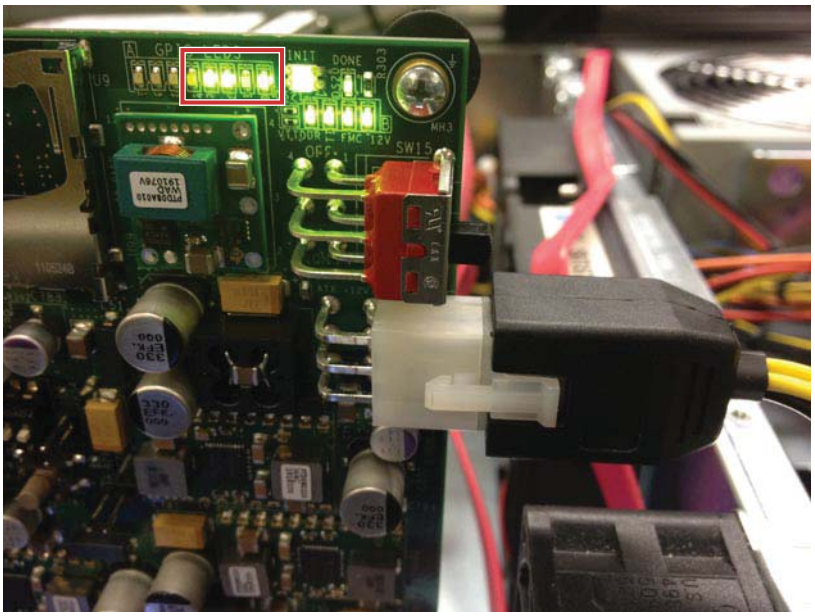
Figure 13: **Power Supply Connection**

3. Make sure the connections are tight, and then power on the PC system.

   Note: If the user wishes to boot Linux from the Fedora 16 Live DVD, place the DVD in the PC's DVD-ROM drive as soon as the PC system is powered on.

4. Verify the status of the design on the KC705 LEDs. The design provides status on the GPIO LEDs on the upper right of the KC705 board (Figure 14). After the PC system is powered on and the TRD has successfully configured, status LEDs, from right to left, should indicate:

- LED 0 — ON if the PCIe link is up
- LED 1 — Flashes if the PCIe user clock is present
- LED 2 — ON if lane width is what is expected, else it flashes (for a 4 lane design, the expected lane width is 4; for an 8 lane design, the expected lane width is 8)
- LED 3 — ON if memory calibration is done
- LED 4 to LED 7 — Not connected



UG883_14_121112

Figure 14: **Location of GPIO Status LEDs (Indicates TRD Status)**

Install the Linux Driver

1. If Fedora 16 is installed on the PC system's hard disk, boot as a root-privileged user, and skip to step 3, page 26.
2. To boot from the Fedora 16 Live DVD provided in the kit, place the DVD in the PC's DVD-ROM drive. The Fedora 16 Live Media is for Intel-compatible PCs. The DVD contains a complete, bootable 32-bit Fedora 16 environment with the proper packages installed for the TRD demonstration environment. For more details, see Fedora Information, page 2. The PC boots from the DVD-ROM drive and logs into a liveuser account. This account has kernel development root privileges required to install and remove device driver modules.

   Note: Users might have to adjust BIOS boot order settings to make sure that the DVD-ROM drive is the first drive in the boot order. To enter the BIOS menu to set the boot order, press the DEL or F2 key when the system is powered on. Set the boot order and save the changes. (The DEL or F2 key is used by most PC systems to enter the BIOS setup. Some PCs might have a different way to enter the BIOS setup.)

   The PC should boot from the DVD-ROM drive. The images in Figure 15 are seen on the monitor during boot up.

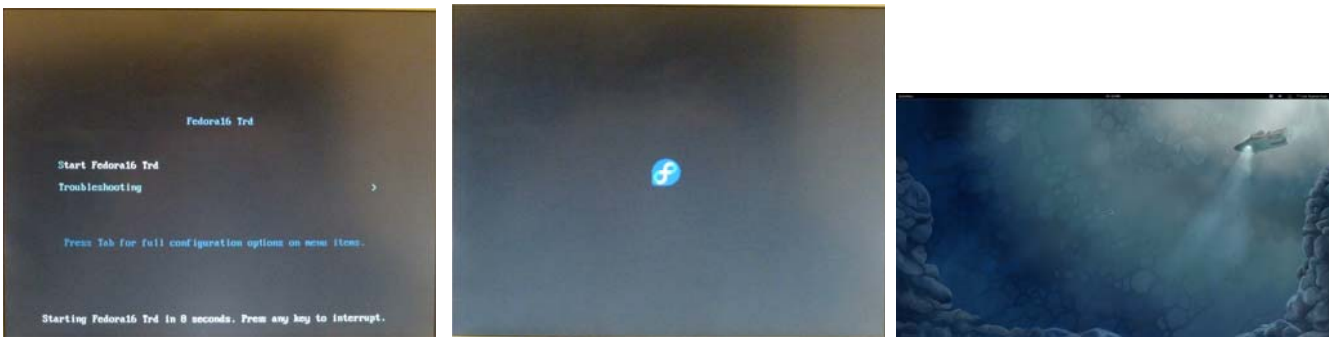


Figure 15: **Fedora 16 Live DVD Booting**

3. After Fedora 16 Core boots, open a terminal window (click **Activities**, click **Application**, scroll down, and click the **Terminal** icon). To find out if the PCIe Endpoint is detected, at the terminal command line, type

   ```
   $ lspci
   ```

   The lspci command displays the devices in the PCI and PCI Express buses of the PC. On the bus of the KC705 card slot is the message

   ```
   Communication controller: Xilinx Corporation Device 7042
   ```

This message confirms that the design programmed into the KC705 board has been found by the BIOS and the Fedora 16 OS. The bus number varies depending on which PC motherboard and slot are used. Figure 16 shows a lspci output for an example system. Xilinx device 7042 has been found by the BIOS on bus number 2 (`02:00.0 - bus:dev.function`).

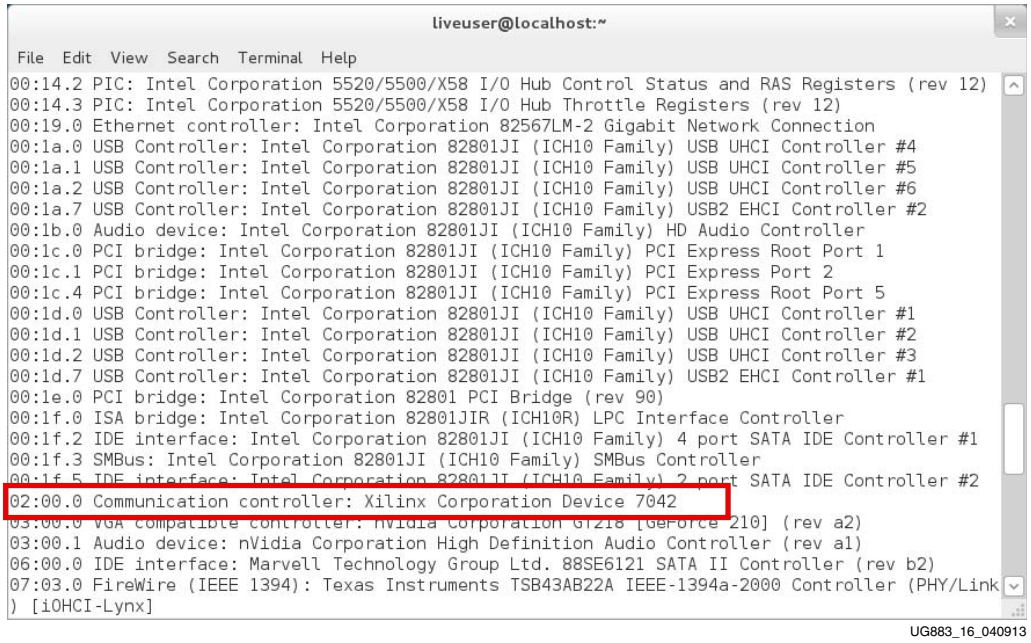


Figure 16: **PCI and PCI Express Bus Devices**

4. Download the reference design from the Docs & Designs tab at www.xilinx.com/kc705 and copy the `k7_pcie_dma_ddr3_base` folder into any directory.
5. To set up and run the TRD demonstration, the software driver should be installed on the PC system. Software driver installation involves:
   a. Building the kernel objects and the GUI
   b. Inserting the driver modules into the kernel.

   After the driver modules are loaded, the application GUI can be invoked. The user can set parameters through the GUI and run the TRD.

   When the user is done running the TRD, the application GUI can be closed and the drivers can be removed.

   A script is provided to execute all the above actions so that the user can quickly start the TRD.

   The `k7_trd_lin_quickstart` script is available in the `k7_pcie_dma_ddr3_base` folder. Right click the script, select **`properties`**, go to the **`permissions`** tab, check the box **`Allow executing file as program`**—this makes the script executable. Close the window.

To run the script, double-click `k7_trd_lin_quickstart` in the `k7_pcie_dma_ddr3_base` folder (Figure 17). The window prompt in Figure 18 appears.

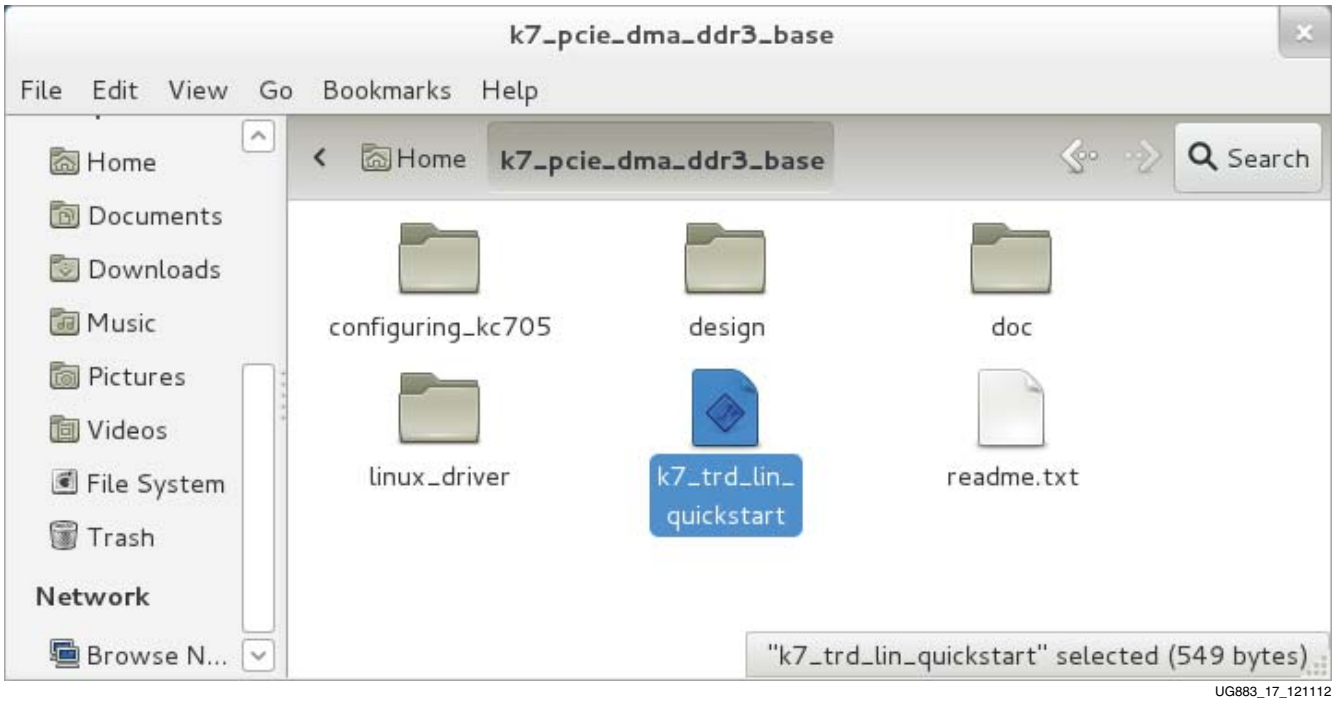


Figure 17: **Load Driver and Launch Application GUI**

Figure 18: **Run in Terminal**

Click **`Run in Terminal`** to proceed. The application GUI is invoked.

Proceed to the next section, Using the Application GUI, to set design parameters and run the TRD.

Using the Application GUI

When the drivers are loaded and the Performance Monitor GUI is invoked, the user can configure the sending and receiving of data. The GUI allows the user to observe the collected statistics and other status information.

1. Click the **`System Status`** tab to verify the status of the KC705 board and the PCIe link (see Figure 19 and Table 4).

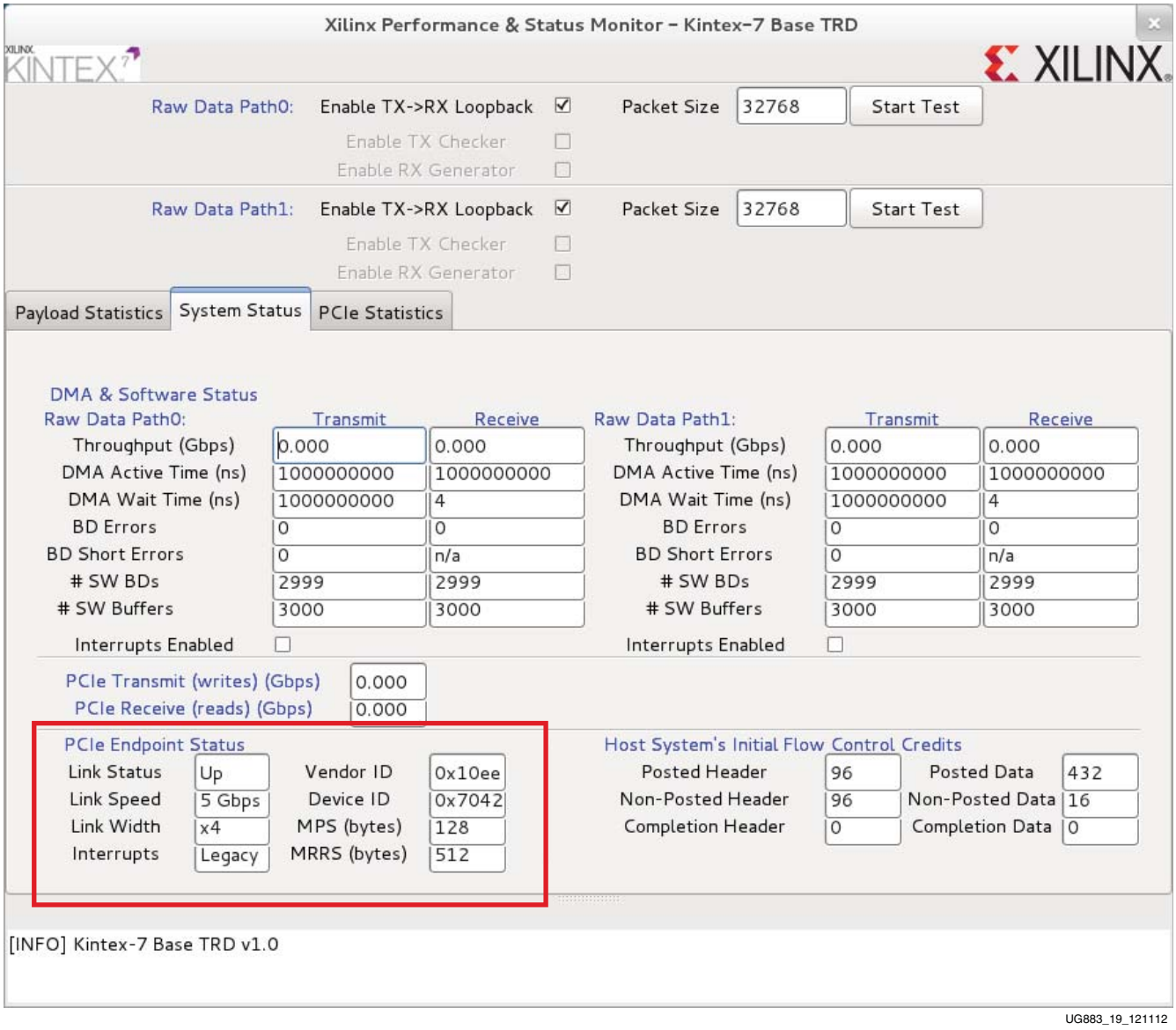


Figure 19: **Verify Board Status in the Performance Monitor**

Table 4: **KC705 Board Status Field Explanations**

Field	Status	Explanation
Link Status	Up	This confirms that the PCIe link is up and a PCIe connection is established between the Kintex-7 FPGA Endpoint for PCI Express and the PC motherboard chipset.
Link Speed	5.0 Gb/s	This confirms that the PCIe link is operating at line rate speed per PCI Express, v2.0.
Link Width	x4	This confirms that the PCIe link is trained as a x4 link.

2. To start data traffic on the two data paths:
   a. Click **`Start Test`** on `Raw Data Path0` as shown in Figure 20. This enables the driver to start generating the data for `Raw Data Path0`.
   b. Click **`Start Test`** on `Raw Data Path1` as shown in Figure 20. This enables the driver to start generating the data for `Raw Data Path1`.

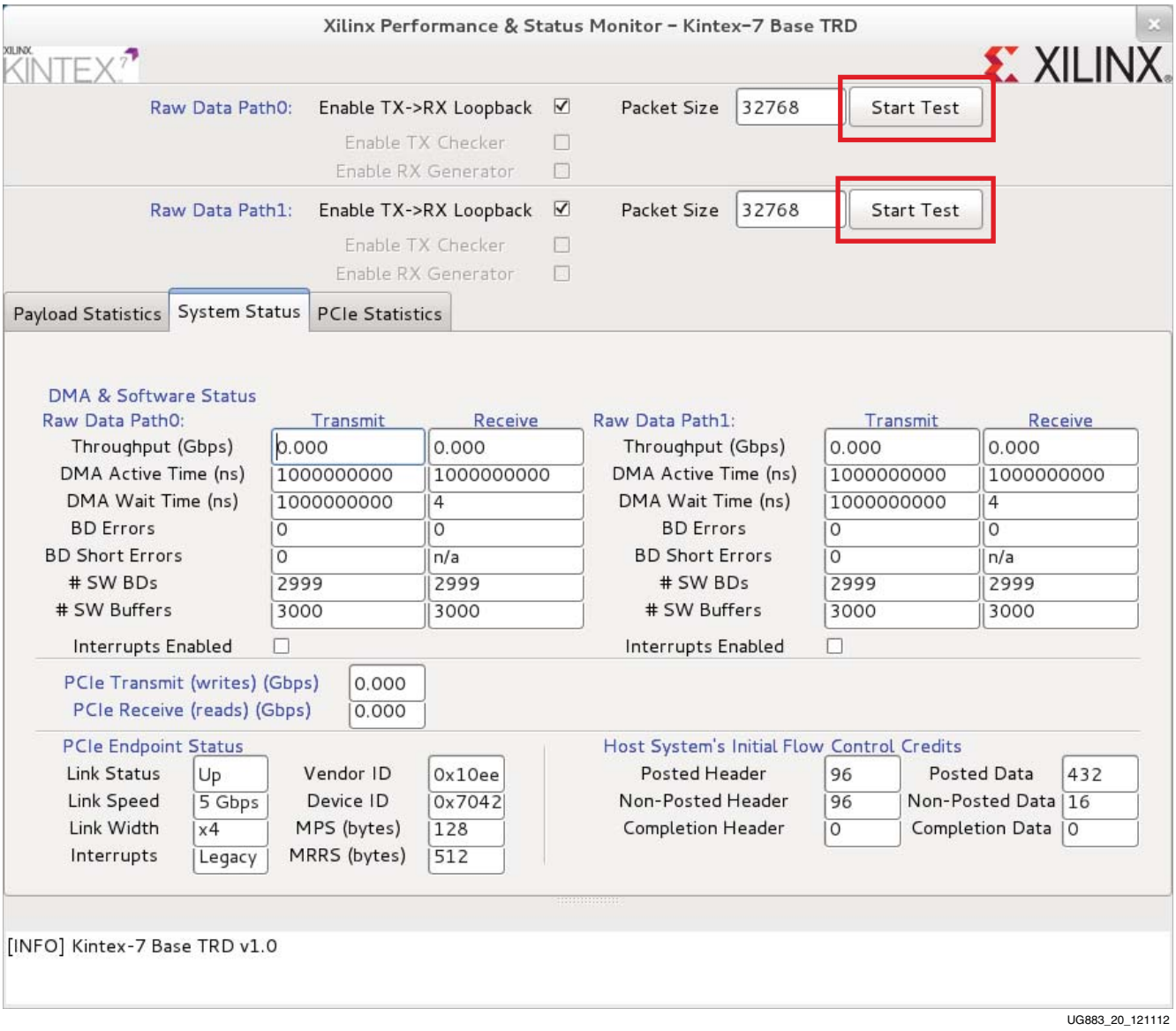


Figure 20: **Start Data Traffic from the Performance Monitor**

3. Verify TRD operations through the status information provided by the GUI (see Figure 21).
   a. Verify the PCIe throughput.
   b. Verify the DMA channel throughput for the `Raw Data Path0`.
   c. Verify the DMA channel throughput for the `Raw Data Path1`.
   d. Verify there are no buffer descriptor errors for error-free operation.

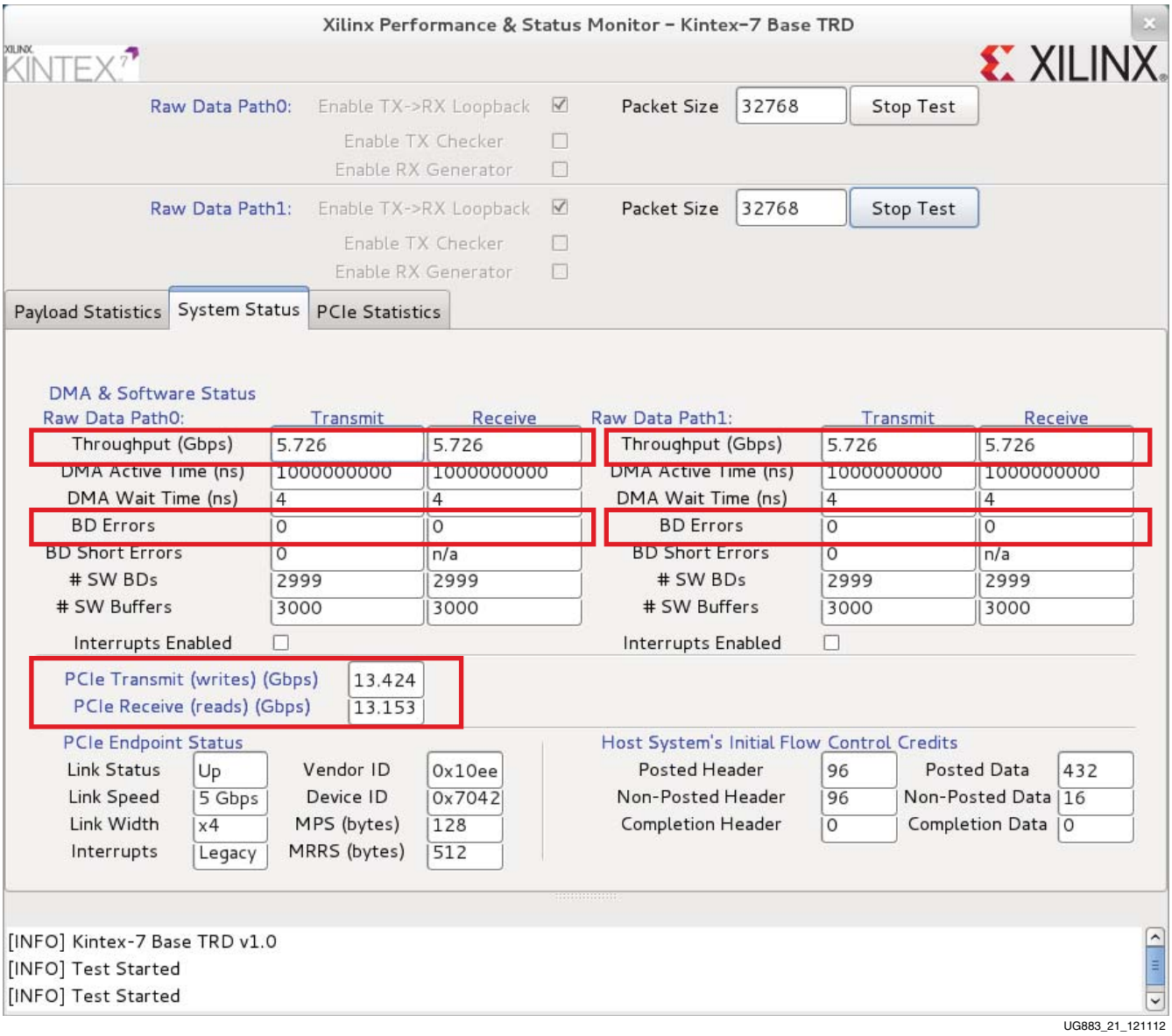


Figure 21: **Verify Error-Free Operation in the Performance Monitor**

The Kintex-7 FPGA PCIe-DMA TRD is now set up and running. Close the Application GUI to unload the software drivers and stop traffic flow.

Evaluating the Kintex-7 FPGA Base TRD

The Kintex-7 FPGA Base TRD provides a Performance and Status monitor application and GUI. The application enables customers to evaluate different system parameters. This section demonstrates performance variances for the PCI Express and DMA interfaces based on the parameters set.

To evaluate the Kintex-7 FPGA Base TRD:

1. Launch the Performance Monitor for the Kintex-7 FPGA Base TRD.
   a. Navigate to the `k7_pcie_dma_ddr3_base` folder.
   b. Double-click `k7_lin_trd_quickstart` (Figure 22)—make sure that the script has executable permission—to launch the Performance Monitor and Status GUI.

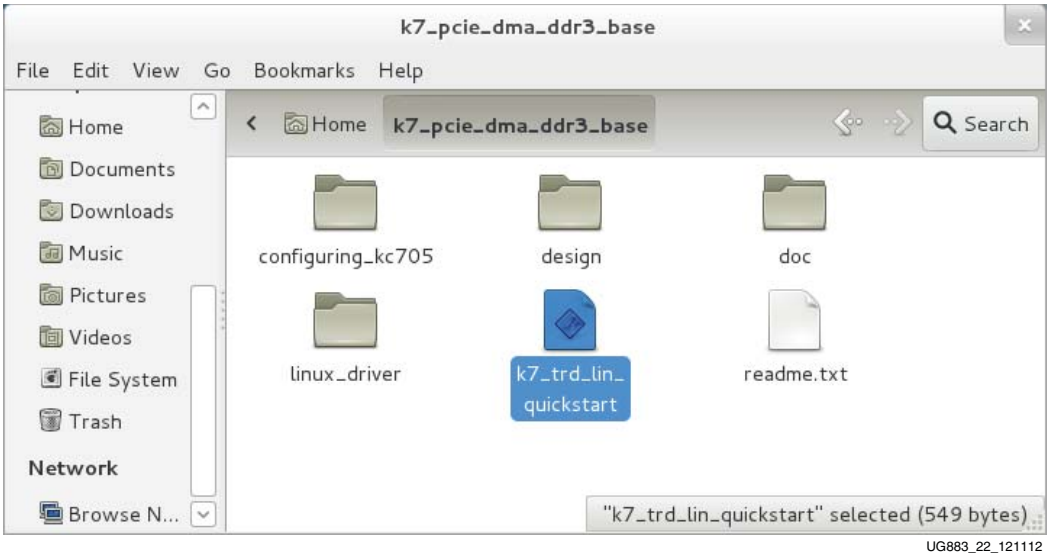


Figure 22: **Launch the Performance Monitor and Status GUI**

   c. A window prompt appears as shown in Figure 23. Click **Run in Terminal** to proceed.

Figure 23: **Run k7_lin_trd_quickstart**

2. Set up the test parameters in the Performance Monitor.
   a. Two data paths are available: `Raw Data Path0` and `Raw Data Path1`. On each path, set the `Packet Size` to a value between 64 – 32,768 bytes.
3. Execute the test, and view payload statistics in the Performance and Status Monitor (see Figure 24).
   a. Click **`Start Test`** to start the performance test.
   b. Click the **`Payload Statistics`** tab to view data transfers on the DMA channels.
   c. Click **`Stop Test`** to stop data traffic.

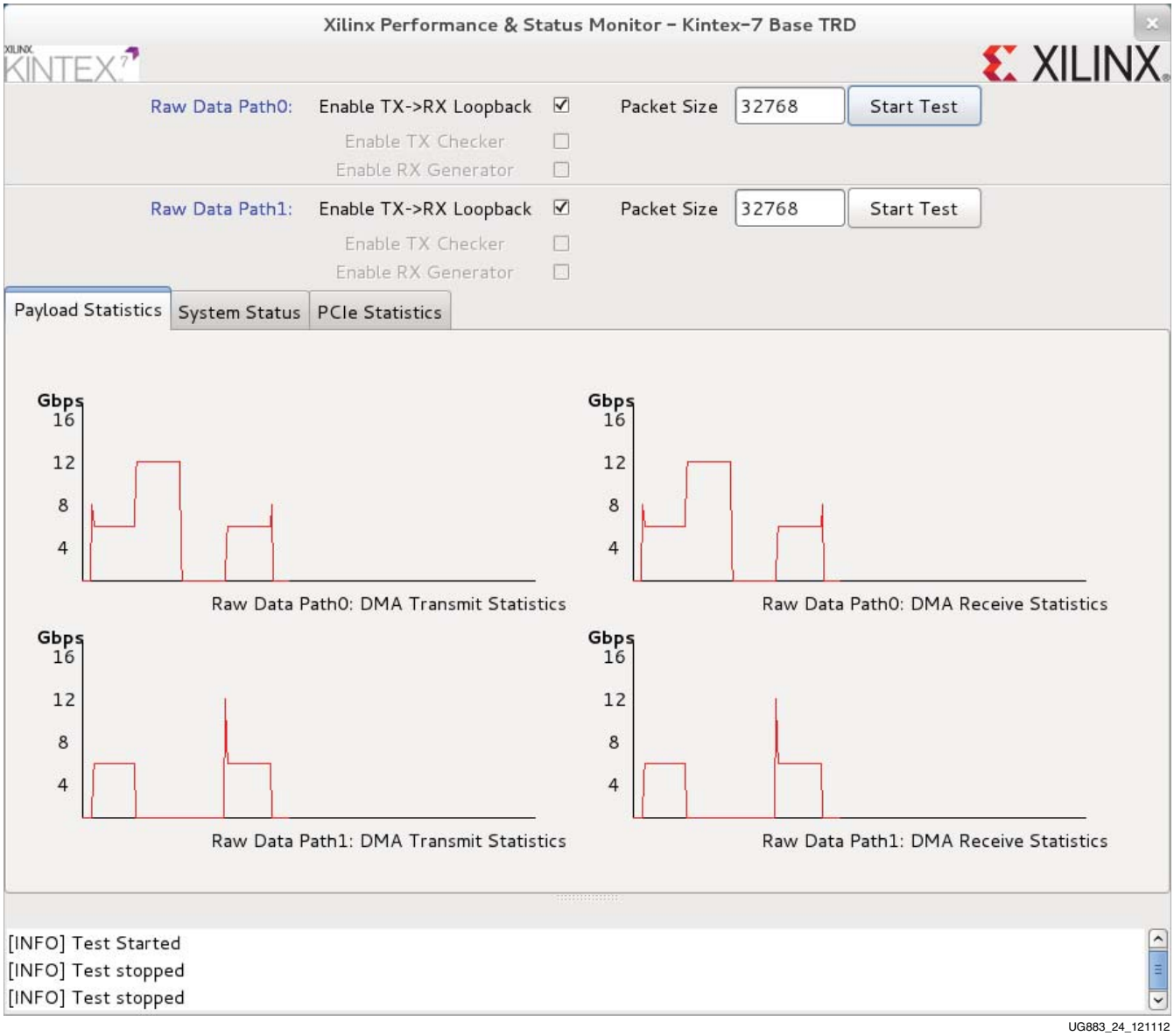


Figure 24: **Payload Statistics**

d. Vary the Packet Size parameters for the Raw Data Paths (see Figure 25) and click **`Start Test`**. Then view the payload statistics to review data transfer rate on the DMA channels. With a decrease in packet size, the performance drops.

Note: Before changing packet size, click **`Stop Test`**, change the size, and then click **`Start Test`**.

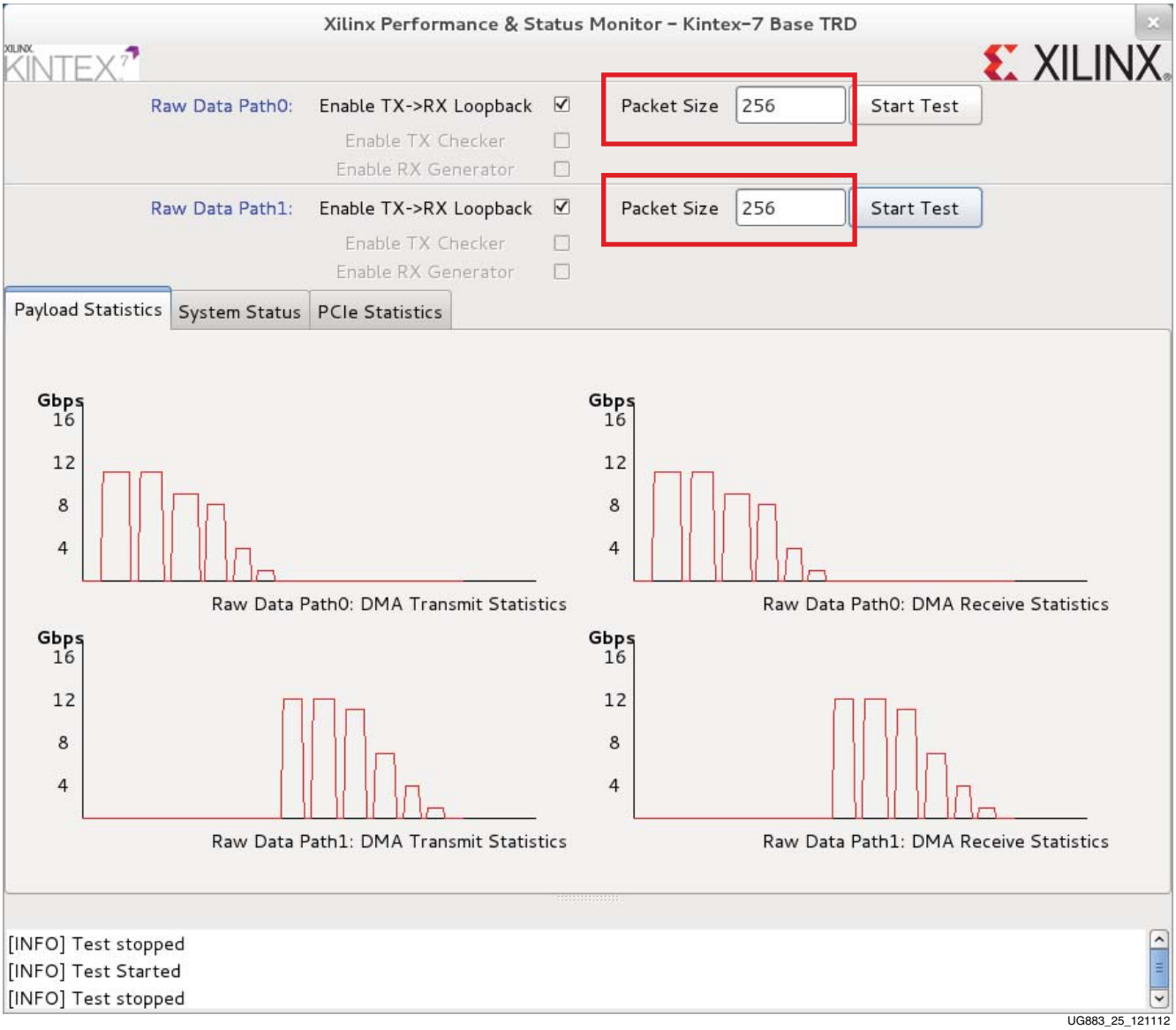


Figure 25: **Effect of Varying Packet Sizes on Performance**

Note: For packet sizes equal to 64 or 128 bytes, the throughput is reduced and might not be visible on the **`Payload Statistics`** tab. The exact values can be viewed on the **`System Status`** tab.

4. Click the **PCIe Statistics** tab to view data transfer numbers with varying packet sizes on the PCIe interface (Figure 26).

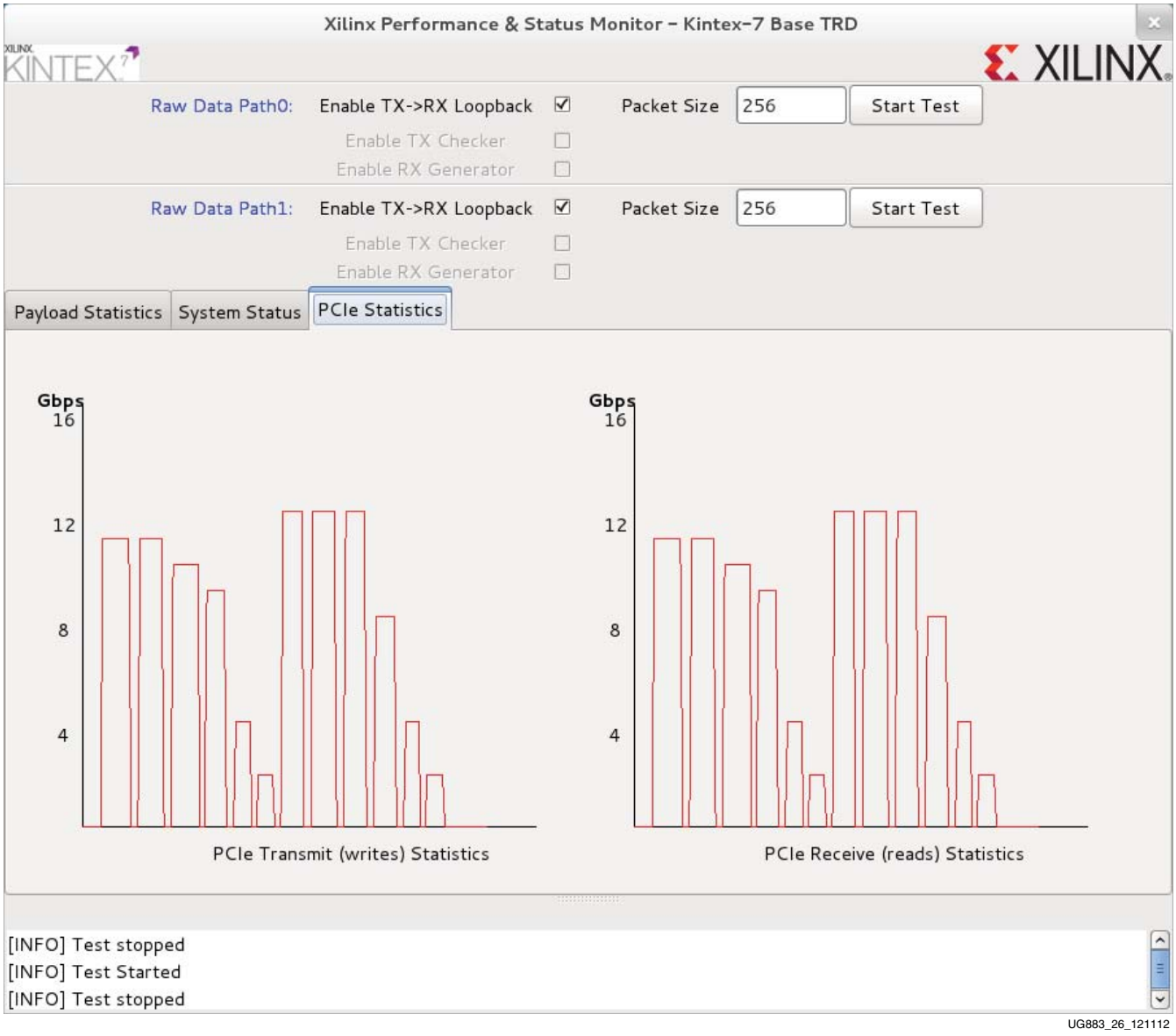


Figure 26: **PCIe Statistics in the Performance Monitor**

The system performance of the Kintex-7 FPGA Base TRD has now been evaluated using the pre-built demonstration design bit file.

Now that the Kintex-7 FPGA Base TRD demonstration has been set up and evaluated, the design can be modified. Before the design can be modified, make sure to install the Vivado Design Suite on a PC. It is not required that tools be installed on the PC system in which the KC705 evaluation board is plugged in by way of the PCIe edge connector.

XILINX

Appendix A

Additional Resources

Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see the Xilinx Support website.

For continual updates, add the Answer Record to your myAlerts.

Solution Centers

See the Xilinx Solution Centers for support on devices, software tools, and intellectual property at all stages of the design cycle. Topics include design assistance, advisories, and troubleshooting tips.

References

The most up to date information related to the KC705 board and its documentation is available on these websites:

Kintex-7 FPGA KC705 Evaluation Kit

Kintex-7 FPGA KC705 Evaluation Kit documentation

Kintex-7 FPGA KC705 Evaluation Kit - Known Issues and Release Notes Master Answer Record (AR 45934)

Vivado Design Suite

These documents and sites provide supplemental material useful with this guide:

1. *KC705 Evaluation Board for the Kintex-7 FPGA User Guide* (UG810)
2. *Kintex-7 FPGA KC705 Base Targeted Reference Design User Guide* (UG882)
3. Tera Term Pro program: hp.vector.co.jp/authors/VA002416/teraterm.html
4. Drivers on the Silicon Labs site: www.silabs.com/support/Pages/software-downloads.aspx
5. *Vivado Design Suite User Guide: Programming and Debugging* (UG908)
6. *AMS101 Evaluation Card User Guide* (UG886)
7. *7 Series FPGAs Integrated Block for PCI Express Product Guide* (PG054)
8. Northwest Logic DMA back end core: www.nwlogic.com/packetdma
9. Fedora project: fedoraproject.org. Fedora is a Linux-based operating system used in the development of this TRD.
10. LabVIEW 32-bit Run-Time Engine: joule.ni.com/nidu/cds/view/p/id/2534/lang/en
11. LabVIEW 64-bit Run-Time Engine: joule.ni.com/nidu/cds/view/p/id/2536/lang/en

12. The GTK+ project API documentation: www.gtk.org/documentation.php. GTK+ is a toolkit for creating graphical user interfaces (GUI).
13. *Vivado Design Suite User Guide: Release Notes, Installation, and Licensing* (UG973)

XILINX

Appendix B

Warranty

THIS LIMITED WARRANTY applies solely to standard hardware development boards and standard hardware programming cables manufactured by or on behalf of Xilinx ("Development Systems"). Subject to the limitations herein, Xilinx warrants that Development Systems, when delivered by Xilinx or its authorized distributor, for ninety (90) days following the delivery date, will be free from defects in material and workmanship and will substantially conform to Xilinx publicly available specifications for such products in effect at the time of delivery. This limited warranty excludes:
(i) engineering samples or beta versions of Development Systems (which are provided "AS IS" without warranty); (ii) design defects or errors known as "errata";
(iii) Development Systems procured through unauthorized third parties; and
(iv) Development Systems that have been subject to misuse, mishandling, accident, alteration, neglect, unauthorized repair or installation. Furthermore, this limited warranty shall not apply to the use of covered products in an application or environment that is not within Xilinx specifications or in the event of any act, error, neglect or default of Customer. For any breach by Xilinx of this limited warranty, the exclusive remedy of Customer and the sole liability of Xilinx shall be, at the option of Xilinx, to replace or repair the affected products, or to refund to Customer the price of the affected products. The availability of replacement products is subject to product discontinuation policies at Xilinx. Customer may not return product without first obtaining a customer return material authorization (RMA) number from Xilinx.

THE WARRANTIES SET FORTH HEREIN ARE EXCLUSIVE. XILINX DISCLAIMS ALL OTHER WARRANTIES, WHETHER EXPRESS, IMPLIED OR STATUTORY, INCLUDING, WITHOUT LIMITATION, ANY WARRANTY OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT, AND ANY WARRANTY THAT MAY ARISE FROM COURSE OF DEALING, COURSE OF PERFORMANCE, OR USAGE OF TRADE. (2008.10)

Do not throw Xilinx products marked with the "crossed out wheeled bin" in the trash. Directive 2002/96/EC on waste electrical and electronic equipment (WEEE) requires the separate collection of WEEE. Your cooperation is essential in ensuring the proper management of WEEE and the protection of the environment and human health from potential effects arising from the presence of hazardous substances in WEEE. Return the marked products to Xilinx for proper disposal. Further information and instructions for free-of-charge return available at: http:\\www.xilinx.com\ehs\weee.htm.